

## **Session Oral 9 (8/8 Thu. 11:30 – 12:42)**

Session Topic: Data Converter, RF/mm-Wave Circuits, and High-Speed Building Blocks

Session Chair: Wei-Bin Yang (Tamkang University) and Chun-Hsing Li (National Tsing Hua University)

Room: 6F 樂廳

### 1. 11:30 – 11:42 (S0204) Monolithic CMOS Microwave Heater with Programmable Thermostat Function

Tzu-Yu Tseng, Hsiao-Chin Chen and Jenq-Shiou Leu

National Taiwan University of Science and Technology

A monolithic CMOS microwave heater with programmable thermostat function is implemented for thermotherapy. To achieve microwave heating, the heater adopts a 2.4-GHz oscillator to generate the microwave and uses an amplifier with LC resonance load to enhance the signal strength. The load inductor is employed as the heat applicator as large electrical field would be created around it. The

microwave heater is then integrated with temperature sensors, a 11-bit SAR-ADC and a comparator to achieve the thermostat function. Dissipating the power of 145 mW, the amplifier delivers the output power of 13.2 dBm. The temperature sensors achieve sensing range from 20 °C to 50 °C, with the sensitivity of 47 mV/°C. When 427mg of agar phantoms is placed above the heater, it can be heated up by 1 °C with 0.1 °C accuracy when the thermostat function is activated.

## 2. 11:42 – 11:54 (S0146) Device Area Allocation for Yield Optimization in Integrated Circuits

Poki Chen and Ahmad Shahid Bhatti

National Taiwan University of Science and Technology

There are very few papers focusing on integrated circuit layout instead of design. Most of them are devoted to the generation of layout patterns to cancel the error caused by systematic mismatch. There are really few papers dealing with random mismatch especially by allocating proper areas to critical

devices for yield optimization. Area allocation strategies for yield optimization are proposed for some important analogue circuits in this paper. To demonstrate the performance, not only full-coverage simulations but also theoretical analyses are revealed. A test chip of the most representative circuit, R-2R ladder network, has been realized in a TSMC 0.35  $\mu\text{m}$  standard CMOS process to verify the excellence of the proposed area allocation strategy. To further ease the burden of analog IC designers and layout engineers, a rule of thumb based on device weights for area allocation with at least close-to-optimum yield is also presented.

3. 11:54 – 12:06 (S0122) A 14-bit Low Power 2-MS/s SAR ADC with Residue Oversampling

Sheng-Wen Huang and Soon-Jyh Chang

National Cheng Kung University

This paper presents a 14-bit successive-approximation register (SAR) analog-to-digital converter (ADC),

which adopts Residue Oversampling and Detect-and-Skip (DAS) techniques for high resolution and low power requirements. The proof-of-concept prototype was fabricated in TSMC 40-nm CMOS technology. At 2-MS/s sampling rates, the measured peak SNDR is 64.94dB without calibration. With a 0.03 standard deviation at each unit capacitor, static performance shows that INL and DNL are +1.25/-0.80 and +1.05/-0.97, respectively.

#### 4. 12:06 – 12:18 (S0060) A 10-Gb/s Equalizer with Digital Adaptation

Jui-Cheng Hsiao, Dai-En Jhou, Hsiu Hsien Ting, and Tai-Cheng Lee

National Taiwan University

An equalizer using a digital adaptive algorithm is proposed to minimize hardware cost. The proposed algorithm uses two analog reference levels to detect the low-frequency and high-frequency components of the input amplitude, respectively. By monitoring the two reference levels, the proposed equalizer can tune its high-frequency gain to compensate the channel loss appropriately. This work has been

fabricated in a 40-nm process, and the equalizer core circuit occupies 0.014 mm<sup>2</sup> and consumes 10 mW from a 1-V supply.

5. 12:18 – 12:30 (S0003) A Flip-Chip-Assembled W-Band Receiver in 90-nm CMOS and IPD Technologies

Te-Yen Chiu, Wan-Ting Hsieh, and Chun-Hsing Li

National Tsing Hua University

A flip-chip-assembled W-band receiver composed of a 90-nm CMOS chip and an integrated-passive-device (IPD) carrier is presented in this work. The chip which integrates a low-noise amplifier (LNA), a single-sideband mixer, a frequency doubler (FD), and a wide-band variable-gain amplifier (VGA), is flip-chip packaged to the IPD carrier through a low-loss interconnect. Experimental results show that the proposed packaged receiver can provide a variable gain from 11.3 to 48.2 dB while having an input 1-dB compression point from -43.7 to -29 dBm as the RF frequency is 90 GHz. The IF

bandwidth and minimum noise figure can be 1.0 GHz and 7.8 dB, respectively. The proposed receiver only consumes 73.9 mW from a 1.2-V supply. To the best of authors' knowledge, this is the first W-band CMOS receiver assembled on an IPD carrier reported thus far.

6. 12:30 – 12:42 (S0063) An S-Band CMOS Mixer-First Single-RF-Port Duplexing FMCW Radar

Hao-Chung Chou (1), Chun-Chieh Peng (1), Yu-Jiu Wang (2), and Ta-Shun Chu (1)

(1) National Tsing Hua University and (2) Tron Future Tech Inc.

A mixer-first single-RF-port duplexing RF frontend is proposed and implemented for frequency-modulated continuous-wave (FMCW) radar applications in this paper. The RF frontend is a bidirectional simultaneous frequency up-and-down converter. Equations of basic parameters of the frontend are derived to provide design criteria. The proposed radar architecture has been evaluated with an S-band (3.3-3.6 GHz) FMCW radar. The radar chip is fabricated in a 65nm CMOS process, and it

consumes 190 mW of DC power under 1.2V supply. A wireless distance measurement has verified the function of the radar chip.