Session Oral 8 (8/7 Wed. 15:30 – 17:00)

Session Topic: VLSI Design for Biomedical Applications

Session Chair: Yuan-Ho Chen (Chang Gung University)

Room: 7F 論語廳+大學廳

1. 15:30 – 15:43 (SC21) VLSI Chip Design for Wireless Body Sensor Network

   Shih-Lun Chen

   Chung Yuan Christian University

   Nowadays, applications of wireless body sensor networks (WBSNs), Internet of Things (IoT), and wearable devices have become wider and wider. These applications provide an effective solution for sustained monitoring, mobile health, self-health management and biological analysis in home-care system. As the demand of light-weight for wearable and portable applications, VLSI circuit has become a

significant trend. For this purpose, we proposed a VLSI chip design which includes an asynchronous interface, a register bank, a reconfigurable filter, a lossless data encoder, an encryption encoder, an effort correct coding encoder, a power management, a resolution controller, a multi-sensor controller, an encryption encoder and a QRS complex detector. The proposed VLSI chip design was synthesized by a TSMC 0.18-µm CMOS process and it can operate at 100-MHz processing rate. Compared with previous designs, this design achieved higher performance, higher security, higher reliability, more functions, more flexibility, higher compatibility and lower cost than previous designs.

2. 15:43 – 15:56 (SC22) Hardware/Software Codesign for Portable Optical Coherence Tomography (OCT) Applications

   Song-Nien Tang, Fu-Chue Tsai, and Yu-Ci Li

   Chung Yuan Christian University

This paper presents a hardware-software codesign scheme for the image formation of the Fourier-domain optical coherence tomography (FDOCT) system. Using a hardware processor, the fast Fourier transform (FFT) together with its front-end DC noise removal and re-sampling operations can be efficiently performed. In cooperation with the hardware unit, a software platform can properly execute the flexible magnitude compression and dynamic range mapping which are associated with the OCT image display. The proposed design could be developed based on a small-scale system, which lends support to the trend of portable FDOCT applications. System-level design verification was performed using an FPGA module and a mobile phone to evaluate the efficacy of the proposed hardware/software codesign scheme. By accessing the raw data through a pattern generator, the 16.2-fps OCT image display (in the 1024x1000 resolution) can be achieved in the developed FPGA-phone verification system.

3. 15:56 – 16:09 (SC23) A Fourier-Domain Optical Coherence Tomography (FDOCT) Imaging System Using the GPU of Raspberry PI for Portable OCT Applications

Song-Nien Tang, Fu-Chue Tsai, and Yu-Ci Li

Chung Yuan Christian University

Recently, the optical coherence tomography (OCT) technology based on the interference principle has been widely applied to the medical image inspection. The Fourier-domain (FDOCT) technology currently is the mainstream modality. In this project, we present an FDOCT image formation system based on the Raspberry PI platform capable of performing all FDOCT imaging operations, including dc removal, re-sampling, real-valued fast Fourier transform (RFFT), magnitude compression and display processing. Moreover, considering the OCT imaging rate, the RFFT computation could be accelerated using the graphics processing unit (GPU) of Raspberry PI. Thus, the high-throughput RFFT calculation can be achieved through sixteen-path parallel processing in common with the employment of an operation-efficient RFFT algorithm. Through the system measurement, a frame of OCT image with the resolution of 1024(axial) by 1000(lateral) pixels can be displayed in 2.7 seconds. Also, the OCT imaging

rate based on the GPU acceleration was 5 times as fast as that generated by pure CPU-based imaging operations.

4. 16:09 – 16:22 (SC24) VLSI Implementation of the Integral Pulse Frequency Modulation Model for Heart Rate Variability System

   Yen Juan, Shung-Ping Wang, and Yuan-Ho Chen

   Chang Gung University

   Heart rate variability (HRV) can be used to assess autonomous control activities. In the HRV analysis method, an integrated pulse frequency modulation (IPFM) model is used to function as a pacemaker and generates a series of heartbeats. In this study, the IPFM model was implemented into a VLSI chip, and the activity spectrum of the autonomic nervous system was estimated using a compression sensing (CS) method. The chip uses the TSMC 180nm CMOS process to design the IPFM model. In this model, the

look-up table method is used to calculate the sine/cosine operations and many nonlinear operations to achieve a low-cost design. In matrix operations, we use a multiplexer to control the signal so that the CS algorithm can be easily applied. The results show that the proposed chip has a gate count of 10.2 k at a 62.5 MHz operating frequency. We can effectively estimate the spectrum of HRV through VLSI implementation on the CS.

5. 16:22 – 16:35 (SC25) A VLSI Implementation of Low Cost Independent Component Analysis (ICA) for Biomedical Signal Separation

   Shung-Ping Wang, Yen Juan, and Yuan-Ho Chen

   Chang Gung University

   Independent component analysis (ICA) is a recently developed algorithm for analyzing blind source separation (BSS). The ICA algorithm can separate directly numbers of mixed signals, without any information about the mixed process or the source signals. It is suitable for digital signal processing,

particularly for dealing with biomedical signals. In this study, we develop a hardware implementation of the extended infomax ICA algorithm for the separation of super-Gaussian signal sources using integrated circuitry (IC). To reducing circuit area and achieving low cost, our proposed design is based on systolic array multiplication, which is usefully reducing many multiplications on the circuit. We also use a lookup table to replace the complicated calculation of the hyperbolic functions tanhθ. When implemented using the TSMC 0.18-µm CMOS process, the proposed ICA circuit achieve an operating frequency of 50 MHz with a gate count of 47 k. According to our simulation results, the architecture is applicable to the separation of mixed medical signals into independent sources.

6. 16:35 – 16:48 (S0108) Variation-Resilient Design Techniques for Energy-Constrained Systems

Bing-Chen Wu and Tsung-Te Liu

National Taiwan University

Process, voltage, and temperature (PVT) variations substantially increase the variability of digital CMOS

logics and reduce the operation robustness, especially for energy-constrained systems with aggressive voltage scaling. This paper reviews several variation-resilient design techniques for addressing PVT variations to improve the energy efficiency of digital CMOS VLSI circuits. The scope includes static and adaptive design techniques for design-time and run-time optimization, respectively. In addition, an emerging adaptive design strategy combining the fully integrated voltage regulator for system-level optimization is also introduced.

7. 16:48 – 17:01 (S0212) Design of the Compiler for a Reconfigurable Accelerator for Edge Computing with Binarized Convolutional Neural Networks

   Ching-Zong Chang, Chi-Jhe Li, and Hsin-Chou Chi

   National Dong Hwa University

   The recent rapid advance of deep learning and Internet of things (IoT) technology has triggered many applications. For these applications, one of the keys is the optimized convolutional neural network (CNN).

Besides, high-performance hardware is critical for supporting the required massive computation. In this paper, we propose a versatile compiler for the FPGA accelerator with binarized CNN. The compiler accepts the high-level description of the CNN, and automatically allocates the FPGA circuits efficiently based on the description. An abstract layer of API is also provided, such that knowledge of FPGA is not required for the engineers of deep learning. We have implemented the accelerator with our compiler. The performance evaluation results show that our system significantly outperforms the popular CPU and GPU solutions with good accuracy.