Session Oral 6 (8/7 Wed. 15:30 – 17:00)

Session Topic: EDA, Testing, and AI

Session Chair: Yu-Guang Chen (National Central University) and

Tong-Yu Hsieh (National Sun Yat-sen University)

Room: 6F 御廳

1. 15:30 – 15:43 (S0189) Clock-less DFT for Dual-rail Asynchronous Circuits (Best Paper Candidates)

   Chia-Cheng Pai, Tsai-Chieh Chen, Yi-Zhan Hsieh, and James Chien-Mo Li

   National Taiwan University

   In this paper, we propose asynchronous circuit scan (A-scan) latch, which can flip between Valid and Empty so that we can shift in and out without any clock. We also propose circuit models that enable traditional ATPG to generate high test coverage patterns for A-scan. Our stuck-at test coverage is 99.64%. This paper

provides a DFT and ATPG solution for testing asynchronous circuits.

2. 15:43 – 15:56 (S0041) NCTUcell: A DDA-Aware Cell Library Generator for FinFET Structure with Implicitly Adjustable Grid Map (Best Paper Candidates)

   Yih-Lang Li (1), Shih-Ting Lin (1), Shinichi Nishizawa (2), Hong-Yan Su (1), Ming-Jie Fong (1), Oscar Chen (3), and Hidetoshi Onodera (4)

   (1) National Chiao Tung University, (2) Saitama University, (3) AnaGlobe Technology, Inc., and (4) Kyoto University

   For 7nm technology node, cell placement with drain-to-drain abutment (DDA) requires additional filler cells, increasing placement area. This is the first work to fully automatically synthesize a DDA-aware cell library with optimized number of drains on cell boundary based on ASAP 7nm PDK. We propose a DDA-aware transistor placement. Previous works ignore the use of M0 layer in cell routing. We firstly propose

an ILP-based M0 routing planning. To improve the routing resource utilization, we propose an implicitly adjustable grid map, making the maze routing able to explore more routing solutions. Experimental results show that block placement using the DDA-aware cell library requires reduce filler cells by 70.9%, which achieves a block area reduction rate of 5.7%.

3. 15:56 – 16:09 (S0107) AIFood: A Large-scale Food Image Dataset for Ingredient Recognition (Best Paper Candidates)

   Gwo Giun (Chris) Lee, Chin-Wei Huang, Jia-Hong Chen, Shih-Yu Chen

   National Cheng Kung University

   In this paper, we introduce a large-scale food image dataset namely AIFood, which is constructed to aim ingredient recognition in food image research. AIFood dataset includes 24 categories and totally 372,095 food images around the world. We collect food images from eight existing food image datasets and a food

website. The food images are relabeled using 24 categories. We preliminarily label each image using existing food information such as dish name and ingredient information. Next, we manually check food images to find out undiscovered ingredients and relabel them. Every image can be labeled more than one category. In addition, food images may have color cast or uneven contrast problems, which may disturb performance of image recognition system. So, we applied preprocessing method which contains automatic white balancing and contrast limited adaptive histogram equalization to improve visual quality of food images. We set constraints which are defined by luminance and chrominance of image to determine if the image is to be preprocessed.

4. 16:09 – 16:22 (S0156) ROAD: An Asymmetric Aging Approach for Improving Reliability of Multi-core Systems

   Yu-Guang Chen (1), Jian-Ting Ke (2), Shu-Ting Cheng (3), and Ing-Chao Lin (2)

   (1) National Central University, (2) National Cheng Kung University, and (3) Yuan Ze University

Multi-core systems have been widely applied in modern computers to obtain stronger calculation power and better performance. However, Negative-Bias Temperature Instability (NBTI) has become one of the most drastic reliability threats. Previous researchers proposed various task assignment and/or dynamic voltage frequency scaling algorithms to tolerance NBTI by maintaining all cores in the multi-core system under similar aging conditions (symmetric aging). We observe that the symmetric aging may reduce the lifetime of a multi-core system. If a critical task (i.e., a task with tight timing constraints) arrives when the system has already operated for years, it is possible that none of the equivalently aged cores can complete the critical task within its timing constraints. This unavoidable timing failure then will shorten the lifetime of the system. With the above observation, this paper proposes a novel reliability improvement framework which realize the concept of asymmetric aging by task graph Retiming, task Ordering, task Assignment under asymmetric aging, and Dynamic voltage selection (ROAD) for multi-core systems. Experimental results show that our approach can significantly increase the system lifetime with no or insignificant

energy overhead.

5. 16:22 – 16:35 (S0209) Morphed Standard Cell Layouts for Pin Length Reduction

   Cheng-Wei Tai and Rung-Bin Lin

   Yuan Ze University

   This article presents a concept called morphed layouts which are layouts of a standard cell with different footprints on the pins of each layout for pin length reduction. The proposed approach can on average reduce total pin length by 12.1% and total wire length by 3.4% without via count increase.

6. 16:35 – 16:48 (S0150) Time-Frame Folding: Back to the Sequentiality

   Po-Chun Chien and Jie-Hong Roland Jiang

   National Taiwan University

In this paper we formulate time-frame folding (TFF) as the reverse operation of time-frame unfolding (TFU), or commonly known as time-frame expansion in automatic test pattern generation (ATPG) and (un)bounded model checking. While the latter converts a sequential circuit into a combinational one with respect to some expansion bound of k time-frames, the former attempts the opposite. TFF arises naturally in the context of testbench generation and bounded strategy generalization, and yet remains unstudied. Unlike TFU, TFF can be highly non-trivial as the sub-circuit of each time-frame can be distinct. We propose an algorithm that finds a minimum-state finite state machine consistent with the input- output behavior of the combinational circuit under folding. Empirical evaluation of our method demonstrates its ability in circuit size compaction and suggests potential use in different application domains.

7. 16:48 – 17:01 (S0085) An Effective Heuristic for 1st- to 2nd-Order Threshold Logic Gate Transformation

   Li-Cheng Zheng (1), Yung-Chih Chen (2), and Jing-Yang Jou (1)

(1) National Central University and (2) Yuan Ze University

This paper presents a non-ILP based method for transforming a 1st-order threshold logic gate (TLG) to a 2nd-order TLG with lower hardware implementation cost. The method works by first extracting 2nd- order inputs based on two sufficient conditions, and then optimizing the weights and the threshold value. The experimental results show that the quality of the proposed method is competitive with the ILP-based method and the proposed method is much more efficient.