Session Oral 2 (8/7 Wed. 13:30 – 15:00)

Session Topic: Power, Sensor, and Other Analog Techniques

Session Chair: Ching-Jan Chen (National Taiwan University) and Hung-Wen Lin (Yuan Ze University)

Room: 6F 御廳

1. 13:30 – 13:43 (S0142) Single-inductor two-boost converter with bidirectional energy flow (Best Paper Candidates)

   Hung-Hsien Wu, Chi-Hsiang Huang, Yen-Yu Chen, Yi-Ting Liou, and Chia-Ling Wei

   National Cheng Kung University

   A single-inductor two-boost dc–dc converter with bidirectional energy flow is proposed. This work combines two dc–dc converters into one by sharing a single inductor, and it is capable of storing energy and powering output load by using the bidirectional inductor current. With the storing state, the

variations on the output voltage are typically negligible when the input voltage changes. According to the measured results, the converter can startup successfully with a 0.55-V input voltage. The voltage range of the storing element is 1.2–1.4 V, and the maximal output power of the proposed converter is 18 mW with its output voltage setting at 1.8 V.

2. 13:43 – 13:56 (S0162) A Low Noise Optical Encoder with Background Light Cancellation Using Photodiodes in Series (Best Paper Candidates)

   You-Shin Chen (1), Tzu-Hsiang Hsu (1), Chien-Wen Chen (2) and Chih-Cheng Hsieh (1)

   (1)National Tsing Hua University and (2)Industrial Technology Research Institute

   This paper presents a low noise readout circuit for the optical encoder. Both absolute and incremental encoders are implemented chip with dual sensor arrays and the corresponding readout circuits. 42 columns of the pixel with adjustable dual-threshold quantizer are implemented in the absolute encoder

with digitized outputs. Four quadrature sinusoidal signals dephasing 90° to each other are generated in the incremental encoder for interpolation. Two opposite phases of photodiodes placed in series are proposed for background light cancellation without adding any extra circuit. A differential transimpedance amplifier (TIA) is followed by the photodiodes to eliminate the residual signals and convert the differential currents into voltage signals. A programmable gain amplifier (PGA) is implemented to fit the input range of the following 12-b SAR ADC. Measurement results show that the SNR reaches 60dB and the maximum displacement error is 0.22μm.

3. 13:56 – 14:09 (S0151) A 0.5V Real-time Computational CMOS Image Sensor with Programmable Kernel for Always-on Feature Extraction (Best Paper Candidates)

   Tzu-Hsiang Hsu and Chih-Cheng Hsieh

   National Tsing Hua University

This paper presents a 0.5V computational CMOS image sensor (C2IS) with array-parallel computing capability for always-on feature extraction. By applying the developed pulsed-width modulation (PWM) pixel and switch-current integration, the in-sensor 8-directional matrix-parallel multiply-accumulate (MAC) operation is realized. Moreover, the analog-domain convolution-on-readout (COR) operation, the programmable 3x3 kernel with 4-bit weights, and the tunable-resolution column-parallel ADC (1b to 8b) are implemented to achieve the real-time feature extraction without use of additional memory. The C2IS prototype has been fabricated and verified to demonstrate the raw and feature images at 480fps with a power consumption of 77/91 (uW) and the resultant FoM of 9.8/11.6 (pJ/pix/frame), respectively.

4. 14:09 – 14:22 (S0016) A Wide-Range Capacitive DC-DC Converter with 2D-MPPT for Soil/Solar Energy Extraction

   I-Che Ou (1), Jia-Ping Yang (1), Chia-Hung Liu (1), Kai-Jie Huang (1), Kun-Ju Tsai (2), Yu Lee (2), Yuan-Hua Chu (2), and Yu-Te Liao (1)

   (1) National Chiao Tung University and (2) Industrial Technology Research Institute

This paper presents a capacitive DC-DC converter with adaptive DC-DC conversion ratios and maximum power point tracking (MPPT) for soil and solar energy extraction. To overcome the varying input power ranges of the soil/solar energy sources, a two-dimension power tracking loop with time-based current slope detection was employed. The design was fabricated in a 0.18-µm CMOS process, achieving >80% efficiency in a throughput power range of 360µW to 25mW in the soil mode and from 400µW to 10mW in the solar mode while the peak system efficiency is 89.5%.

5. 14:22 – 14:35 (S0187) A Low-Area Programmable Low-Pass-Filter with Automatic -3dB Frequency Calibration

   Zhi-Sheng Zhang, Tzu-Hao Lin, Hung-Wen Lin

   Yuan Ze University

This paper proposes a wide f-3dB range low-pass filter (LPF) and its f-3dB calibration circuit. By using the replica LPF cell to design a oscillator and controlling the oscillation frequency, the f-3dB of LPF could be programmable among different process corners. Simulation results show that the calibrated f-3dB frequency has an error about 6% to the target frequency. The power consumption of the calibration system is about 3.7% to the LPF core.

6. 14:35 – 14:48 (S0124) A Bandgap Voltage Reference Circuit with Calibration Technique for Reducing Process Variation

Chiao-Han Yang and Shuenn-Yuh Lee

National Cheng Kung University

In this paper, we present a high precision bandgap voltage reference (BGR) circuit with calibration technique to reduce process variation. In traditional BGR circuits, the process variation can be calibrated

to achieve near-zero voltage variation by first order compensation, but the temperature coefficient is still varying from 5 to 50 ppm/˚C in different processes corner. In order to get more precise reference voltage, a new compensation circuit is implemented in this paper to accomplish second order compensation. The proposed circuit can automatically calibrate the reference voltage of BGR circuit when BJTs and MOSFETs are operated in TT corner and Resistors operate in any process corner. The BGR circuit is realized in TSMC 0.18-μm CMOS process occupying active area of 0.8217 mm2. The average temperature coefficient is 29.39 ppm/˚C at temperature from 0˚C to 120 ˚C, the average power consumption is 104.94 μW under 1.8-V supply voltage, and power supply rejection ratio (PSRR) are –39.6 dB@100 Hz and -40.7 dB@1 kHz.

7. 14:48 – 15:01 (S0075) Distributed Diode-Triggered SCR for Broadband ESD Protection in CMOS Technology

   Chun-Yu Lin, Yu-Hsuan Lai, and Zih-Jyun Dai

   National Taiwan Normal University

Electrostatic discharge (ESD) protection design is needed for integrated circuits; however, the ESD protection devices beside the I/O pad may cause negative impact on the circuit performance. To achieve both excellent ESD robustness and good broadband performance, a silicon-controlled rectifier (SCR) with trigger diodes and matching inductor to form a novel distributed diode-triggered SCR (π-SCR) is presented in this work. As compared with the conventional π-diode in silicon, the π-SCR can reduce the clamping voltage during the critical positive-to-VSS (PS) ESD test, and the high-frequency performance is not seriously degraded (insertion loss <2dB within 0-20GHz in this work). Besides, the π-SCR does not suffer the latchup issue in low-voltage CMOS technology, and it has the potential to further reduce the clamping voltage during other ESD tests. Therefore, the π-SCR will be a good choice for broadband ESD protection in CMOS technology.