Session Oral 14 (8/9 Fri. 10:20 – 11:20)

Session Topic: Machine Learning for EDA

Session Chair: Ing-Chao Lin (National Cheng Kung University)

Room: 6F 茗廳

1. 10:20 – 10:32 (SB21) Register Clustering by Effective Mean Shift Algorithm

   Iris Hui-Ru Jiang and Tung-Wei Lin

   National Taiwan University

   As the wide adoption of FinFET technology in mass production, dynamic power becomes the bottleneck to achieving low power. Therefore, clock power reduction is crucial in modern IC design. Register clustering can effectively save clock power because of significantly reducing the number of clock sinks and register pin capacitance, clock routed wire length, and the number of clock buffers. In this talk, we review prior

works on register clustering and present effective mean shift to naturally form clusters according to register distribution without placement disruption. Unlike clique partitioning and k-means, effective mean shift fulfills the requirements to be a good register clustering algorithm because it needs no prespecified number of clusters, is insensitive to initializations, is robust to outliers, is tolerant of various register distributions, is efficient and scalable, and balances clock power reduction against timing degradation. Experimental results show that effective mean shift achieves superior power and timing balancing, as well as efficiency and scalability.

2. 10:32 – 10:44 (SB22) Early-stage power grid analysis based on machine learning techniques

   Chi-Hsien Pao and Yu-Min Lee

   National Chiao Tung University

   With new technology advances, the growing size of the power grid makes IR drop analysis become more

challenging and can no longer be solved efficiently by traditional methods. As a result, we propose a machine-learning-based static IR drop prediction model that can predict the IR drop of any given node on the power grid. Whenever designers locally change the power grid structure for optimization or robustness, we do not have to re-analyze the whole circuit again as a brand new circuit, which is time-consuming. We extract eleven features that can capture the behavior of the power grid and are very scalable, and use XGBoost as our prediction model, which is based on the regression tree ensemble. XGBoost is extremely powerful and used by most of the winners in many competitions. Experimental results show our method can accurately and efficiently be applied to large-scaled design.

3. 10:44 – 10:56 (SB23) Decision-Tree-Based Classification Method for SMD Electronic Components

Yun-Jie Ni (1), Yi-Ting Chen (2), Yan-Jhih Wang (2), and Tsung-Yi Ho (1)

(1) Naional Tsing Hua University and (2) FootPrintKu Inc.

Achieving automation by machine learning has been an upward trend for recent years. However, some know-how only keep in engineers' mind which is not recorded such as footprint drawing for Printed Circuit Board (PCB). Drawing rules for footprints such as area of Design for Assembly (DFA) bound, route keepout, and etc, are actually vary between types of components. Therefore, a classification method for footprints without type labels in databases is needed. In this paper, we propose a decision-tree-based classification method for Surface Mounting Device (SMD) electronic components. Decision trees can deal with numeric and categorical data and are understandable which helping analyzing drawing rules. Information in footprints, such as pads number, component height, and pin pitch from SMD components is considered as input features. Objective function of decision trees is adjusted to reduce leaf nodes of the tree. Thus, this method provides a better way to classify SMD electronic components and help analyzing design rule.

4. 10:56 – 11:08 (SB24) On Efficient Learning-based Performance Exploration for Analog Circuit Synthesis

   Po-Cheng Pan, Chien-Chia Huang, and Hung-Ming Chen

National Chiao Tung University

An efficient synthesis technique for modern analog circuits is important yet challenging due to the repeatedly re-synthesis process. To precisely explore the analog circuit performance limitation on the required technology is time consuming. This work presents a learning-based framework for searching the limitation of analog circuits. With hierarchical architecture, the dimension of solution space can be reduced. Bayesian linear regression and support vector machine model are selected to speed up the algorithm and better performance quality can be retrieved. Experimental results show that our approach on two analog circuits can achieve up to 9x runtime speed-up without surrendering performance qualities.

5. 11:08 – 11:20 (SB25) Machine Learning-based Pin Accessibility Prediction and Optimization during Placement

   Tao-Chun Yu and Shao-Yun Fang

National Taiwan University of Science and Technology

With the continuous scaling down of process nodes, standard cells become much smaller and cell counts are dramatically increased. Pin accessibility becomes one of the major issues causing design rule violations (DRVs). To tackle this problem, many recent works apply machine learning-based techniques to predict whether a local region has DRV or not by regarding global routing (GR) congestion and local pin density as the main features during the training process. Empirically, however, DRV occurrence is not necessary to be strongly correlated with the two features in advanced nodes. In this paper, we propose a deep learning-based DRV predictor without referring to GR congestion and pin density to identify whether a DRV will exist or not due to bad pin accessibility. Experimental results show that the proposed models are superior than those of previous studies in terms of all quantitative metrics. Additionally, the numbers of DRVs can be dramatically reduced by applying the proposed model-guided detailed placement flow.