

Session Oral 1 (8/7 Wed. 13:30 – 15:00)

Session Topic: Circuit Design for Advanced Sensing Applications

Session Chair: Kun-Chih (Jimmy) Chen (National Sun Yat-Sen University)

Room: 6F 樂廳

1. 13:30 – 13:43 (SA11) A CMOS Temperature-to-Digital Converter Based on a Chopped Continuous-time

Delta-Sigma Modulator

Po-Yu Li, Wei-En Lee, and Tsung-Hsien Lin

National Taiwan University

In this work, a resistor-based temperature is presented. The resistive temperature sensing module is embedded in a 2nd-order 1-bit continuous-time delta-sigma modulator (CTDSM) to realize a hardware- and energy-efficient temperature-to-digital converter. To achieve low noise, chopping technique is

applied to mitigate the mismatch and flicker noise of the first-stage amplifier. A finite impulse response (FIR) filter is added to the feedback path to address the noise fold-back that is attributed to the input dependent error voltage when using chopper. The proposed circuit consumes 183.6 μW from a 1.8-V supply voltage. The temperature range is -40°C to 100°C . At a single conversion time of 333 μs , the temperature resolution is better than 0.003°C ($1\ \delta$), which lead to a resolution FoM of $0.55\ \text{pJ}^\circ\text{C}^2$.

2. 13:43 – 13:56 (SA12) A Novel High-Resolution Area-Efficient All-Digital Temperature Sensor Design in Temporal Domain

Kun-Chih (Jimmy) Chen and Chung-Hsien (Joseph) Chiu

National Sun Yat-Sen University

Due to the advancement of the process technology, the power density of the modern System-on-Chip (SoC) is increased and results in serious thermal problem. Many dynamic thermal managements (DTMs)

were proposed in recent years, the full-chip temperature information is captured relying on the on-chip temperature sensors. The conventional temperature sensors contain ADCs to convert the temperature sensitive voltage/current signal to the digital output results. However, the area overhead of the conventional analog temperature sensor becomes large when the requirement of the temperature sensing accuracy becomes strict. To solve the problem, we adopt the feature of the temperature-sensitive signal propagation delay to design an all-digital temperature sensor. The proposed all-digital thermal sensor adopts one single delay line to generate a temperature-sensitive pulse, and the width of the pulse is proportional to the measuring temperature. Afterward, we involve the time-to-digital converters (TDC) to convert the pulse width information to the digital temperature information. By using the TSMC CMOS 0.18 μm process, the proposed all-digital temperature sensor can achieve more precise sensing resolution than the related works. The achieved sensing error is with -1.0°C to 1.0°C .

3. 13:56 – 14:09 (SA13) Power-efficient Cyclic Voltammetric Electrochemical Sensing Readout Circuitry with Current-Reducer Ramp Waveform Generation

Yi-Chia Chen, Shao-Yung Lu, Siang-Sin Shan, and Yu-Te Liao

National Chiao Tung University

This paper presents an electrochemical sensing chip with an integrated current-reducer pattern generator and a low-noise chopper-stabilization potentiostat circuit. The pattern generator, utilizing the current reducer technique and pseudo resistors, creates a sub-Hz ramp signal for the cyclic voltammetric measurement without large-size passive components. The proposed design adopts a chopper-stabilization potentiostat and time-based converter to reduce the amplitude noise effects. The design is fabricated using a 0.18- μm CMOS process and achieves a 41pA current resolution in the current range of $\pm 5\mu\text{A}$ while maintaining the R2 linearity of 0.998. The power consumption of the design is 16 μW when a 5 μA sensing current is detected. The power efficiency of the readout interface is 0.31 and

the sensing current dynamic range is 108dB. The design is fully integrated into a single chip.

4. 14:09 – 14:22 (SA14) A 2.4 GHz Gm-Boosted Complementary Current-Reuse Colpitts VCO with FoM of 189 dBc/Hz in 0.18 μm CMOS

Yu-Chieh Huang, Sheng-Kai Chang, and Kuang-Wei Cheng

National Cheng Kung University

This paper presents a differential Colpitts voltage-controlled oscillator (VCO) for low power and low phase noise applications. Gm-boosted and complementary current-reuse techniques improves the current efficiency and achieves low power consumption. In addition, a clover-shaped inductor is utilized for reduction of inductive crosstalk. The prototype VCO is fabricated in a 0.18 μm CMOS technology, and has a power dissipation of 1.4 mW from a 1.1-V supply voltage. The measurement results show that the VCO can operate at frequencies of 2.34 to 2.55 GHz with a tuning range of 8.6%, and achieves a phase noise of -122.85 dBc/Hz at 1MHz offset, with FoM of 189 dBc/Hz.

5. 14:22 – 14:35 (SA15) A 13.56-MHz Wireless Power Transfer Transmitter with Impedance Compression

Network for Biomedical Applications

Fu-Wen Chang and Ping-Hsuan Hsieh

National Tsing Hua University

A wireless power transfer (WPT) transmitter with class-E power amplifier is presented in this work. In the target application of implantable biomedical systems, variations of load condition and coil separation degrade the power transfer capability (PTC) and power conversion efficiency (PCE) significantly. In the proposed design, we adopted an impedance compression network (ICN) to compress the resulting impedance variation and to stabilize the performance. Duty-cycle control is introduced for further improvement. Designed and implemented with a 0.18- μm CMOS process, at 13.56 MHz, simulation results show that more than 30 mW of output power can be obtained with coupling coefficient from

0.06 to 0.30. The maximum output power is 58.97 mW, and the maximum power conversion efficiency is 54.4% with drain efficiency of 81.0%. Compared to conventional structures, the proposed design achieves wide dynamic range while meeting the target output power and efficiency.

6. 14:35 – 14:48 (SA16) A High-Efficiency Power Management IC with Power-Aware Multi-path Rectifier for Wide-Range RF Energy Harvesting

Hao-Yi Kuo, Shu-Hsuan Lin, Chen-Yi Kuo, and Yu-Te Liao

National Chiao Tung University

A highly-integrated CMOS power-management system with wide-range RF for ultra-high frequency (UHF) wireless energy harvesting is presented. To avoid environment-caused sudden power loss and to scavenge energy efficiently, the proposed power management system adopts power-aware rectifier architecture and adaptive DC-DC conversion ratios according to the input power level. The proposed

system was fabricated in a 0.18- μm CMOS process. The system achieved a peak RF/DC conversion efficiency of 59%, a sensitivity of -11.6dBm, and a 13.5dB RF input range for at least 20% power efficiency at a 100K Ω load. At the high input power region (>-9dBm), the proposed architecture improves to about 15% efficiency when compared to a conventional rectifier followed by a linear regulator. The peak efficiency of the entire system is 37%.

7. 14:48 – 15:01 (SA17) A High-Power-Efficiency Low-Input Low-Output Thermoelectric Energy Harvesting Interface for Internet-of-Things Devices

Meng-Jung Tsou, Tze-Yun Su, Philex Ming-Yan Fan, and Po-Hung Chen

National Chiao Tung University

This paper presents an energy harvesting interface for low-voltage energy-efficient Internet-of-Things (IoT) devices in standard 0.18- μm CMOS technology. The proposed boost converter along with the capacitive bootstrapping technique converts the voltage from a thermoelectric generator to a

near-threshold output voltage. The proposed capacitive bootstrapping technique generates a positive and negative bias pair to reduce the significant conduction losses of power transistors in a low-voltage operation. Besides, to efficiently extend the system's output power range, the internal bias voltages are automatically adjusted according to the loading conditions. The converter combines constant on-time technique with digital zero current detection to achieve both low power consumption and low reverse inductor current. The experimental results demonstrate a maximum power conversion efficiency of 76% over a 1 μ W–500 μ W load range.