國 立 中 正 大 學

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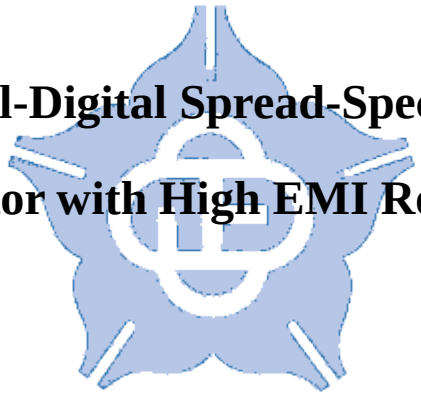
碩 士 論 文

具有極佳的電磁干擾效應衰減效果之全數位展頻時脈產生器



Design of All-Digital Spread-Spectrum Clock Generator with High EMI Reduction

研 究 生：何威達

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同意其提付 碩 士學位論文考試

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摘要

近年來，電磁干擾的議題越來越被重視。原因在於現今高速傳輸之電路通常會產生嚴重的電磁干擾，並容易影響周遭電路之運作。因此，為了防範電子產品中所衍生出來的電磁干擾，目前已有數種電子傳輸介面制訂相關規格以防制過於嚴重的電磁干擾，例如 DisplayPort 等數位顯示介面。

在本論文中，我們提出具有極佳電磁干擾效應衰減效果之全數位展頻時脈產生器。此全數位展頻時脈產生器可以達到真實展頻量之要求。此外，為了防止在展頻時遭遇製程、電壓、以及溫度變化而導致中心頻率偏移，我們以兩種不同版本之機制來維持頻率穩定度，其一為快速鎖定機制，另一機制為以計數器為基底來穩定頻率。

此快速鎖定之全數位展頻時脈產生器使用 90 奈米製程之標準元件庫實現，其運作電路之面積為 200μm × 200μm。由量測結果得知，在 270MHz 頻率之電磁干擾效應衰減量於 0.5%與 2%之展頻量分別為 14.64dB 以及 19.69dB。此外，該電路以 1.0V 電壓於 270MHz 頻率下之功率消耗為 443μW。另一版本之電路為以計數器為基底之全數位展頻時脈產生器。該電路之運作面積為 85μm × 85μm 並以 65 奈米製程之標準元件庫實現。其模擬之電磁干擾效應衰減量各以 270MHz 及 162MHz 作用頻率於 0.5%與 1.5%之展頻量分別為 13.99dB 與 20.23dB。此電路以 1.0V 電壓於 270MHz 頻率下之功率消耗為 163.9μW。另外，此兩版電路因為是以標準元件所設計而成，因此可以輕易的移植至不同製程，所以本論文所提出之全數位展頻時脈產生器非常適合應用於現今之系統晶片。

Abstract

In recent years, electromagnetic interference (EMI) problem is more and more popular. High speed transmission usually causes severe EMI, and that will influence the operation of neighbor circuits. Therefore, there are several devices have defined the specifications to restrict the EMI, such as DisplayPort which is a digital display interface.

In this thesis, an all-digital spread spectrum clock generator (ADSSCG) with high EMI reduction performance is presented. The proposed ADSSCG can provide a truly programmable spreading ratio. In order to maintain the frequency stability while performing triangular modulation, two frequency maintenance mechanisms are proposed to overcome the process, voltage, and temperature (PVT) variations. We proposed two versions of ADSSCG in this thesis, the fast-relocked ADSSCG and counter based ADSSCG.

The proposed fast-relocked ADSSCG is implemented in a standard performance 90nm CMOS process, and the active area is 200μm × 200μm. The experimental results show that the EMI reduction is 14.61dB with 0.5% spreading ratio and 19.69dB with 2% spreading ratio at 270MHz. The power consumption is 443μW at 270MHz with 1.0V power supply. The other version is the counter-based ADSSCG. The active area is 85μm × 85μm with a standard performance 65nm CMOS process. The EMI reduction is 13.99dB with 0.5% spreading ratio at 270MHz and 20.23dB with 1.5% spreading ratio at 162MHz. For the power dissipation, it consumes 163.9μW at 270MHz with 1.0V power supply. Moreover, these two versions are designed with standard cells, and this approach can be ported to different processes very easily, and it’s very suitable in system-on-chip (SoC) era.

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Chapter 1

Introduction

1.1 Electromagnetic Interference Overview

For most electronic equipment, phase-locked loop (PLL) is an essential circuit in these components. As the process technique grows up rapidly, the circuit area and its power consumption occupy less cost. Besides, the whole circuit operation frequency is much faster than several years ago. Hence, the modern very large scale integrated (VLSI) circuit design tends to small, faster, and low-power. These trends will be very important in system-on-chip (SoC) design.

In recent years, the high-speed clock generator is a more and more popular circuit due to the system requirement with the advanced process technology progress. However, there may exist severe electromagnetic interference (EMI) in the clock generator when its operation at higher frequency. The EMI may disturb the neighbor circuits, making these circuits work abnormally, especially for the SoC applications.

There are several types of sources induce EMI, one of the source is the clock generation from PLL. For instance, the diagram of DisplayPort [1] is shown in Fig.1.1. DisplayPort is a digital display interface which is used to connect the video source to a display device such as the computer monitor. The physical layer of DisplayPort is shown in Fig.1.2. DisplayPort physical layer requires a clock generator such as a PLL to provide a clock to the encoder, serializer, and clock-and-data recovery (CDR) circuit. That clock will induce the EMI, and then influence the operation of other

circuits in the physical layer.

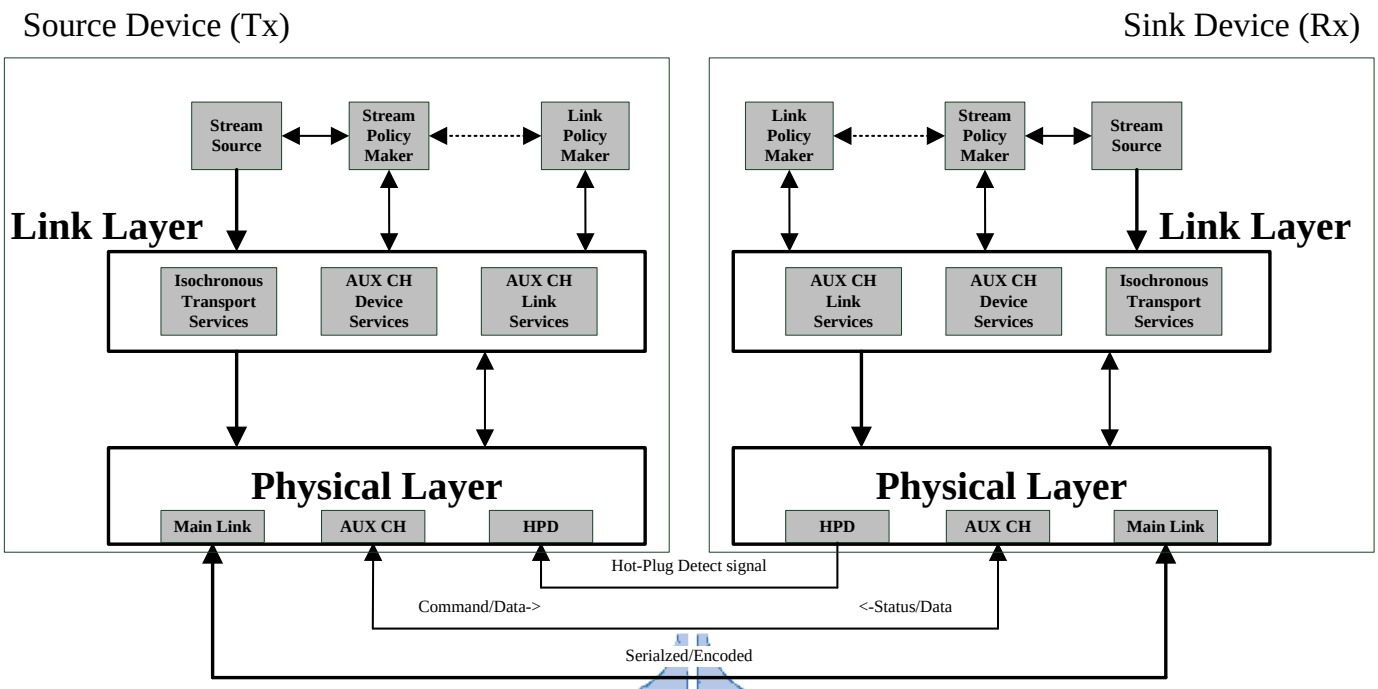


Fig. 1.1: The architecture of the DisplayPort.

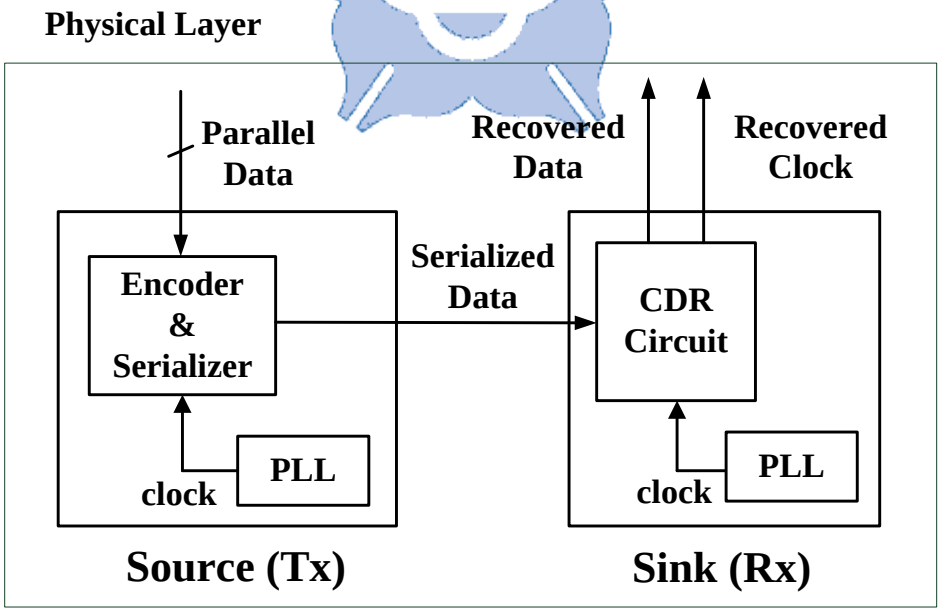


Fig. 1.2: The architecture of the DisplayPort physical layer.

The EMI will be severer as the PLL operating at higher frequency, higher voltage

and more current. The EMI usually arises from incidental radio frequency emitters, not only for the clock generators in VLSI nowadays, but also in other electric equipment such as electric motors, electric power transmission lines, bug zappers, thermostats, and so on.

1.2 Conventional Techniques of EMI Mitigation

The noise from other component usually causes the EMI, and will influence neighbor circuit operation. In order to prevent the interference, there are two commits, Federal Communications Commission (FCC) and CISPR which is under the commit of International Electrotechnical Commission (IEC), have made criteria on the amount of EMI that any piece of electronic equipment may radiate at any frequency. Hence, in order to overcome these noises, there are several techniques proposed to prevent the circuits from interfering. These techniques are metal shielding, pulse shaping filter, slew rate control, differential clocking, low voltage differential signaling (LVDS), spread-spectrum clocking, and so on.

Metal shielding [2] is a general solution to protect the neighbor circuits from EMI. Fig. 1.3 is the photo about the board level shielding. This technique can reduce the EMI by blocking the electromagnetic radiation. It is a commonly approach to against the EMI, especially for the system in a package (SiP) [2]. However, this technique may take too much cost in the SoC applications, because it will increase the area and weight of the whole system. Therefore, this technique is unsuitable for the SoC applications.

Fig. 1.3: Metal shielding to block external noise; this photo is captured from the ORBEL website of http://www.orbel.com.

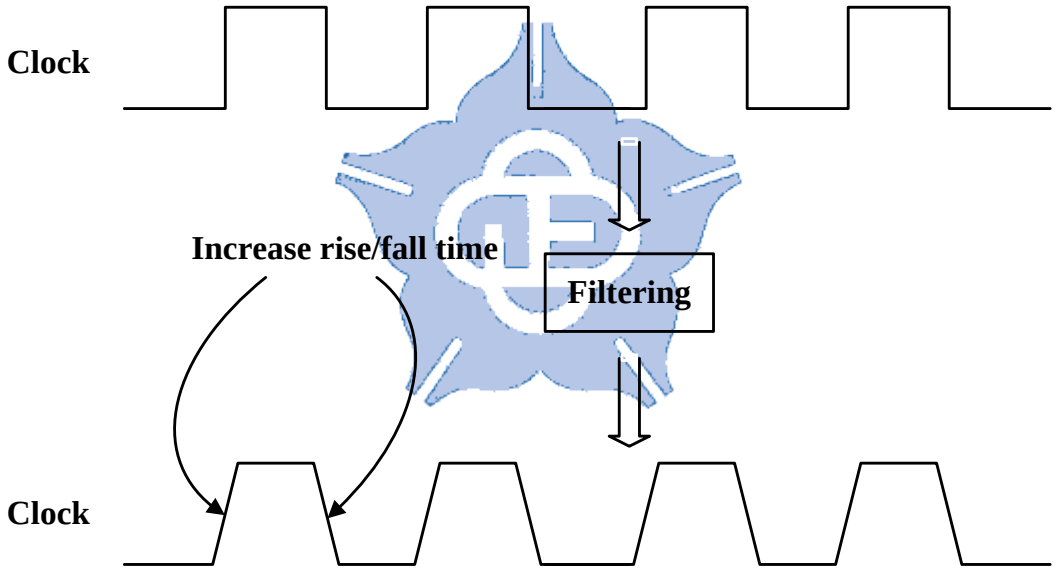


Fig. 1.4: Reduce peak power by pulse shaping filtering.

Pulse shaping filter [3] is the other technique to mitigate the EMI. One factor of peak power which is produced by the external clock is dependent on the clock rise time and fall time. Therefore, the electromagnetic radiation can also be reduced by filtering the rise time and fall time as shown in Fig. 1.4. However, this technique requires expensive cost of the chip area due to the extra filter, and it's hard to be

applied in high-frequency applications. Besides, the rise time and fall time may be deviated if the process, voltage, and temperature (PVT) variations occur. Moreover, the increased rise time and fall time may influence the jitter performance. Therefore, this technique is not suitable for modern VLSI circuits.

In order to improve pulse shaping filtering, slew rate controlling [4] is proposed. This method is similar to pulse shaping filtering technique, but there is still some difference. Slew rate controlling is proposed to control the output current to control rising edge and falling edge. With this technique, it's not only reduces the EMI but also improves the jitter performance. Nevertheless, the effect of EMI reduction is not very obviously, and this technique is hard to be implemented in high-frequency circuit, too.

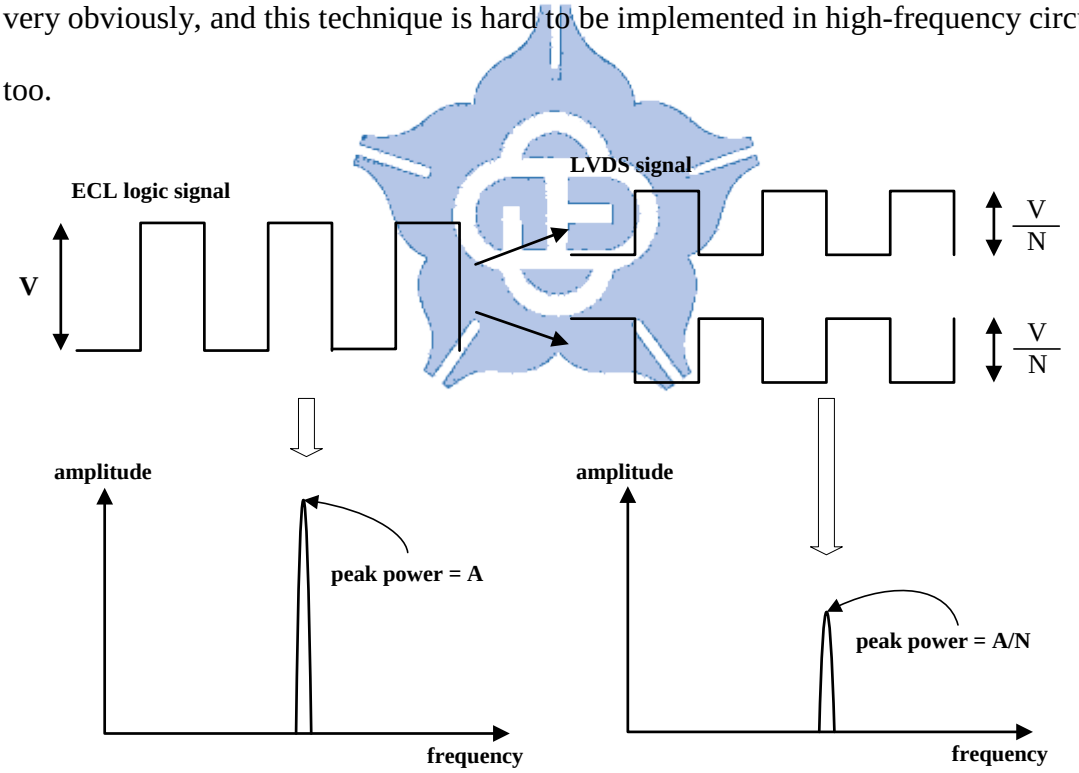


Fig. 1.5: Diagram of LVDS operation and its spectrum.

Low voltage differential signaling (LVDS) [5] is an effective technique to reduce redundant noise. It is based on two paths with low-voltage signal to replace

conventional emitter coupled logic (ECL) signal (Fig.1.5). This technique can integrate with low-voltage system, thus directly decreasing the signal level. With the decreasing signal, the spectrum amplitude is diminished. However, LVDS requires the complex routing and difficult implementation.

1.3 Introduction to Spread-Spectrum Clock Generator

There are some conventional approaches proposed to reduce EMI that discussed in Section 1.2. However, these techniques have some drawbacks. One of these drawbacks is expensive cost. The other drawback is the applicability in high-frequency system. Although LVDS can achieve the low cost and high frequency purpose, the system designing is very difficult. Therefore, spread-spectrum clock generator (SSCG) [6] is proposed to reduce the EMI with lower cost and simpler design complexity, and it's acceptable to apply the circuit to a high-frequency system.

Spread-spectrum clock generator is a PLL-based circuit. The spread-spectrum is realized with frequency modulation technique to disperse the energy of clock. For conventional PLL circuit, especially for high-frequency circuit, the output clock may bring severe EMI. In order to diminish EMI, some papers propose the spread-spectrum technique to mitigate this effect. With the spread-spectrum technique, the noise of the output clock can be dispersed to achieve a lower peak power. Fig. 1.6 shows the clock before and after spread spectrum. The red section is the spread-spectrum off state, and the peak power is very high. After turn on the spread-spectrum function, the peak power has been diluted to a lower magnitude. This phenomenon can lessen the EMI, and make the neighbor components operating

profitably.

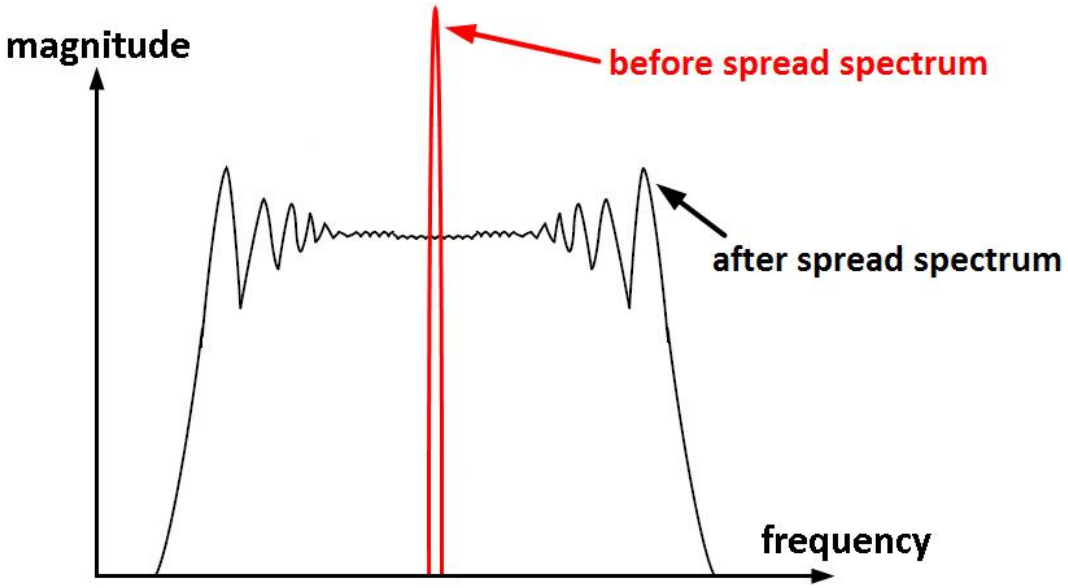


Fig. 1.6: Reduce peak power with spread-spectrum technique.

The SSCGs are widely adopted in many data transfer devices such as DisplayPort. Fig. 1.7 shows more detail architecture of Fig. 1.2. In the physical layer, it usually composes with scrambler, encoder, and parallel-to-serial (P-to-S) converter in transmitter. On the other side, the receiver is composed with de-scrambler, decoder, and serial-to-parallel (S-to-P) converter. The both sides require PLL to drive P-to-S converter and S-to-P converter. In order to reduce EMI, it uses SSCG to replace PLL. Besides, it requires a CDR circuit in front of S-to-P converter to recover the serialized data and spread-spectrum clock.

The EMI problems not only exist in PLL but also exist in transferred data. Once the parallel data consist of regular patterns, this phenomenon will result in severe EMI. Therefore, it usually requires a scrambler in the transmitter and a de-scrambler in the receiver. In Fig. 1.7, the scrambler will transposes the repeated pattern, and recover the unintelligible data by de-scrambler.

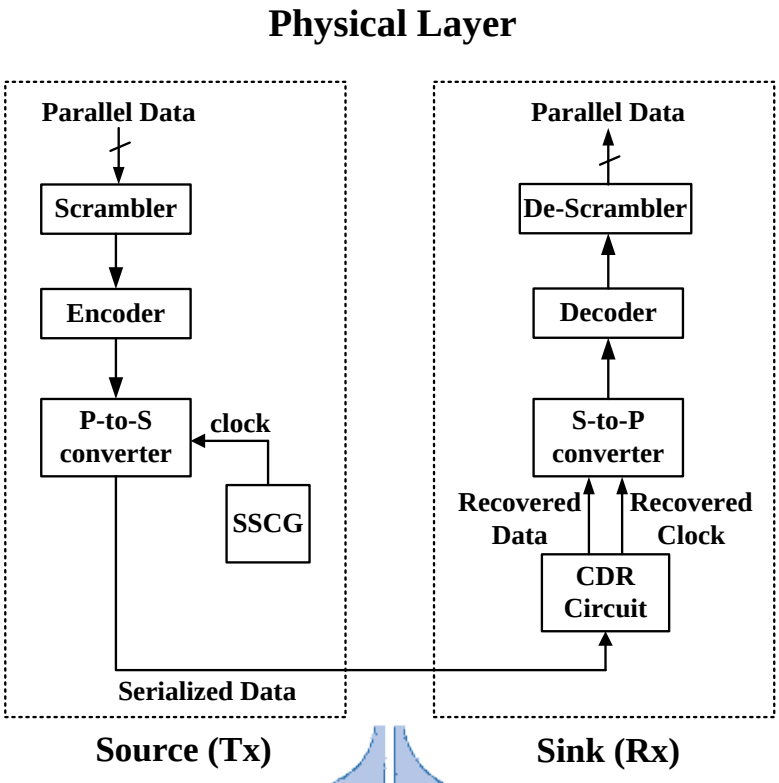


Fig.1.7: Detail architecture of DisplayPort physical layer.

To compare with conventional approaches, SSCG has the advantages of low cost, easy for integration, high-frequency operation, and excellent EMI reduction performance. Hence, this approach is widely adopted in SoC applications, and this topic is more and more popular.

Chapter 2

Concepts of Spread-Spectrum Clock Generator

2.1 Modulation Type

Spread spectrum is the technique to disperse the energy of clock to close-by frequency domain. According to the dispersed frequency direction, spread spectrum is classified into three modulation types. Fig. 2.1 shows the different modulation types, up-spread, center-spread, and down-spread.

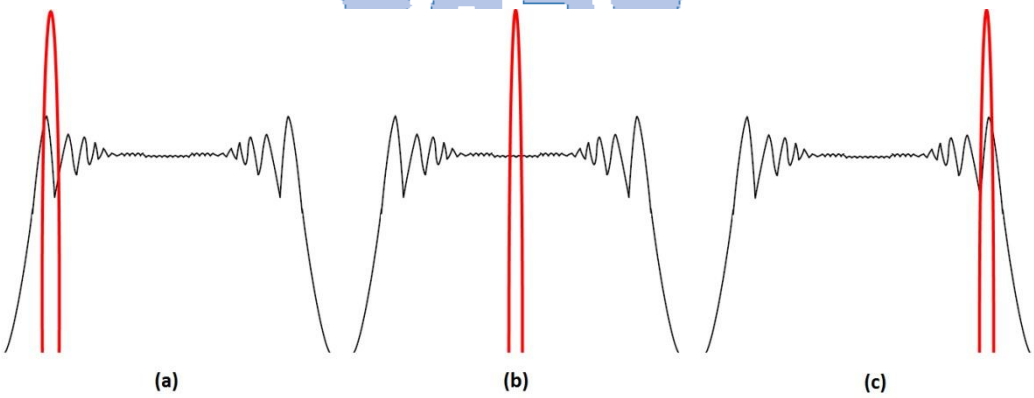


Fig. 2.1: Modulation type of (a) up-spread (b) center-spread (c) down-spread.

Up-spread modulates the frequency domain to a faster frequency range (Fig. 2.1(a)). This modulation type is seldom adopted in integrated system. Because the received circuit may not work due to the original timing constraint is to operate in the nominal frequency. Most designs are still adopted center-spread or down-spread to

develop their circuit, and the up-spread is usually an appendant function [7] with these two modulation types.

Center-spread is the type to disperse its frequency domain to the neighboring region as shown in Fig. 2.1(b). Unlike up-spread, the output frequency is not only extends to a higher frequency, but also extends to a slower frequency than nominal frequency [8]. In other words, there are half time of spread spectrum operating in a higher frequency than nominal frequency and the other part operating in a lower frequency. Unavoidably, the disadvantage of center-spread is the higher than nominal frequency as up-spread. Nevertheless, the long-term-average frequency of spread spectrum is close to the un-spread-spectrum state, making it more convenient to maintain the frequency stability. Besides, in the same spreading ratio, the maximal difference of center-spread between nominal frequency and spread-spectrum frequency is less than up-spread and down-spread. Therefore, in the same maximal frequency difference, the EMI reduction of center-spread will make the best effect than the other two modulation types. In this thesis, our proposed SSCG is adopted center-spread as our modulation type according to these above characteristics.

The last modulation type, down-spread [9], is a modulation type that decelerates the output frequency to perform spread spectrum (Fig. 2.1(c)). Because the spread-spectrum frequency is slower than the nominal frequency, the timing constraint will not be concerned. This modulation type is widely adopted in SSCG because it can integrate with other system very easily, that make it be designed in SoC applications. Therefore, most specifications like Serial ATA [10], USB [11], PCI Express [12], and DisplayPort [1] main link support spread-spectrum with down-spread in their system.

2.2 Relationship between Several SSCG Parameters and EMI Reduction

In reality, the EMI reduction effect is theoretically depended on the following equation [13]:

$$A_{dB} = 6.5 + 9\log\left(\frac{R_{\%}}{100}\right) + 9\log\left(f_{MHz}\right) \quad (2.1)$$

From Eq. 2.1, A_{db} is the result of EMI attenuation, $R_{\%}$ is spreading ratio, and f_{MHz} is operation frequency. This equation is the theoretical formula for a general case. However, in reality circuit application, spreading ratio and operation frequency are not the only two parameters to decide EMI reduction.

There are several parameters that may deteriorate the performance of EMI reduction. These parameters are very important, and they are modulation profile, spreading ratio, modulation frequency, and operation frequency [14]. Because these parameters not only decide the EMI reduction but also influence the circuit cost, such as the active area and power consumption. Therefore, it is important to decide appropriate values to these parameters.

2.2.1 Modulation Profile

Modulation profile is the plan composed with frequency domain and power magnitude. Due to different frequency modulation manner, the output clock will generate different modulation profile, too.

There are many modulation profiles for SSCG, and the essential profiles are

sinusoidal modulation, triangular modulation, and Hershey-Kiss modulation [6]. Fig. 2.2 shows the relationship between three modulation profiles and their power spectral density respectively.

Sinusoidal modulation is a basic modulation profile (Fig. 2.2(a)). As implied by the name, sinusoidal modulation generates the spread-spectrum clock in the frequency domain with a sinusoidal waveform as Eq. 2.2:

$$f_{MHz} = \sin(2\pi \cdot f_m \cdot t) \tag{2.2}$$

Where f_{MHz} is the operation frequency, f_m is modulation frequency, and t is clock execution time. However, this modulation profile is difficult to be implemented in SSCG. Besides, the peak power of the spectrum is at both sides, and that will decrease the performance of EMI reduction. Therefore, this modulation profile is rarely adopted in the SSCG.

The other modulation profile is triangular modulation [15]. This profile generates the spread-spectrum clock in the frequency domain with a triangular waveform as shown in Fig. 2.2(b). The equation is shown in Eq. 2.3:

$$f_{MHz} = \frac{8}{\pi^2}\sum_{k=0}^{\infty}\left[(-1)^k \cdot \frac{\sin((2k+1)f_m \cdot t)}{(2k+1)^2}\right] \tag{2.3}$$

Eq. 2.3 is the infinite Fourier series to converge to the triangle wave [16]. Although the equation is very complicated, it's easy to be implemented in the circuit. The SSCG only requires speed up or slow down the output clock linearly to achieve spread-spectrum purpose. Besides, the EMI attenuation is better than sinusoidal modulation. Therefore, this approach is more and more popular and is a major

modulation profile for SSCG. In this thesis, our proposed design also adopts triangular modulation as our modulation profile.

The last modulation profile is Hershey-Kiss modulation [17]. Fig. 2.2(c) shows the frequency profile. This profile increases the frequency occupation time in the nominal frequency, and decreases the occupation time of both side of frequency domain. Eq. 2.4 shows the Hershey-Kiss profile with a third-order equation:

$$f_{MHz} = \begin{cases} 0.45t^3 + 0.55t, & \text{if } -1 \le t \le 1 \\ -0.45(t-2)^3 - 0.55(t-2), & \text{if } 1 \le t \le 3 \end{cases} \quad (2.4)$$

This modulation profile can maintain the power spectral density as a flatten spectrum. Therefore, the peak power can be reduced because of the equally distributed amplitude. However, the circuit implementation with this modulation profile is very difficult. Some articles have proposed the SSCG with Hershey-Kiss modulation. Nevertheless, these circuits also paid a heavy price like the large chip active area, and require static random access memory (SRAM) to record the modulation profile [18]. Although there is a smaller area SSCG with Hershey-Kiss reported recently [19], the profile is hard to be controlled and result in a worse spectrum profile.

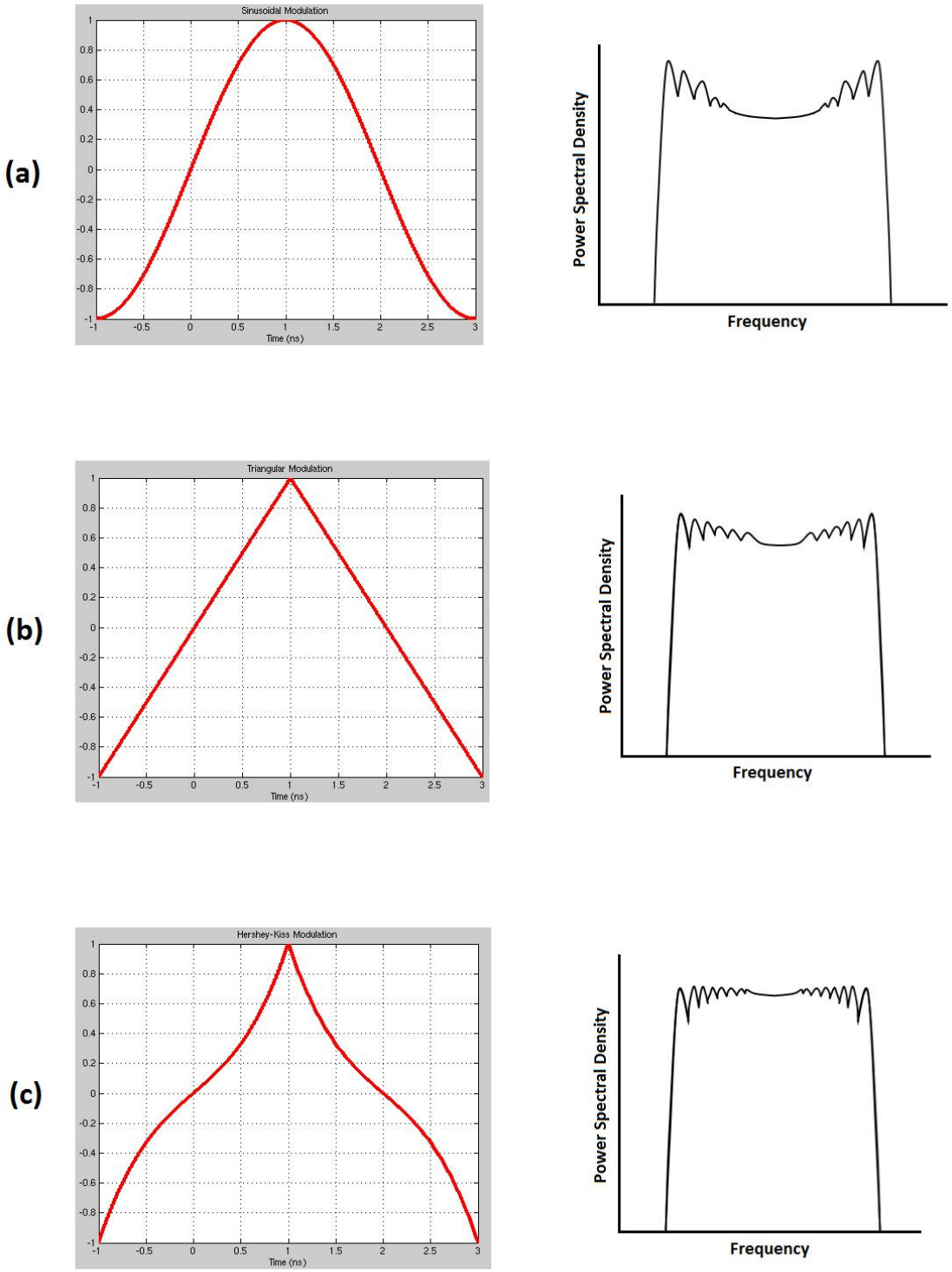


Fig. 2.2: Modulation profile of (a) sinusoidal modulation (b) triangular modulation (c) Hershey-Kiss modulation.

2.2.2 Spreading Ratio

Spreading ratio is a key point to decide the EMI reduction. The larger spreading ratio is set, the higher EMI reduction can be achieved. Fig. 2.3 shows the relationship between EMI attenuation and spreading ratio with the same output frequency (270 MHz) and modulation frequency (31.25 kHz) with a triangular modulation.

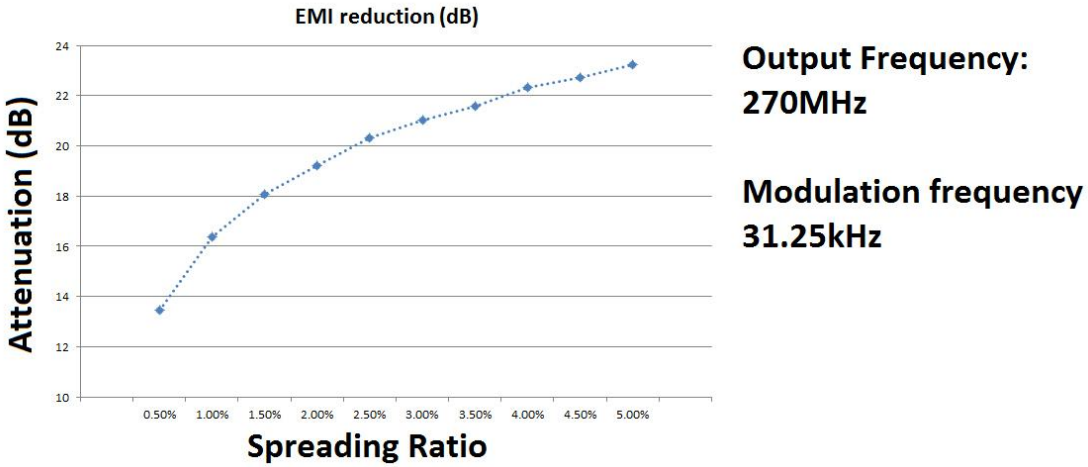


Fig. 2.3: Relationship between EMI reduction and spreading ratio.

In Fig. 2.3, we can see that the EMI reduction is slightly increased with the enlarged spreading ratio. Hence, the wider spreading ratio can have more EMI reduction. Nevertheless, wider spreading ratio may influence the performance of whole chip operation if the spreading ratio is too large. The spread-spectrum clock slows greatly than the nominal frequency will decrease the circuit performance. Oppositely, the spread-spectrum clock fastens greatly than the nominal frequency will suffer from the timing violations.

Therefore, most SSCGs are designed with 0.5% (5000ppm) spreading ratio, because the 0.5% spreading ratio is enough. Due to this reason, there are rare applications specify the SSCG to perform spread spectrum with more than 0.5 % spreading ratio.

2.2.3 Modulation Frequency

Modulation frequency is an important parameter to make a great impact on the EMI reduction performance. Fig. 2.4 shows the experimental result for the relationship between modulation frequency and EMI reduction with the same output frequency (270 MHz) and the same spreading ratio (1.0%).

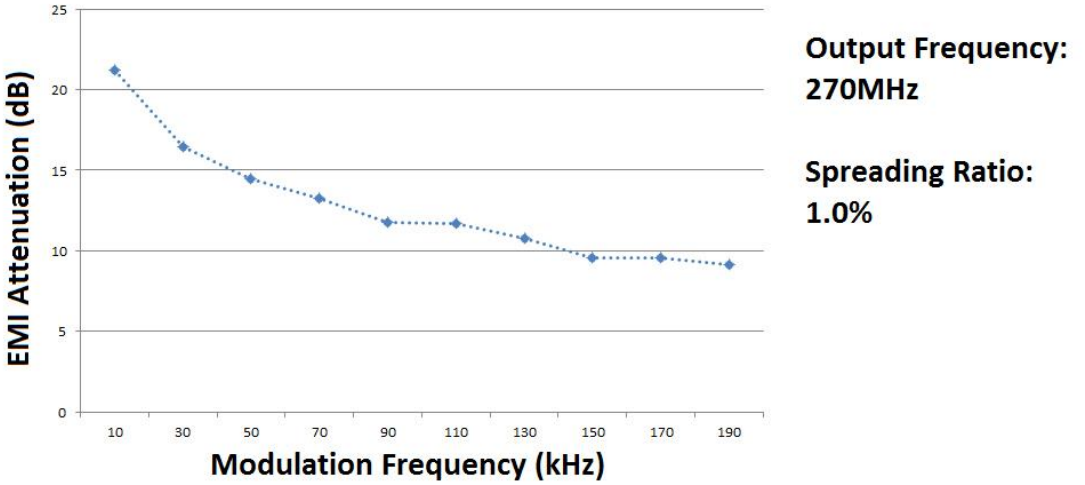


Fig. 2.4: Relationship between EMI reduction and modulation frequency.

In Fig. 2.4, we can see that the lower modulation frequency can make a better EMI attenuation effect. Higher modulation frequency will result a poor EMI reduction. Besides, the higher modulation frequency may be opaque to the whole system, and make the receiver circuit harder to take over the input signal.

Although the lower modulation frequency can make a better EMI attenuation effect, too slow modulation frequency is not allowed. Once the modulation frequency is slower than 30 kHz, it's probably detected by the FM receivers. Therefore, the modulation frequency is usually defined in the range between 30 kHz to 50 kHz.

2.2.4 Operation Frequency

The operation frequency of the SSCG is the other parameter to determine the EMI reduction. Fig. 2.5 is the figure about the relationship between EMI reduction and the operation frequency with the same condition in spreading ratio (1.0%) and modulation frequency (31.25 kHz).

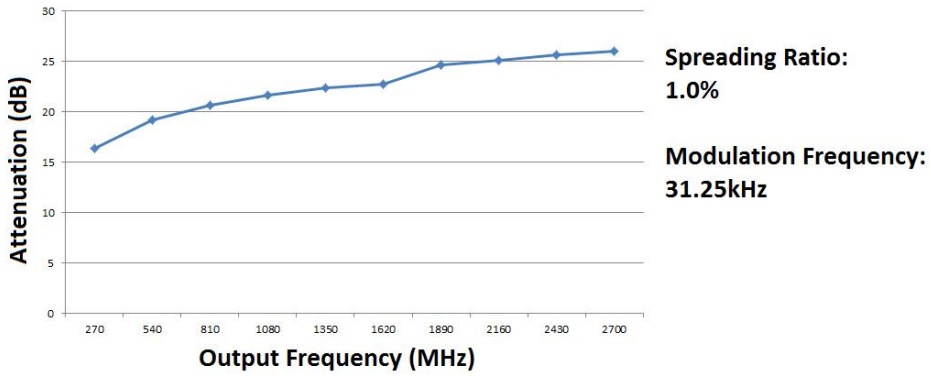


Fig. 2.5: Relationship between EMI reduction and operation frequency.

In Fig. 2.5, we can see that the EMI reduction is proportional to the output frequency. The reason for this phenomenon is that higher operation frequency without spread spectrum will cause the higher peak power. Therefore, the effect of peak power variation between a spread-spectrum clock and a spread-spectrum-off clock is more obvious.

2.3 Modulation Method

Nowadays, there are numerous SSCG researches published. These SSCGs are proposed with different approaches to improve the relative performance. However, these SSCGs can be grouped as four modulation methods. These methods are modulation on reference clock, modulation on oscillator, modulation on output clock,

and modulation on frequency divider.

2.3.1 Modulation on Reference Clock

The initial concept of SSCG is proposed in 1994 [6], and it is proposed with the modulation type on reference clock. This modulation type is very intuitively. Fig. 2.6 shows the operation of the modulation type on reference clock. It modulates the pulse width of reference clock which fed into the PLL. With the modulated pulse width of the reference clock, PLL will keep tracking the reference clock to adjust output frequency, and achieve the spread-spectrum effect. This technique achieves a simple idea to perform spread spectrum with an external resource. However, that may cause jitter once the reference clock transmits the modulated clock to the PLL. Therefore, this method is unreliable, because modulation on reference clock usually suffers the unexpected jitter, and that may cause the PLL clock output irregularly. Hence, this modulation method is hardly any adopted in recent years. Most of SSCGs are adopted with the other three modulation methods.

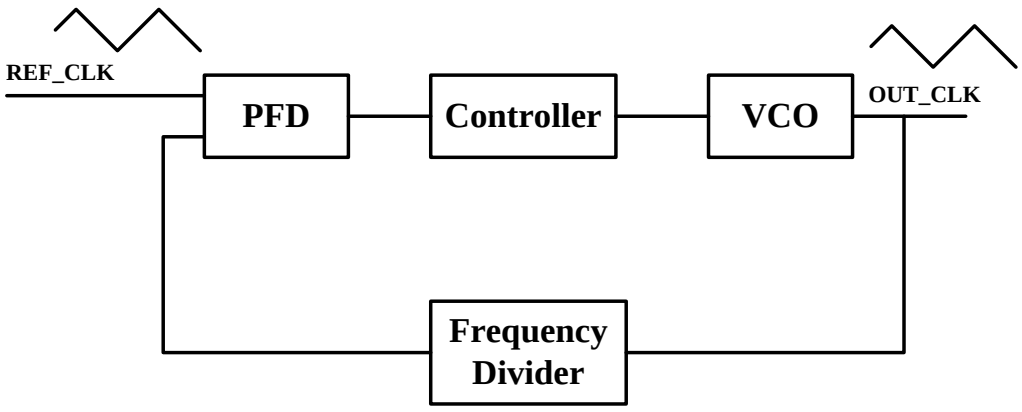


Fig. 2.6: Modulation on reference clock.

2.3.2 Modulation on Oscillator

The other modulation method is modulation on DCO or on VCO [20]. Because the output frequency is controlled by oscillator, directly controls DCO or VCO is a straight approach to perform spread spectrum. Therefore, it's a simpler modulation method to implement SSCG. Furthermore, this approach can result a better EMI reduction because of the directly modulation on the oscillator. Fig. 2.7 shows the architecture of this modulation method.

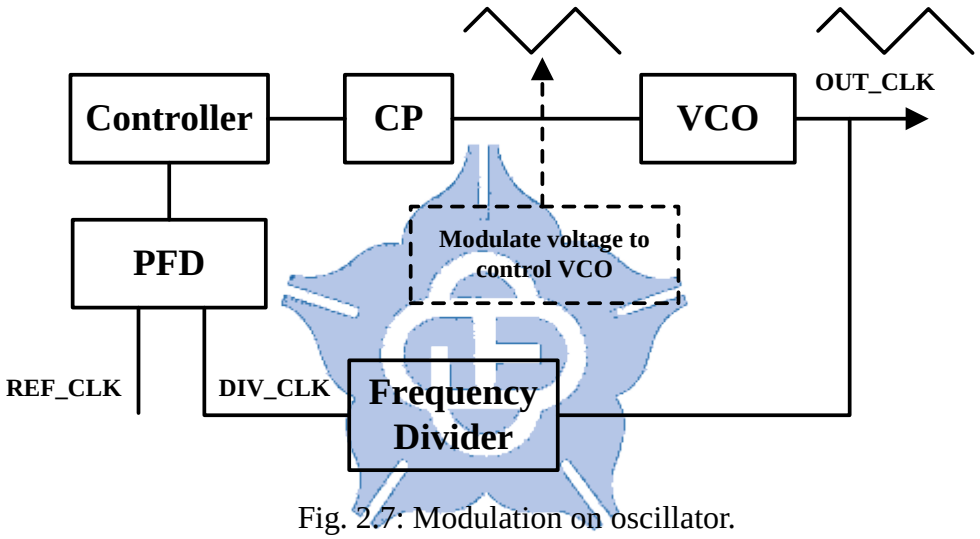


Fig. 2.7: Modulation on oscillator.

In this thesis, we adopt this modulation method to implement our SSCG. With the digital approach, the SSCG directly modulates DCO control code to perform spread spectrum very easily. Besides, the digital approach with DCO modulation can also perform an accurate triangular modulation profile.

This modulation method has several disadvantages. The critical drawback is that it cannot against PVT variations. In other words, most SSCG with this modulation method have no solution to avoid the PVT variations. Therefore, if there is any PVT variation existed, the average frequency will be changed, and then the output

frequency diverges from the nominal frequency. Furthermore, this modulation method cannot decide the exactly spreading ratio. If the PVT variation occurs, not only the average frequency is diverged but also the spreading ratio will be inaccurate with the expected value. Therefore, how to overcome these problems becomes an important issue in this modulation method. Leaving these drawbacks aside, modulation on oscillator still have a good performance for EMI reduction. Therefore, this method is widely chosen in the SSCG.

2.3.3 Modulation on Output Clock

Modulation on output clock is a recently proposed approach to perform spread spectrum. This modulation method is proposed to control the output clock, and then modulate the output clock using the digital controlled delay line (DCDL) [21] or phase selector [22] (Fig. 2.8).

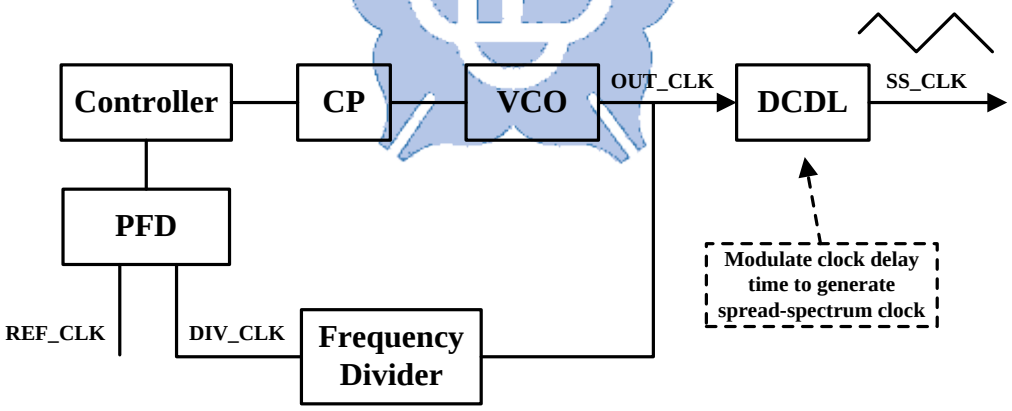


Fig. 2.8: Modulation on output clock.

This modulation method can be realized with an all-digital approach. With the DCDL, the modulation profile can be decided more flexibly. Besides, the output clock before feeding into the DCDL is in the lock state. Therefore, this approach has a higher stability as compared with other modulation method.

Although this modulation method has the above advantage, there are still some drawbacks exist. The most evident drawback is the circuit cost. This SSCG is based on a PLL with an additional DCDL, and the additional DCDL may occupy larger chip area and consumes more power. Besides, due to the input clock of DCDL is from the PLL clock, the operation of DCDL is at high frequency. If the SSCG is developed for a high-speed application like SATA [10], the whole chip of DCDL may not work in such high frequency.

2.3.4 Modulation on Frequency Divider

The last modulation method is modulation on frequency divider [23]. Fig. 2.9 shows the architecture of this modulation method. The frequency divider changes the divide ratio to modulate the divided clock, after getting the modulated-divided clock, the output clock will be adjusted to perform spread spectrum. From Fig. 2.9, we can see that it's a typical fractional-N PLL (FNPLL).

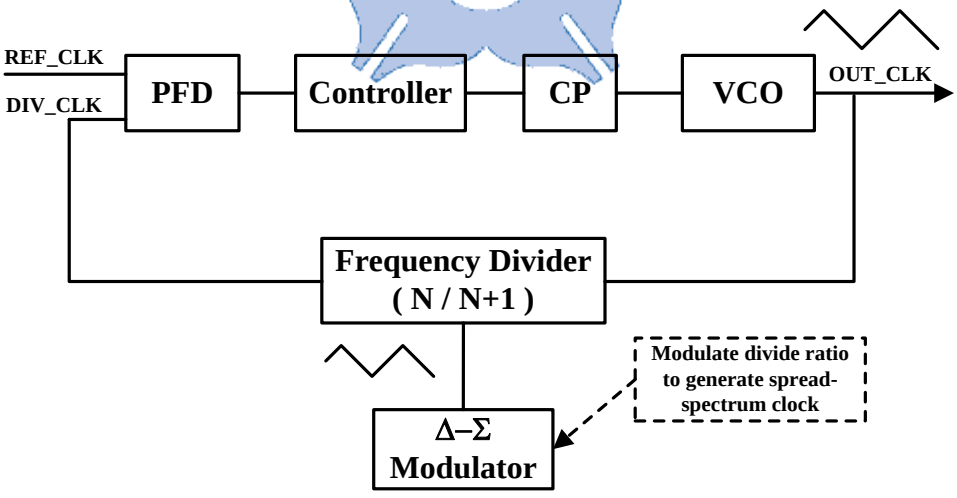


Fig. 2.9: Modulation on frequency divider.

With this modulation method, it can realize more accurate spreading ratio, because it modulates the divide ratio approach to control the frequency divider and

perform relative spreading ratio. Besides, no matter the whole loop is in spread-spectrum state or not, the PLL is keeping tracking the divided clock stably. Hence, this modulation method has a better jitter performance. Moreover, the EMI reduction is better than the modulation on reference clock and modulation on output clock. Furthermore, the circuit cost compares with other method, also occupies smaller area.

Modulation on frequency divider is the most popular method because of the above advantages. However, there are still some disadvantages exist. First, the circuit design requires a very carefully plan. That will increase the design difficulty. Besides, the modulation profile is hard to maintain. When the frequency modulation is in the polarity of speeding up and slowing down, the generated modulation profile is probably flatter than the ideal triangular modulation profile as shown in Fig. 2.10(a). This phenomenon may decrease the EMI reduction effect as shown in Fig. 2.10(b). From Fig. 2.10(b), the peak power is at the both sides, and thus results worse EMI reduction effect.

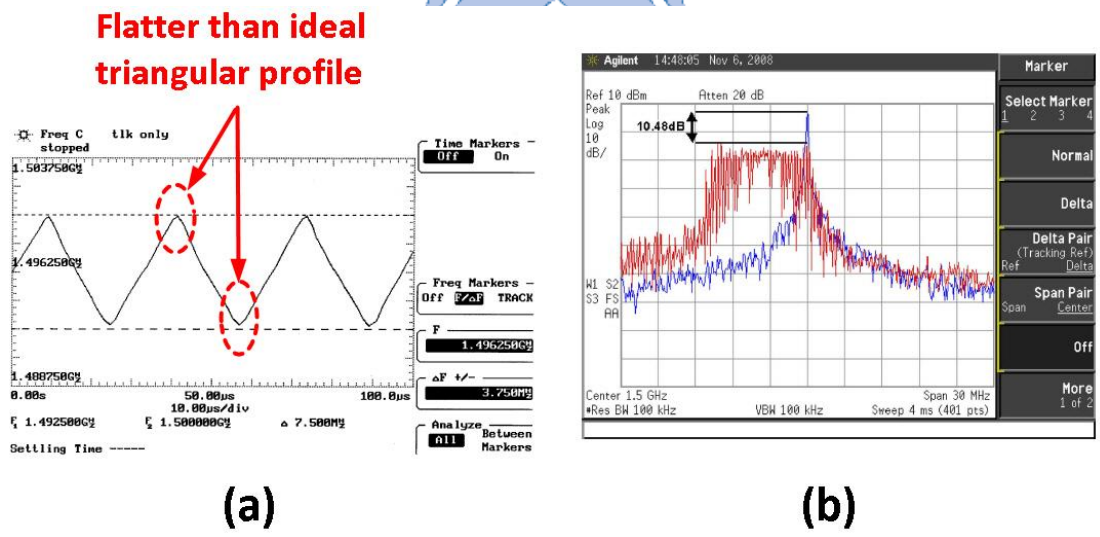


Fig. 2.10: Drawback of modulation on frequency divider; the two figures are captured form [24] (a) modulation profile (b) the corresponding power spectrum.

2.4 Drawback of Conventional SSCG

2.4.1 SSCG with Analog Approach

The concept of SSCG is proposed two decades ago [6]. After the concept proposed, this topic is more and more popular because SSCG is necessary for many applications. Most papers are proposed the SSCG with analog approach. The analog approach can implement SSCG for high-speed applications. Therefore, there are many SSCGs proposed for the high speed applications like SATA-I to SATA-III [10] and USB 1.0 to USB 3.0 [11].

The above discussion is the advantage of analog SSCGs. However, in order to perform small amount of spreading ratio, analog SSCG usually requires a large capacitor to perform spread spectrum. For instance, the modulation method on frequency divider, due to the quantization noise of divider, usually requires a large on-chip capacitor [25]. Besides, the other method, modulation on VCO, also requires a large on-chip (Fig. 2.11(a)) even the off-chip capacitor (Fig. 2.11(b)) as the loop filter to realize the spread spectrum. Up to now, all the analog SSCGs occupy very large area.

The other drawback is process issue. The analog SSCG have to re-design the whole chip if it's ported to different process. This problem will make it be unsuitable for SoC applications. Besides, as the progress of advanced process technology with lower supply voltage, the analog approach will suffer severe leakage current and narrow working range.

As the above result, the analog SSCGs have some critical disadvantages, and are not suitable for the advanced process technology. Therefore, to implement the SSCG with digital approach is a trend.

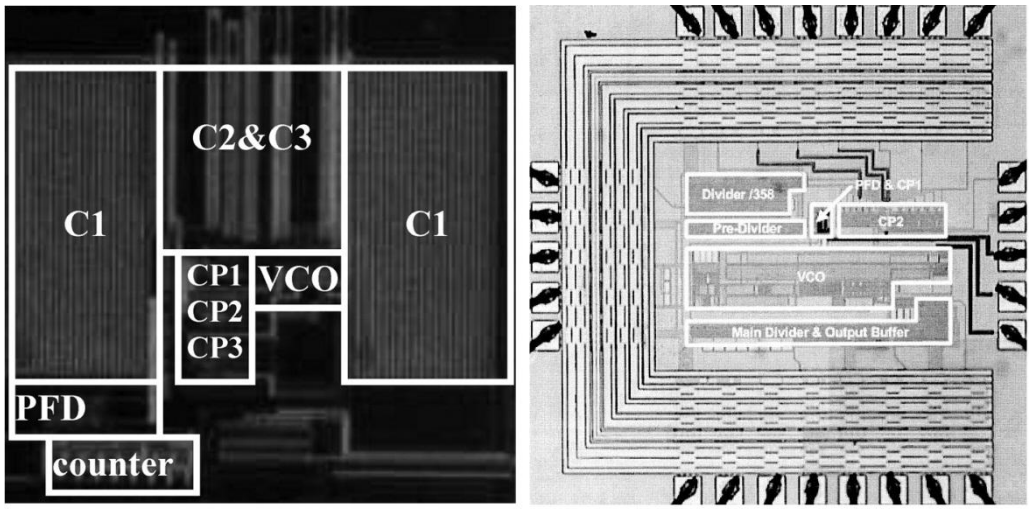


Fig. 2.11: Chip micrograph of analog SSCG (a) add large on-chip capacitors [20] (b) add on-chip and off-chip capacitors [15].

2.4.2 SSCG with Digital Approach

The published paper amount of digital SSCGs is less than analog approach. However, due to the progress of advanced process technology, more and more all-digital SSCGs (ADSSCG) had been proposed in recent years.

At first, the ADSSCG is proposed with the modulation method on output clock in 2007 [21]. After that, the methods of modulation on DCO [26] and on frequency divider [24] are proposed one after another. These ADSSCGs have the characteristics of low power and small area purpose. Besides, due to the output frequency is decided from DCO code which is provided from controller. It can achieve a quick lock-in time when the loop is restarted after circuit stall mode. For instance, in order to save more power consumption, some SSCGs may not always in execution. They may be in stall state when the receiver circuit goes off, and are restarted when the receiver circuit requires the clock resource. In this case, analog SSCGs have to restart to search for the correct output frequency, and this approach usually take a long lock-in time (Fig.

2.12(a)). In digital SSCGs, they can record the DCO code at lock-in state, and restore the DCO code when the SSCG is restarted as shown in Fig. 2.12(b). Hence, the digital approach can shorten the lock-in time even though the loop is restarted.

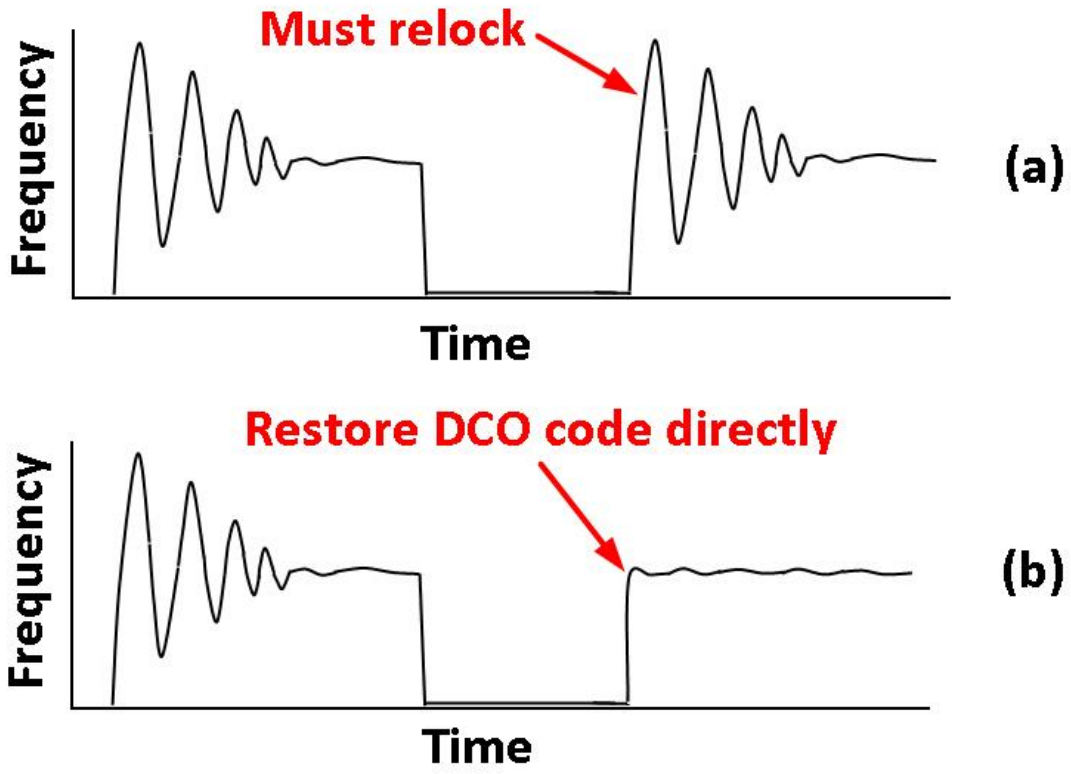


Fig. 2.12: SSCG in the restart situation (a) analog SSCG (b) digital SSCG

The digital approach can reduce more chip area and achieve lower power consumption. However, due to the limitation of output frequency, there is no high-speed ADSSCG proposed yet. Besides, the DCO resolution is the other issue. A high resolution DCO can disperse the frequency domain more averagely, but most DCO for ADSSCG are designed with worse resolution. The other important problem is the non-monotonic problem [27]. In order to achieve a low-power ADSSCG, the DCO usually adopted the ladder-shaped ring oscillator. This approach can reduce redundant power consumption. Nevertheless, there may be some overlapped frequency range in spread spectrum.

There is another ADSSCG proposed with the modulation on frequency divider [24]. In this paper, the DCO resolution is enhanced enough to disperse the frequency domain averagely. However, this DCO will cause the narrow output clock range. Besides, as compared with other ADSSCG, this approach cannot support a programmable spreading ratio. Moreover, due to the modulation on frequency divider, the triangular modulation profile has some region been more concentrative, that may result a worse EMI reduction performance.

2.4.3 Conventional Programmable SSCG

For the widely application, some SSCGs are proposed with a programmable spreading ratio. The programmable spreading ratio can make SSCG more flexibly. With the variety spreading ratio, it can change different conditions to achieve required EMI reduction.

Currently, there are three major methods to implement a programmable SSCG. First method is setting different divide ratio to perform different spreading ratio [28]. This method can realize more correct spreading ratio. However, this approach may increase the design complexity of delta-sigma modulator. Therefore, the programmable SSCG is hardly developed with this modulation method.

The second method is modulating output clock from PLL clock with DCDL or phase selector [29]. As we discussed in Section.2.3.3, this approach can achieve any modulation profile. Therefore, this method can also implement with a programmable spreading ratio. However, it certainly produces some problems like the implementation cost.

The third method is directly changes the oscillator [27]. No matter this method controls the DCO with changing control code ratio or controls the VCO with

changing voltage control ratio to achieve programmable ratio, their implementations are both simpler than the first method. However, it cannot maintain the same spreading ratio if there exists PVT variations. For example, if the ADSSCG turn on spread-spectrum function with 1.0% spreading ratio, it may spread five DCO control code to perform the appropriate spreading ratio in the initial planning stage (Fig. 2.13(a)). After suffering the temperature variation, the SSCG still spread five DCO control code to perform spread spectrum, while the actual spreading ratio may be changed to 1.5% spreading ratio (Fig. 2.13(b)). This situation may cause the timing violation in the whole chip operation. Therefore, how to provide a correct spreading ratio is a very important issue.

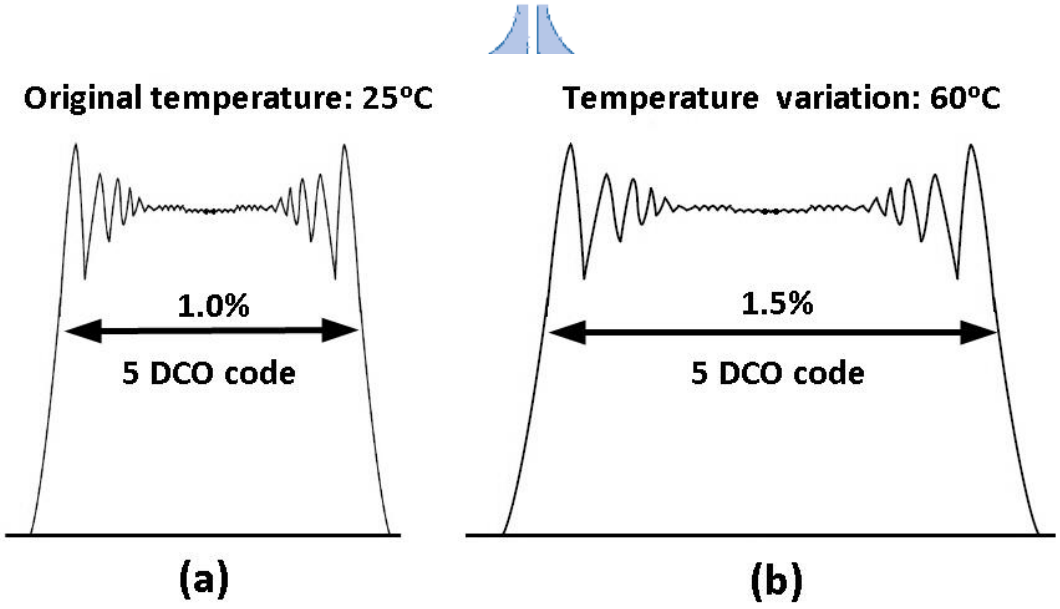


Fig. 2.13: Spreading ratio with the same spread DCO code (a) 1.0% spreading ratio in 25°C (b) 1.5% spreading ratio in 60°C

Chapter 3

Architecture of All-Digital Spread-Spectrum Clock Generator

3.1 The Proposed Fast-relocked ADSSCG

From Chapter 2, different modulation methods have been introduced individually, and we integrate these modulation methods into a comparison table in Table 3.1.

Table 3.1: Comparison of the four modulation methods

	Reference clock	**DCO/VCO**	**Output clock**	**Frequency divider**
Implementation difficulty	Simple	Simple	Complex	Complex
Area cost	Low	Low (digital) / High (analog)	High	Median
Power consumption	Low	Low (digital) / High (analog)	High	Median
High frequency supportability	Inappropriate	Appropriate	Inappropriate	Appropriate
Spreading ratio supportability	Bad	Good	Good	Median
EMI reduction	Bad	Good	Median	Median
Frequency stability	Bad	Bad	Good	Median

From Table 3.1, we can see that the two modulation methods of modulation on

DCO/VCO and modulation on frequency divider have more advantages than the other two methods. Modulation on DCO/VCO has more advantages than modulation on frequency divider. However, the frequency stability is a very important issue for SSCG. The poor frequency stability means that the SSCG cannot against PVT variations. Actually, the modulation method on VCO/DCO not only suffers frequency drift in spread-spectrum state but also influence the spreading ratio. Consequently, most SSCGs choose the method on frequency divider rather than modulation on DCO/VCO, because modulation on frequency divider can achieve better frequency stability. Therefore, in order to overcome the PVT variation, we proposed two versions of ADSSCG to maintain frequency stability.

In Section 3.1, we will propose our ADSSCG to improve the drawbacks of conventional SSCGs. The proposed fast-relocked ADSSCG is our version 1 ADSSCG, and this circuit achieves the advantages of high EMI reduction performance, low power, small area, truly programmable spreading ratio, and high frequency stability.

3.1.1 Fast-relocked Mechanism

3.1.1.1 Difficulty of SSCG Stability

When SSCG is in spread-spectrum state, it does not have external information to maintain the average frequency. This may influence the nominal frequency especially for the modulation on DCO/VCO method. Fig. 3.1 shows the SSCG in spread-spectrum state, where REF_CLK is reference clock and DIV_CLK is divided clock. There is almost no phase error between REF_CLK and DIV_CLK before spread spectrum like the lower-left portion of Fig. 3.1. However, in the spread-spectrum state, it will perform spread spectrum, and not refer to the reference

clock information. This will let the nominal frequency be drifted. The lower-right portion of Fig. 3.1 is at the end of one modulation cycle. In the end of the profile, the phase error between REF_CLK and DIV_CLK is increased. It's probably suffered the PVT variation in spread-spectrum state, and the nominal frequency may be changed if there is no mechanism to re-track the frequency.

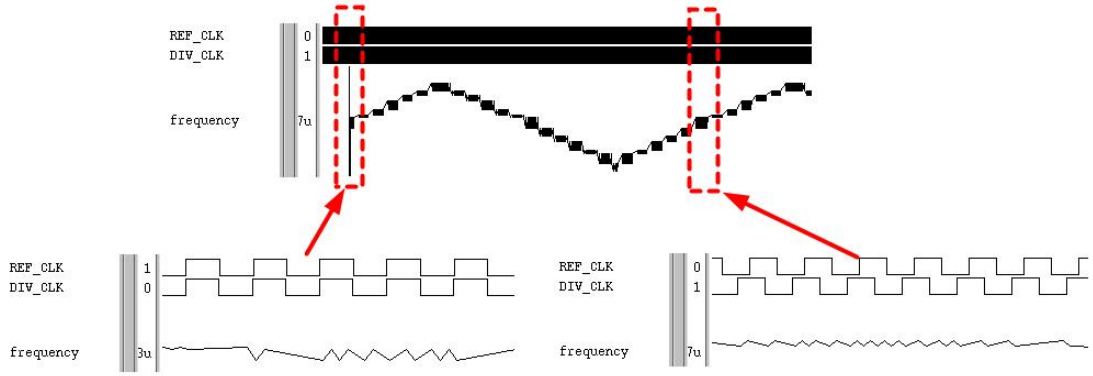


Fig. 3.1: Phase error in spread-spectrum state.

One of the possible approaches to avoid frequency drift is to re-track the correct nominal frequency. Fig. 3.2(a) shows re-track mechanism where y-axis represents the DCO control code. In Fig. 3.2(a), we can see that one modulation cycle is composed of 16 steps. After the SSCG finishes one modulation cycle, it starts to re-track the correct frequency. This approach may take too much time in re-tracking if the phase error between reference clock and divided clock is very large. The large phase error may break the spread-spectrum profile, and then make a poor EMI reduction performance. Hence, in order to shorten the re-tracking time, the division triangular modulation with re-track mechanism is proposed in Fig. 3.2(b) [26]. This approach increases the number of re-tracking times to ensure the phase error is under control. However, this approach still takes too much time in re-track. Besides, due to a large jump in DCO control code, this approach will induce a large cycle-to-cycle jitter. Consequently, these two re-track mechanisms are unsuitable for spread-spectrum

applications.

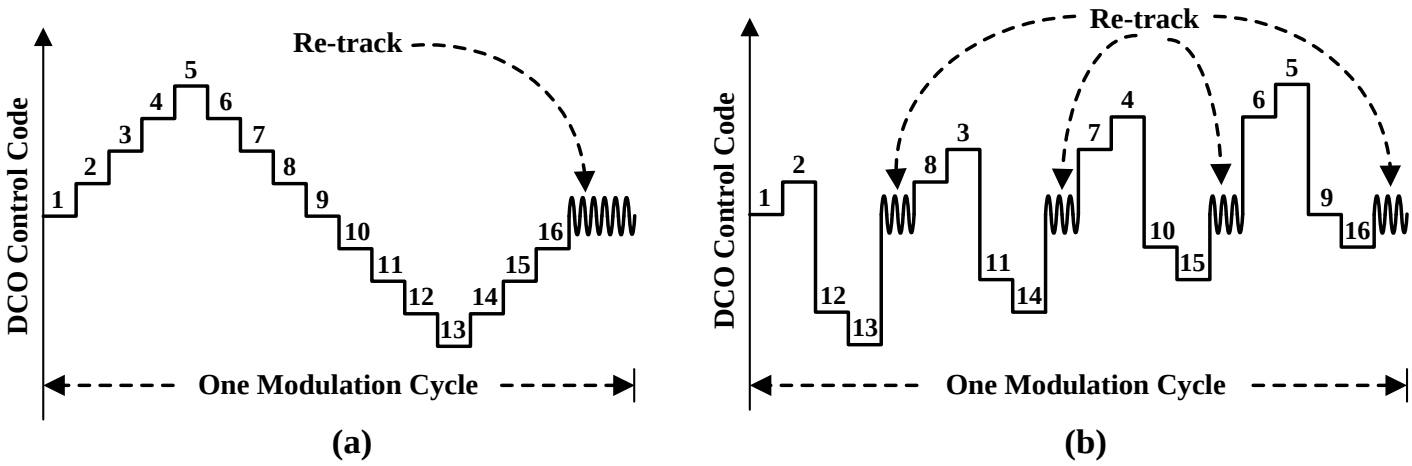


Fig. 3.2: Use relock mechanism in spread spectrum state (a) relock at the end of triangular modulation profile (b) relock with division triangular modulation.

3.1.1.2 Advantage of the Proposed Fast-relocked Mechanism

The discussion in Section 3.1.1.1 shows the difficulties of frequency stability maintenance for SSCGs especially for the modulation method on DCO/VCO. Therefore, if we can overcome PVT variations with spread spectrum, then this modulation method will be better than modulation on frequency divider. Hence, the re-track techniques are proposed to maintain frequency stability which introduced in Section 3.1.1.1. Although these two techniques take too much time in re-tracking, the concept is acceptable for frequency maintenance. Hence, our design target is to shorten the re-tracking time.

In Section 3.1, we proposed an ADSSCG with a novel method to maintain frequency stability. This technique is called fast-relocked mechanism. As the name is denominated, this technique can let the ADSSCG be relocked in a very short time while performing spread spectrum.

Fig. 3.3 shows the conventional relock mechanism (Fig. 3.3(a)) and proposed fast-relocked mechanism (Fig. 3.3(b)). The conventional relock mechanism may take too much time in phase re-track. Therefore, the power spectral density will be heaped in the center region. This long re-tracking time will cause a poor EMI reduction performance as shown in Fig. 3.3(a). In our proposed ADSSCG, the fast relock mechanism can let the phase alignment be relocked in a very short time. Hence, this approach will not accumulate too much time in the nominal frequency domain. With the shorten relock time, the peak power can be dispersed to different frequency domain, and make a better EMI reduction as shown in Fig. 3.3(b).

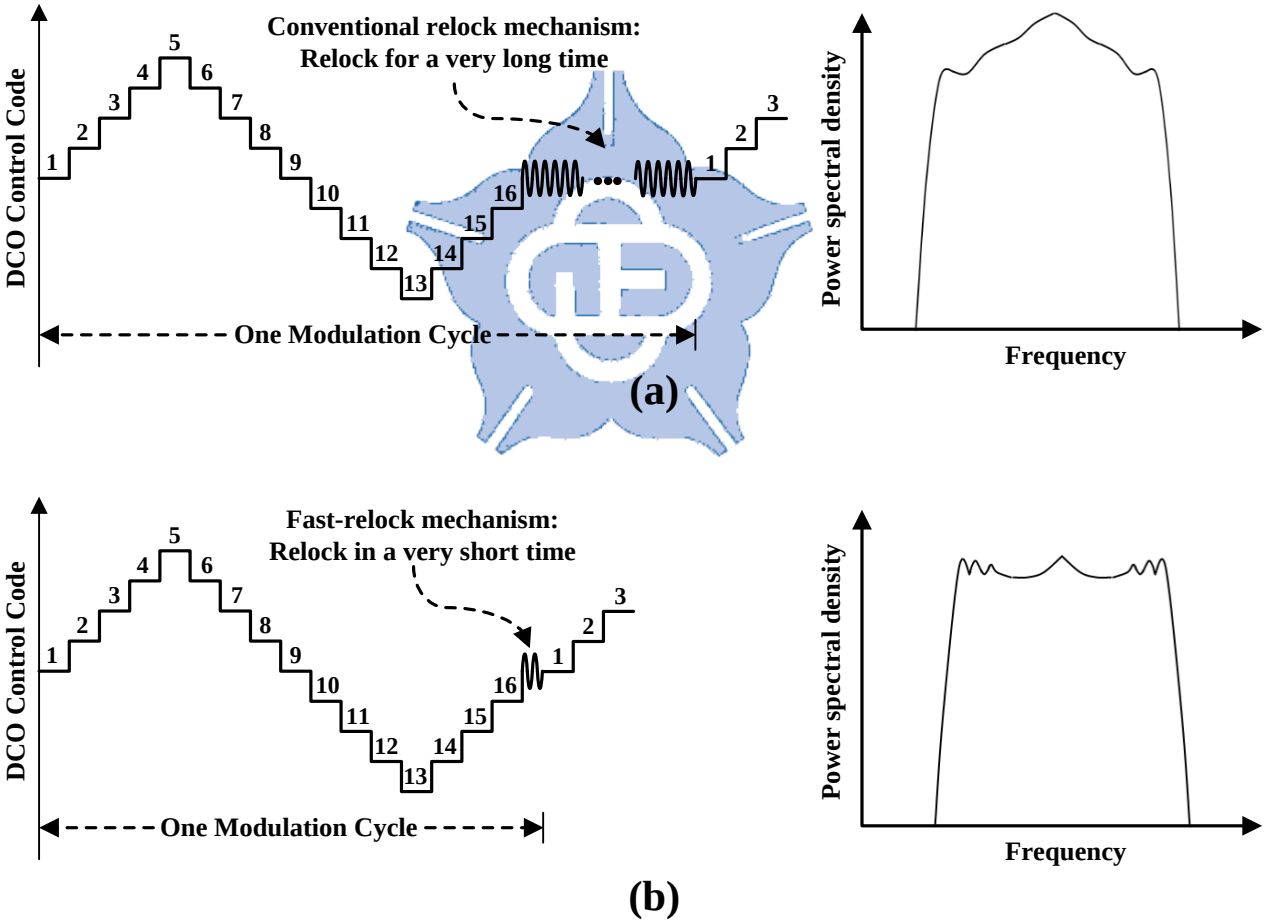


Fig. 3.3: Relock mechanism and its power spectral density (a) conventional relock mechanism (b) proposed fast-relocked mechanism.

There is another characteristic of the proposed fast-relocked SSCG. As the programmable spreading ratio is discussed in Section 2.4.3, the SSCG modulated on DCO/VCO can provide a flexible and programmable spreading ratio. However, Fig. 2.13 shows that conventional SSCG with a programmable spreading ratio mechanism may exhibit an incorrect spreading ratio with PVT variations. Table 3.2 shows the comparison table of programmable spreading ratio SSCGs with different modulation methods. In Table 3.2, we can see that there exist tradeoffs between the two modulation methods. Therefore, if we can improve the programmable spreading ratio to avoid PVT variation, then this SSCG can be applied to more applications.

Table 3.2: Comparison of programmable spreading ratio SSCG with different modulation methods.

	SSCG with programmable spreading ratio	
Modulation method	**Modulation on DCO/VCO**	**Modulation on frequency divider**
Advantages	More flexible (based on the DCO resolution).	Can work in different process corner; Can get a corresponding spreading ratio with the defined input.
Disadvantages	May be inaccurate when suffer PVT variation; Probably exceed the defined spreading ratio; Cannot get corresponding spreading ratio with the defined spreading range.	Inflexible (additional spreading ratio requires complex planning); Probably exceed the defined spreading ratio.

In order to improve the unstable spreading ratio, we propose a novel technique to realize the truly programmable spreading ratio. This approach can improve the drawbacks of the directly modulation on DCO SSCG and keep its original advantage.

To summarize the proposed ADSSCG, this version can achieve the characteristics of low power, small area, low design complexity, high portability, high frequency stability, high EMI reduction performance, accurate triangular modulation profile, and a truly programmable spreading ratio.

3.1.1.3 Fast Relock with Stop Feedback Clock Technique

The discussion in Section 3.1.1.1 concludes the phase re-tracking issue. The larger phase error will result in longer time to relock. Therefore, we propose a new technique to disable frequency divider to realize fast relock.

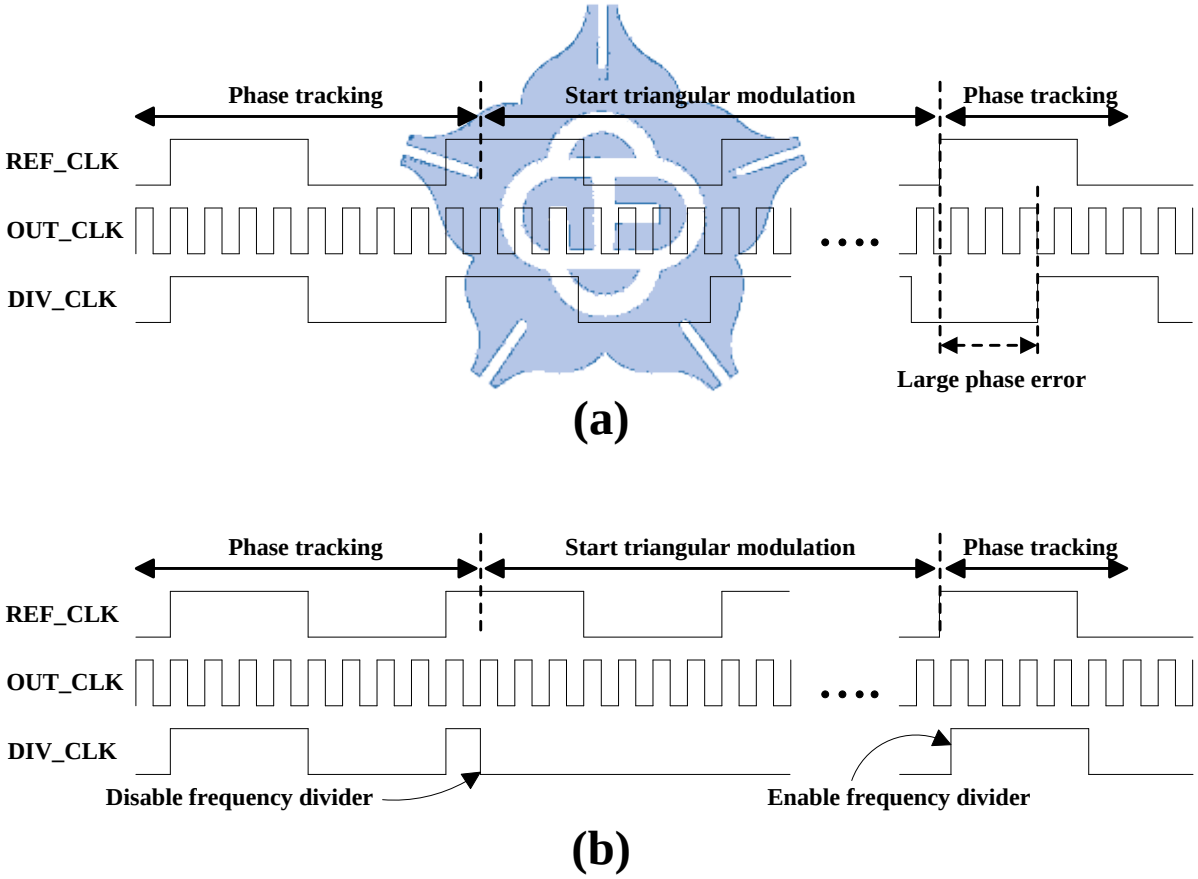


Fig. 3.4: Timing diagram of the operation of spread spectrum (a) conventional SSCG (b) proposed fast-relock ADSSCG.

Fig. 3.4 shows the operation diagram of a conventional re-tracking SSCG and the proposed fast-relock SSCG for disabling frequency divider. The conventional SSCG will re-track the phase after one modulation cycle (Fig. 3.4(a)). In the beginning of phase re-track, the accumulated phase error may be very large, and it results in a long time for re-tracking. Fig. 3.4(b) shows the proposed method which disables the frequency divider during triangular modulation and enables it in the beginning of phase re-tracking. From Fig. 3.4(b), we can see that the frequency divider is disabled when the ADSSCG start to perform spread spectrum generation, and let the ADSSCG be an open-loop. Subsequently, in the end of one modulation cycle, the frequency divider is triggered by reference clock for the enabled operation. Then, the frequency divider starts up the divided clock immediately. Therefore, the phase error between reference clock and divided clock is cancelled. After the phase relock is complete, the frequency divider is disabled again and the new modulation cycle is continued.

With the disabling and enabling technique to maintain the nominal frequency, the proposed ADSSCG can achieve good frequency stability and perform an accurate triangular modulation profile as shown in Fig. 3.5 which is a zooming figure of Fig. 3.4(b).

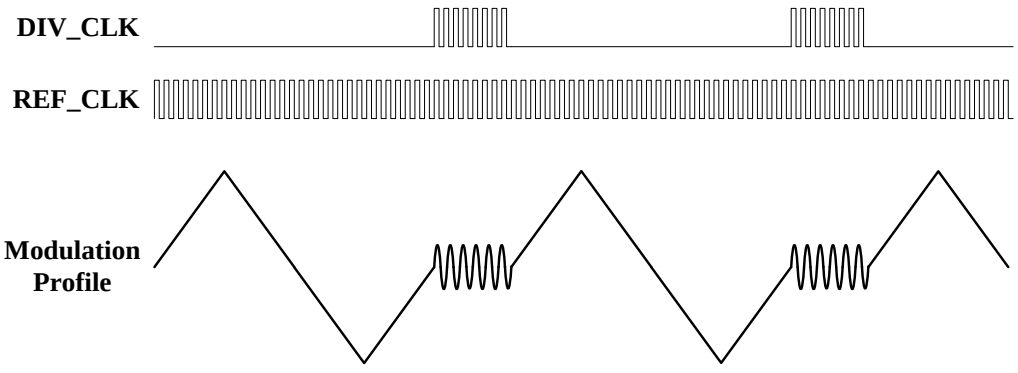


Fig. 3.5: Proposed fast-relock technique with the zoom-out waveform.

3.1.2 Truly Programmable Spreading-Ratio Decision Method

For the modulation method on DCO, the spreading ratio of ADSSCG depends on the spreading range. For instance, if there is an ADSSCG with 270MHz output frequency and DCO resolution is 3ps, and it decides to perform spread spectrum with 30 DCO code. The spreading ratio with the given spreading range is calculated by Eq. 3.1:

$$spreading\_ratio = \frac{spread\_range \times DCO\_resolution}{SSCG\_clock\_period} = \frac{30 \times 3}{10^6/_{270}} = 2.43\% \quad (3.1)$$

From Eq. 3.1, we can see that spreading ratio is decided by the above three parameters (*spread_range*, *DCO_resolution*, and *SSCG_clock_period*). In these parameters, DCO resolution is the most important parameter to determine the spreading ratio. The other two parameters (*spread_range* and *SSCG_clock_period*) are insensitive to the PVT variation while DCO resolution is altered with these variations. That is why most SSCG cannot provide a correct spreading ratio with the corresponding spreading range.

Therefore, we propose a novel method to decide the correct spreading ratio with a corresponding spreading range. The proposed truly programmable spreading-ratio decision method adopts two times of up-down polarity change to determine the current DCO resolution. After the DCO resolution is decided, the correct spreading ratio can be realized with an appropriate spreading range. For example, the correct spreading range can be calculated in Eq. 3.2 if DCO resolution is 2.5ps and the spreading ratio is set to 1%:

$$spread\_range = \frac{spread\_ratio \times SSCG\_clock\_period}{DCO\_resolution} = \frac{1\% \times 10^6/270}{2.5} = 14.815 \qquad (3.2)$$

Hence, the spreading range calculated from Eq. 3.2 is 14.815. In order to avoid over spreading, this equation is added a floor function as shown in Eq. 3.3:

$$spread\_range = \left\lfloor \frac{spread\_ratio \times SSCG\_clock\_period}{DCO\_resolution} \right\rfloor = \lfloor 14.815 \rfloor = 14 \qquad (3.3)$$

Therefore, the calculated spreading range is 14 DCO code with the conditions with 1% spreading ratio, 2.5ps DCO resolution, and at 270 MHz operation frequency.

The above formula can calculate an appropriate spreading range if we have the information of current DCO resolution. However, it's difficult to get current DCO resolution. As we mentioned before, we use two times of up-down polarity change to decide current DCO resolution. The truly programmable spreading-ratio decision method is explained in the following flowchart (Fig. 3.6).

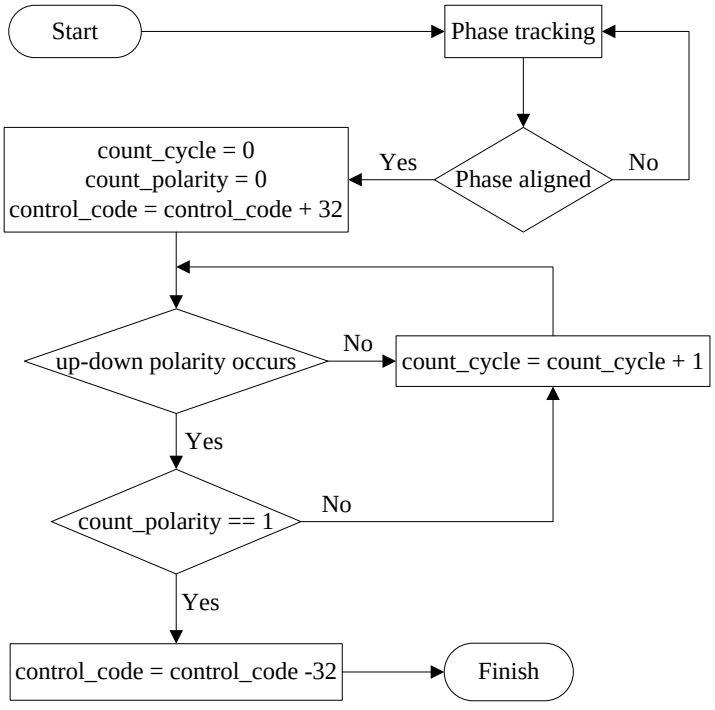


Fig. 3.6: Flowchart of the truly programmable spreading-ratio decision method.

In our proposed fast-relock ADSSCG, the DCO is adopted a ladder-shaped architecture, which is composed with the coarse-tuning stage and one fine-tuning stage. In the proposed DCO, one coarse-tuning resolution is equal to 32 times of fine-tuning resolution, and the detail circuit design will describe in Section 4.2. In Fig. 3.6, we add 32 to control code to represent adding one coarse-tuning code. After two times of up-down polarity change complete, we have got the accumulated counter (*count_cycle*). With the data of *count_cycle*, we can get the derivation about current coarse-tuning resolution. For instance, if the number of *count_cycle* is 120, then the coarse-tuning resolution is calculated in Eq. 3.4:

$$coarse\_tuning\_resolution = \frac{SSCG\_clock\_period}{count\_cycle} = \frac{10^6/270}{120} = 308.642 \text{ ps} \qquad (3.4)$$

From Eq. 3.4, we can see that current coarse-tuning resolution is 308.642 ps. Therefore, the fine-tuning resolution (DCO resolution) is calculated by Eq. 3.5:

$$fine\_tuning\_resolution = \frac{coarse\_tuning\_resolution}{32} = \frac{308.642}{32} = 9.645 \text{ ps} \qquad (3.5)$$

The DCO resolution can be calculated on the above description. However, it's a complicated procedure if we directly adopt the above calculation. It also takes too much circuit cost if the calculation is implemented in the chip. Therefore, we simplify the above procedure to make the truly programmable spreading ratio be implemented in chip with smaller circuit area cost. In order to explain the procedure with a simpler manner, we take Fig. 3.7 as an example.

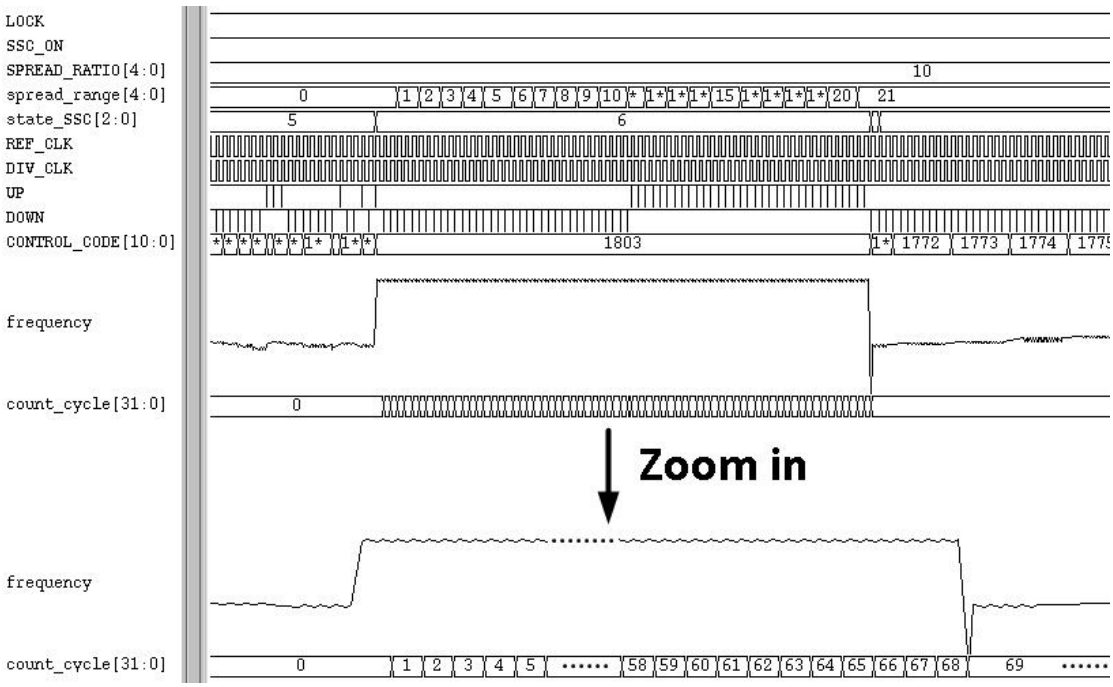


Fig. 3.7: Waveform for the calculation of truly programmable spreading ratio.

In Fig. 3.7, spreading-ratio code is set to 10. We set the percentage of the fine-tuning resolution and the coarse-tuning resolution for clock period as *F_percent* and *C_percent* respectively. Besides, the percentage of one spreading-ratio code is set as *K*, where *K* is a constant, and we will give an appropriate number to fit our requirement in the latter discussion. Therefore, the number of spreading-ratio code which is set to 10 means that the required spreading ratio is ten times of *K*. In other words, if the constant of *K* is set to 0.4%, then the required spreading ratio is calculated in Eq. 3.6:

$$spread\_ratio = ratio\_code \times K = 10 \times 0.4\% = 4\% \quad (3.6)$$

From Eq. 3.3, we can make a derivative equation to Eq. 3.7:

$$srpead\_range = \frac{ratio\_code \times K}{F\_percent} = \frac{ratio\_code \times K}{C\_percent/32} \quad (3.7)$$

The equation Eq. 3.7 can be reduced to Eq. 3.8 based on Eq. 3.4 to get *C_percent*:

$$C\_percent = \frac{coarse\_tuning\_resolution}{SSC\_clock\_period} = \frac{1}{count\_cycle} \quad (3.8)$$

Therefore, the equations of Eq. 3.7 and Eq. 3.8 can be combined as Eq. 3.9:

$$\frac{ratio\_code \times K}{C\_percent/32} = \frac{ratio\_code \times K}{\frac{1}{32} \times \frac{1}{count\_cycle}} = ratio\_code \times K \times 32 \times count\_cycle \quad (3.9)$$

The spreading range can be calculated by Eq. 3.9. Because the parameters, *K* and number 32, are constant in Eq. 3.9, we set the product of K and number 32 be a constant *U* in Eq. 3.10 and derive Eq. 3.9 to Eq. 3.11:

$$U = K \times 32 \quad (3.10)$$

$$spread\_range = ratio\_code \times count\_cycle \times U \quad (3.11)$$

The number of *U* is determined by *K*, which is the percentage of one spreading-ratio code. In order to simplify this formula (Eq. 3.11), we set constant *U* to be 1/16. Therefore, the number of constant K is induced in Eq. 3.12:

$$K = U \times \frac{1}{32} = \frac{1}{16} \times \frac{1}{32} = 0.1953125\% \quad (3.12)$$

From Eq. 3.12, we can see that the spreading range can be calculated with a smaller circuit area cost if we set *K* to 0.1953125%, and this number is close to 0.2%. The equation Eq. 3.11 is available for up-spread or down-spread. However, our proposed ADSSCG performs spread spectrum with center-spread, and we have to avoid getting an odd DCO code number in spreading range. Hence, this spreading range calculated from Eq. 3.11 should be divided by 2 then and add a floor function, and then multiply 2 as shown in Eq. 3.13.

$$spread\_range = \left\lfloor (ratio\_code \times count\_cycle) \times \frac{1}{32} \right\rfloor \times 2 \quad (3.13)$$

The final equation is in Eq. 3.13, and we take Fig. 3.7 as an example. In Fig. 3.7, the number of cycle count is 69, and the spreading ratio is set to 1.953125% ($spred\_ratio \times K = 10 \times 0.1953125\% = 1.953125\%$). Therefore, the spreading range is calculated in Eq. 3.14:

$$spread\_range = \left\lfloor (10 \times 69) \times \frac{1}{32} \right\rfloor \times 2 = 42 \quad (3.14)$$

From Eq. 3.14, we found the spreading range is 42. It's means that we should spread 42 DCO codes to achieve the 1.953125% spreading ratio. Therefore, for center-spread, the ADSSCG should spread 21 DCO codes higher and lower than the nominal frequency respectively (see the variable *spread_range* in Fig. 3.7).

The equation Eq. 3.13 looks like it requires three multiplications and one division to get the result. In fact, this equation will not require any multiplication and

division. First, the division of $\frac{1}{32}$ and multiplication of 2 can be realized with a shifting operation. The product of $ratio\_code \times count\_cycle$ can accumulate *ratio_code* in *count_cycle* cycles, thus this operation can be implemented with addition.

With the truly programmable spreading-ratio decision method, we can perform spread spectrum with a correct spreading ratio with PVT variations. Besides, the complex calculation is also simplified saved with a small circuit area cost.

3.1.3 Overview of the Proposed Fast-relocked ADSSCG

3.1.3.1 Block Diagram

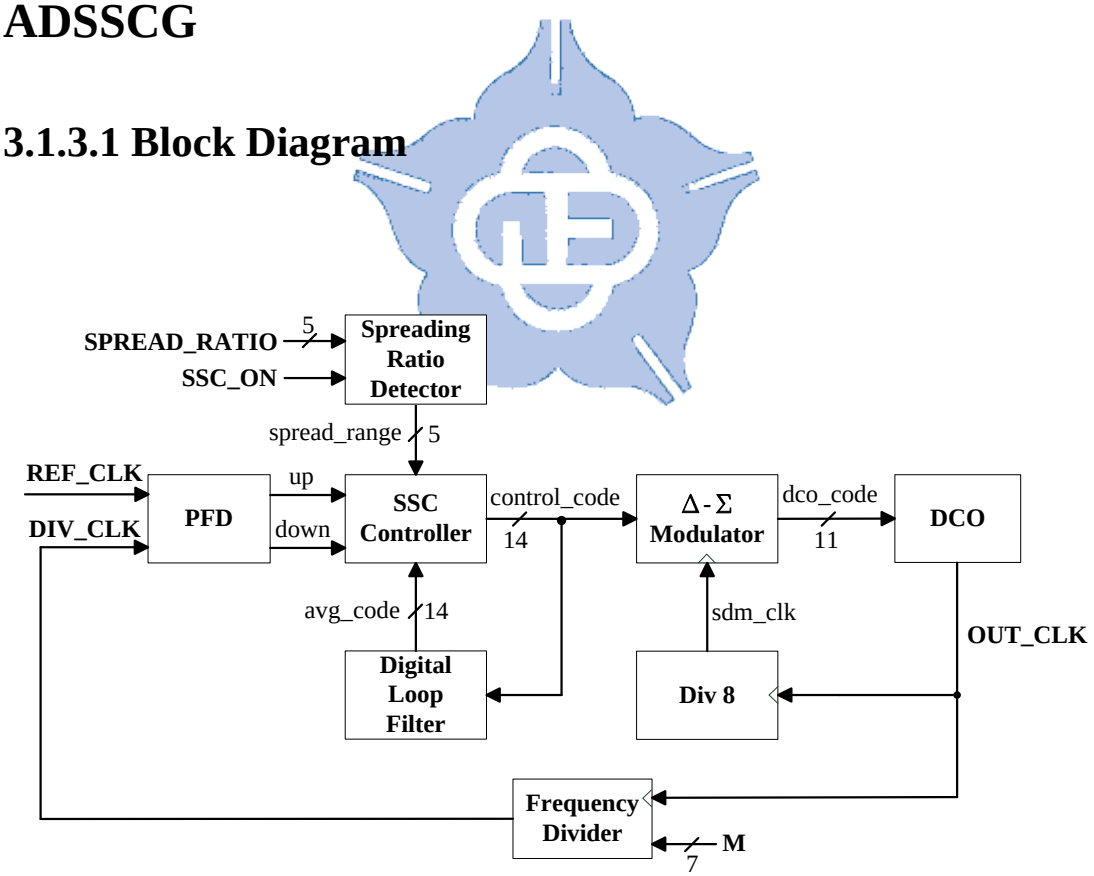


Fig. 3.8: Block diagram of proposed fast-relocked ADSSCG.

Fig. 3.8 shows the block diagram of proposed fast-relocked ADSSCG. This ADSSCG is composed of a phase and frequency detector (PFD), a spread-spectrum clock (SSC) controller, a spreading ratio detector, a digital loop filter, a delta-sigma modulator (DSM), a low-power monotonic DCO, and a frequency divider.

The proposed ADSSCG is adopted the modulation method on DCO. Therefore, the SSC controller directly controls the DCO control code (control_code) to perform the center-spread triangular modulation on the output frequency. According to the spreading range (spread_range) which is calculated from spreading ratio detector, the SSC controller modulates the output frequency to achieve the corresponding spreading ratio, and the detail operation of SSC controller will be discussed in Section 3.1.4. The spreading ratio detector is proposed to find the spreading range with the truly programmable spreading ratio decision method, and this decision method has been explained in Section 3.1.2.

In order to generate a smooth triangular modulation profile, the DCO resolution is further enhanced by employing a DCO dithering scheme through a 3-bit first-order delta-sigma modulator (DSM). The integer part of the DCO control code has 11 bits, and the fractional part of the DCO control code has 3 bits. The operation speed of the DSM is the output clock frequency divided by 8. Due to the enhancement of the DCO equivalent resolution, the proposed ADSSCG can provide a better EMI reduction with a smaller spreading ratio, and this proposed DSM will be discussed in Section 3.1.6.

The digital loop filter [30] is applied in the ADSSCG to generate a stable average frequency to eliminate the jitter effects of the reference clock. The loop filter can generate a 14-bit baseline DCO control code (avg_code) for the SSC controller. Thus, the SSC controller can keep updating the triangular modulation profile with PVT variations. This proposed DLF is discussed in Section 3.1.5.

A PFD and a monotonic DCO are designed with standard cells, thus they can be

easily ported to different process in a very short time. The monotonic DCO is proposed to overcome non-monotonic phenomenon when perform spread spectrum, and the circuit implementation and the non-monotonic issue will be discussed in Section 4.2. The circuit design PFD will explain in Section 4.1.

3.1.4 SSC Controller

The major technique of this ADSSCG is fast-relocked mechanism. This technique is controlled by the SSC controller. Therefore, the flowchart of this proposed SSC controller is shown in Fig. 3.9.

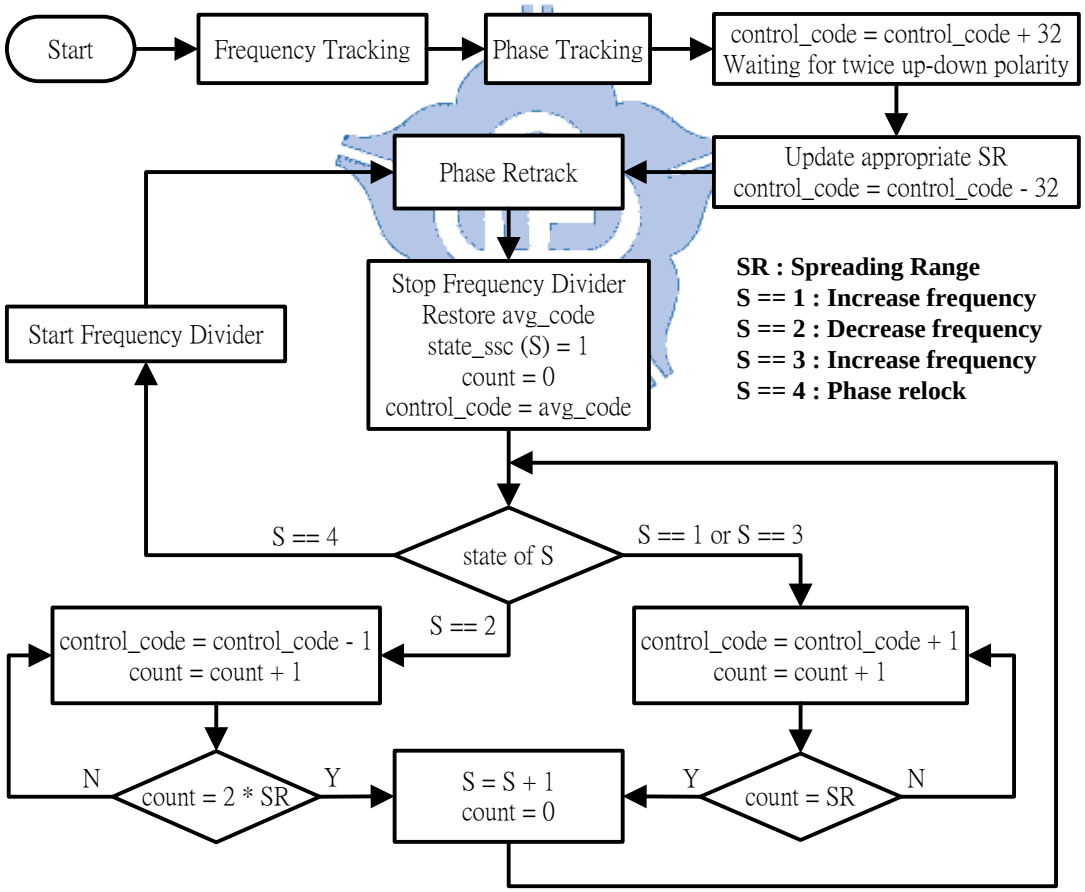


Fig. 3.9: Flowchart of the operation of SSC controller.

After the system is reset, the SSC controller starts to perform frequency tracking. In order to increase frequency tracking speed, this state is searched with only adjust coarse-tuning code until the coarse step is converged to one code. After frequency tracking is finish, the state of phase tracking is started. Phase tracking search the correct frequency with fine-tuning code adjustment. When fine-tuning step is converged to one fine-tuning code, the DSM is started. Because the DSM is adopted to enhance the DCO resolution to the third digit after the decimal point, the baseline control code which is provided from DLF is important in this state to enhance the lock-in speed. Hence, the frequency and phase tracking is operated as a normal PLL.

When the frequency and phase tracking is in lock state, the spread-spectrum function is turned on, and start to detect the spreading range (SR) by spreading-ratio detector which is described in Section 3.1.2.

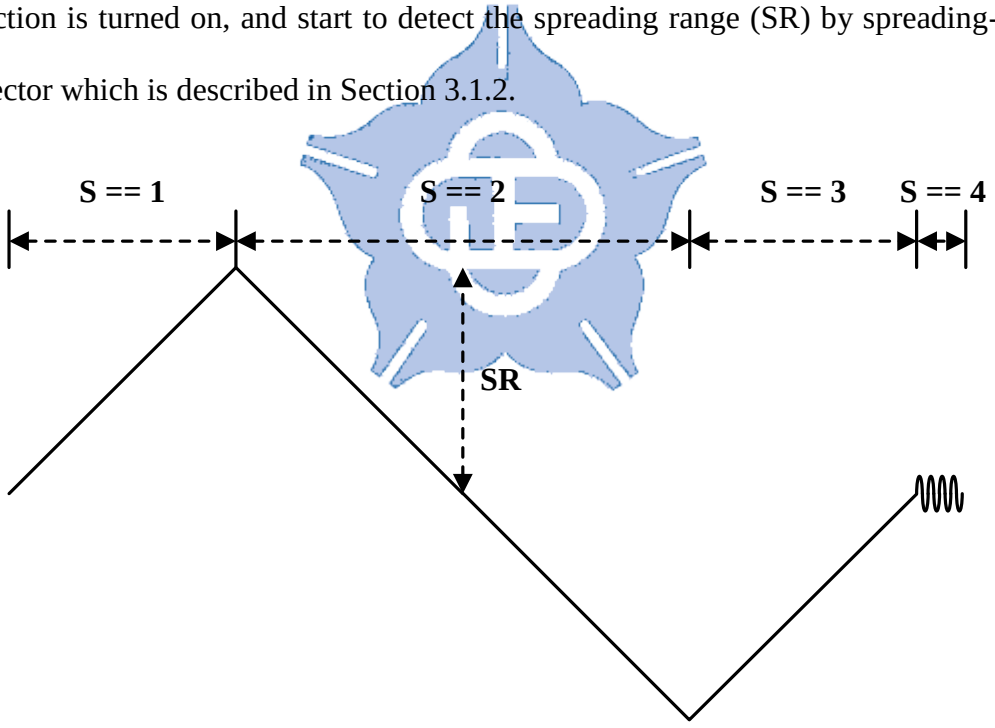


Fig. 3.10: Four stages of the spread spectrum.

The modulation type of our proposed ADSSCG is center-spread. Hence, there are four stages in the spread-spectrum state, and the four stages are represented in the modulation profile as shown in Fig. 3.10. Before start first stage (S == 1), the

frequency divider is stopped to let the ADSSCG be an open-loop, and then initialize other parameters. The first stage (S == 1) is spread up the frequency with SR control code. The second stage (S == 2) is spread down the frequency with two times of SR control code. The third stage (S == 3) is spread up the frequency with SR control code again. Finally, the fourth stage (S == 4) enables the frequency divider and starts to perform fast-relock mechanism. After the fourth stage is finished, the new triangular modulation cycle is continued.

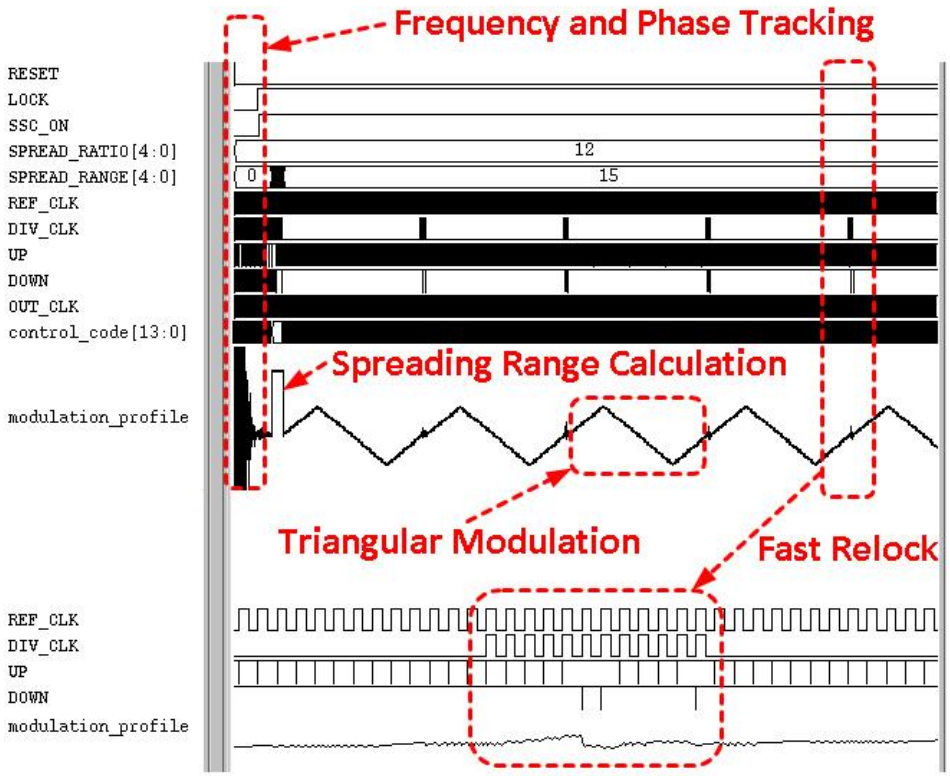


Fig. 3.11: Simulated waveform of proposed fast-relocked ADSSCG.

Fig. 3.11 shows the waveform of the SSC controller. The operation is the same as the flowchart shown in Fig. 3.9. After system is reset, the proposed ADSSCG performs frequency and phase tracking until the PLL is locked. When the PLL is locked, spreading-ratio detector begins to calculate the appropriate spreading range. After that, the SSC function is turned on, and the frequency divider is stopped during

the triangular profile generation. The spreading ratio is dependent on the spreading range which is provided form spreading-ratio detector. As compared with other SSCGs, the proposed ADSSCG operates as an open-loop while performing spread spectrum generation. Therefore, an accurate triangular modulation profile can be achieved without the disturbance comes from the PFD. However, the reference clock jitter effects and the PVT variations will influence the frequency stability of the output clock. Thus, in the proposed ADSSCG, at the end of the triangular modulation, the SSC controller performs a fast frequency and phase relock to maintain the frequency stability. In addition, the loop filter which will describe in Section 3.1.5 can filter out the reference clock jitter effects during the relock process. From Fig. 3.11, we can see that the zoom-in section is the waveform of fast phase tracking. This region shows that the phase relock is very efficient, and relocked tightly in few cycles.

3.1.5 Digital Loop Filter

For all-digital PLL (ADPLL), the frequency and phase tracking is realized with the adjusting control code by the controller. Fig. 3.12 shows the procedure of frequency and phase tracking. From Fig. 3.12, we can see that a larger DCO control code results in a higher output frequency. The dotted line in Fig. 3.12 is the baseline control code. This baseline control code is in the nearby region of the locked control code. Therefore, if we can find this baseline control code earlier, then the lock in time can be achieved in a shorter time. Besides, the baseline control code can prevent the frequency drift if it comes a sever jitter on the reference clock suddenly. As a result, it’s very important to acquire the correct baseline control code as fast as possible.

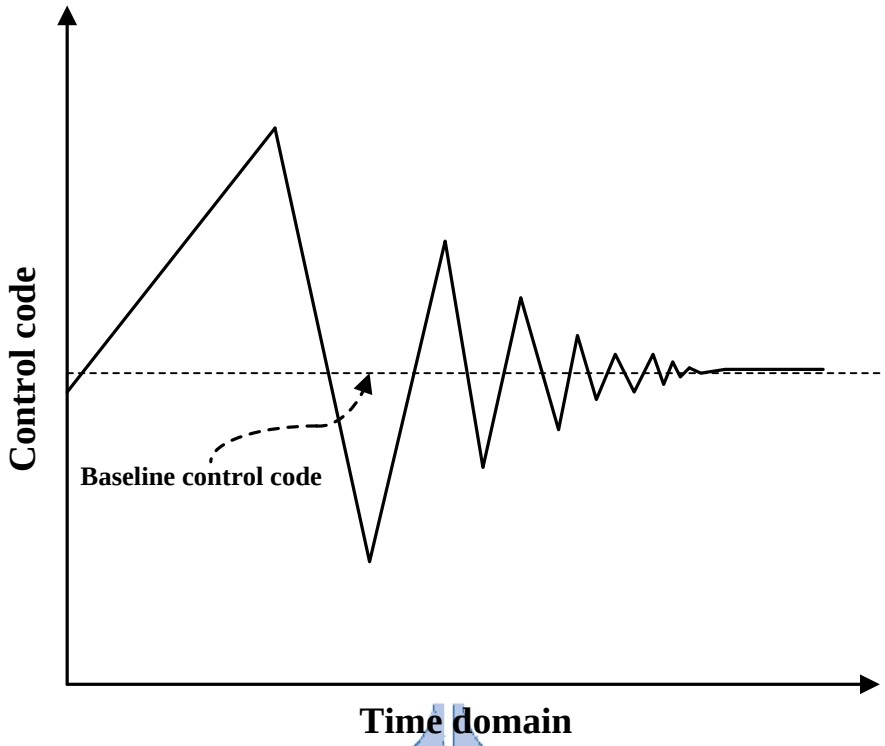


Fig. 3.12: ADSSCG frequency and phase tracking profile.

In fact, the correct baseline control code cannot get in the beginning of frequency and phase tracking, but the approximate baseline control code can be estimated. The baseline control code will be more accurately with the frequency tracking is in operation. The detail operation of baseline control code maintenance is described in the flowchart as shown in Fig. 3.13.

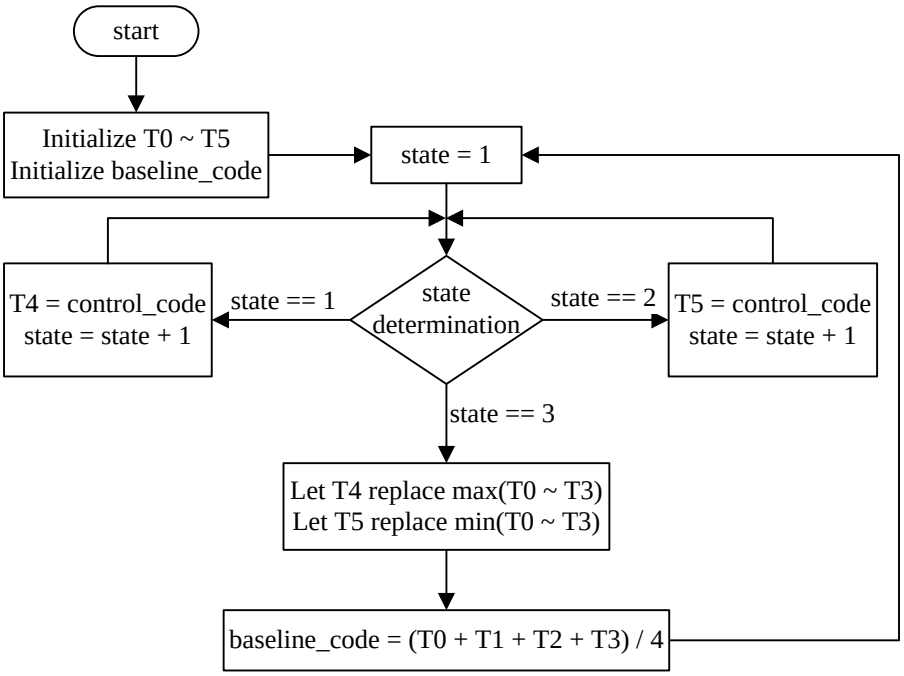


Fig. 3.13: Flowchart of baseline control code maintenance.

In Fig. 3.13, the five registers of T0, T1, T2, T3, T4, and T5 are utilized to store control code, and there are three states of this flowchart. The first two states assign current control code to T4 and T5 in two cycles. In the third state, the maximum and minimum registers of T0~T4 are picked out, and then replace the picked up registers with T4 and T5 respectively. After that, the average control code of T0~T4 are calculated, and let the average control code be stored in baseline control code.

With getting the baseline control code, the ADSSCG can not only shorten the duration of frequency and phase tracking, but also avoid reference clock jitter. Fig. 3.14 shows the technique to avoid the frequency drift. The control code will make a pullback if the up-down polarity occurs in frequency and phase tracking state. Therefore, this technique can reduce lock-in time, and make the frequency tracking more stable.

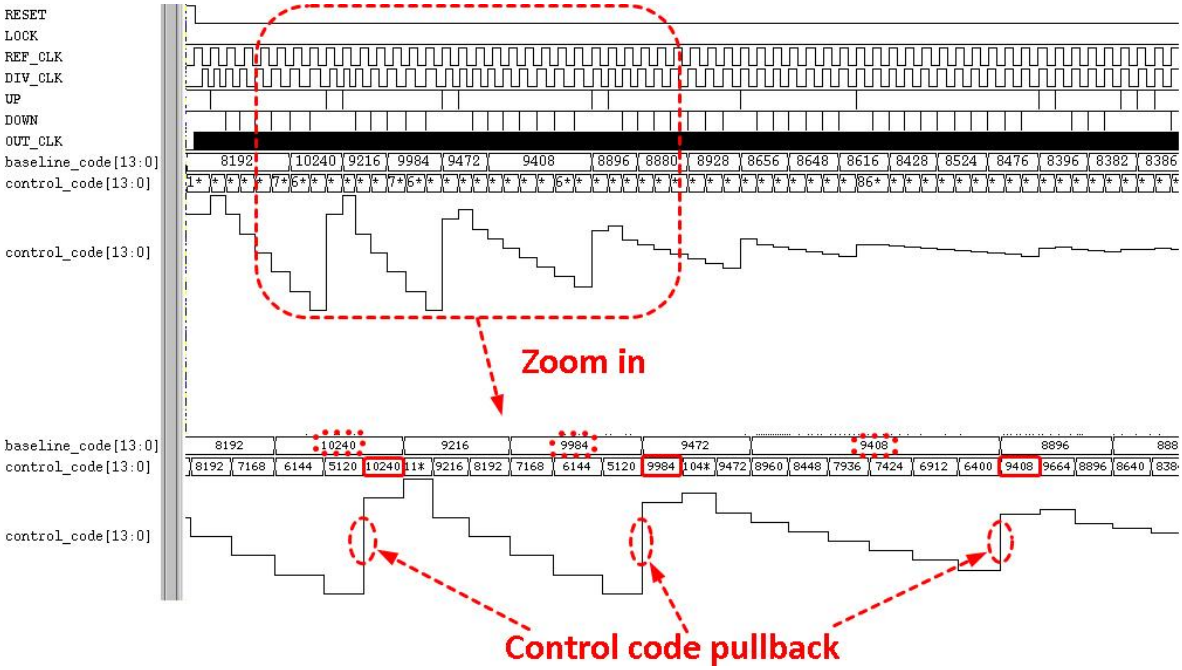


Fig. 3.14: Control code pullback with proposed digital loop filter.

3.1.6 Delta-Sigma Modulator

For the DCO, especially for the wide-range ADPLL, the resolution is usually a bottleneck. The ADPLL with a worse DCO resolution will deteriorate the phase error even though the output clock is in lock state. The wide-range ADPLL with a very high resolution will result in huge circuit cost. Therefore, it is a tradeoff between DCO resolution and the circuit cost.

In order to minimize phase error, the DSM is added in front of DCO to enhance DCO resolution [31]. The DSM enhances DCO resolution with dithering technique. Fig. 3.15 shows the diagram of DCO code dithering.

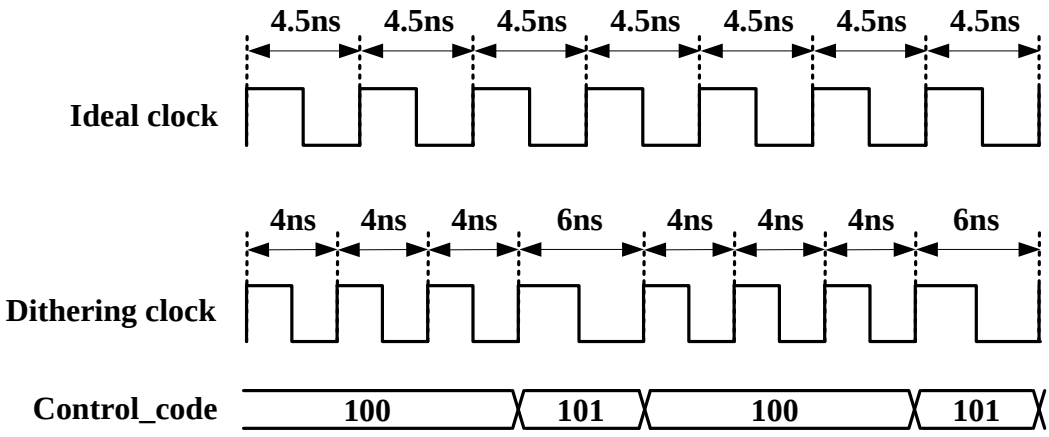


Fig. 3.15: Enhance DCO resolution with dithering technique.

The ideal clock period in Fig. 3.15 is 4.5ns. However, due to the real clock period if 4ns and its resolution is 2ns, the clock cannot perform the real output clock with 4.5ns clock period. Therefore, the DSM uses the dithering technique to allot appropriate ratio of the limited resolution DCO clock. In this case, the DSM distributes three cycles of 4ns clock period and one cycle of 6ns clock period to realize the average clock period with 4.5ns.

This dithering technique can reduce phase error effectively. Besides, the DSM which is added on DCO can also improve the EMI reduction performance. The better resolution of DCO can make more dispersed spectrum, and achieves better EMI reduction performance.

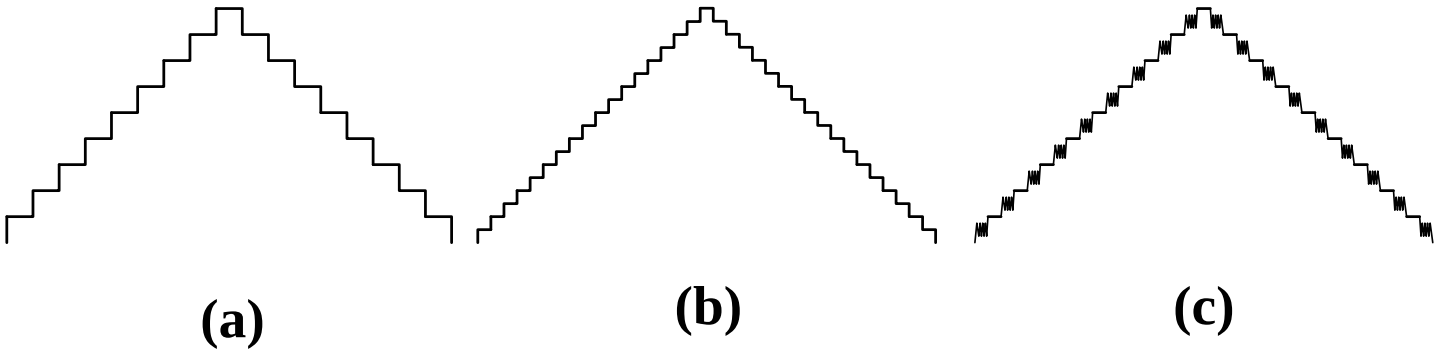


Fig. 3.16: Triangular modulation with different DCO: (a) DCO with normal resolution (b) DCO with better resolution (c) dithering DCO with normal resolution.

Fig. 3.16 shows triangular modulation with different DCO types. Fig. 3.16(a) is the general ADSSCG with normal DCO resolution. This ADSSCG performs spread spectrum to reduce peak power with worse EMI reduction. Fig. 3.16(b) is the other ADSSCG with a better DCO resolution, and will achieve a better EMI reduction performance. The last ADSSCG (Fig. 3.16(c)) with dithering technique can make better EMI reduction result than the first type ADSSCG.

In this thesis, we adopt a DSM in the DCO to enhance the DCO resolution to third digit after the decimal point. Hence, the EMI reduction performance can be improved in our experimental result as shown in Fig. 3.17. From Fig. 3.17, we can see the comparison of peak power between DSM-added ADSSCG and DSM-less ADSSCG is further reduced by 6.7dB.

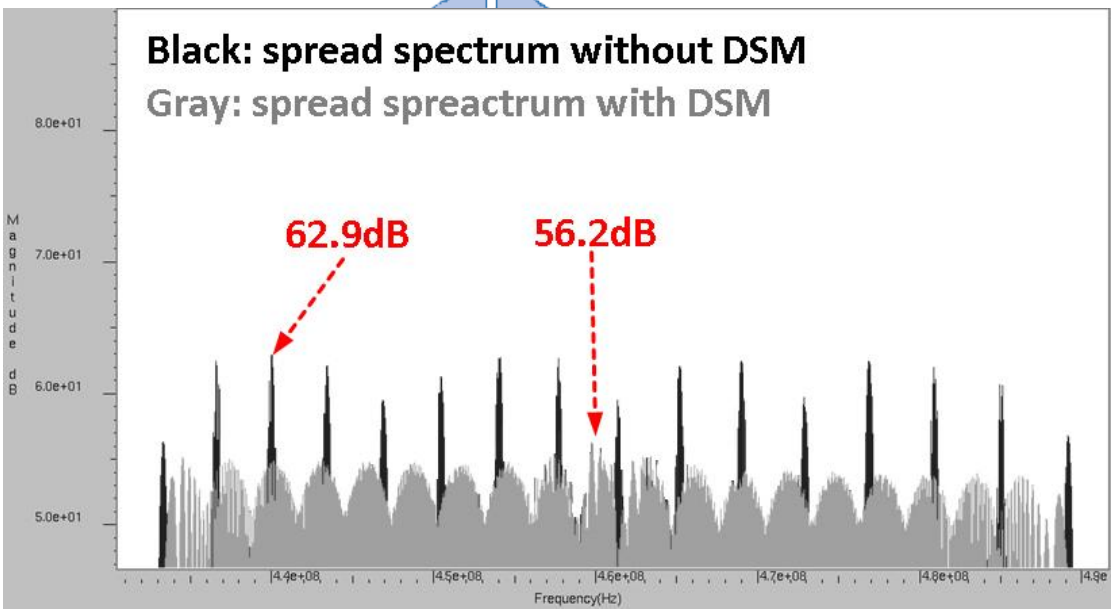


Fig. 3.17: Power spectral density analysis with and without DSM.

Although more fractional bits in the DSM can make better EMI reduction performance, too many fractional bits may result in slower modulation frequency. Therefore, the fractional bit in the DSM is decided to 3-bit, and this can make the modulation frequency in the range 30 kHz to 50 kHz with a 0.5% spreading ratio.

3.2 The Proposed Counter-Based ADSSCG

The proposed fast-relocked ADSSCG can avoid frequency drift and prevent PVT variation. However, this version still exist some drawbacks. First, the modulation frequency is unpredictable due to the fast-relocked mechanism. Because it's not always take the same lock-in time when it perform fast-relock mechanism, that may cause every modulation cycle time different as shown in Fig. 3.18.

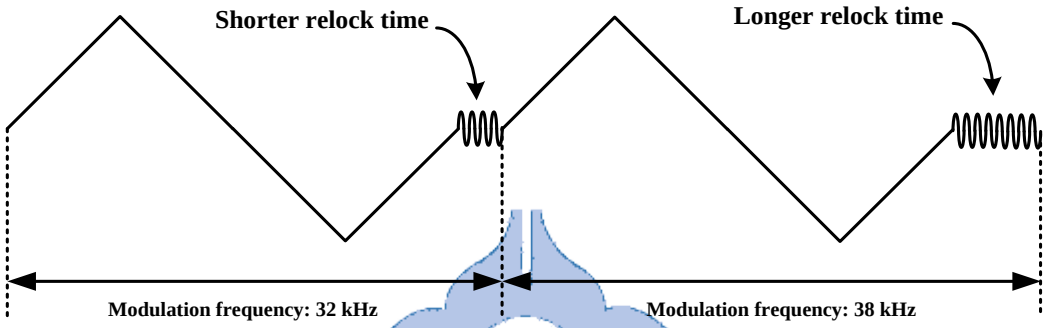


Fig. 3.18: Fast-relocked ADSSCG with different relock time.

From Fig. 3.18, we can see that the fast-relocked mechanism can shorten the lock-in time, but it cannot make the triangular modulation profile with the equally modulation frequency.

There is another disadvantage in the fast-relocked ADSSCG. Although this proposed ADSSCG can improve frequency stability, the average frequency of spread-spectrum clock still has some deviations from the un-spread-spectrum clock. For instance, the operation frequency of ADSSCG is 270 MHz. When it starts to perform spread spectrum in center-spread, the average operation frequency should be 270 MHz, too. However, with the fast-relocked mechanism, this ADSSCG can only keep the frequency from drifting. The actual average frequency still has some deviations from 270 MHz.

3.2.1 Counter-Based Frequency Maintenance Mechanism

In order to achieve an accurate average frequency, the average frequency of the reference clock should be the identical to the divided clock. In other words, the total cycle counts of reference clock should be the same with divided clock, and this concept is similar to the PLL purpose. Nevertheless, how to keep the cycle count of modulated divided clock equal to reference clock is a very difficult objective.

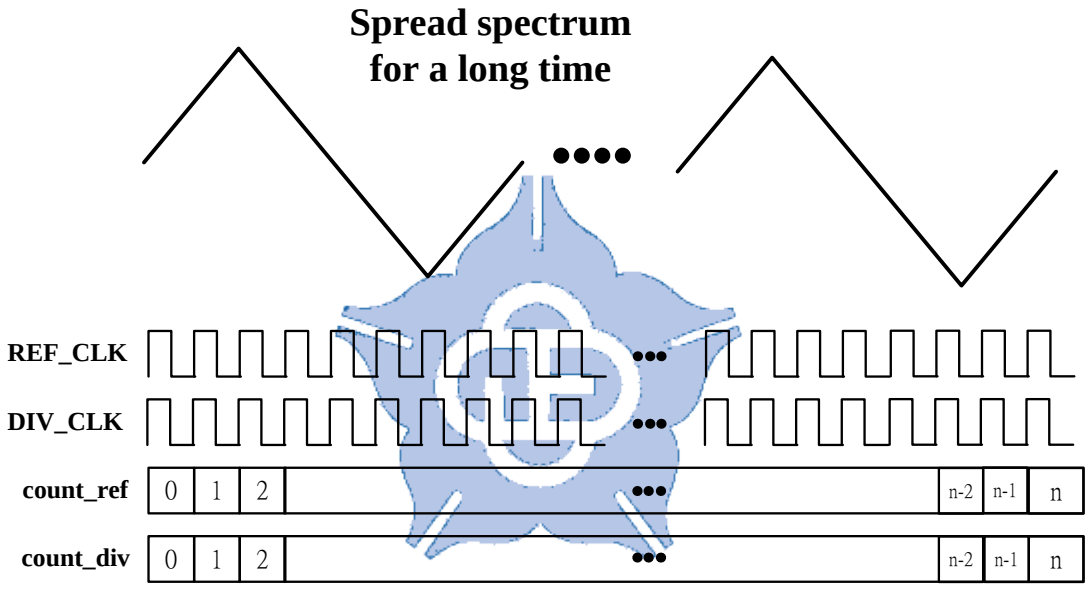


Fig. 3.19: Total cycle count of reference clock and divided clock.

Fig. 3.19 shows the diagram of total cycle count. The divided clock is modulated due to the spread-spectrum function is operated. After long time, the total cycle count of reference clock and divided clock is equal. Hence, this ADSSCG achieves high frequency stability even though the spread-spectrum function is turned on, and this is our design target in the second version ADSSCG.

In order to derive useful information, we choose the point in the end of one modulation cycle, because the cycle count of divided clock is close to reference clock.

If we acquire the cycle count information from other point of modulation profile, then we will get a wrong data, and that will mislead the clock count determination. The time point decision is shown in Fig. 3.20

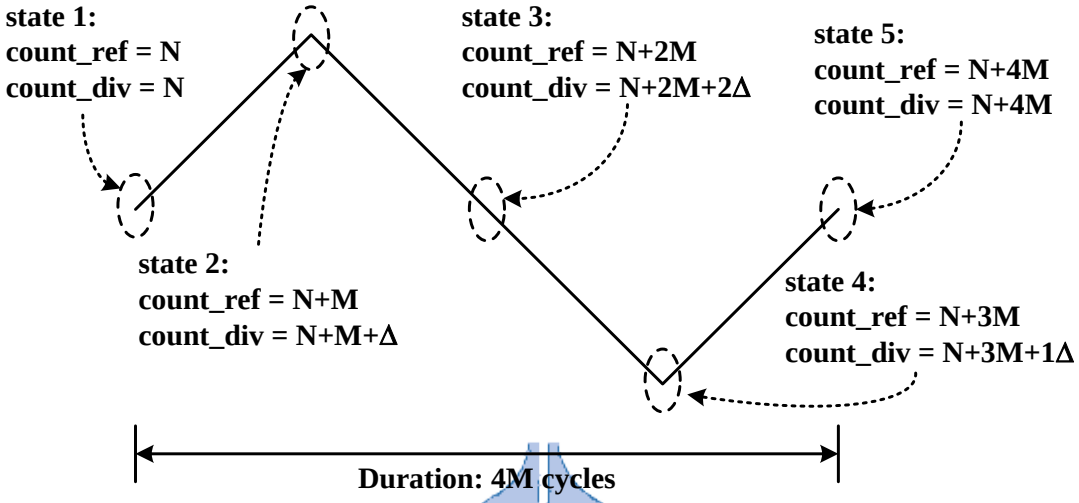


Fig. 3.20: Time point decision for cycle count determination.

From Fig. 3.20, we can see the timing diagram where count_ref represents the cycle count of reference clock and count_div represents the cycle count of divided clock. In the beginning (state 1), the cycle count of reference clock is equal to divided clock (count_ref = N, count_div = N). After spread spectrum, divided clock is speeded up. Therefore, the cycle count in state 2 have some difference (count_ref = N +M, count_div = N + M + Δ). In state 3, the cycle count difference between reference clock and divided clock will be a maximum value (count_ref = N + 3M, count_div = N + 3M + 2Δ). Although the divided clock will slow down in state 4, the cycle count of divided clock still larger than reference clock (count_ref = N + 4M, count_div = N + 4M + Δ). In the end of one modulation cycle, divided clock will be modulated to nominal frequency. Hence, the cycle count of these two clocks will be minimized in state 5. Consequently, it's a better decision to choose the point in the end of one

modulation cycle.

The diagram of Fig. 3.20 is an ideal case. However, the cycle counts may be different in these two clock counters. Therefore, the output frequency will be adjusted if the cycle count error occurs in state 5.

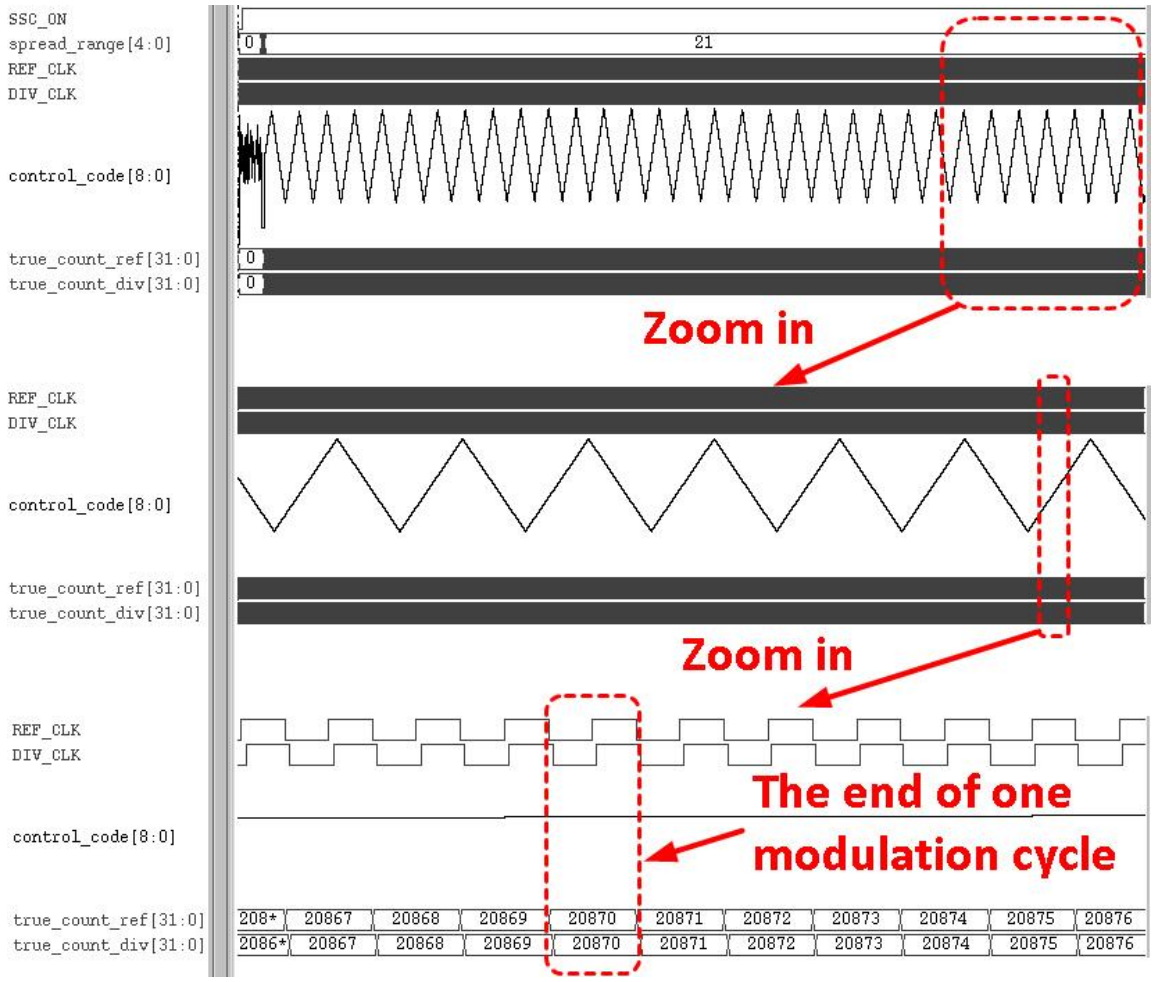


Fig. 3.21: Waveform of proposed counter-based ADSSCG.

Fig. 3.21 shows the simulated waveform. The decision point is at the marked area, and it adjusts the frequency continuously. Hence, the cycle count of reference clock and divided clock is almost aligned even though it performs spread spectrum for a long time. In Fig. 3.21, the cycle count of reference clock and divided clock are both in the number of 20870, this represents the ADSSCG has a high frequency stability

characteristic.

This counter-based ADSSCG has a high frequency stability when spread spectrum. Besides, the proposed ADSSCG have no redundant time in spread-spectrum state. This improvement not only makes more accurate triangular modulation profile, but also keeps modulation frequency unchanging.

3.2.2 Overview of the Proposed Counter-Based ADSSCG

3.2.2.1 Block Diagram

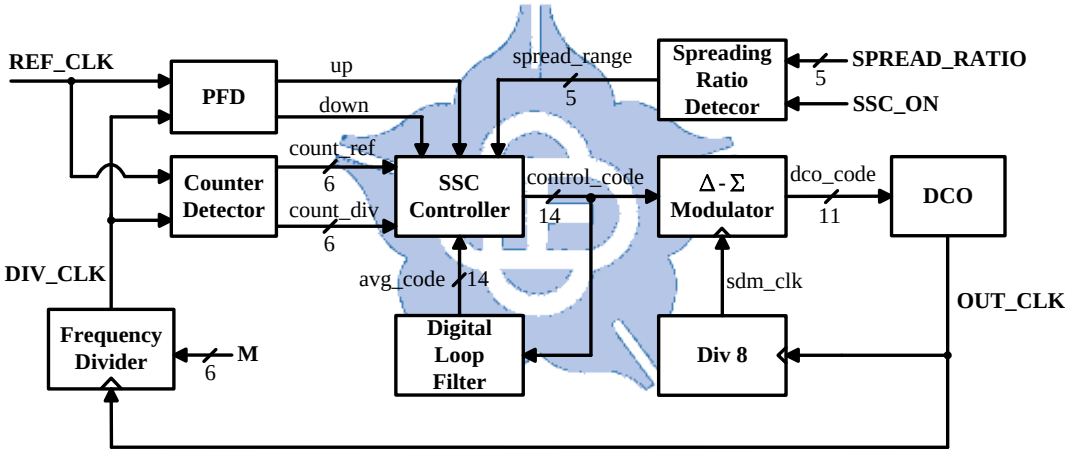


Fig. 3.22: Block diagram of proposed counter-based ADSSCG.

Fig. 3.22 shows the block diagram of proposed counter-based ADSSCG. The block diagram is similar to the fast-relocked ADSSCG in Fig. 3.8. This ADSSCG is composed of a phase and frequency detector (PFD), a counter detector, a spread spectrum clock (SSC) controller, a spreading ratio detector, a digital loop filter, a delta-sigma modulator (DSM), a monotonic DCO, and a frequency divider.

This counter-based ADSSCG is designed with the architecture based on the first version circuit. The difference is the frequency divider will not be controlled. Besides,

in this proposed counter-based ADSSCG, we add a counter detector to calculate count cycle counts of reference clock and divided clock to realize the counter decision technique. The concept of counter decision technique has described in Section 3.2.1, and the detail operating method of this proposed counter detector will be discussed in Section 3.2.3.

Because the whole operation before perform spread spectrum is discussed in Section 3.1.3, we will not reiterate the description on the operation flow and its usage of repeated circuit.

3.2.3 Counter-Based SSC Controller

The major operation controlled by the SSC controller. It controls the whole operation flow. The flowchart is shown in Fig. 3.23. After the frequency and phase tracking is completed, the controller is started to perform spread-spectrum function, and the modulation type is center-spread. There are four states of spread spectrum (state_ssc) in Fig. 3.23. The first three states directly modulate the DCO code to generate a triangle modulation profile, and the spreading range is a programmable variable to decide the corresponding spreading ratio. The fourth state is frequency adjustment state. In the fourth state, the controller will determine the information of count_ref and count_div from counter detector, and adjust the frequency. After frequency adjustment, the new triangle modulation is continued.

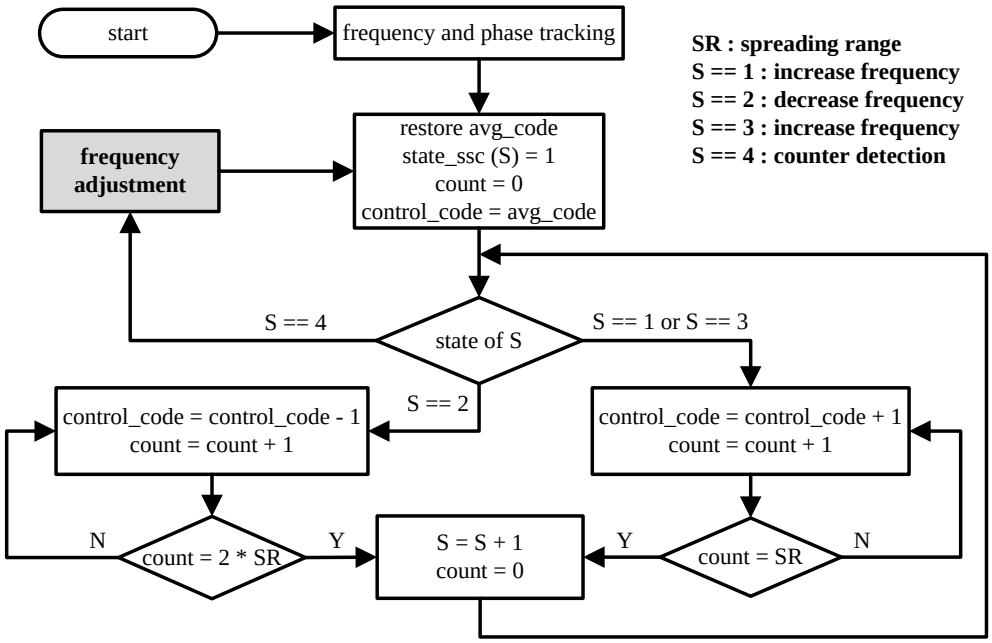


Fig. 3.23: Flowchart of the proposed counter-based ADSSCG operation.

The counter decision technique requires two counters to determine current average frequency, and adjust the frequency of output clock. It's a simple idea to maintain frequency stability. However, the bit size of these two counters is a bottleneck. It's impossible to accumulate cycle count with infinite increasing because of the limited counter bit size. Therefore, the counter will face overflow problem, and this will result in erroneous judgment.

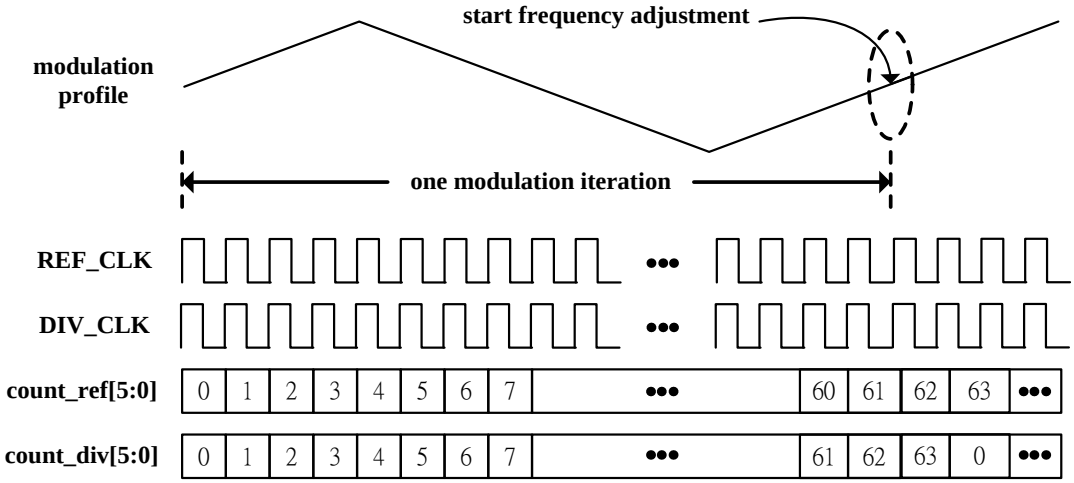


Fig. 3.24: Modulation profile and frequency adjustment position.

The two counters count_ref and count_div provide the information about the long-term average frequency of the reference clock and divided clock. Therefore, the controller will start frequency adjustment to compare the two counters in the end of one modulation iteration as shown in Fig. 3.24. In order to reduce the cost, the bit size of the counters is set to 6 bits. There may be some misjudgements if the counters are overflowed due to the limited counter bit size. In order to avoid these misjudgements, the frequency adjustment mechanism is proposed in the flowchart shown in Fig. 3.25.

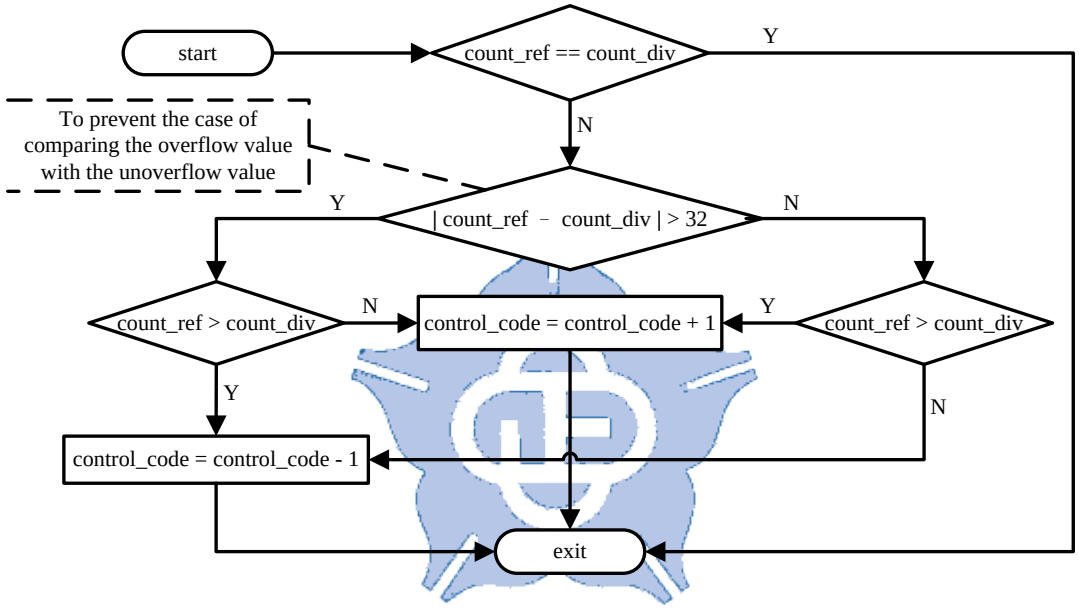


Fig. 3.25: Flowchart of the decision of frequency adjustment mechanism.

The flowchart in Fig. 3.25 shows the method to avoid misjudgements. For example, if the number of count_ref is 63 and the number of count_div is 0, then the general decision may conclude the result which reference clock is faster than divided clock. Actually, the correct result is contrary to this determination. Therefore, this flowchart shown in Fig. 3.25 is proposed to solve the problem.

With the frequency adjustment mechanism, the average frequency can be easily maintained and against PVT variation. Besides, the bit size can also be minimized with the decision method of frequency adjustment.

3.2.4 Digital Loop Filter Improvement

In Section 3.1.5, the digital loop filter is proposed to shorten PLL lock-in time and reduce jitter. This digital approach occupies less circuit area compares with analog loop filter. However, the DLF still holds a high percentage in whole chip area. Therefore, the DLF is improved to reduce redundant part to minimize circuit area and keep the same performance.

From the flowchart which is shown in Fig. 3.13, we can see that the maximum value and minimum value are picked out in the same time. However, the action to select maximum and minimum value is the major cost in the proposed DLF. Hence, if we can reduce one maximum function (F_MAX) or minimum function (F_MIN), the circuit area can be further reduced.

In the design of proposed DLF, the F_MAX and F_MIN are realized with the Chipware component in logic synthesizer. In our observation, the two functions can be realized with either Chipware. For F_MAX as an example, if there are three variables T0, T1, T2, and their value are shown below:

$T0 = (1010)_{binary}$

$T1 = (1101)_{binary}$

$T2 = (0111)_{binary}$

The maximum value from these three variables is T1, and it can be picked out by F_MAX very easily. The minimum value in the three variables is T2, and it's not available be picked out if we use F_MAX directly. In order to use one chipware to solve this problem, we can invert these three variables.

$T0 = (0101)_{binary}$

$T1 = (0010)_{binary}$

$T2 = (1000)_{binary}$

After inverting these three variables, the minimum value can be found with F_MAX. Therefore, with this technique, the functions of F_MAX and F_MIN can be realized with only chipware component. The flowchart of the improved DLF is shown in Fig. 3.26.

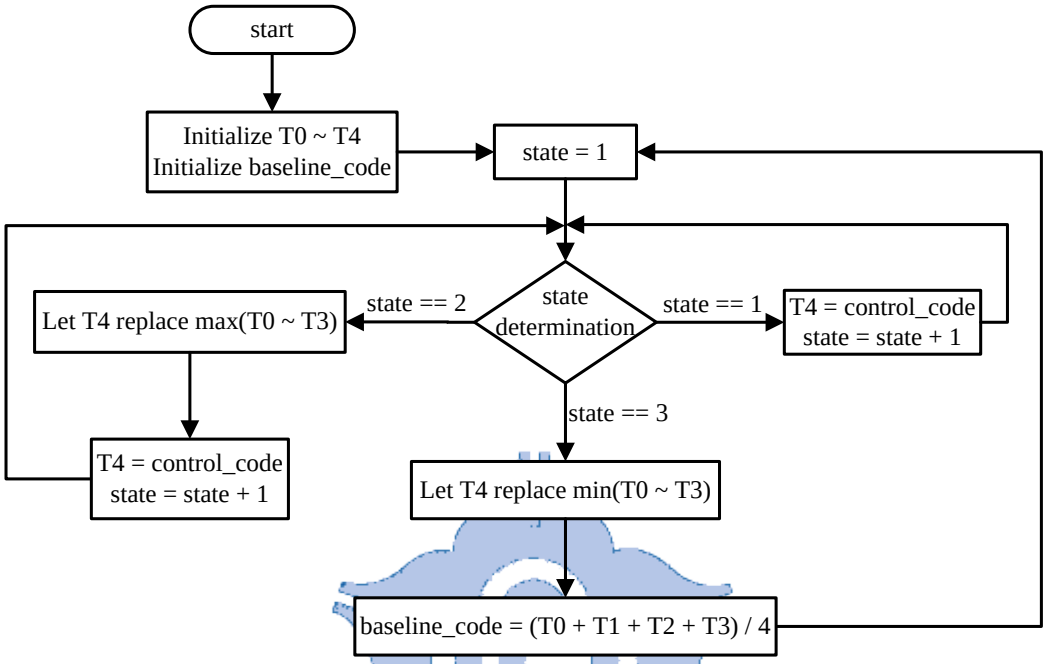


Fig. 3.26: Flowchart of improved DLF.

Table 3.3: Gate count data of original DLF and improved DLF.

	Original DLF	**Improved DLF**
Gate count	2311	1317

Table 3.3 shows the gate count information of the original DLF and improved DLF. From this table, we can see that the new DLF make the advancement to be 55% area with original DLF. Although the circuit area can be saved largely, the two DLFs' jitter performance are similar as shown in Fig. 2.27.

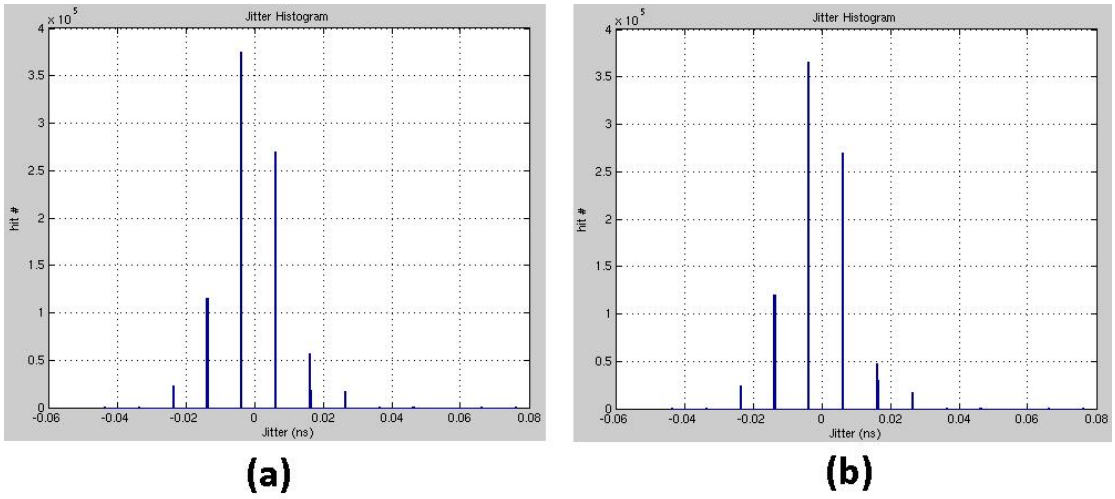


Fig. 3.27: Jitter histogram of (a) Original DLF (b) Improved DLF.

Chapter 4

Circuit Design and Implementation of ADSSCG

4.1 Phase and Frequency Detector

4.1.1 Structure

The PFD structure is shown in Fig. 4.1. This PFD is designed with standard cells [32]. It's used to detect lead-lag condition of reference clock and divided clock. If the PFD is triggered earlier by reference clock, and that means the frequency of reference clock is faster than divided clock. In this case, the UP signal is generated with a low pulse to deliver a speed-up command to SSC controller. In other case, if divided clock triggers the PFD earlier, than the DOWN signal will generated, and send to SSC controller.

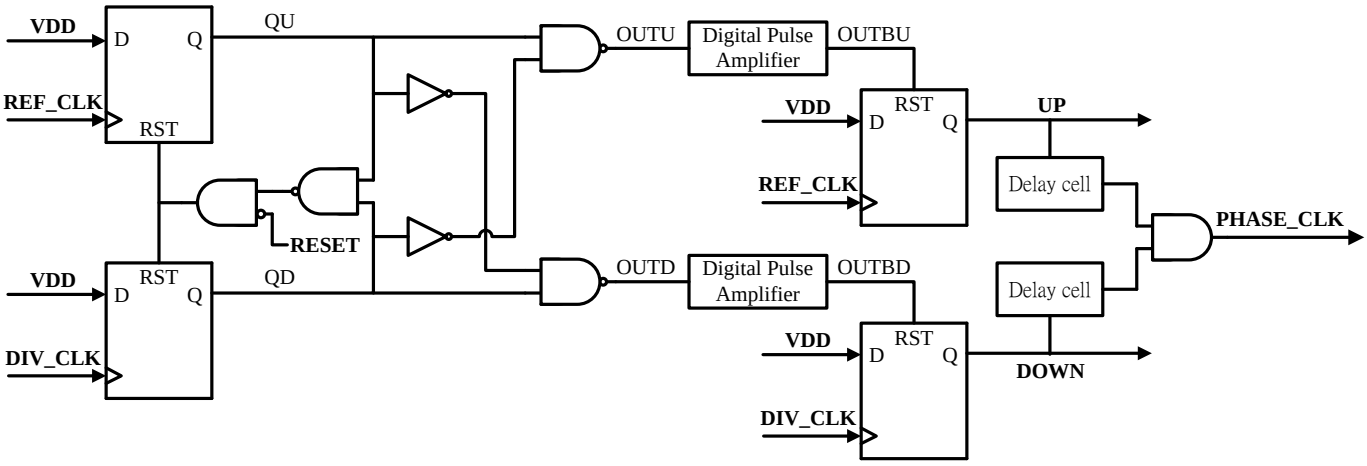


Fig. 4.1: Structure of proposed PFD.

After detecting lead-lag condition and generate UP or DOWN signal, the UP/DOWN signals will send to SSC controller. Hence, it's necessary to generate an extra clock signal to trigger SSC controller. In Fig. 4.1, the clock signal PHASE_CLK is generated with the AND-gate of delayed UP and DOWN.

Due to the delay of circuit transition time, the PFD have dead zone once the phase error between reference clock and divided clock is very closely. If the phase error is extremely small, then the pulse from the signals OUTU and OUTD may too transient to feed into SSC controller correctly. Therefore, the pulse amplifier is adopted [32] to enlarge the pulse as shown in Fig. 4.2.

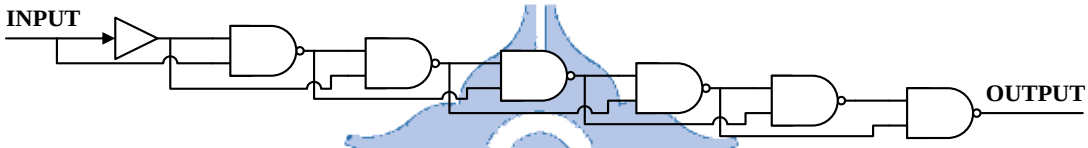


Fig. 4.2: Digital pulse amplifier architecture.

4.1.2 Simulation Results

Fig. 4.3 shows the simulated waveform of the PFD. In the beginning, reference clock is faster than divided clock, and the initial phase error is 9ps. Therefore, after detecting the two clocks, UP signal is asserted because of the lead reference clock. In Fig. 4.3, the phase error is decreased with 1ps per-cycle. Therefore, we can see that the UP signal can detect the minimum phase error in 2ps. Similarly, the DOWN signal can also detect 2ps phase error. Therefore, this PFD can realize 2ps dead zone.

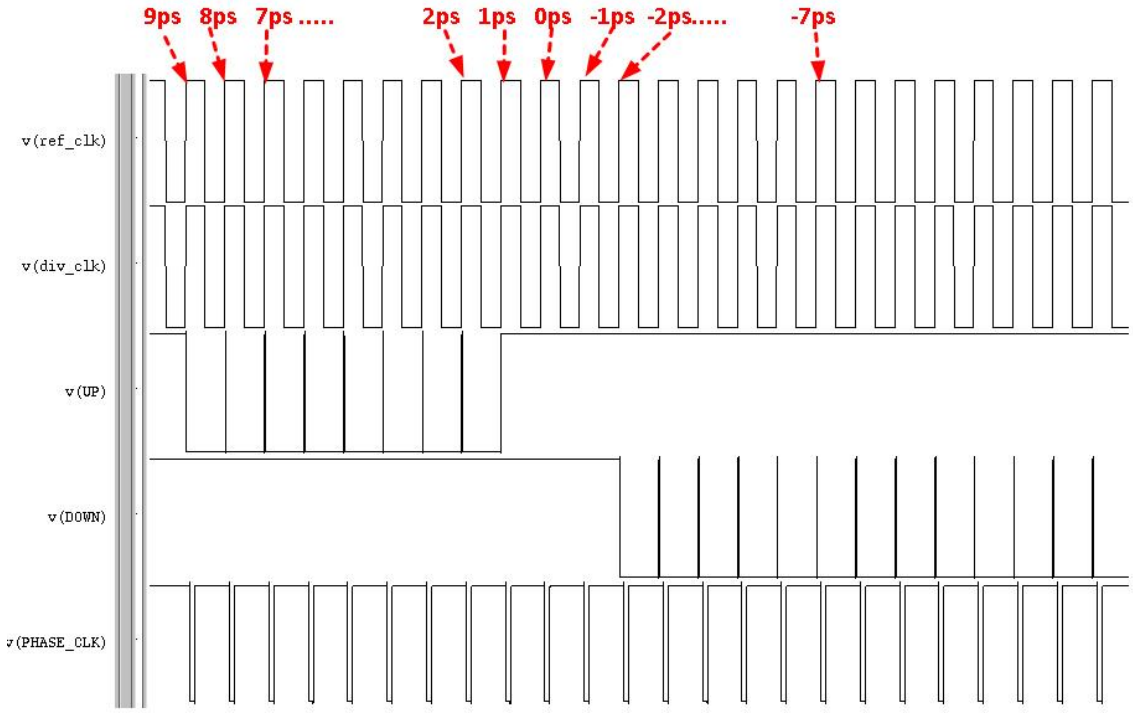


Fig. 4.3: The simulated waveform of proposed PFD.

4.2 Monotonic Low-Power Digital Controlled Oscillator

4.2.1 Relationship between DCO and Spread-Spectrum Effect

There are several parameters to determine the performance of SSCG. An excellent SSCG will make good EMI reduction performance, and one of these conditions to decide the EMI reduction effect is the circuit design of DCO. Therefore, the DCO characteristic is important for ADSSCG.

In our prior discussion in Section 3.1.6, we proposed a DSM in our ADSSCG to enhance the DCO resolution. Hence, the frequency of DCO will be output with dithering technique as shown in Fig. 3.16(c), and the dithering technique can also

improve the EMI reduction. However, this technique is used to reduce phase error, it cannot enhance the really DCO reduction like Fig. 3.16(b). If we require a high resolution output clock, then it's necessary to improve the DCO circuit.

For current published ADSSCGs, a high resolution DCO is proposed with three-stage differential ring oscillator and the digitally controlled pMOS arrays to control the frequency [24]. This ADSSCG can achieve a high DCO resolution and achieve nice EMI reduction effect. However, it cannot be applied in wide range applications. Besides, this architecture may consume too much power and occupies large chip area. Therefore, this ADSSCG is unsuitable for low-power applications. In order to reduce power consumption and make a low-lost DCO, the cascading-DCO architecture is proposed as shown in Fig. 4.4 [33]. This DCO architecture is composed with a coarse-tuning circuit and a fine-tuning circuit. With the two-stage architecture, the circuit area can be saved, and reduce unnecessary power dissipations.

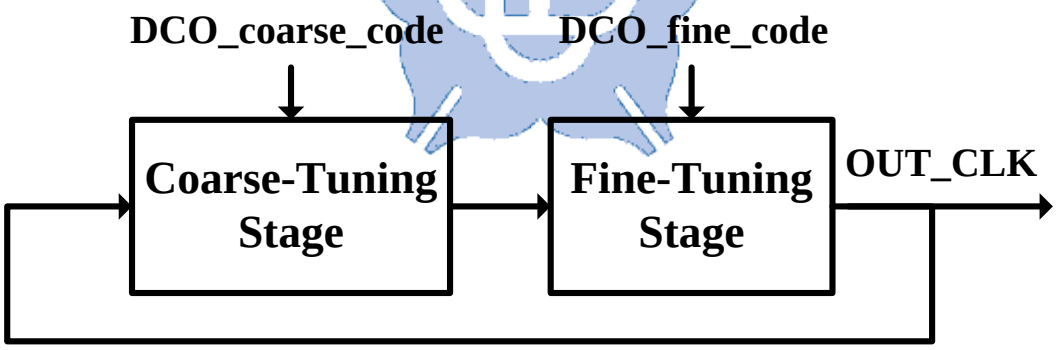


Fig. 4.4: Architecture of cascading-DCO.

The cascading-DCO can achieve a low-power and low-cost approach. Nevertheless, this DCO may cause non-monotonic problem. Fig. 4.5 shows the phenomenon of non-monotonic DCO. In Fig. 4.5, the output frequency is speeded-up with the increasing fine-tuning DCO code. When the DCO code crosses different

coarse-tuning stage, the sub-frequency band may be overlapped. For example, in Fig. 4.5, we can see x-axis represents the DCO code with coarse-tuning part and fine-tuning part (coarse.fine), and the period with the code 0.9 (coarse.fine = 0.9) is similar to the code of 1.5 (coarse.fine = 1.5).

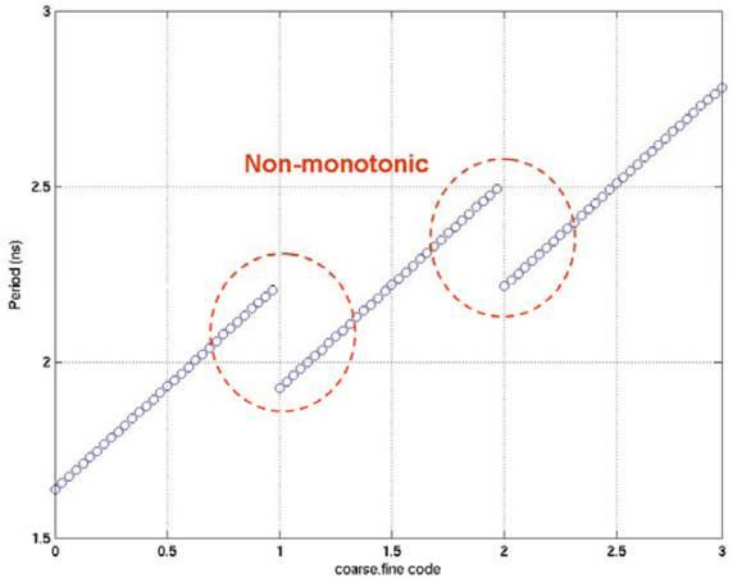


Fig. 4.5: Non-monotonic DCO relationship between DCO code and period.

This non-monotonic phenomenon may deteriorate the phase error and result in worse jitter performance for ADPLL. Besides, if this non-monotonic DCO is adopted in ADSSCG, the peak power may be concentrated and result in worse EMI reduction as shown in Fig. 4.6.

In this thesis, we proposed a low-power monotonic DCO to overcome the problems which are discussed above, and the follow sections will describe the circuit design of our proposed DCO.

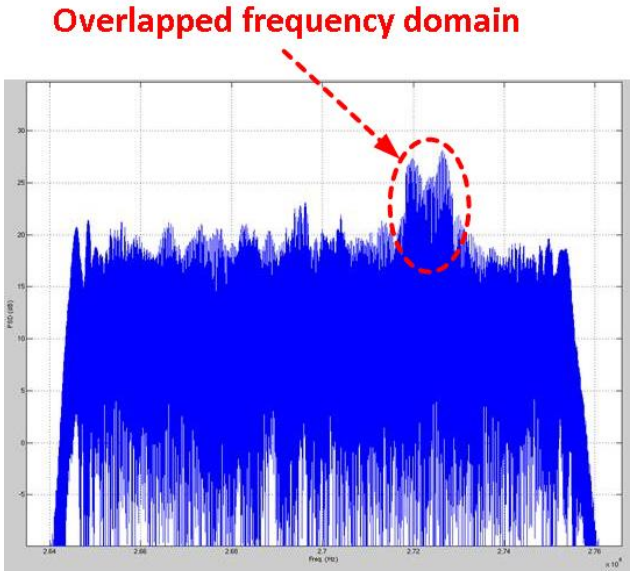


Fig. 4.6: Power spectral density of ADSSCG with non-monotonic DCO.

4.2.2 Structure of Coarse-Tuning Circuit

For the cascading-DCO, it requires a coarse-tuning circuit and a fine-tuning circuit. In order to save the power consumption, a ladder-shaped coarse-tuning circuit is published in [34]. Fig. 4.7 shows the architecture of coarse-tuning circuit. This coarse-tuning circuit has 32 coarse-delay cells (CDC) which is composed with a NAND-gate and an inverted multiplexer. These NAND-gates is controlled by the coarse-tuning code to disabled redundant power consumption, and achieve a low-power approach. There are two signals CA_OUT and CB_OUT be feed into the fine-tuning circuit to enhance DCO resolution, and the delay difference is equal to one CDC delay time.

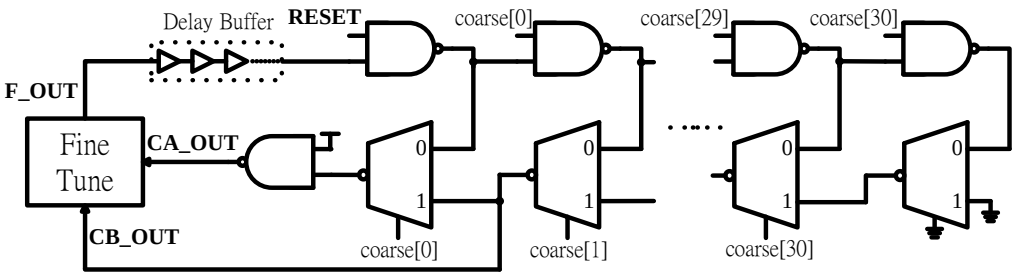


Fig. 4.7: Architecture of conventional ladder-shaped coarse-tuning circuit [34].

This architecture can achieve low-power approach, and it's appropriate for ADSSCG. However, the coarse-tuning resolution of this monotonic DCO is not small enough. Besides, due to the long transition time of the inverted-multiplexer, this architecture has a glitch problem when it changes difference from high speed to low speed as shown in Fig. 4.8. This phenomenon may influence the frequency divider to generate a wrong divided clock, and may cause the whole chip fail in extreme cases.

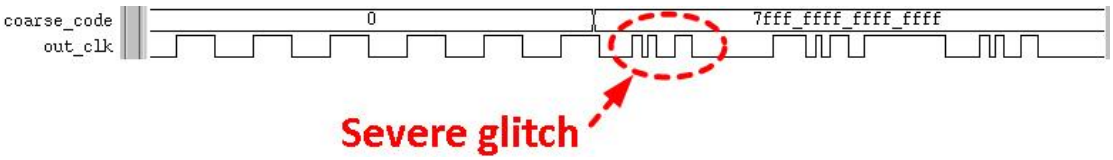


Fig. 4.8: Glitch occurs when crossing different coarse-tuning code.

In order to solve these above problems, we proposed a modified ladder-shaped coarse-tuning circuit which is design with standard cells as shown in Fig. 4.9. This coarse-tuning circuit is consist 64 CDCs. The CDC is composed with three NAND-gates, and this CDC can achieve the same function with one NAND-gate and one inverted-multiplexer. With this approach, the coarse-tuning resolution can enhance to be two NAND-gates delay time. Besides, the NAND-gate transition time is very small because it can be composed with only four transistors. Hence, the glitch problem is very slight. After feed the clock into the proposed fine-tuning circuit, the glitch can be almost eliminated. To balance the output loading of CA_OUT and CB_OUT, we add a dummy cell after CA_OUT. This technique can make the DCO output frequency be more linearly.

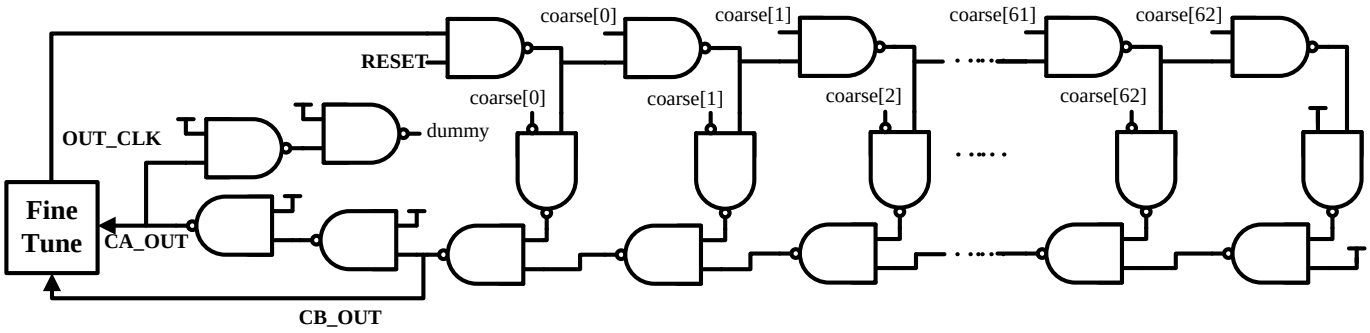


Fig. 4.9: Proposed ladder-shaped coarse-tuning circuit.

4.2.3 Structure of Fine-Tuning Circuit

Fig. 4.10 shows the proposed fine-tuning circuit. This fine-tuning circuit is designed with interpolating technique [35], and it's also designed with standard cells. There are 62 tri-state buffers, and the switches are different on both side. The proposed interpolating fine-tuning circuit sets different states to interpolate an appropriate output clock ratio. There are always 31 tri-state buffer be turned on. It divides one coarse-tuning code to 32 parts. With the proposed interpolating approach, we can achieve monotonic response between the DCO code and output frequency very easily.

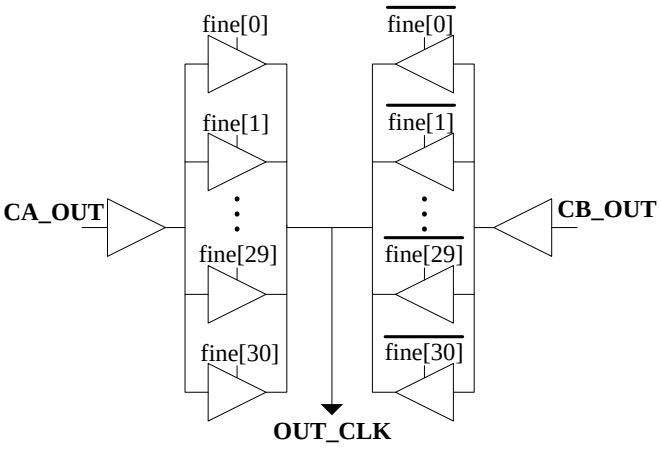


Fig. 4.10: Architecture of proposed interpolating fine-tuning circuit.

4.2.4 Simulation Result

In this thesis we proposed two versions ADSSCG in different process technology with the same DCO architecture. The fast-relocked ADSSCG (version 1) is designed with 90nm CMOS technology, and the counter-based ADSSCG (version 2) is designed with 65nm CMOS technology.

Fig. 4.11 shows the clock period with whole coarse-tuning code. From this figure, we can see the coarse-tuning stage shows high linearity. The operation frequency of Fig. 4.11(a) is in the range from 621ps to 6761ps with 90nm process. The version 2 ADSSCG operated the frequency range from 3247ps to 6607ps as shown in Fig. 4.11(b). The coarse-tuning resolution of these two versions are 97.5ps (version 1) and 53.3ps (version 2) respectively.

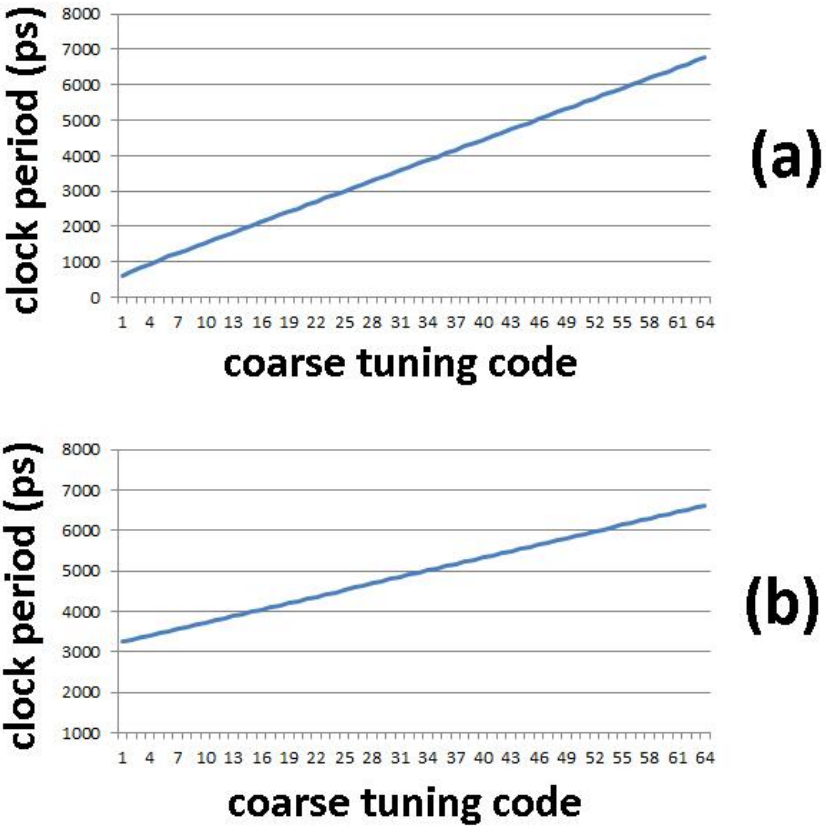


Fig. 4.11: Relationship between coarse-tuning code and clock period (a) DCO with 90nm process (b) DCO with 65nm process.

The simulation result of fine-tuning circuit is shown in Fig. 4.12. From this figure, we can see that there is no overlapped frequency domain. Fig. 4.12(a) seems higher linearity than Fig. 4.12(b). However, due to the different process, the fine-tuning resolution of Fig. 4.12(a) is 3.03ps and Fig. 4.12(b) is 1.67ps. The linearity of these two DCOs is similar.

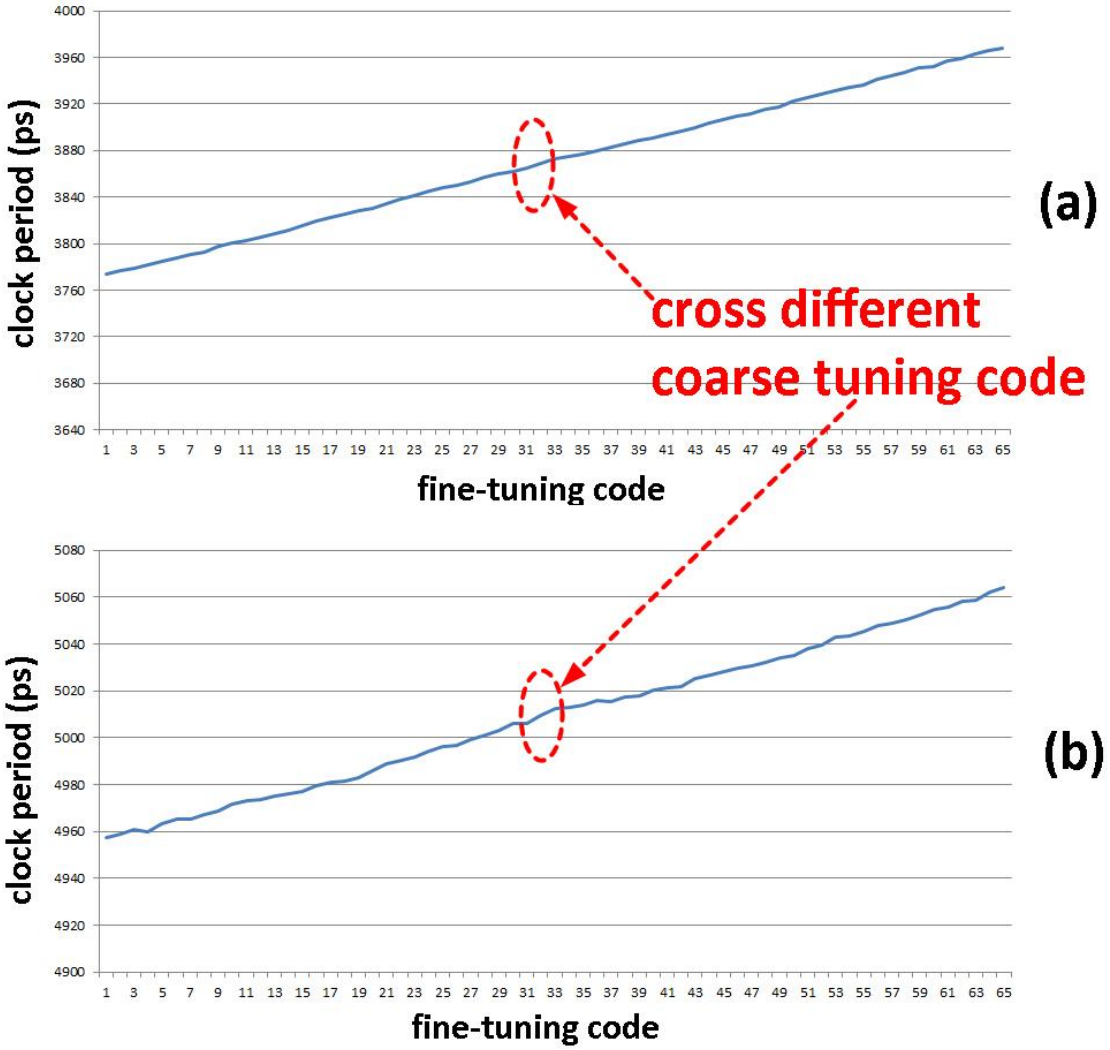


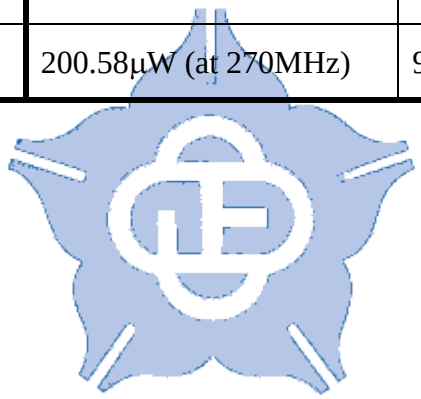
Fig. 4.12: Relationship between fine-tuning code and clock period (a) DCO with 90nm process (b) DCO with 65nm process.

The power dissipation of version 1 DCO is 200.58μW at 270MHz and version 2 consumes 93.63μW at 270MHz. Table 4.1 shows the performance table of the proposed monotonic low-power DCO with different process techniques. With this

proposed DCO, we can minimize the power consumption and achieve a monotonic response when crossing different coarse-tuning code. Therefore, this proposed DCO is very suitable for ADSSCG. Besides, because the proposed DCO is designed with standard cells, it can be ported to different process very easily and it's very suitable for SoC applications.

Table 4.1: Performance table of the two versions of proposed DCO.

	Version 1 (90nm process)	**Version 2 (65nm process)**
Coarse-tuning resolution	97.5ps	53.3ps
Fine-tuning resolution	3.03ps	1.67ps
Output frequency	148MHz ~ 1610MHz	150MHz ~ 307MHz
Power consumption	200.58μW (at 270MHz)	93.63μW (at 270MHz)



Chapter 5

Experimental Results

5.1 Experimental Results of Proposed Fast-relocked ADSSCG

5.1.1 Simulation Result

This proposed fast-relocked ADSSCG is implemented on standard performance TSMC 90nm CMOS process. The chip layout is shown in Fig. 5.1. The active area is $200 \times 200\ \mu m^2$ and the chip area is $624 \times 624\ \mu m^2$. The simulated power consumption is 0.396mW at 270MHz operation frequency.

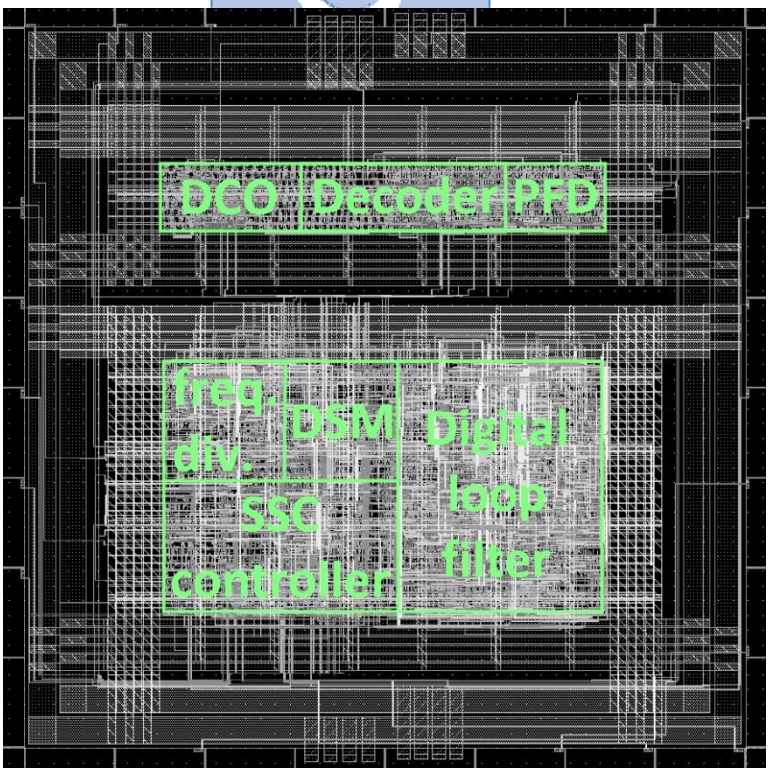


Fig. 5.1: Chip layout of proposed fast-relocked ADSSCG.

Fig. 5.2 shows the simulated power spectral density of the fast-relocked ADSSCG at 270MHz. The EMI reduction with 1% spreading ratio is 14.96dB.

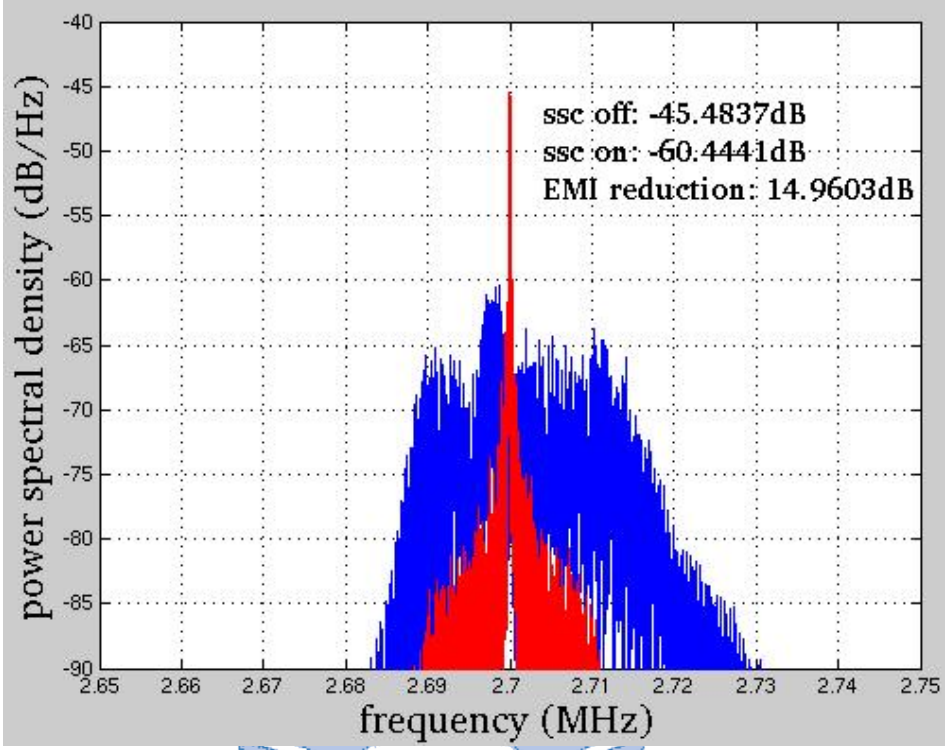


Fig. 5.2: Simulated power spectral density at 270MHz with 1% spreading ratio.

In order to prove the proposed fast-relocked ADSSCG can against PVT variation. We alter the voltage in spread-spectrum state in Fig. 5.3. In Fig. 5.3, the supply voltage is in the range from 0.9V to 1.1V, and the zoom-in view shows the case of voltage variation and fast-relocked waveform. Although the relock time will be increase due to the voltage variation, the nominal frequency can be calibrated eventually. With the same case, the SSCG performs spread spectrum with frequency divider modulation is hard to deal with PVT variation. Because the frequency divider modulated SSCG keeps tracking the reference clock, the modulation profile may be broken or spend a very long time to restore the original operation. Hence, this fast-relocked ADSSCG can perform spread spectrum in worse environment.

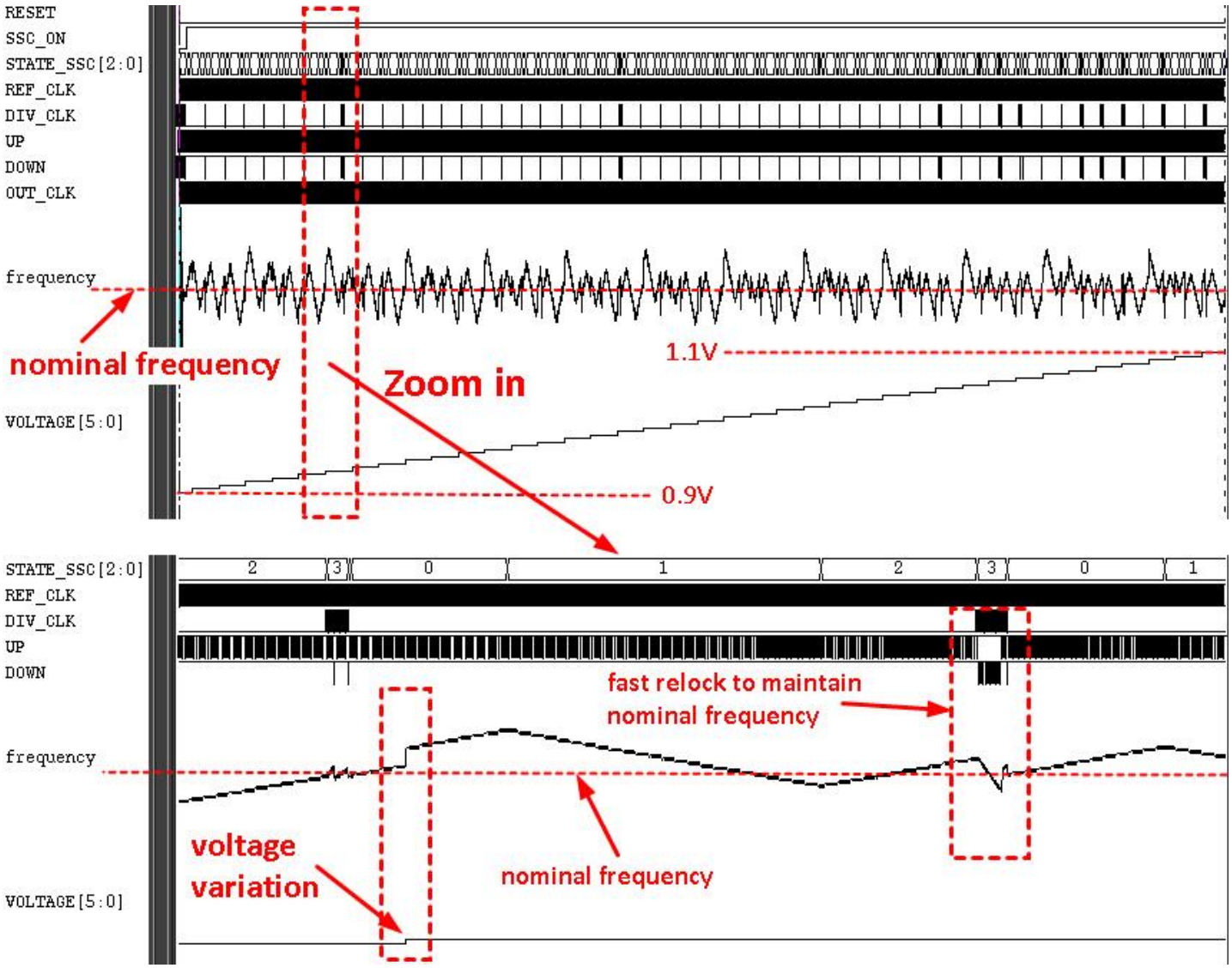


Fig. 5.3: The simulated waveform of ADSSCG operation with voltage variation.

5.1.2 Experimental Environment

Fig. 5.4 shows the chip floor plan and I/O plan of the proposed fast-relocked ADSSCG and the Pad description is shown in Table 5.1. In Table 5.1, the input Pad SPREAD_RATIO represents the spreading ratio code, and one spreading ratio code can perform 0.1953125% spreading ratio. Therefore, the theoretical maximal spreading ratio is 6.0546875%. More bit size can get more spreading ratio. However, this maximal spreading ratio in our circuit can be applied to most applications. Hence, the bit size of SPREAD_RATIO is enough.

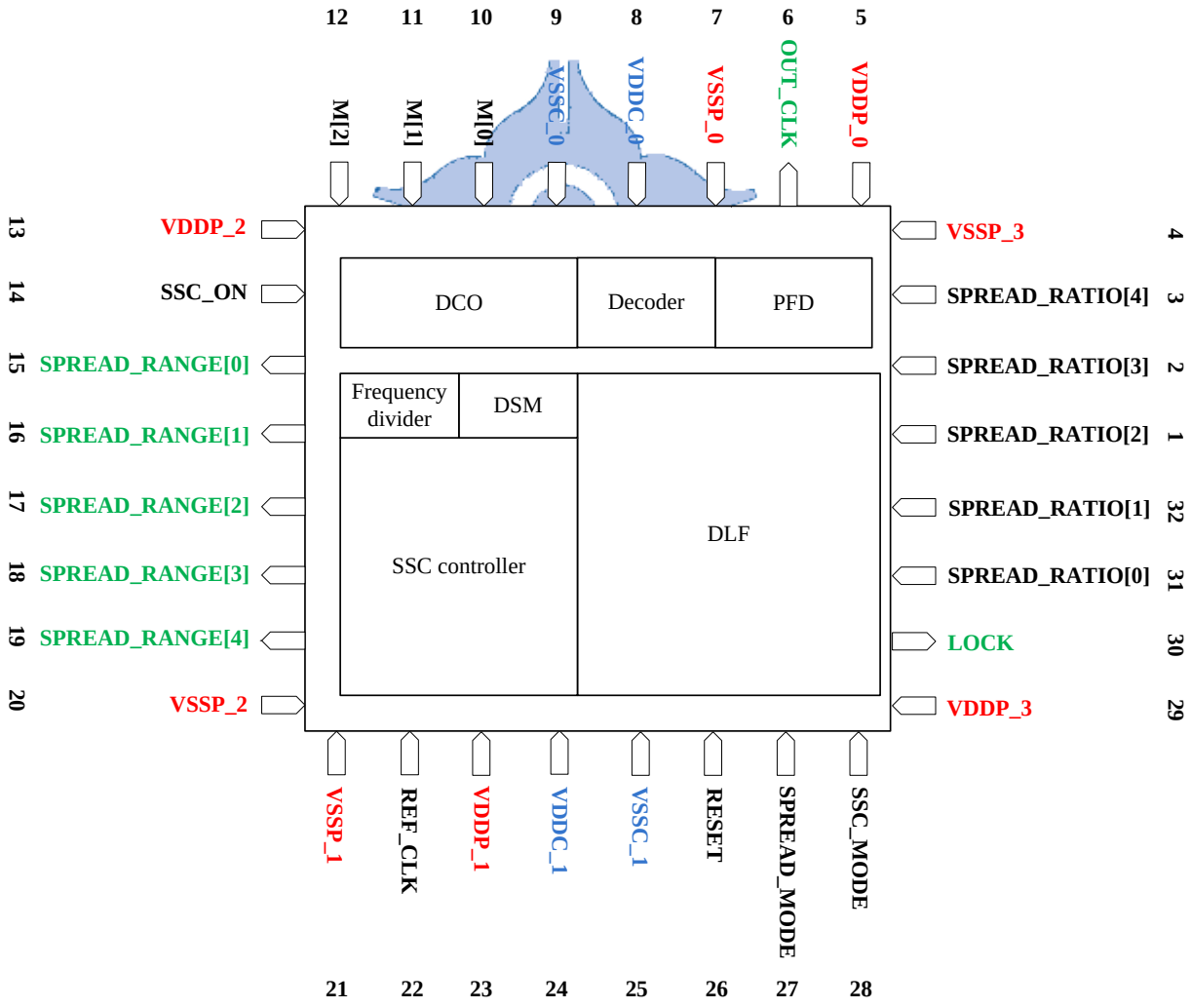


Fig. 5.4: Chip floor plan and I/O plan.

Table 5.1: I/O PAD description.

<table>
<tr><th>input</th><th>bits</th><th>function</th></tr>
<tr><td>RESET</td><td>1</td><td>reset chip</td></tr>
<tr><td>REF_CLK</td><td>1</td><td>input clock</td></tr>
<tr><td>SSC_ON</td><td>1</td><td>perform spread spectrum</td></tr>
<tr><td>SSC_MODE</td><td>1</td><td>center/down spread select</td></tr>
<tr><td>SPREAD_MODE</td><td>1</td><td>spreading ratio/range select</td></tr>
<tr><td>SPREAD_RATIO</td><td>5</td><td>decide the amount of spreading ratio/range</td></tr>
<tr><td rowspan="9">M</td><td rowspan="9">3</td><td colspan="2">select the operation frequency</td></tr>
<tr><td>value</td><td>code output</td></tr>
<tr><td>0</td><td>162MHz</td></tr>
<tr><td>1</td><td>189MHz</td></tr>
<tr><td>2</td><td>216MHz</td></tr>
<tr><td>3</td><td>243MHz</td></tr>
<tr><td>4</td><td>270MHz</td></tr>
<tr><td>5</td><td>297MHz</td></tr>
<tr><td>6</td><td>324MHz</td></tr>
<tr><td>7</td><td>351MHz</td></tr>
<tr><th>output</th><th>bits</th><th>function</th></tr>
<tr><td>LOCK</td><td>1</td><td>frequency and phase tracking complete</td></tr>
<tr><td>OUT_CLK</td><td>1</td><td>ADSSCG output clock</td></tr>
<tr><td>SPREAD_RANGE</td><td>5</td><td>Output corresponding spreading range with specified spreading ratio</td></tr>
</table>

The microphotograph of the proposed fast-relocked ADSSCG is shown in Fig. 5.5. This ADSSCG is designed with all standard cells in TSMC 90nm CMOS technology. The area of the chip with I/O pads is $624 \times 624\ \mu m^2$, and the core area is $200 \times 200\ \mu m^2$. In the floor plan in Fig. 5.4, we divide the chip into two sections. The upper part is unconstrained part, this section contains DCO, PFD, and decoder. The lower part is constrained part, this section contains digital circuit including SSC controller, DLF, frequency divider, and DSM.

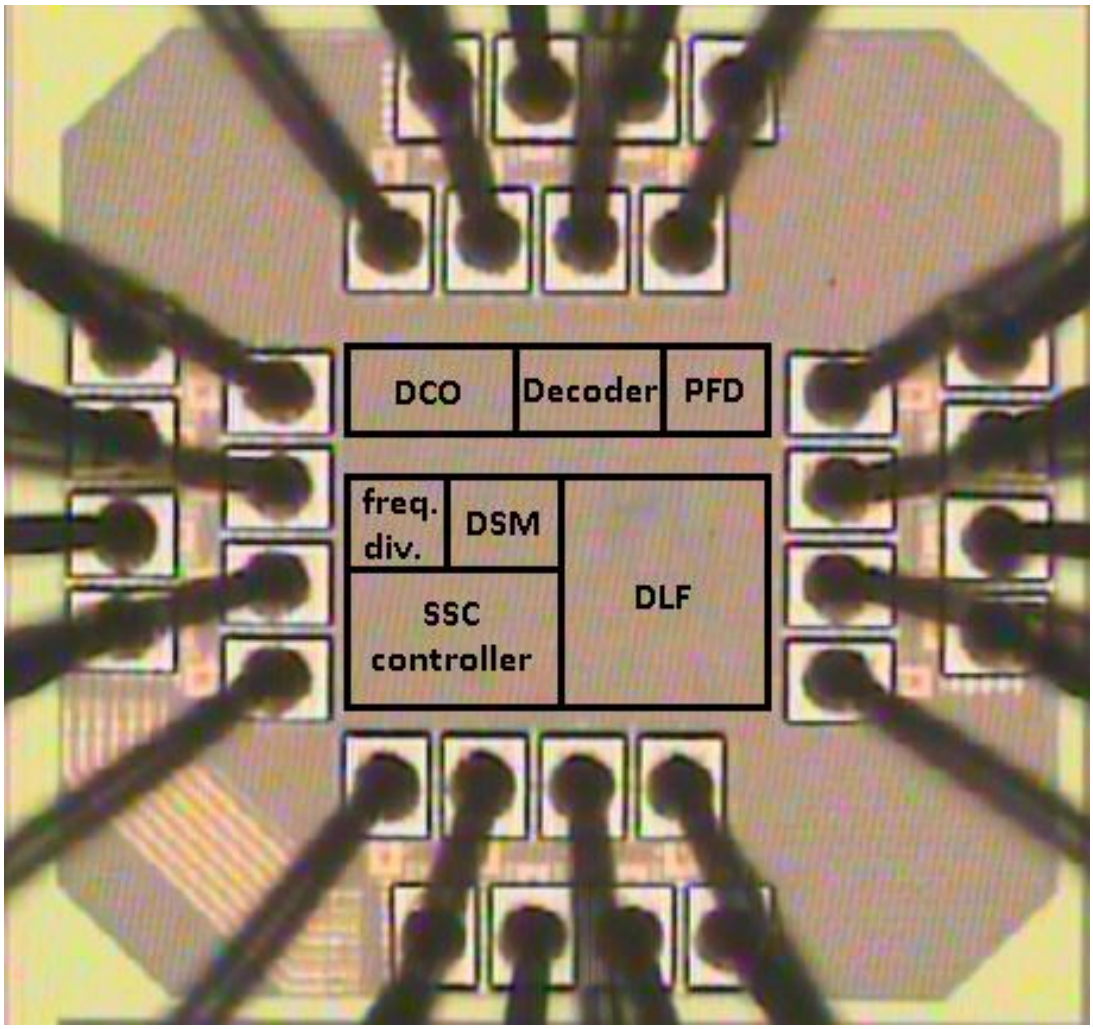


Fig. 5.5: The microphotograph of proposed fast-relocked ADSSCG.

5.1.3 Measurement Result

This proposed fast-relocked ADSSCG has taped out with a standard performance TSMC 90nm CMOS process. The measured power dissipation result is shown in Table 5.2.

Table 5.2: Measured power consumption of fast-relocked ADSSCG with different conditions.

	162MHz	**270MHz**
SSC on	343μW	443μW
SSC off	358μw	477μW

The power spectral density of spread-spectrum off state at 270MHz operation frequency is shown in Fig. 5.6. From this figure, we can see that the peak power is -2.47 dBm with 100 kHz resolution bandwidth (RBW) and 100 kHz video bandwidth (VBW).

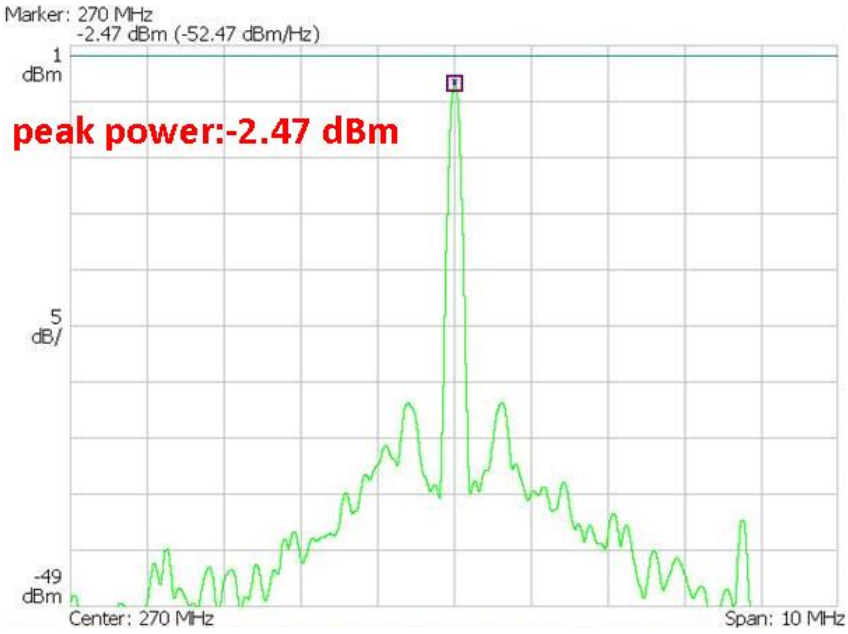


Fig. 5.6: Power spectral density of spread-spectrum off at 270MHz.

After perform spread spectrum, the peak power can be reduced as shown in Fig. 5.7. The EMI reduction with 0.5% spreading ratio is 14.61 dB (Fig. 5.7(a)). When spreading ratio is set to 2%, the EMI reduction effect can be enhanced to 19.69dB as show in Fig. 5.7(b). Finally, Fig. 5.7(c) shows that the performance of EMI reduction is 20.77dB with 2.5% spreading ratio.

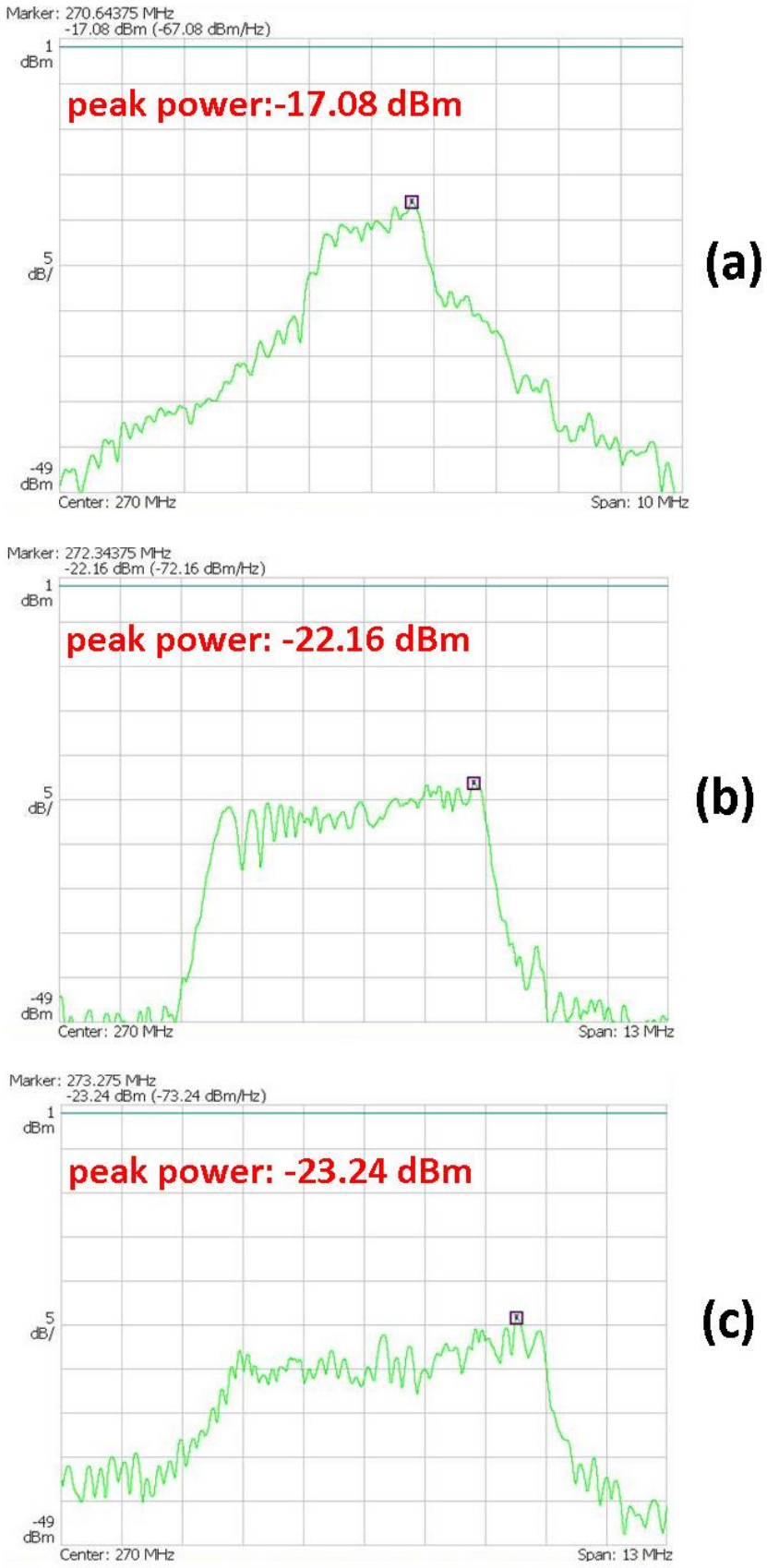


Fig. 5.7: Power spectral density at 270 MHz when spread spectrum with the spreading ratio of (a) 0.5% (b) 2.0% (c) 2.5%.

When the operation frequency is slowed down to 162MHz, the EMI reduction performance is decreased. Because the higher operation frequency can make better EMI reduction result as we mentioned in Section 2.2.4. Fig. 5.8 shows the power spectral density of the spread-spectrum off state (Fig. 5.8(a)) and spread-spectrum on state (Fig. 5.8(b)). The EMI reduction in Fig. 5.8(b) is 10.95dB with 0.5% spreading-ratio.

Fig. 5.8: Power spectral density at 162MHz (a) spread-spectrum off state (b) spread-spectrum clock with 0.5% spreading ratio.

Fig. 5.9 shows the power spectral density with different supply voltage. Because the fast-relocked mechanism can keep tracking the reference clock, there is no frequency drift in these figures. Fig. 5.9(a) shows the power spectral density with 0.5% spreading ratio and 1.0V supply voltage at 270MHz operation frequency. Due to the truly programmable spreading-ratio decision method is adopted. The spreading ratio in Fig. 5.9(b) and Fig. 5.9(c) are identical with voltage variations. Therefore, the proposed ADSSCG can against PVT variation even though the spread-spectrum clock in operating.

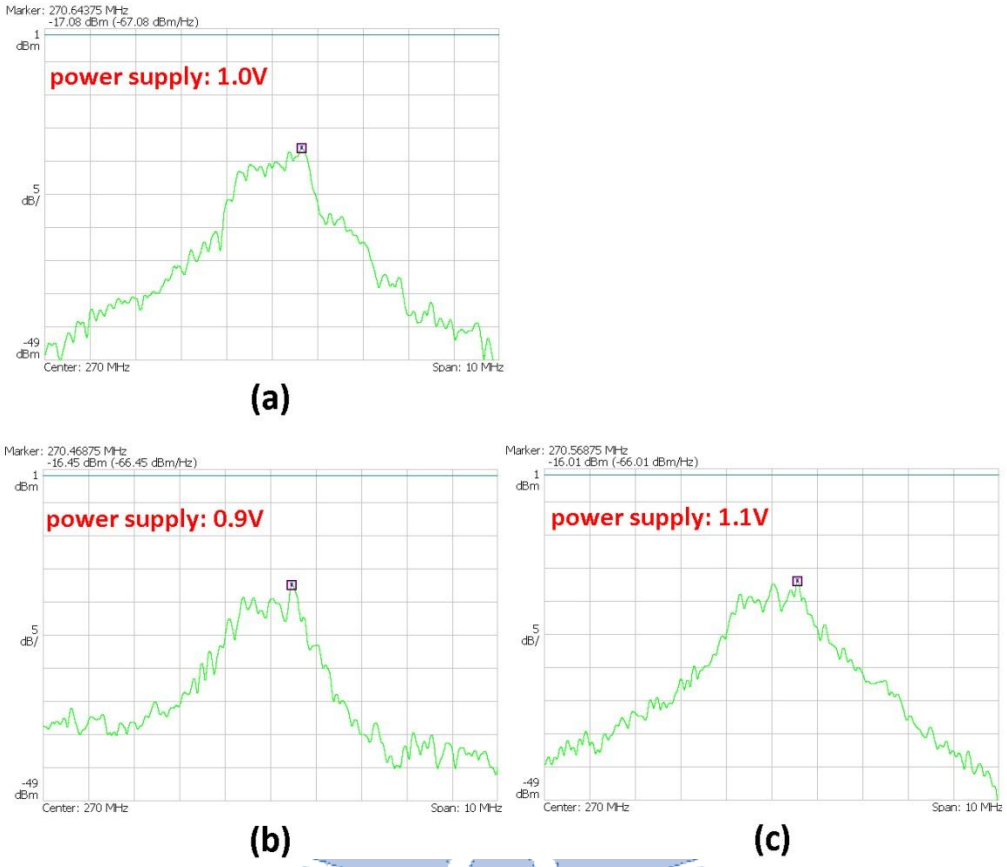


Fig. 5.9: Power spectral density with the same 0.5% spreading ratio at (a) 1.0V supply voltage (b) 0.9V supply voltage (c) 1.1V supply voltage.

We also measure the jitter performance in spread-spectrum state. The cycle-to-cycle jitter at 270MHz with 3% spreading ratio is 791ps as shown in Fig. 5.10, and Fig. 5.11 shows the period jitter with the same setting is 983ps. This jitter performance is not very good. There are some possible reasons to explain the jitter performance. One possible reason is that the input reference clock jitter influences the ADSSCG operation. The other possible reason is the mechanism of DLF. As we mentioned in Section 3.1.5, we use the baseline DCO code to restore the nominal frequency and to minimize the phase error. However, if a large reference clock jitter causes a large control code change, this technique may cause a severe jitter. Nevertheless, this ADSSCG still maintains high frequency stability.

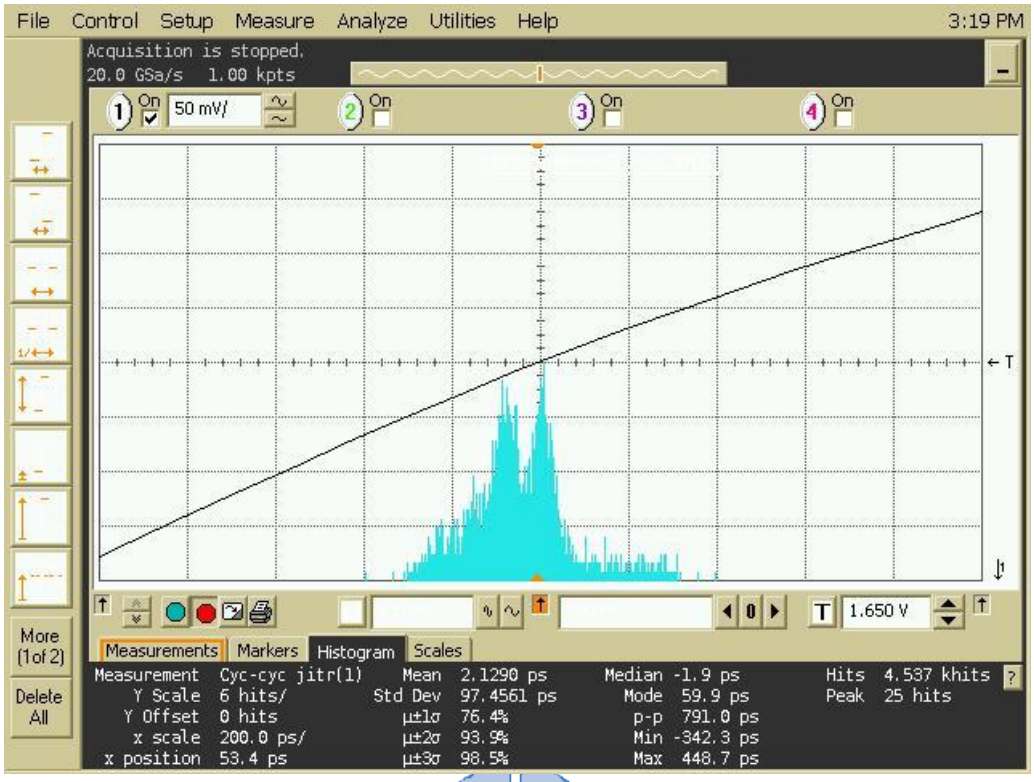


Fig. 5.10: The cycle-to-cycle jitter at 270MHz with 3% spreading ratio.

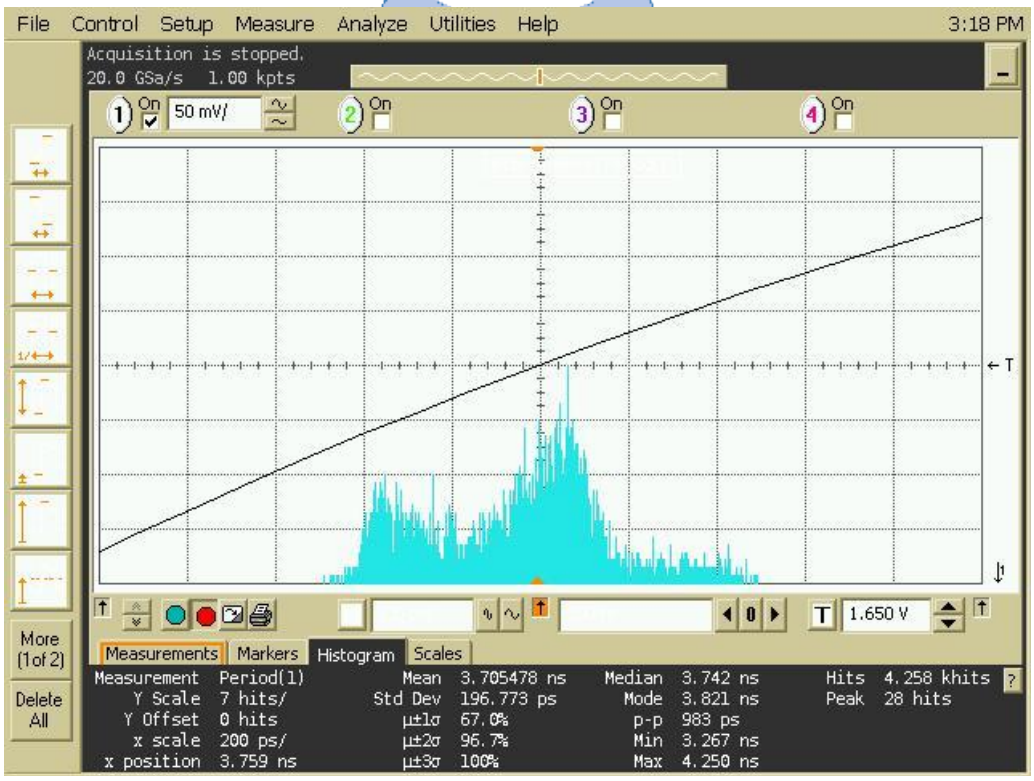


Fig. 5.11: The period jitter at 270MHz with 3% spreading ratio.

5.2 Experimental Results of Proposed Counter-Based ADSSCG

5.2.1 Simulation Result

This proposed counter-based ADSSCG is implemented on standard performance UMC 65nm CMOS process. The chip layout is shown in Fig. 5.12. The active area is $85 \times 85\ \mu m^2$ and the chip area is $555 \times 555\ \mu m^2$.Because the counter-based ADSSCG is implemented in 65nm process and eliminate redundant DLF area, the total area is much smaller than fast-relocked ADSSCG.

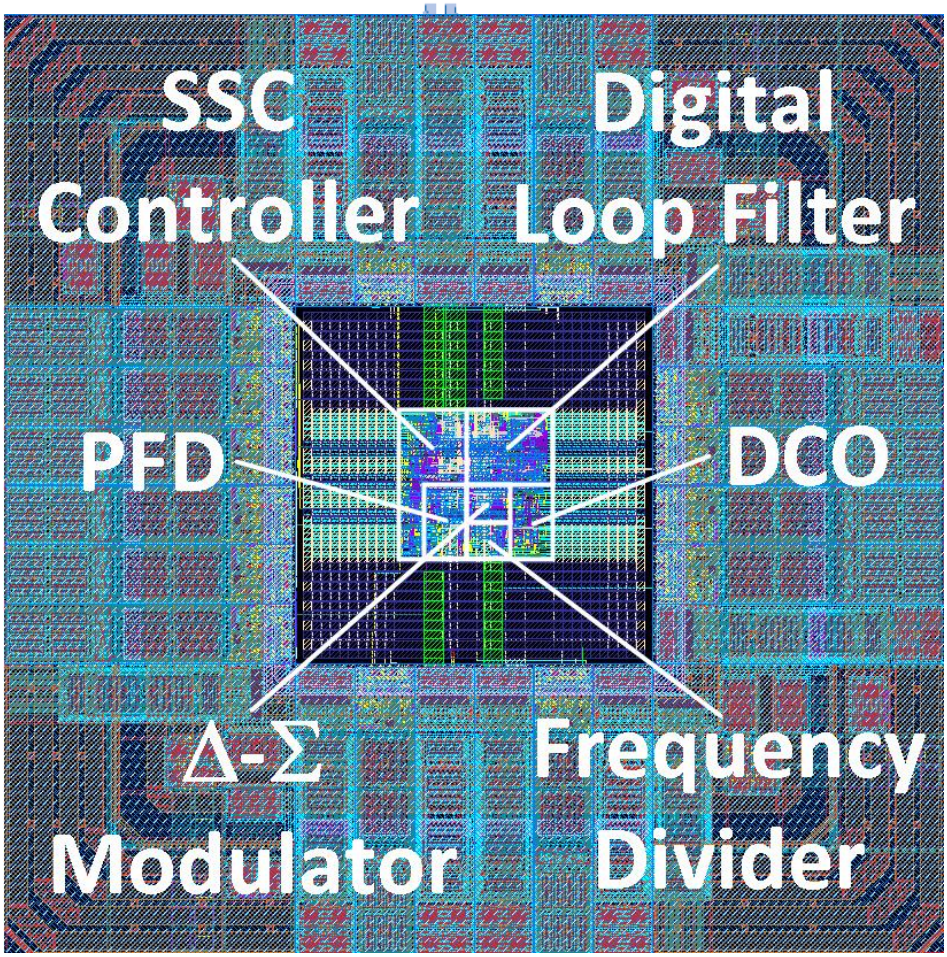


Fig. 5.12: Chip layout of proposed counter-based ADSSCG.

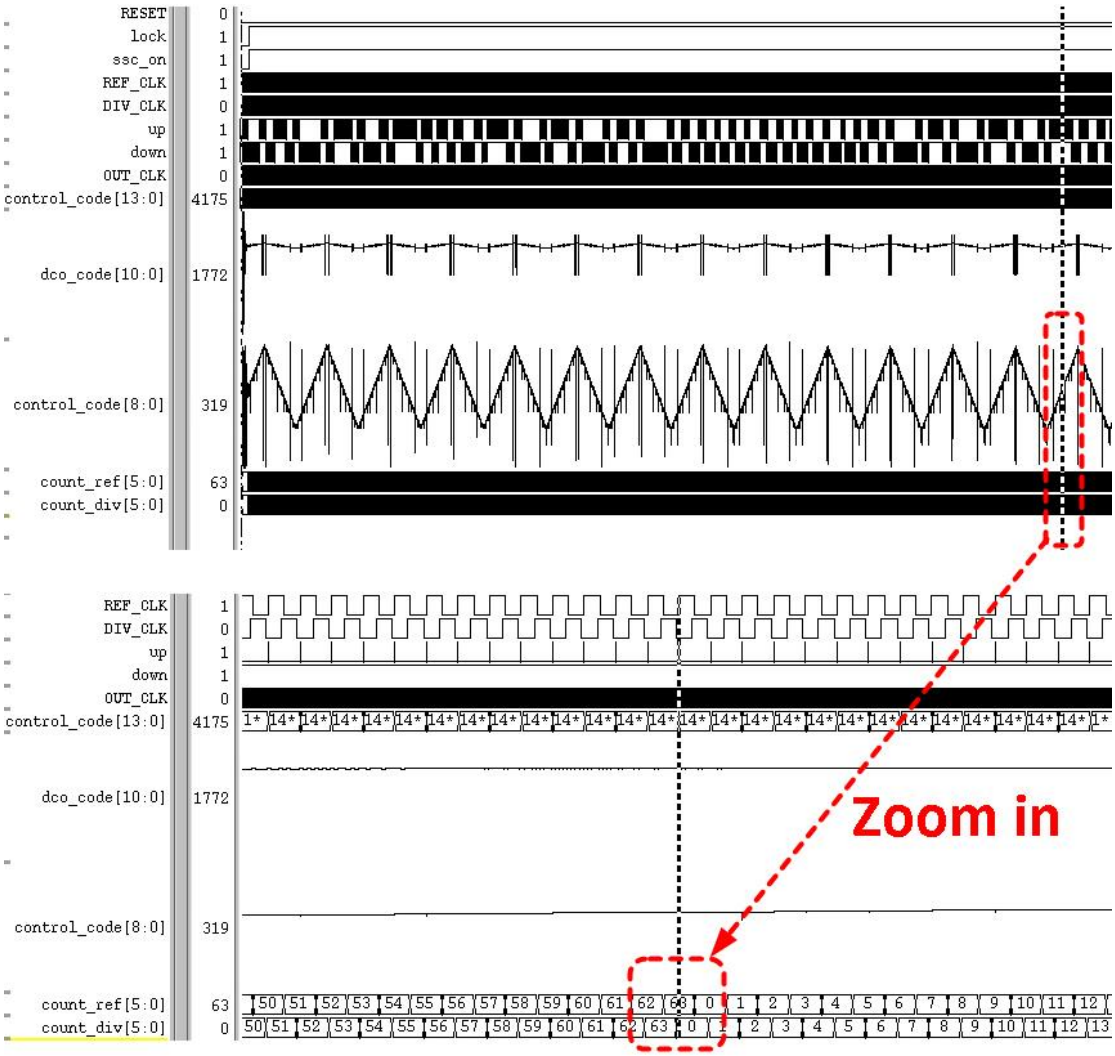


Fig. 5.13: Simulated waveform of proposed counter-based ADSSCG.

Fig. 5.13 shows the simulated waveform. In this figure, the total cycle count of reference clock is almost equal to the cycle count of divided clock even though it has performed spread spectrum for a long time. If the two counters are equally, then we can ensure the average frequency of divided clock is equal to reference clock.

The simulated power consumption is shown in Table 5.3. This counter-based ADSSCG consumes low power dissipation to achieve spread-spectrum clock. One reason to achieve low power approach is due to the advanced process. Besides, this counter-based ADSSCG disables the fast-relocked technique which will consume higher power for phase tracking.

Table 5.3: Simulated power consumption of counter-based ADSSCG with different conditions.

	162MHz	270MHz
SSC on	173.86μW	163.82μW
SSC off	172.82μW	163.93μW

Fig. 5.14 shows the simulated power spectral density of the counter-based ADSSCG at 270MHz. The EMI reduction with 0.5% spreading ratio is 13.99dB in Fig. 5.14(a), and Fig. 5.14(b) shows the 20.59dB EMI reduction with 1.5% spreading ratio.

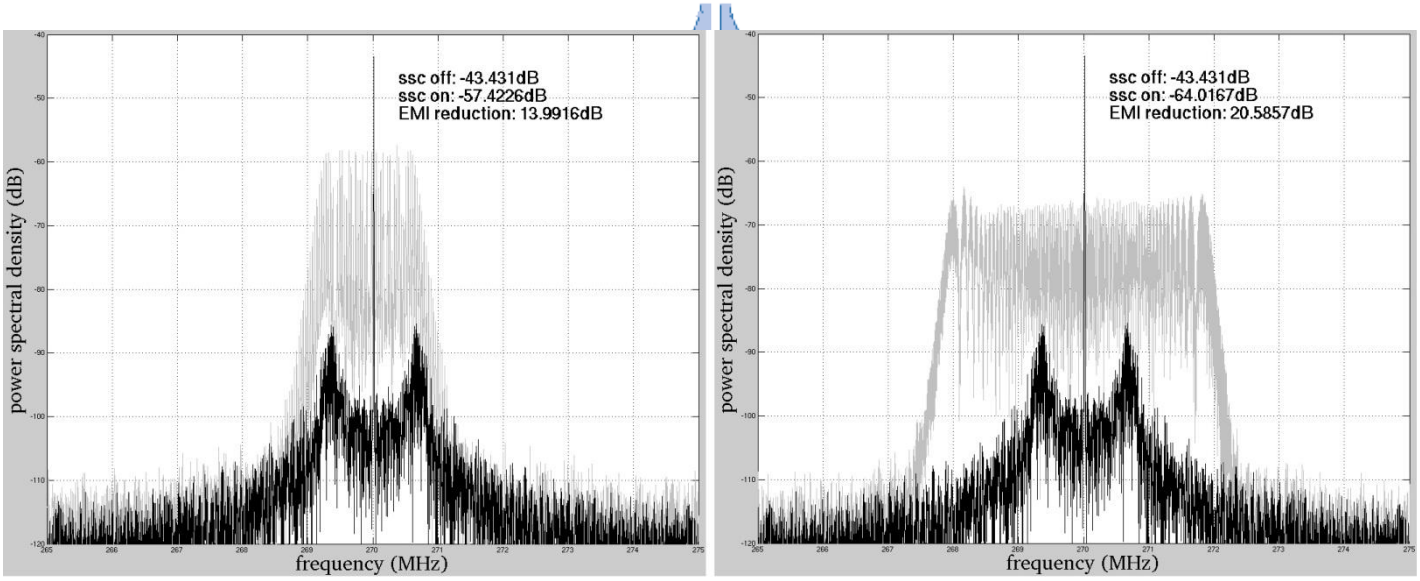


Fig. 5.14: Simulated power spectral density at 270MHz (a) with 0.5% spreading ratio (b) with 1.5% spreading ratio.

The simulated power spectral density at 162MHz is post in Fig. 5.15. From this figure, we can see the EMI reduction in Fig. 5.15(a) is 13.24dB with 0.5% spreading ratio. With the 1.5% spreading ratio, the EMI reduction at 162MHz is 20.23dB as

shown in Fig. 5.15(b).

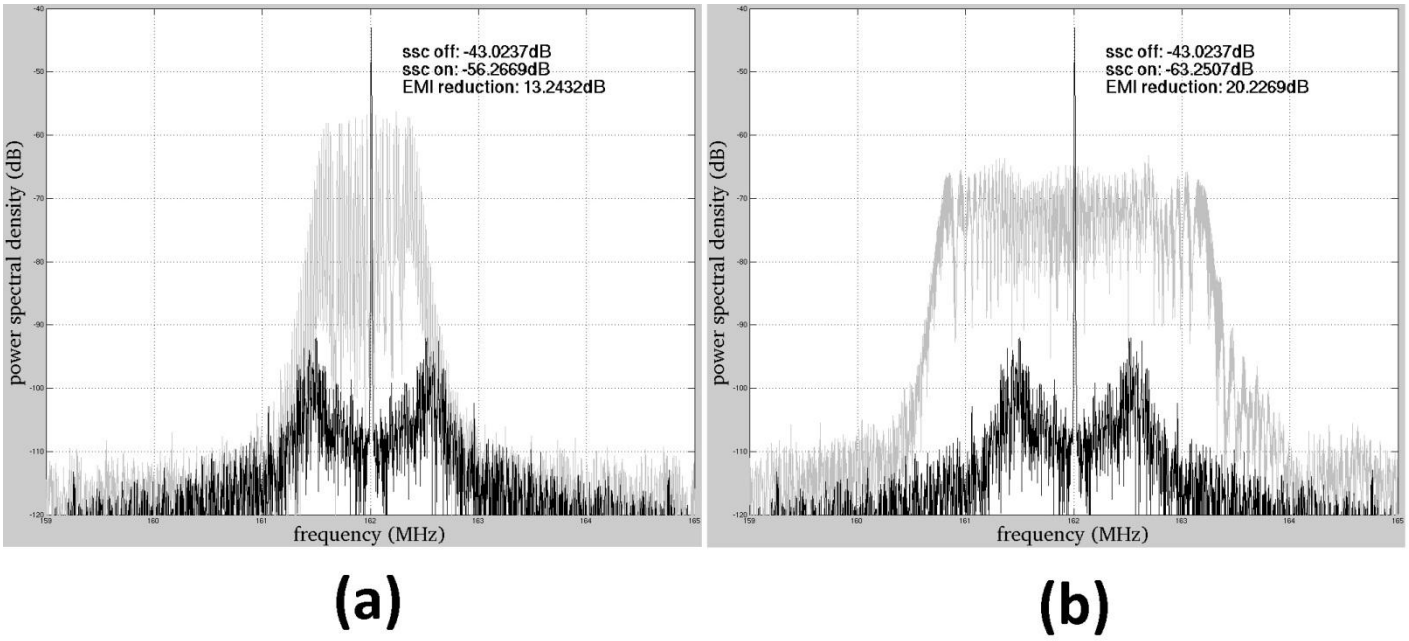


Fig. 5.15: Simulated power spectral density at 162MHz (a) with 0.5% spreading ratio (b) with 1.5% spreading ratio.

5.3 Comparison

In order to highlight the characteristics of our proposed ADSSCG, we make a comparison table in Table 5.4. The first column is the related papers and our proposed ADSSCG, and labels Ver.1 and Ver.2 represents fast-relocked ADSSCG and counter-based ADSSCG. From this comparison table, our power dissipation consumes lowest power. Beside, due to the all-digital approach, our core area also occupies the smallest area. Moreover, for the EMI reduction with 0.5% spreading ratio, our ADSSCGs show the best performance.

Table 5.4: Performance comparisons.

	Modulation profile	Modulation method	EMI reduction	Output frequency	Process	Core area	Power consumption	Peak-to-peak jitter
Ver.1	Triangular	All-Digital (DCO modulation)	14.61dB (0.5%) (@ 270MHz) 19.69dB (2%) (@ 270MHz) 10.95dB (0.5%) (@ 162MHz)	162MHz ~ 270MHz	90nm	0.04 mm^2	443μW (@ 270MHz)	983ps
Ver.2	Triangular	All-Digital (DCO modulation)	13.99dB (0.5%) (@ 270MHz) 20.22dB (1.5%) (@ 162MHz)	162MHz ~ 270MHz	65nm	7225 μm^2	163.82μW (@ 270MHz)	NA
2003 JSSC [15]	Triangular	Analog PLL (VCO modulation)	11dB (2.5%) (@ 266MHz)	66MHz ~ 266MH	0.35μm	2.0 mm^2	300mW (@ 266MHz)	162ps
2010 JSSC [18]	Arbitrary	Digital Delay-Line	20.5dB (6%) (@ 750MHz)	180MHz ~ 1.27GHz	65nm	0.044 mm^2 (excluding PLL)	44mW (@ 1.27GHz) (excluding PLL)	93ps
2009 JSSC [24]	Triangular	All-Digital (ΔΣ PLL)	10.48dB (0.5%) (@ 1.5GHz)	1.5GHz	0.18μm	0.2 mm^2	15mW (@ 1.5GHz)	28.4ps
2011 TVLSI [26]	Division triangular	All-Digital (DCO modulation)	15dB (10%) (@ 27MHz) 9.5dB (1%) (@ 54MHz)	27MHz ~ 54MHz	0.18μm	0.156 mm^2	1.2mW (@54MHz)	NA
2011 TCAS2 [36]	Triangular	Analog PLL (VCO modulation)	8.75dB (0.5%) (@ 270MHz)	162MHz ~ 270MHz	0.18μm	1.8 mm^2	19mW (@ 270MHz)	42.8ps
2009 TEMC [37]	Triangular	Analog PLL (two-point modulation)	10.14dB (0.5%) (@1.5GHz)	1.5GHz	0.18μm	0.2112 mm^2	15.33mW (@1.5GHz)	35ps
2011 JSSC [38]	Triangular	Analog PLL (ΔΣ PLL)	16.12dB (0.5) (@6GHz)	6GHz	90nm	0.2475 mm^2	27.7mW (@6GHz)	8.54ps

Chapter 6

Conclusion and Future Works

6.1 Conclusion

In this thesis, we have presented several solutions to build up an all-digital spread-spectrum clock generator (ADSSCG) to maintain frequency stability while perform spread spectrum. We proposed two versions of ADSSCG.

The Ver.1 is fast-relocked ADSSCG. This version use feedback clock controlling technique to minimize the phase error between reference clock and divided clock. After the phase error is minimized, the phase tracking can be shortened. With this technique, we can perform an accurate triangular modulation profile and achieve high EMI reduction performance.

The Ver.2 is counter-based ADSSCG, this version adopt two counters to accumulate reference clock and divided clock cycles. In spread-spectrum state, these two counters will feed into SSC controller and then adjust the frequency to avoid PVT variation. With this counter-based mechanism, the Ver.2 ADSSCG can perform a perfect triangular modulation profile and result an excellent EMI reduction.

These two versions are both designed with standard cells. Therefore, the proposed ADSSCG not only achieve a low power purpose but also save the cost of active area. Besides, this approach let the ADSSCG be ported to different processes in a very short time. Therefore, the proposed ADSSCG is suitable for system-on-chip (SoC) applications.

6.2 Future Works

In this thesis, our ADSSCG exists some drawbacks. The first problem is the bad jitter performance. In the measurement result in Section 5.1.3, the period jitter and cycle-to-cycle jitter performs unfavorable result. One possible reason is the input reference clock jitter is not very clear, and this input jitter may influence the ADSSCG operation. The other possible reason is the mechanism of DLF. Therefore, if we can provide a clearer reference clock and modify our DLF architecture, the jitter performance will be improved.

There is another issue about modulation frequency. In most applications for SSCG, the modulation frequency is specified in the range from 31 kHz to 33 kHz. However, our ADSSCG cannot perform the required modulation frequency, because our modulation frequency is decided by the spreading ratio. If we can perform difference spreading ratio in the same modulation frequency, then the proposed ADSSCG will be applied extensively.

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