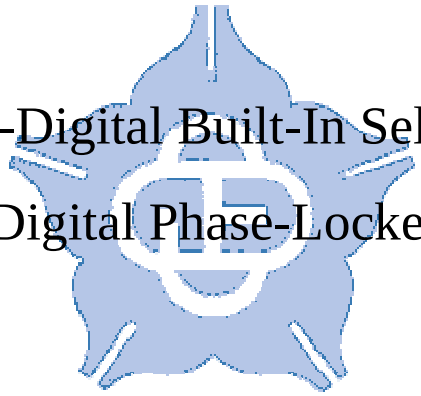
國 立 中 正 大 學

資訊工程研究所碩士論文

應用於全數位鎖相迴路之自我測試電路設計

Design of All-Digital Built-In Self-Test Circuit for All-Digital Phase-Locked Loops



研 究 生 ：朱薇蓉

指 導 教 授 ：鍾菁哲 博士

中華民國 一百 年 七 月

國立中正大學碩士班研究生

學位考試同意書

本人所指導 資訊工程學系

研究生 朱薇蓉 所提之論文

應用於全數位鎖相迴路之自我測試電路設計 Design of an All-Digital Built-In Self-Test Circuit for All-Digital Phase-Locked Loops

同意其提付 碩 士學位論文考試

指導教授 鍾菁哲 簽章

100年6月2日

國立中正大學碩士學位論文考試審定書

資訊工程學系

研究生朱薇蓉 所提之論文

應用於全數位鎖相迴路之自我測試電路設計 Design of an All-Digital Built-In Self-Test Circuit for All-Digital Phase-Locked Loops
經本委員會審查，符合碩士學位論文標準。

學位考試委員會
召　集　人 李順裕 簽章

委　　員 [illegible]

[illegible] [illegible]

[illegible] [illegible]

[illegible] [illegible]

指　導　教　授 [illegible] 簽章

中華民國 102 年 7 月 12 日

應用於全數位鎖相迴路之自我測試電路設計

學生：朱薇蓉　　指導教授：鍾菁哲 博士

國立中正大學資訊工程學系暨研究所

摘要

本論文提出應用於全數位鎖相迴路之自我測試電路，將電路內嵌於晶片做自我測試來取代外部儀器來測試電路。這樣一來，不但可以節省外部儀器的昂貴費用，也可以減少因外接儀器而產生訊號干擾進而造成量測的誤差。本論文提出其測試架構主要分為兩大部分。

第一部分，利用鎖相迴路輸出時脈的抖動量來判斷此電路的抖動是否於容忍範圍內。為了增加量測準確率，此論文使用除頻器代替類比放大器以放大抖動量，這樣一來，可以減少線性放大範圍受製程(process)、電壓(voltage)、以及溫度(temperature)的影響，而除頻器也是容易實現的數位電路；其次，使用游標尺環形震盪器量化抖動值以及循環控制延遲線產生延遲一週期時脈當作自我參照測試訊號，不同於先前作法，不僅不用外部輸入無抖動量之時脈來量測，也可以降低電路面積。

另一部分，除了由輸出時脈的抖動量來做辨別，此論文也進一步探討由鎖相迴路之架構來做量測電路。此論文中，主要分成測試頻率-週期偵測電路(Phase-Frequency Detector)、震盪器控制器(Oscillator Controller)以及除頻器(Frequency Divider)三區塊，盡量以不破壞各區塊內部架構的電路來設計此測試鎖相迴路。因此不但不會破壞鎖相迴路的迴路，對鎖相迴路的效能也不會影響太大。

Design of All-Digital Built-In Self-Test Circuit for All-Digital Phase-Locked Loops

Student：Wei-Jung Chu Advisor：Dr. Ching-Che Chung

Department of Computer Science and Information Engineering,
National Chung Cheng University

Abstract

In this thesis, we propose a design of an all-digital built-in self-test circuit for all-digital phase-locked loops (ADPLLs). Testing circuits are embedded on chip to test the circuit instead of using external instruments. In this way, it not only can save the cost of external instruments, but also can decrease error of measured results which needs to pass through the I/O Pads. Because the external instruments would produce the noise influence and the ground bounce caused by the I/O pad transitions affects the measurement, off-chip measurement circuits will make measured errors. We propose a built-in self-test circuit can be divided into two cases, namely built-in jitter measurement (BIJM) circuit and the built-in self-test (BIST) circuit.

The built-in jitter measurement (BIJM) circuit measures the jitter of phase-locked loop output to determine the performance of PLL. For increasing accuracy of jitter measurement, the circuit extends the jitter by using the frequency divider circuit as a timing amplifier (TA). In the way, it can solve the problem of analog timing amplifiers (TAs) that they have small linear region and the linear region is easily affected by process, voltage, and temperature variations. Besides, the frequency divider circuit is a simple digital circuit and it is easily to implement with standard cells. In addition, the time-to-digital converter (TDC) with the verinier ring

oscillator (VRO) quantizes the jitter and the cycle-controlled delay line (CCDL) circuit produces the signal with one-period delay as the self-test reference clock. Unlike the some prior approaches, the proposed BIJM circuit doesn't need on external clock that is jitter-free clock, and also can decrease the area overhead.

Beside the jitter measurement, this thesis also discusses the testing circuit for the phase-locked loops (PLLs). The proposed built-in self-test (BIST) circuit mainly tests the phase-frequency detector (PFD) circuit, the oscillator the controller circuit, and the frequency divider circuit. We avoid destroying the existing structure to design the testing circuit for the PLL, and the testing circuit slightly affects the performance of the PLL.

Acknowledgements

I would like to express the deepest appreciation to my advisor Dr. Ching-Che Chung who has the attitude and the substance of a genius. He continually encourages and guides the research for many difficulties, and I would give him and his family me best wishes faithfully.

I would like to thank all the S3lab members and give my best wishes for fruitful attainments. I also thank the friends that I've met among two years at National Chung Cheng University I learned a great deal. Finally, I would like to thank my parents, my sister, and my brothers for their support and comfort my when I feel depressed. And I hope them happy and heath forever.

Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 Motivation

The phase-locked loop (PLL) is a mixed-signal circuit used for many applications such as clock generation, timing recovery, frequency synthesizer and clock de-skew. It plays an important role in system-on-chip (SOC) design. Nevertheless, if the PLL doesn't work correctly, it may lead to the overall system failure. Thus it can be seen, it is important to examine the operation of the PLLs before testing the SOC designs.

Traditionally, most of PLL test approaches focus on function test and the jitter measurement. The jitter performance is one of the most important characteristics of the PLLs. Many pieces equipment are required to measure the clock jitter such as a real-time sampling oscilloscope, a spectrum analyzer and other dedicated jitter measurement instruments. Moreover, those instruments need to wait a long time to collect the jitter data and the ground bounce caused by the I/O pad transitions affects the accuracy of the off-chip jitter measurement. However, the cost of those instruments is very expensive.

Additionally, there are many PLLs placed on the SOC design to produce various clock rates for different memory and I/O interfaces. In the way, it is very difficult to measure internal nodes signals of PLL by off-chip instruments. In addition, it should consider the effect of power line and substrate noise and it will increase the testing cost especially.

For above reasons, on-chip measurement circuit is becoming an attractive approach, and it also called built-in self-test (BIST) circuit. From those BIST circuits,

the built-in jitter measurement (BIJM) is the popular approach to determine the performance of the PLLs.

No matter how, the built-in self-test (BIST) circuits need consider the area overhead, power consumption and test cost. Those circuits not only should make those parameters lower as possible as we can, but also avoid affecting the performance of PLLs.

1.2 Design Test Circuit for PLL Overview

1.2.1 Architecture of PLL

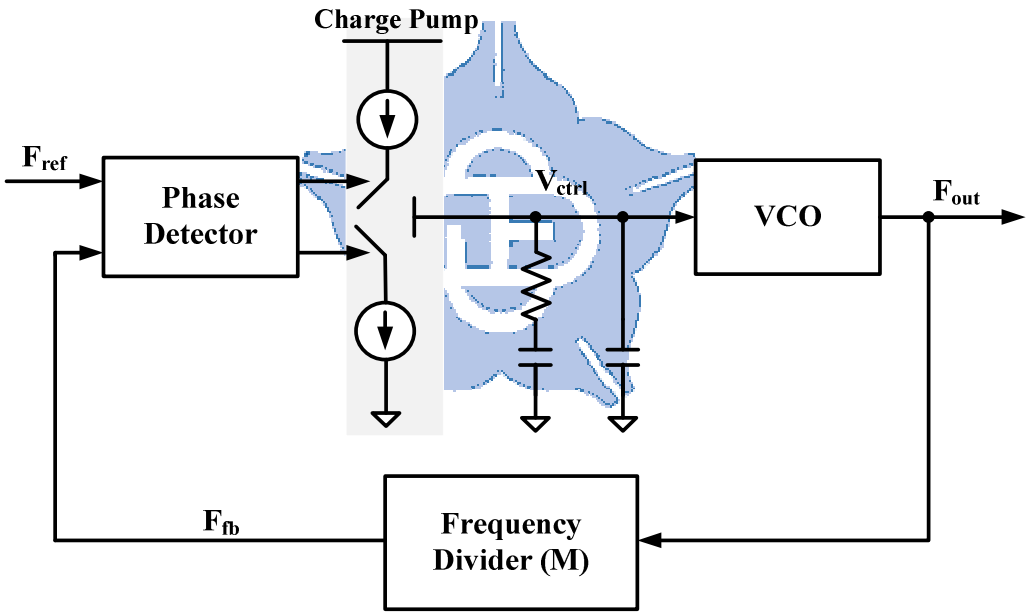


Fig. 1-1 The simple structure of the charge-pump based PLL

Fig. 1-1 presents the simple structure of the phase-locked loop (PLL) [1][2], and it is composed of a phase detector (PD) circuit, a charge pump (CP) circuit, a loop filter (LF) circuit, a voltage-controlled oscillator (VCO) circuit and the frequency divider with ratio M. The charge-pump (CP) circuit controls the controlled voltage by the change of the input clock frequency, and the loop filter (LF) is used to filter out the extreme clock noisy. Subsequently, the LF delivers the filtered control voltage to

the VCO and produces the excepted output frequency. However, the structure suffers from the challenges of MOS leakage problem in advanced CMOS technology, and it would generate the non-anticipate output clock frequency. The all-digital phase-locked loop (ADPLL) is the all-digital circuits. Hence, the ADPLL should have better testability.

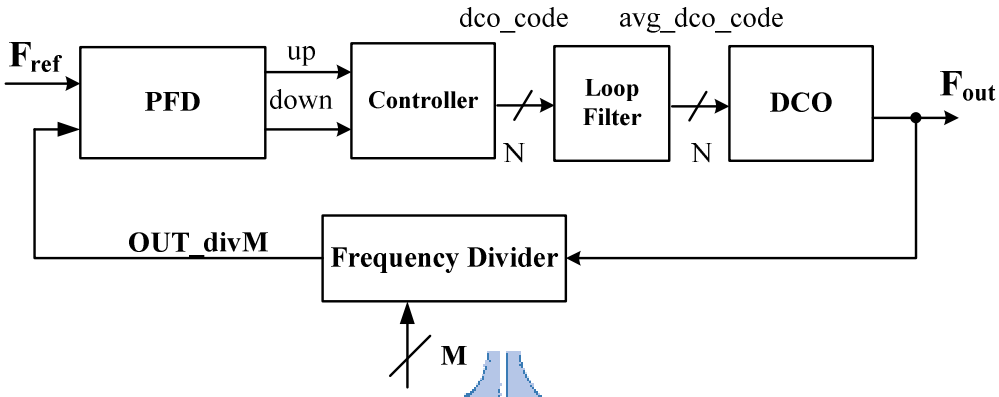


Fig. 1-2 The architecture of all-digital phase-locked loop (ADPLL)

Fig. 1-2 shows the architecture of all digital phase-locked- loop (ADPLL), and it is composed of five blocks, namely phase-frequency detector (PFD) circuit [3], controller circuit, loop filter (LF) circuit, digital controlled oscillator (DCO) circuit [4] and frequency divider. In ADPLL architecture, they are all-digital circuits except the phase-frequency detector (PFD) circuit and the digital-controlled oscillator (DCO) circuit. Among the ADPLL circuit, the PFD circuit is bang-bang PFD in [4]. Moreover, this thesis discusses the design test circuit for all-digital phase-locked loop. The ADPLL can generate a signal (F_{out}) that has fixed relation to the reference signal (F_{ref}) as shown in Eq1-1, and the working principle is described as follows.

$$F_{out} = M * F_{ref} \quad \text{(Eq 1-1)}$$

First, the PFD will detect the phase error and frequency difference between input signal (F_{ref}) and divided signal (OUT_divM), and sent the up or down signal to announce whether the REF_CLK signal leads the divider signal. In other words, if the

F_{ref} leads the OUT_divM, the down signal that output of the PFD block will generate a low pulse. Besides, when the phase error falls into the dead-zone of PFD, the up signal and down signal will remain high. Therefore, the controller block will receive the PFD output and generate the code (dco_code) to control the DCO. In controller block, the binary search is used to achieve the goal code quickly. Nevertheless, the dco_code is easily affected by input jitter and dead-zone of PFD. To improve the jitter performance, the LF block is used to filter out those noise effects and to calculate the average code (avg_dco_code). Through the average code, the DCO will oscillate output clock frequency. Finally, the frequency divider generates the required frequency that is multiply of the reference clock.

1.2.2 Specifications of ADPLL

Table 1-1 The specifications of ADPLL

Parameter	**Description**
Target Process	Target Foundry Process
Reference Clock (Capture Range)	Minimum and Maximum clock reference frequency
Output Clock (Lock Range)	Minimum and Maximum clock output frequency
Programmable Input and Feedback Divider	Minimum and Maximum divide ratios for input and feedback divider
Lock-in Time (#cycle)	Maximum required lock-in time
Re-lock time (#cycle)	Maximum re-lock time responds to a input change
Output Jitter (ps)	Maximum output jitter
Root-Mean-Square (RMS) Jitter (ps)	RMS output jitter
Peak-to-Peak Jitter (ps)	Pk-Pk output jitter
Output Phase Drift (ps)	Maximum phase error between reference and output
Power consumption (mW)	Maximum dynamic/static power consumptions

We can determine the PLL through the specifications. The specifications of ADPLL are shown in Table 1-1, and the detail descriptions of the rest blocks are following. Beside the indirectly testing PLL, the parameters of PLL also can be refer to determine the operation of PLL [5].

1.2.2.1 Reference Clock and Output Clock

The reference clock signal and output clock signal are also called capture range and lock range respectively. Both of they are the important measured parameters of operation frequency of the PLLs. The capture range is the range of input clock frequency which the PLL can acquire lock signal, and the lock range is the range of output clock frequency which the PLL can remain the output clock frequency.

1.2.2.2 Lock Time and Re-Lock Time

The lock time means that the output frequency from the initial frequency to the expected output clock frequency. However, lock time is influenced by process, voltage, temperature (PVT) variations. In other case, the factor of divider and the DCO output clock frequency are unchanged, and the input clock frequency is changed. Therefore, the re-lock time is the time for PLL to realign the phase of the feedback clock.

1.2.2.3 Jitter

In the relative jitter information of specifications of PLL, we can determine the PLL through the output jitter, the root-mean-square (RMS) jitter and the peak-to-peak (Pk-Pk) jitter. The detail description of output jitter will discuss in next chapter. Moreover, the RMS jitter is the standard deviation value of output clock frequency jitter which collected in interval period, and the Pk-Pk jitter is the difference of the maximum jitter value and the minimum jitter value. Their formulas are described as the following equations.

$$J_{RMS} = \sqrt{\frac{\left(J_i - \overline{J}\right)^2}{N_{jitter}}} \quad \text{(Eq 1-2)}$$

Where the J_i is *i*-th value of the output jitter, and the $\overline{J}$ is the average value of the output jitter, the N_{jitter} is the number of output jitter values in interval time, and the J_{RMS} is the root-mean-square value of output jitter in interval time.

$$J_{Pk} = J_{max} - J_{min} \quad \text{(Eq 1-3)}$$

Where the J_{max} is the maximum jitter of output jitter and the J_{min} is the minimum jitter at present, and the J_{Pk} is the peak-to-peak jitter in interval time.

Nevertheless, if the RMS jitter and Pk-Pk jitter exceed the threshold value which is different in different clock frequency, the PLL will be failed. However, the RMS jitter and the Pk-Pk jitter takes a long time to calculate.

1.2.3 Design Challenges for Test PLL

Some of design test circuits use the above parameters and some of design test circuits [33][37][35][40] use the indirect measurement to observe the operation of PLL, but it is still difficult to observe directly the signals of internal nodes. Moreover, there are many challenges for designing test circuits for ADPLL.

First of all, there are many PLLs placed on the chip to offer various clock rates for memory and I/O interfaces. It is difficult to test each PLL by off-chip measurement instruments, and those measurement instruments are expensive. Besides, the output rate of the test input clock signal is limited by the I/O pad. Therefore, the built-in self-test (BIST) circuit is proposed, and the built-in jitter measurement (BIJM) circuit is proposed for jitter measurement.

Secondly, even though the all-digital phase-locked loops are digital circuits, the digital-controlled oscillator (DCO) circuit and the phase-frequency detector (PFD)

circuit are still difficult to be tested individually because of the DCO circuit and the PFD circuit are not purely digital logic circuits.

Thirdly, the most important in the parameter of specifications is jitter performance. Moreover, the time difference is becoming too smaller to be measured because of the advance of the process, both of the data rates and the speed of the clock increases are quickly. For measuring the small jitter, the timing amplifier (TA) is proposed [17][20-22][29]. The TAs extend jitter, and also can increase the accuracy of jitter measurement.

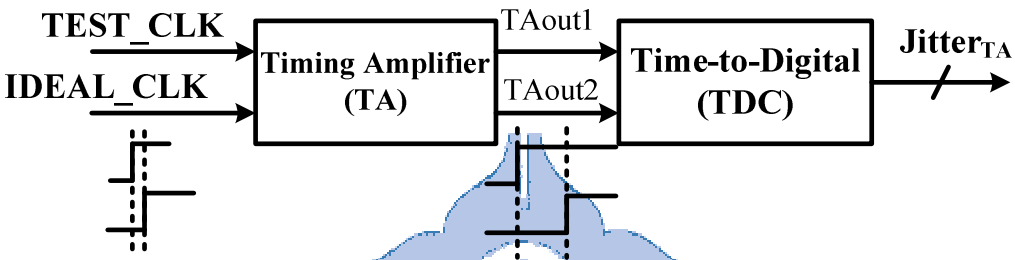


Fig. 1-3 The concept of built-in jitter measurement with timing amplifier

Nowadays, the concept of a built-in jitter measurement circuits is shown in Fig. 1-3, and it is composed of a timing amplifier (TA) circuit and a time-to-digital converter (TDC) circuit. The input of TA is the test signal that we want to measure the jitter (TEST_CLK), and the reference signal (IDEAL_CLK) that samples testing clock to measure jitter. Furthermore, the TDC converts the time difference into digital codes. Moreover, the linearity of TA is very important to obtain a precise jitter measurement result, and the resolution of TDC also affects accuracy of the jitter measurement.

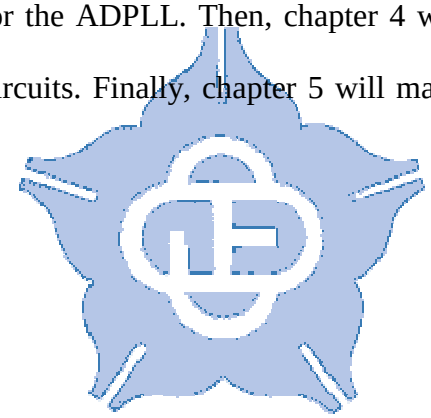
Finally, no matter the BIJM circuits or other test PLL circuits, most of those circuits need a jitter-free clock frequency as a reference clock to determine the jitter performance. In fact, it is very difficult to acquire a jitter-free clock as a reference clock input. Therefore, the self-referred structure [10][11][14][15][17][18][22][30] is

utilized to solve the problem of jitter-free clock. In the self-referred structures, an attractive approach is one-period delay structure.

1.3 Thesis Organization

In this thesis, we propose two circuits to test PLL, the built-in jitter measurement (BIJM) circuit and the built-in self-test circuit for ADPLL, and the simulation environment is in 65 nm CMOS process.

In chapter 2, it will describe the proposed built-in jitter measurement (BIJM) circuit and detail architecture. In chapter 3, it will present the proposed built-in self-test (BIST) circuit for the ADPLL. Then, chapter 4 will show the experimental results of the proposed circuits. Finally, chapter 5 will make conclusion and discuss the future works.



Chapter 2 Built-In Jitter Measurement for ADPLL

2.1. Jitter Definition

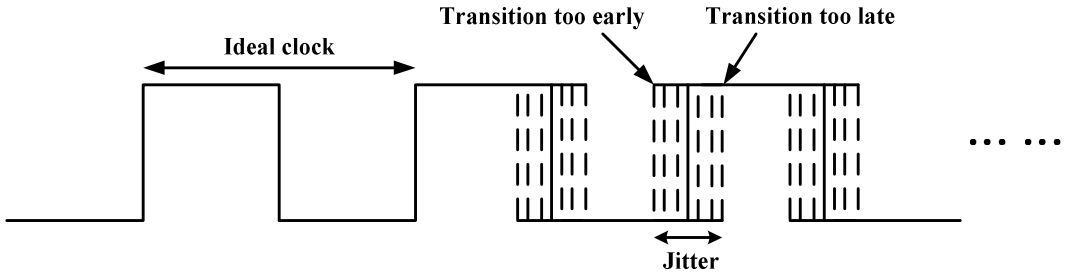


Fig. 2-1 Jitter definition

The jitter can be defined as the variation of a signal with respect to its ideal position in interval time as shown in Fig. 2-1. There are many elements that can affect the output clock jitter, such as the device noise, supply variations, and interference coupled from nearby circuits. The common jitter can be categorized into three types, namely period jitter, cycle-to-cycle jitter and N-cycle jitter [6].

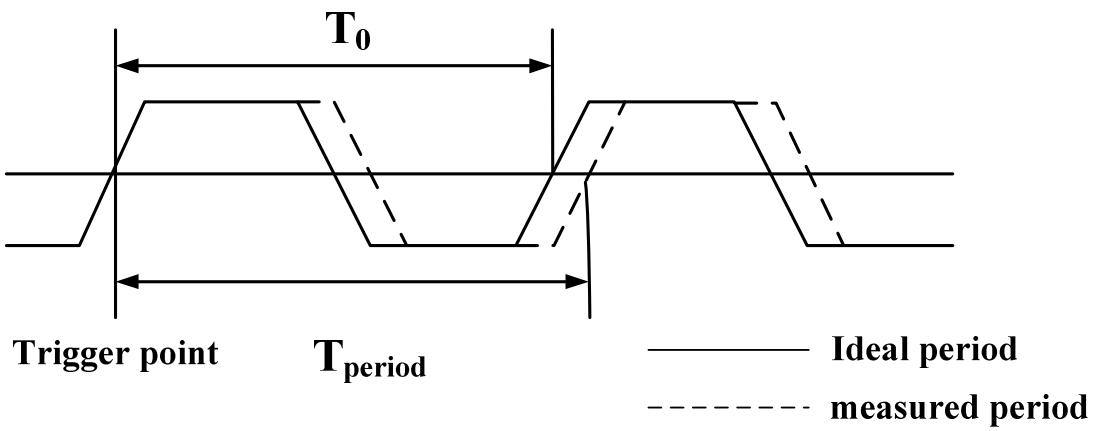


Fig. 2-2 The definition of period jitter (J_{period})

First of all, the period jitter (J_{period}) is the time difference between the measured cycle period and the ideal cycle period as shown in Fig. 2-2, and the period jitter can be calculated in the following equation.

$$J_{period} = T_0 - T_{period} \quad \text{(Eq 2-1)}$$

Where the J_{period} is the period jitter of the input clock signal, the T_0 is the ideal cycle period, and the T_{period} is the measured cycle period.

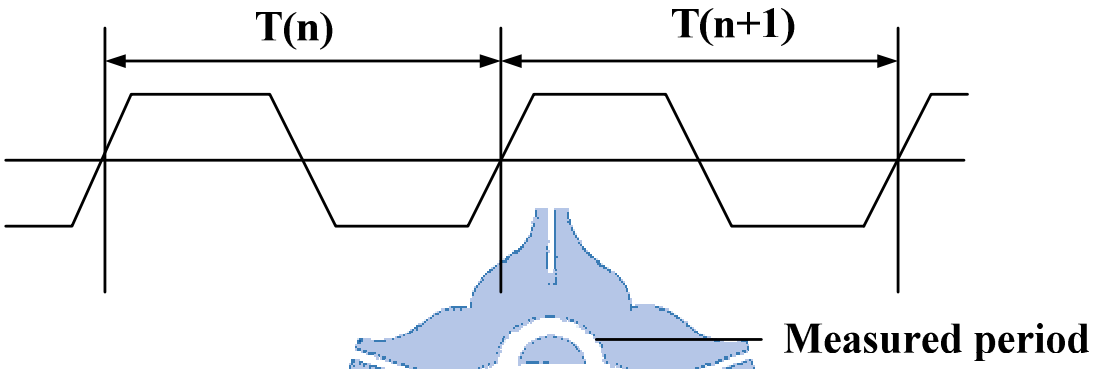


Fig. 2-3 The cycle-to-cycle jitter (J_{cc})

Second, the cycle-to-cycle jitter (J_{cc}) is the time difference of adjacent cycle periods as shown in Fig. 2-3, and the cycle-to-cycle jitter can be measured by following equation.

$$J_{cc} = T(n+1) - T(n) \quad \text{(Eq 2-2)}$$

Where the J_{cc} is the cycle-to-cycle jitter, T(n) is the n-th measured cycle period, and the T(n+1) is the (n+1)-th measured cycle period.

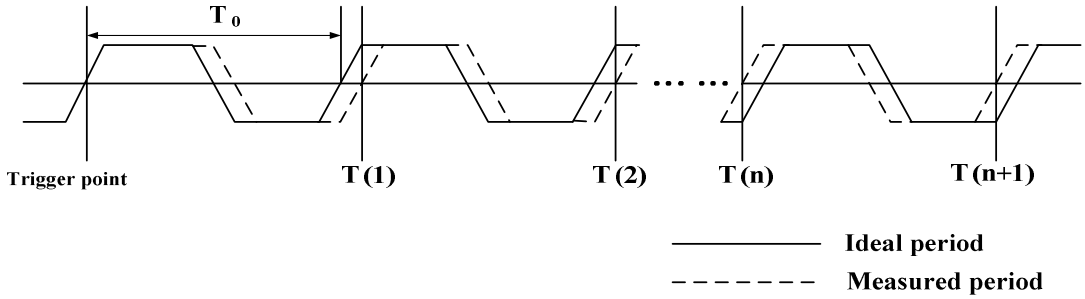


Fig. 2-4 The N-cycle definition (J_{long})

Third, the N-cycle jitter (J_{long}) is the time displacement of the edges of a clock relative to the triggering edge of the same clock as shown in Fig. 2-4, and it is also called the long-term jitter. The jitter value can be calculated by following equations.

$$J_{long} = T(n) - n * T_0 \quad \text{(Eq 2-3)}$$

Where the J_{long} is the N-cycle jitter, the T0 is he ideal cycle period, and the T(n) is the n-th cycle period.

However, the period jitter can measure the Peak-to-Peak (Pk-Pk) jitter and the root-mean-square (RMS) value, and the cycle-to-cycle jitter is important to measure the margins of setup time and hold time, and the long-term jitter can be used measure the average of input clock frequency, and is very important in data transmission

2.2. Conventional BIJM circuits

According to the previously discussion, since there are many PLLs on the chip, it is not easy to measure the run-time jitter performance of the on-chip PLLs by off-chip jitter measurement instruments. Therefore, the on-chip jitter measurement circuits are proposed to measure jitter, and they are also called built-in jitter measurement (BIJM) circuits [7-30].

In the section 1.2, some of BIJM circuits use the timing amplifier (TA) to enlarge the jitter for improving the accuracy of jitter measurement [17][20-22][29].

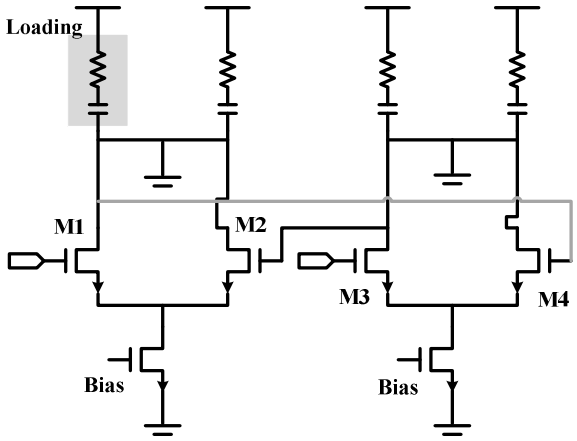


Fig. 2-5 The schematic of analog timing amplifier [45]

Fig. 2-5 presents the schematic of analog timing amplifier circuit in [17][20][21][[45]. The linearity of timing amplifier would affect the jitter measurement, so it is important to amplify jitter with linearity. Moreover, the analog time amplifiers often have a very small linear region and this linear region is easily affected by process, voltage, temperature (PVT) variations. Therefore, a post-silicon calibration is often needed to improve the linearity of the timing amplifier (TA), and the calibration cost increases the total cost of the built-in jitter measurement (BIJM) circuits.

We will describe the BIJM circuits by its measured architecture in following sections, and the time-to-digital converter (TDC) is the more popular approach to quantize the time difference.

2.2.1. Time-to-Digital Converter

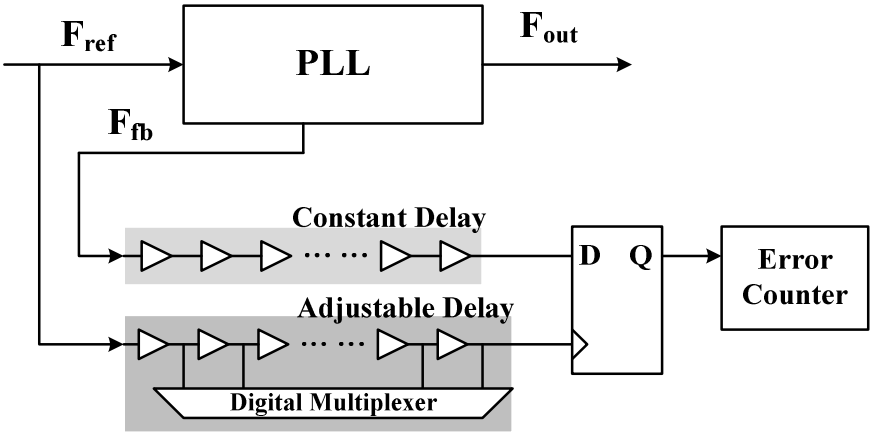


Fig. 2-6 The delay line for jitter measurement [7]

The time-to-digital converter (TDC) structure [7-22] is the popular method to measure jitter, and the earlier proposed structure is the delay line circuit [7-10], and we discuss the representational circuit as shown in Fig. 2-6. The signal which is connected to the fixed delay line (constant delay line) is the PLL output divided by the frequency divider, and it is the feedback signal in PLL. Then, the constant output delivers to the data of the D-flip-flop and the PLL input is connected to the clock of the D-flip-flop with a digitally-controlled adjustable delay line. Therefore, the resolution of jitter measurement circuit is the delay time step of the adjustable delay line. The maximum delay time of the adjustable is approximately twice times longer than the constant delay time.

Moreover, the D-flip-flop compares the output with the excepted value, and the error counter will record the results. The excepted value is always logic "1", and the error counter will count downward. However, the structure can't achieve a high resolution with the process variation, and it has a large area overhead. For improving the resolution, the vernier delay line (VDL) circuit is proposed [11-15].

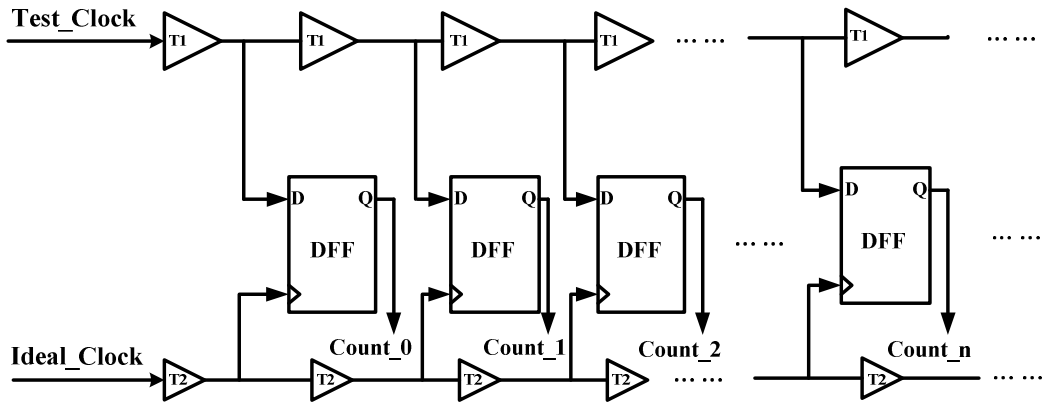


Fig. 2-7 The simple structure of vernier delay line (VDL)

The structure of the TDC circuit with VDL structure is shown in Fig. 2-7, and the structure of VDL uses two delay lines with different tapped delay, delay time T1 and delay time T2. The test clock is connected to the upper delay line, and the reference clock with ideal period is connected to the lower delay line. Moreover, the upper delay line with delay time step T1 must be longer than lower delay line with delay time step T2, and the resolution of the BIJM circuit is equal to (T1-T2). The TDC with VDL structure can improve the resolution of BIJM circuit, but the structure still has a large area overhead when the range of the input clock period width becomes wider.

However, the DL structure and the VDL structure have the same problem that their area overhead is large, and those logic gate will make the mismatch problem that every logic gate doesn't have the same rise/fall time delay change entirely in process, voltage, and temperature (PVT) variations. Thus, the resolution will be different with PVT variations, and affects the accuracy of jitter measurement. Therefore, the vernier ring oscillator (VRO) circuits are utilized in [16-20] to reduce the area overhead and solve the mismatch problem.

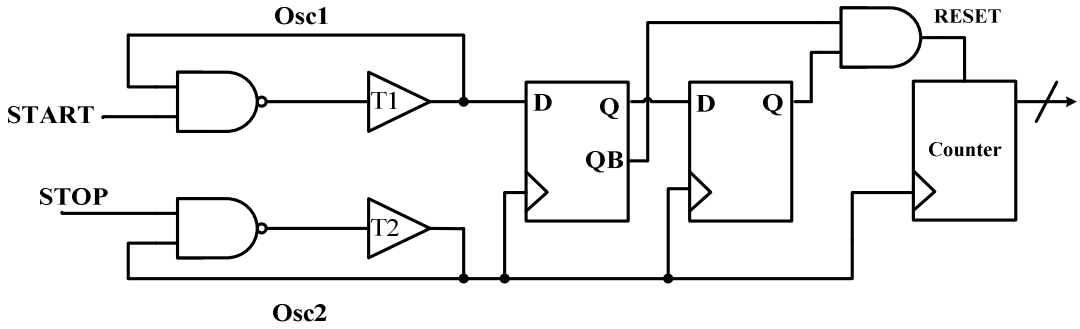


Fig. 2-8 The structure of vernier ring oscillator [16]

Fig. 2-8 shows the structure of the vernier ring oscillator (VRO) in [16], and it uses two pairs of ring oscillators to quantize the pulse width information into digital codes. The resolution of TDC is equal to the period difference between the "Osc1" clock and the "Osc2" clock in the VRO structure, and the period of T1 must longer than the period of T2.

Table 2-1 The comparison table of the time-to-digital converter

Architecture	**DL [7-10]**	**VDL [11-15]**	**VRO [15-20]**
Test time	Run-time	Run-time	Long time
Resolution	Low resolution	High resolution	High resolution
Area	Large overhead	Large overhead	Small overhead
Gates mismatch	yes	yes	no

Table 2-1 shows the comparison of the TDC circuits with different typed delay line. Therefore, the VRO not only can maintain high resolution of TDC, but also reduces the area overhead. Thus, it is suitable for the built-in jitter measurement (BIJM) circuits design.

2.2.2. Others Architecture

1. Interpolated [23]：

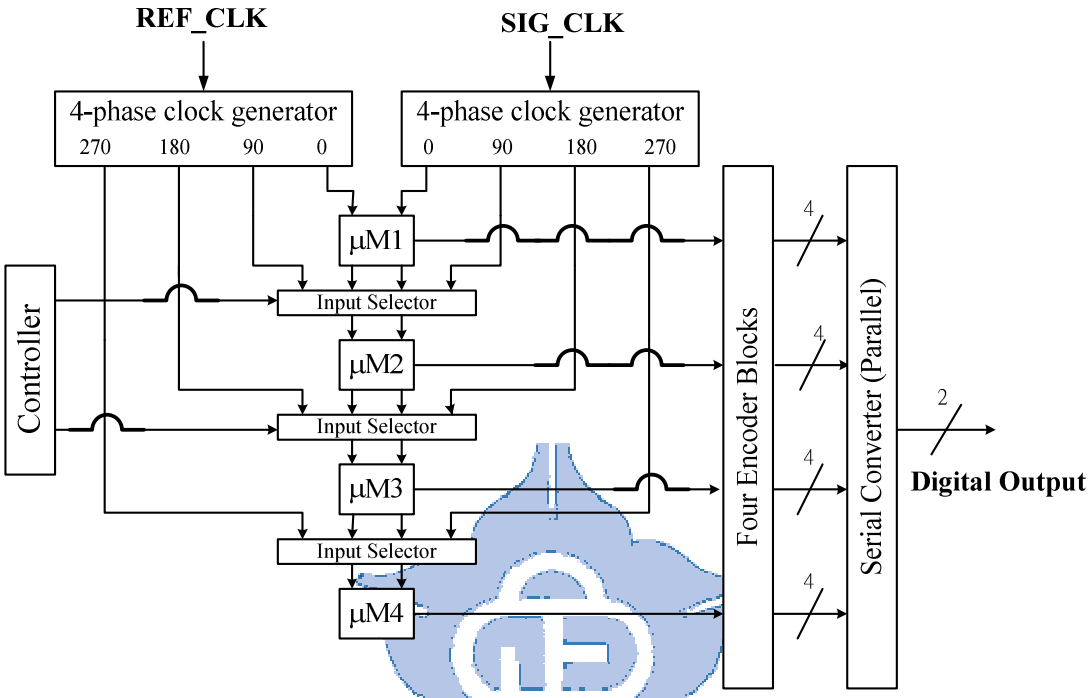


Fig. 2-9 The structure of the BIJM with interpolated technique

Fig. 2-9 presents the interpolated jitter measurement circuit [23], and it composed of two 4-phase clock generator circuits, four micro-measurement macro circuits (μMs), four encoder circuits, a parallel-to-serial converter to receive the outputs of four encoder circuits, input selector circuits, and a controller.

The 4-phase clock generator can generate 4-phase signal, 0°, 90°, 180° and 270°, respectively. Fig. 2-9 shows the timing diagram of the 4-phase signal from "REF_CLK" clock and "SIG_CLK" clock. Then, the four μMs can measure jitter for each phase. The μMs use hierarchical vernier delay line (VDL) to quantize jitter with high resolution.

Therefore, this approach uses the interpolated jitter oversampling can decrease the quantization noise, and uses the hierarchical vernier delay line (VDL) to achieve high resolution.

2. Time-to-Voltage Converter [24][27]：

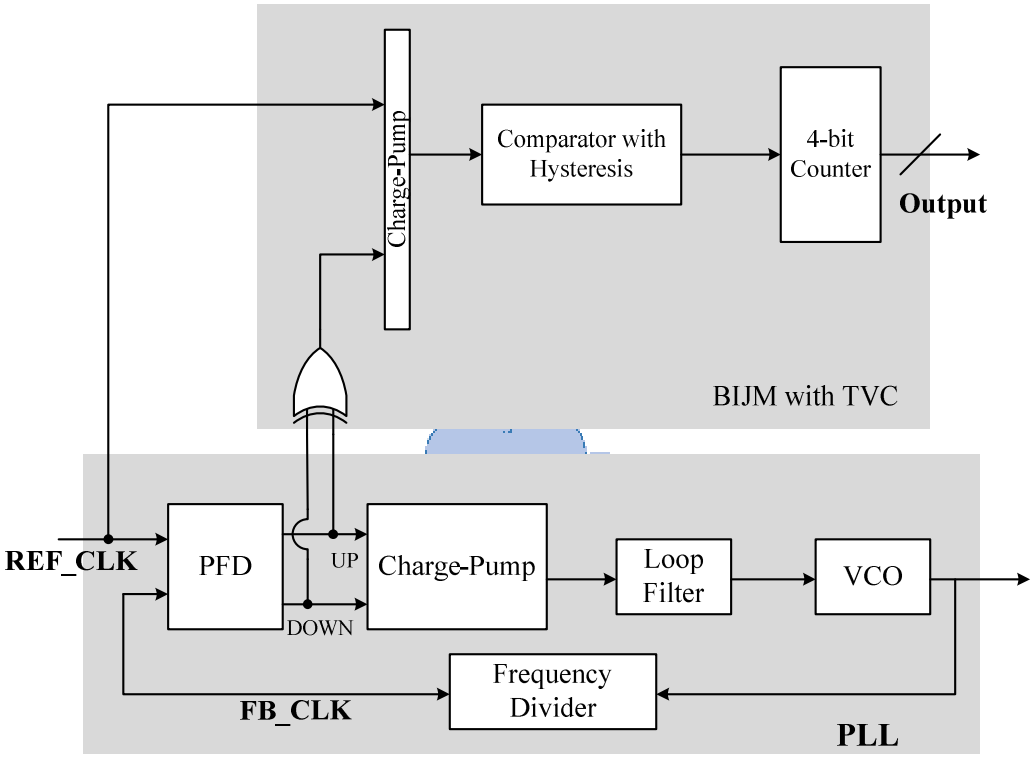


Fig. 2-10 The structure of the BIJM circuit with TVC technique

Fig. 2-10 presents the structure of the built-in jitter measurement (BIJM) circuit based time-to-voltage structure [24], and it composed of a charge-pump circuit, a XOR gate, an analog comparator with hysteresis, a capacitor, and a 4-bit counter.

The phase-frequency detector (PFD) circuit of this approach detects the timing difference of the PLL input clock (REF_CLK) and the PLL feedback clock (FB_CLK). The XOR gate gets the pulse width of timing difference by combining the "UP" signal and the "DOWN" signal.

The time-to-voltage converter (TVC) turns timing difference into voltage by using a charge-pump circuit and a comparator circuit. Then, the analog-to-digital (ADC) circuit converters the voltage into the digital code. However, it has a large overhead problem because of the ADC circuit needs high resolution.

3. Analog-to-Digital Converter[28]：

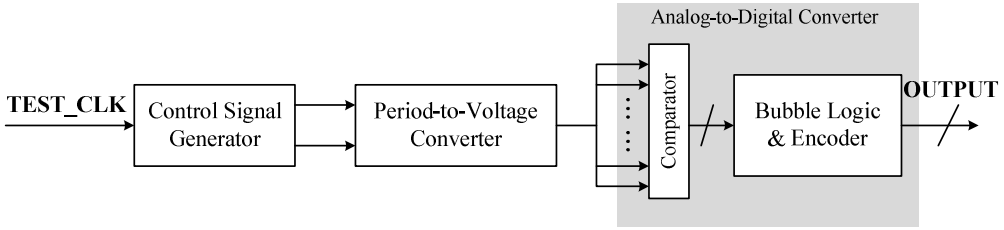


Fig. 2-11 The structure of the BIJM circuit with ADC technique

Fig. 2-11 shows the structure of the BIJM circuit based analog-to-digital converter (ADC) structure, and it is composed of a control signal generator circuit, a period-to-voltage converter circuit, and a analog-to-digital converter.

The period-to-voltage converter circuit charges the capacitance and delivers to the input of the ADC by a charge-pump circuit. In ADC structure, the comparators are all-digital, and use inverter delay chain to set the voltage threshold. Finally, the encode circuit outputs the digital code.

In [28], it doesn't have external jitter-free clock as reference clock, but it would have a large overhead when it needs high resolution in ADC structure.

4. Sampling [25]：

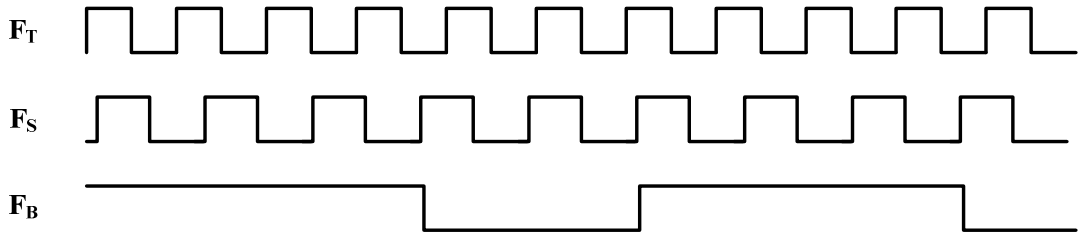


Fig. 2-12 The timing diagram of the BIJM circuit with sampling technique

Fig. 2-12 shows the timing diagram of the BIJM circuit based sampling, and the test clock signal is sampled by the slower clock frequency. The phase error is the difference of the test clock (F_T) and the sampling clock (F_S). It only has a D-type Flip/Flop to sample test clock, and it can reduce the noise and the process-sensitive circuitry. Additionally, it is synthesizable circuit. However, the jitter of the sampling clock can affect the jitter measurement results, and it is not easy to acquire a jitter-free clock signal.

From above mentioned approaches, most of those BIJM circuits need an external jitter-free clock signal as reference clock signal to measure jitter. In fact, it is very difficult to acquire a jitter-free clock signal. Therefore, the self-referred test circuit is an attractive approach to built-in self-test circuit.

2.2.3. Self-Referred Test

In prior built-in jitter measurement (BIJM) circuits, those need an external reference clock to measure the jitter performance of the PLL. In fact, it is very difficult to acquire a jitter-free clock as reference clock input. Therefore, the self-referred structure is proposed in [10][11][14][15][17][18][22][30] to avoid using

an external reference clock input. Besides, it can decrease the error of measurement. In self-referred structure, the reference clock is generated from the test clock input. Among those structures, the most popular self-referred structure uses a one-period delay (OPD) circuit [10][[11][14][15][17][22] to produce the required reference clock. The output clock goes through the delay which is set to one period of test clock. In this way, the input frequency range of the built-in jitter measurement (BIJM) circuit is restricted by the length of the delay line.

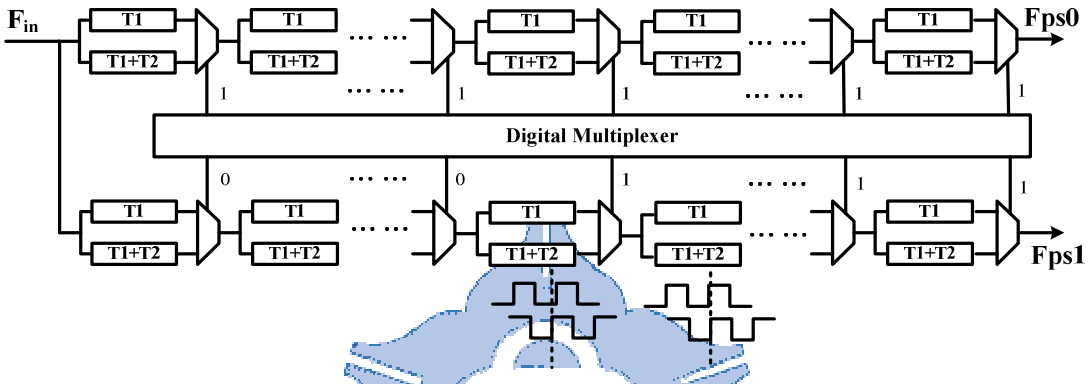


Fig. 2-13 The structure of one-period delay [11]

Most of one-period delay (OPD) structures use either time-to-digital converter (TDC) or manual adjustment delay. Fig. 2-13 shows the OPD circuit with TDC structure [11][15]. In time-to-digital converter (TDC) circuit, it has a large area overhead when the frequency range of input clock becomes wider, and it takes a long time to acquire the one-period clock. Additionally, the resolution of TDC also affects the original jitter value and the accuracy of jitter measurement.

2.3. Proposed BIJM Circuit

2.3.1. Structure Overview

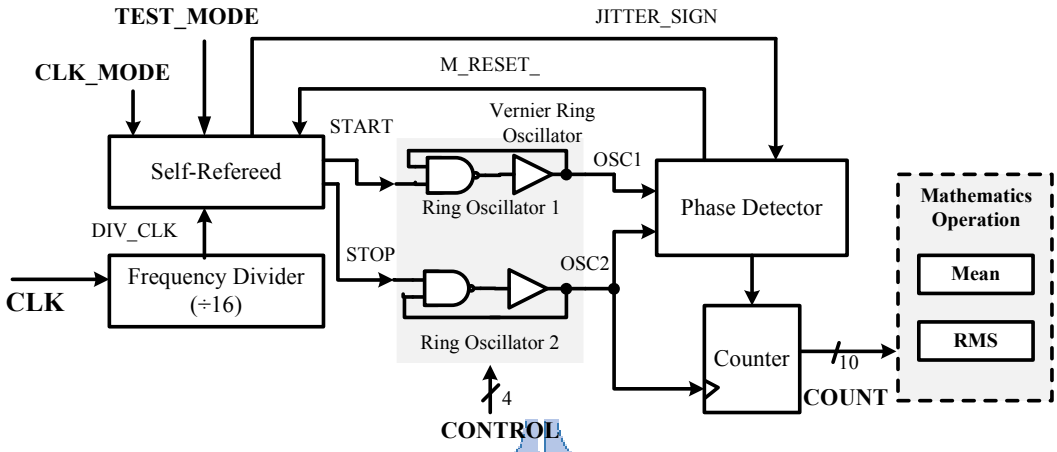


Fig. 2-14 The structure of proposed built-in jitter measurement (BIJM) [46]

The proposed built-in jitter measurement (BIJM) circuit [46] is shown in Fig. 2-14, and it is composed of a frequency divider circuit, a self-refereed (SR) circuit, a vernier ring oscillator (VRO) circuit, a phase detector (PD) circuit, a 10-bit counter circuit and a mathematics operation block. The proposed BIJM uses the vernier ring oscillator (VRO) structure [18] as a time-to-digital converter (TDC) circuit, and a frequency divider circuit with a fixed divider ratio (16) is taken as a timing amplifier (TA) to amplify the input jitter.

The principle of proposed circuit is as following. The test clock (CLK) is divided by the frequency divider and then outputs as "DIV_CLK". Moreover, the self-referred (SR) circuit generates a clock with delay time that is set to one period of the input clock. Subsequently, the self-refereed circuit chooses the beginning and the end of measurement by the input clock and one-period delayed input clock, and output as the "START" signal and the "STOP" signal, respectively. Therefore, the "START" clock

and the "STOP" clock are outputted for the VRO. The "START" clock triggers the upper ring oscillator (OSC1), and the "STOP" clock triggers the other ring oscillator (OSC2). In the structure of VRO circuit, the oscillation frequency of the "OSC1" should be slower than the "OSC2". Therefore, the PD is used to detect when the "OSC2" signal catches up with the "OSC1" signal. When the PD detects the change of the phase polarity, the reset signal (M_RESET_) is sent to the self-refereed circuit, and the self-refereed circuit will generate the "START" signal and the "STOP" signal again for the next jitter measurement. In the moment, the 10-bit counter records the cycle number of "OSC2" until the OSC1 clock lags behind the "OSC2" clock. Therefore, the counter value (COUNT) will deliver to the mathematics statistic operation block to calculate the mean and the root-mean-square (RMS) value of the test clock. Moreover, the counter value needs to multiply by the VRO resolution to count the real jitter value, and the resolution of BIJM is the period difference between the "OSC1" clock and the "OSC2" clock.

However, the resolution (R_{VRO}) of the VRO circuit varies with process, voltage and temperature (PVT) variations. Hence, the counter value can’t be known directly used at the jitter measurement result unless the resolution of the VRO circuit (R_{VRO}) is determined. Therefore, the calibration process to the venier ring oscillator (VRO) is utilized to obtain the resolution for calculating jitter.

Therefore, the proposed BIJM circuit has two operation modes, the calibration mode, and the normal mode, and the mode selection control pins are the "CLK_MODE" and "TEST_MODE" of the self-refereed circuit. The calibration mode is used to obtain the resolution (R_{VRO}) of the VRO circuit with a known input test clock (CLK) frequency, and the resolution (R_{VRO}) can be adjusted by the "CONTROL" signal if needed. Then, in the normal mode, the BIJM circuit measures the jitter value of the input test clock (CLK), and the output counter value can be used

to calculate the jitter.

The rest sections describe the following. The section 2.3.2 discusses the frequency divider is used as a timing amplifier (TA), and the section 2.3.3 describes the detail structure of the self-refereed circuit, and the section 2.3.4 describes the structure of cycle-controlled delay line (CCDL), and section 2.3.5 discusses the TDC with VRO structure and how to record the relative jitter value.

2.3.2. Frequency Divider

In recent years, the timing amplifier (TA) in a built-in jitter measurement (BIJM) circuit is an attractive method to amplify the input jitter, and the accuracy of jitter measurement can be further improved. Moreover, the analog timing amplifiers (TAs) are easily affected by process, voltage and temperature (PVT) variations and those often have a small linear region. For solving the problem of analog timing amplifier, we use the frequency divider as timing amplifier to extend the timing difference. Especially, the frequency divider is a simple digital circuit, and it is easy to be implemented with standard cells. Then, we will discuss why the frequency divider achieves the function of timing amplifier (TA).

In general, the jitter histogram of the PLL's output clock usually looks like a normal distribution random variable. Among the normal distribution, the root-mean-square (RMS) value and the peak-to-peak (Pk-Pk) value are two important parameters of the jitter histogram.

First, we discuss the relationship between the RMS value of the input clock jitter and the clock jitter through the frequency divider. In [21], Assume x(t) is the input clock jitter, and the y(t) is the clock jitter through frequency divider, and the relationship is presented as following:

$$
\begin{aligned}
&y_1 = x_1 + x_2 + \cdots + x_n \\
&y_2 = x_{n+1} + x_{x+2} + \cdots + x_{2n} \\
&\vdots \\
&y_k = x_{(k-1)*n+1} + x_{(k-1)*n+2} + \cdots + x_{kn} \\
&\vdots
\end{aligned}
\qquad \text{(Eq 2-4)}
$$

It also can be define the new random variables sequence as following:

$$
\begin{aligned}
&S_1 = \{x_1, x_{n+1}, x_{2n+1}, \dots\} \\
&S_2 = \{x_2, x_{n+2}, x_{2n+1}, \dots\} \\
&\vdots \\
&S_n = \{x_n, x_{2n}, x_{3n}, \dots\} \\
&\\
&Hence, Y = S_1 + S_2 + \cdots + S_n
\end{aligned}
\qquad \text{(Eq 2-5)}
$$

From [21], we can know that the mean of Y (M_Y) is equal to the sum of the mean of S_n, and the variance of Y (σ_Y) is equal to the sum of the variance of S_n. Therefore, they can be described as following：

$$
\begin{aligned}
&M_Y = M_{S_1} + M_{S_2} + \cdots + M_{S_n} \\
&= \frac{\sum_{i=0} x_{i*n+1}}{k} + \frac{\sum_{i=0} x_{i*n+2}}{k} \cdots + \frac{\sum_{i=0} x_{(i+1)*n}}{k} = n * M_x
\end{aligned}
\qquad \text{(Eq 2-6)}
$$

$$
\sigma_Y^2 = \sigma_{S_1}^2 + \sigma_{S_1}^2 + \cdots + \sigma_{S_n}^2 = n * \sigma_x^2
\qquad \text{(Eq 2-7)}
$$

From above equations, we can acquire the relationship between the input clock jitter and the divided clock jitter, and it will prove the inferential results by simulation results by following description.

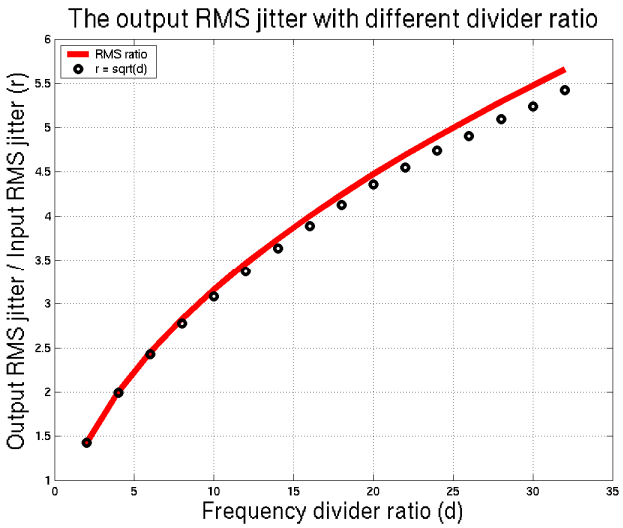


Fig. 2-15 The relationship of the input and output RMS jitter

We can observe the simulation results of the ratio (r) of the output RMS jitter value divided by input RMS jitter value with different divider ratio (d) as shown in Fig. 2-15. Moreover, the relationship can be modeled as $r = \sqrt{d}$, and the RMS value is the square root of the variance value. Thus as we can see, the inferential results and the simulation results are matching.

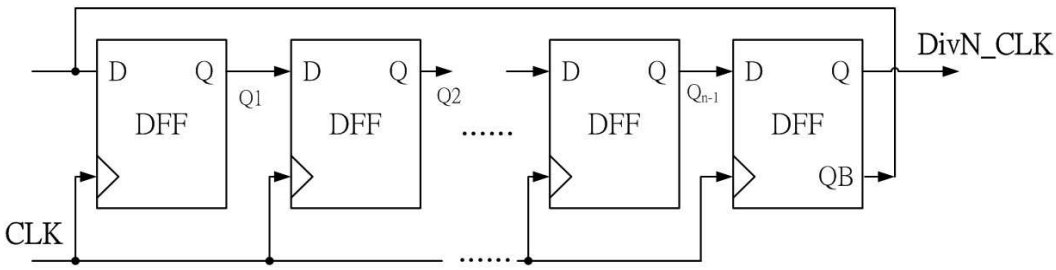


Fig. 2-16 The structure of a Johnson counter

In this thesis, the Johnson counter is utilized to amplify jitter, and the structure of the divider is shown in Fig. 2-16. Compared with the analog timing amplifier (TA), the frequency divider is a simple digital circuit, and it is easy to be implemented with standard cells. In this way, the design complexity of the timing amplifier (TA) can be greatly reduced by the proposed architecture.

2.3.3. Self-Referred

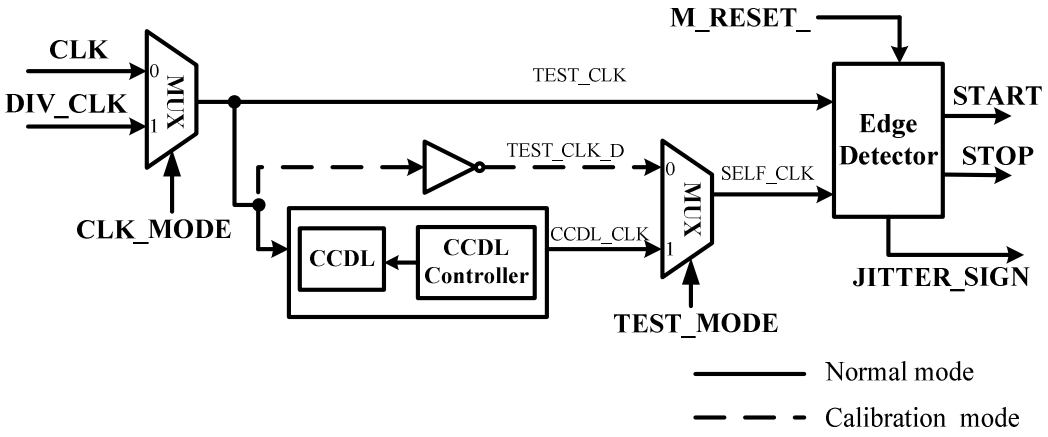


Fig. 2-17 The proposed self-referred circuit

The structure of the proposed self-referred (SR) circuit is shown in Fig. 2-17, and the principle is as following. The operation of the proposed design can be divided into two modes, the calibration mode (the dotted line) and the normal mode (the solid line).

In calibration mode, the goal of the mode is to acquire the resolution of the vernier ring oscillator (VRO) circuit. Moreover, the switch of former multiplexer (CLK_MODE) is set “0” to choose the input clock as input of self-referred circuit (TEST_CLK), and the switch of latter multiplexer (TEST_MODE) is also set “0” to choose the inverted input clock (TEST_CLK_D) as self-test clock (SELF_CLK) as shown in dotted line in Fig. 2-17. Therefore, the edge detector (ED) circuit will generate the "START" signal and the "STOP" signal to the measured circuit.

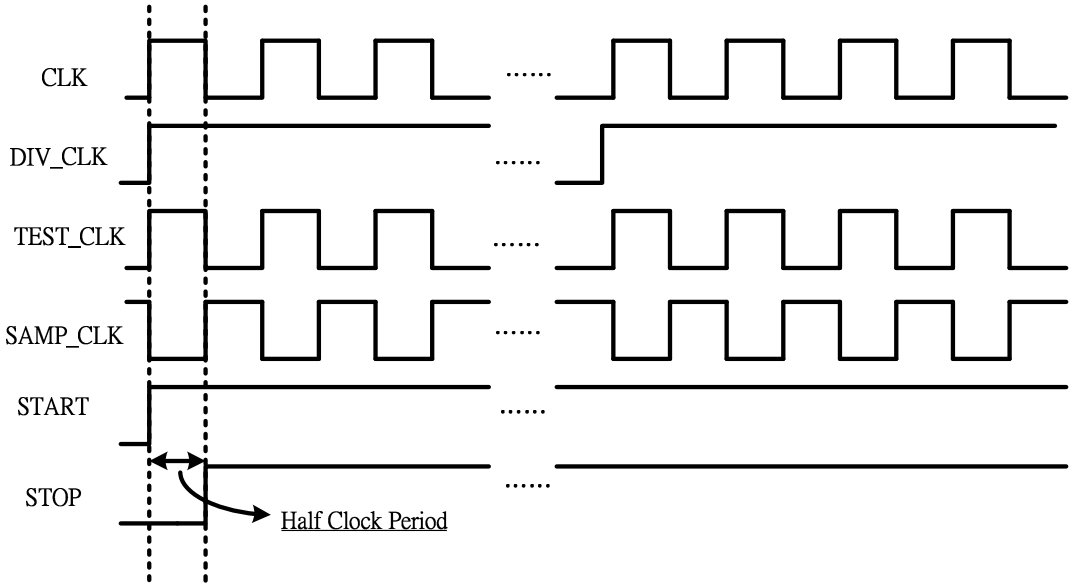


Fig. 2-18 The timing diagram of the calibration mode

In this way, the beginning and end of the measurement is one half clock period of the input clock as shown in Fig. 2-18. Then, the VRO circuit can quantize the timing difference between the "START" signal and the "STOP" signal to obtain the counter value for one half of the test clock (CLK) period, and the resolution (R_{VRO}) of VRO can be calculated by the following equation.

$$R_{VRO} = \frac{T}{2} \times \frac{1}{|256 - N_{cal}|} \quad \text{(Eq 2-8)}$$

Where T is the clock period of input clock (CLK), N_{cal} is the mean of the counter values among calibration mode, and R_{VRO} is the resolution of the VRO circuit.

After the calibration is done, in the normal mode, the value of "CLK_MODE" chooses the clock which we want to test, and input clock and the divided clock. If we want to test the input clock, the "CLK_MODE" should set to "0". On the other hand, if we want to test the divided clock, the "CLK_MODE" should set to "1". Then, we will discuss the operation of normal mode in latter case. The former multiplexer chooses the divided clock as "TEST_CLK", and the latter multiplexer chooses the output of cycle-controlled delay line (CCDL) circuit as the solid line in Fig. 2-17. The

output of CCDL (CCDL_CLK) is delayed by one cycle period and outputted as the "SELF_CLK". Moreover, the "SELF_CLK" clock signal is the clock with delay that is set to one input clock period. It means that the timing difference between the "TEST_CLK" signal and the "SELF_CLK" is equal to the phase error of the each cycle period and first cycle period. If we assume the first cycle period as a ideal reference clock, the phase error is equal to the definition of the period jitter that introduced in Chapter 1.

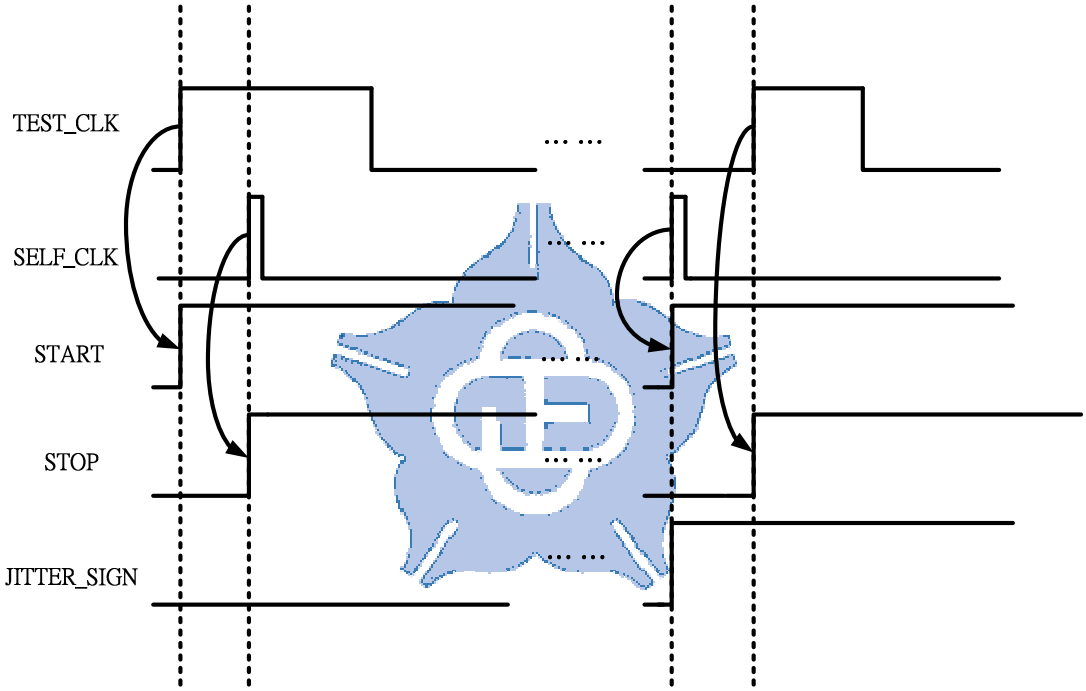


Fig. 2-19 The timing diagram of normal mode with signed jitter

However, the ED circuit can detect the sign of the jitter, if the "TEST_CLK" leads the "SELF_CLK", the output jitter is defined as positive. Therefore, the "JITTER_SIGN" signal is set to “0”. Oppositely, if the "TEST_CLK" clock lags the "SELF_CLK" clock, the JITTER_SIGN is set to "1". Hence, if the "JITTER_SIGN" is set to "0", the "TEST_CLK" clock signal is outputted as "START" signal and the "SELF_CLK" is outputted as "STOP" signal. Otherwise, the "START" signal chooses the "SELF_CLK" as output signal and the "STOP" signal chooses the "TEST_CLK"

as output signal as shown in Fig. 2-19.

In addition, we use the CCDL structure [43][44] to implement one-period delay (OPD) structure. However, most of OPD structures use either the time-to-digital converter (TDC) or manual adjustment, and those have a large area overhead when the range of the input becomes wider. Therefore, we use cycle-controlled delay line (CCDL) circuit [43][44] to delay one clock period can reduce the area overhead, and we will detail describe in next session.

2.3.4. Cycle-Controlled Delay Line

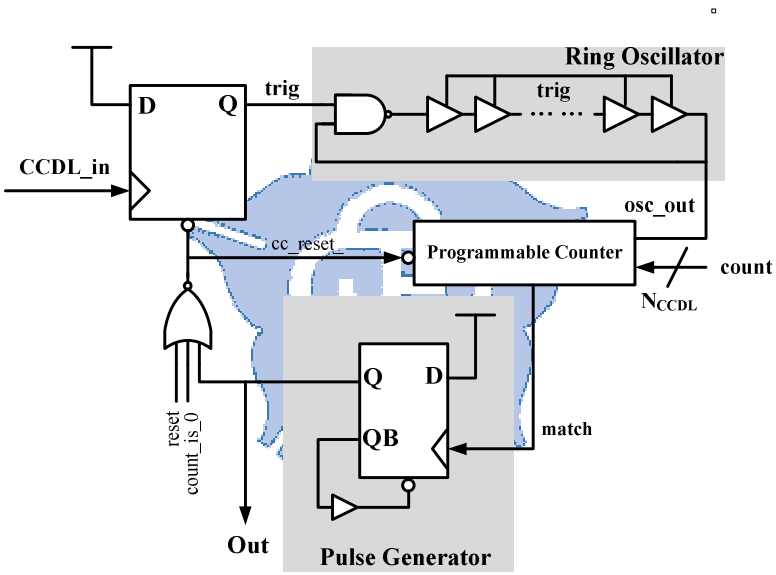


Fig. 2-20 The structure of cycle-controlled delay line (CCDL) [43]

The structure of cycle-controlled delay line (CCDL) [43] is shown in Fig. 2-20. Unlike the prior paper, the proposed CCDL is composed of a positive edge trigger, cycle-controlled delay line and one 2-to-1 multiplexer. The "CCDL_in" signal will trigger the D-type Flip/Flop, and the "trig" signal is to prevent the additional signal to the programmable counter circuit. When the ring oscillator starts oscillating, the "osc_out" signal will trigger the programmable counter to count upward. It counts upward until the count of programmable counter is equal to the input count that the

controller inputted. In the moment, the "match" signal will be high, and triggers the pulse generator to generate a pulse to reset the D-type Flip/Flop and the programmable counter. The timing difference between the "CCDL_in" clock and the "Out" clock is multiple of the period of the ring oscillator, and it can be expressed as following.

$$T_{CCDL} = c * T_{OSC}, \quad for \quad c = 0 \backsim 2^{N_{CCDL}} - 1$$

Where the T_{CCDL} is the timing difference the "CCDL_in" clock and the "Out" clock, the T_{OSC} is the period of the ring oscillator, and the c is the times the CCDL reuses.

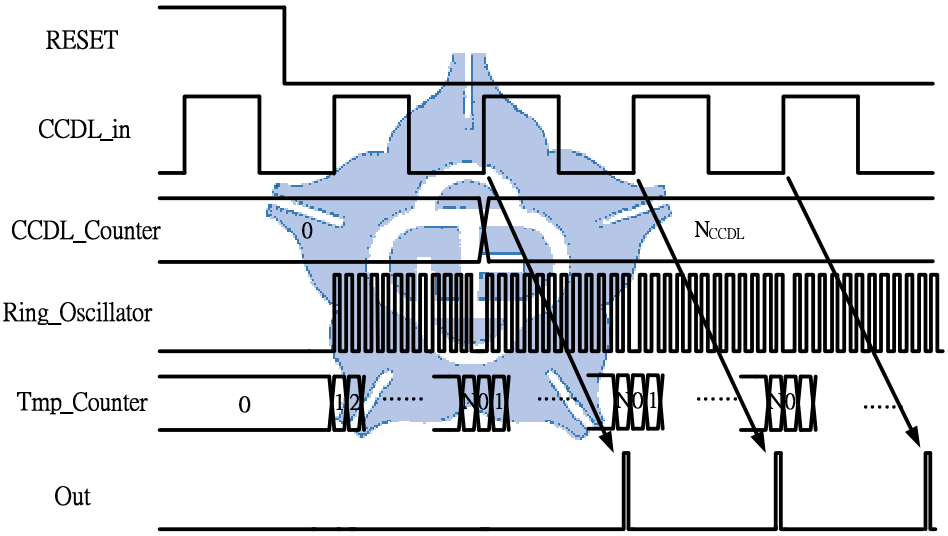


Fig. 2-21 The timing diagram of CCDL

The timing diagram of the proposed CCDL is shown in Fig. 2-21. The input signal (TEST_CLK) triggers the positive edge cycle-controlled delay cell. It means that it will start to oscillate when the first positive edge comes, and the ring oscillator will oscillate until the count number is equal to the input count (N_{CCDL}) from the CCDL controller. The "Out" clock generates the pulse with the delay time that is set to one input clock period. When the N_{CCDL} is zero, the "count_is_0" signal will pull high and the input "CCDL_in" clock is bypassed to the output of CCDL. It can be

seen, the CCDL structure can generate one-period delay clock quickly, and it also can reduce the area overhead.

2.3.5. Vernier Ring Oscillator

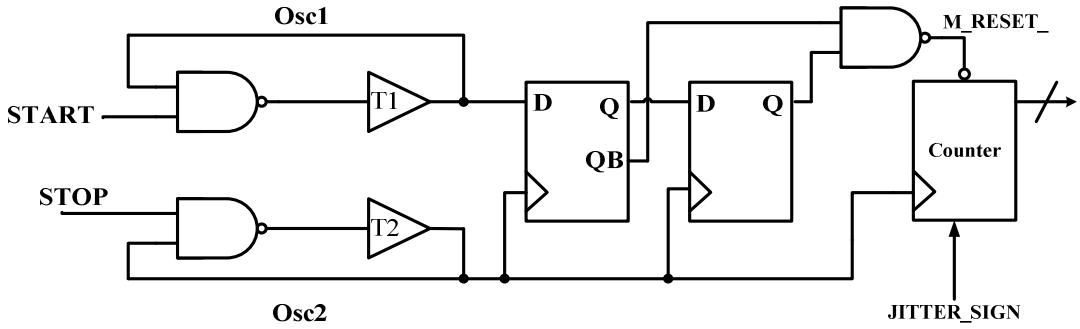


Fig. 2-22 The structure of vernier ring oscillator (VRO) [18]

The time-to-digital converter (TDC) with vernier ring oscillator (VRO) structure in built-in jitter measurement (BIJM) is a popular approach to measurement jitter [7-31]. The structure of VRO [18] is shown in Fig. 2-22, and each ring oscillator is composed of an NAND gate and a serial delay cell.

In the structure of VRO, the "START" signal triggers the upper ring oscillator (OSC1) and the "STOP" signal triggers the other ring oscillator (OSC2), and the clock frequency of upper ring oscillator should be slower than the other. It means that the delay time T1 will be longer than the delay time T2, and the "START" signal always leads the "STOP" signal.

Subsequently, the phase detector (PD) circuit is utilized to detect when the "OSC2" catches up the "OSC1", and the counter will record the cycle number of "OSC2" until the "OSC1" lags behind the "OSC2".In the moment, the PD circuit produces a low pulse (M_RESET_) to reset the counter. The "JITTER_SIGN" signal from self-referred circuit controls counter upward count or downward count.

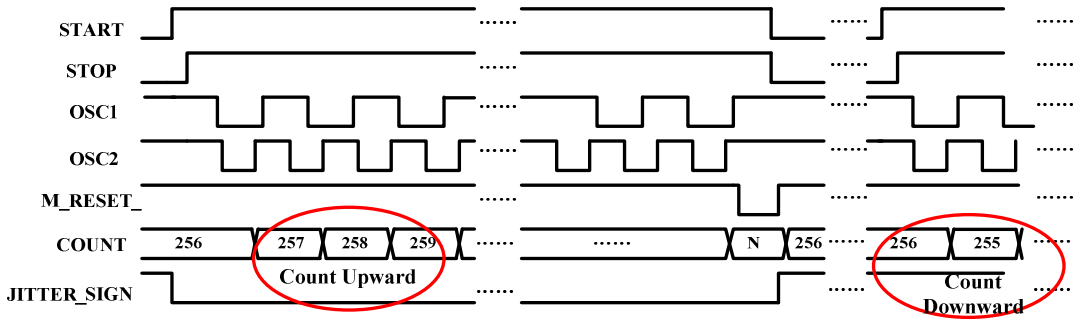


Fig. 2-23 The timing diagram of the VRO and the PD in BIJM circuit.

Fig. 2-23 shows the timing diagram of the VRO circuit and the PD circuit. The "START" clock and the "STOP" clock trigger the "OSC1" and the "OSC2", respectively. The "OSC1" is always triggered earlier than "OSC2", and the PD detected when the "OSC2" catches up the "OSC1". When the "OSC1" lags behind the "OSC2", the "M_RESET_" signal generates a low pulse to reset the counter. The initial value of the counter is set to “256” in each jitter measurement. If the "JITTER_SIGN" signal is “0”, the counter will count upward until the negative edge of the M_RESET_ signal is produced. Oppositely, if the "JITTER_SIGN" is “1”, the counter will count downward until the negative edge of the "M_RESET_" signal is produced. The TDC circuit with VRO structure can decrease the area overhead, and it can solve the problem of the logic gated mismatch. Therefore, it is suitable for BIJM circuit to measure jitter.

Form above mentioned built-in jitter measurement (BIJM) circuit, we can acquire the counter codes, but we don’t know the real jitter value. Therefore, we can acquire the resolution of the BIJM circuit from Eq2-8 in calibration mode. Additionally, from the edge detector (ED) circuit, we can acquire the sign of input jitter to measure sign of jitter. When the "JITTER_SIGN" signal is set to “0”, the counter will count upward. Oppositely, the counter will count downward, when the "JITTER_SIGN" signal is set to “1”. The initial value of counter is "256", and the output counter has 10 bits.

2.4. Mathematic Statistics of Jitter

From the previously mentioned, the root-mean-square (RMS) value is one of important characteristics in jitter measurement, and the average of jitter also is the important parameter in RMS measurement.

Up to now, there are many methods to calculate the average counter code in average measurement circuits. The difference of maximum jitter and minimum jitter is the simplest method to calculate the average. However, it is easily affected by the extreme value. The moving average (MV) is the common method to calculate the average for a long time. No matter how, it will need a lot of registers to store those counter codes in the interval time. Therefore, the filter average can avoid the effect of extreme value, reduce the number of registers, and smooth the results in [42]. Nevertheless, it meets others problem so that it would affect the mathematic results. If it appears closed values continuously, the temporarily buffers can't allow others values to represent even though the value maybe is average values in jitter measurement. In this thesis, we improve the moving average (MV) approach to meet our need.

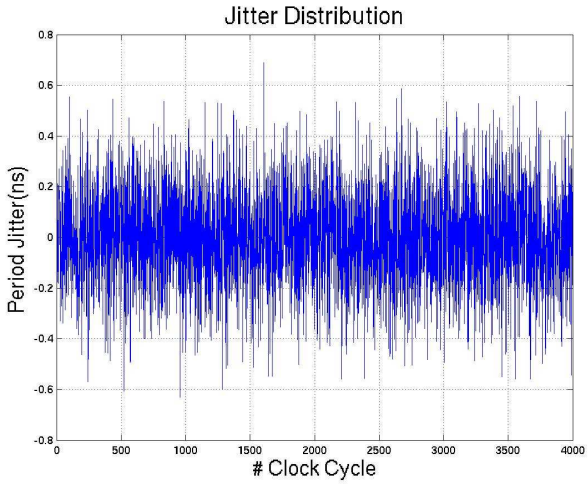


Fig. 2-24 The jitter distribution with radon variables

Moreover, the jitter distribution is generally normal distribution with random variables is shown in Fig. 2-24. Thus, it can be consider that those mean of different internal time are close. The simple concept of improved moving average is shown in Fig. 2-25.

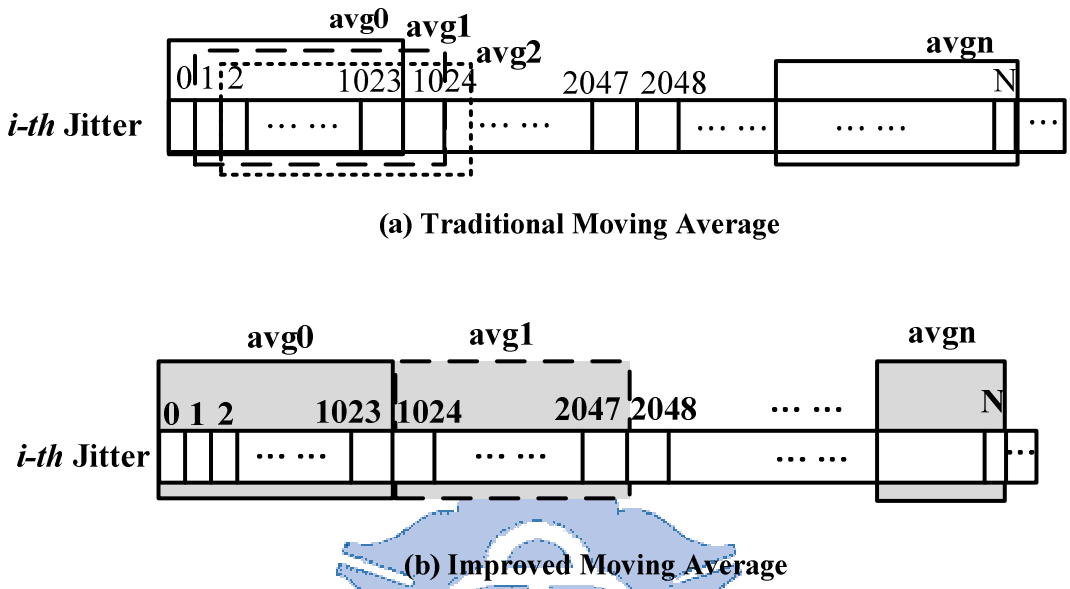


Fig. 2-25 The concept of moving average (a) conventional moving average, (b) improved moving average

In this way, the improved MV doesn't need a lot of registers to store measured jitter results. The simulation will show the results to prove. The RMS value is one of the most important characteristics in jitter measurement, and we can measure the RMS value to determine out measured results. The RMS value is calculated in the following equation.

$$J_{RMS} = \sqrt{\frac{\sum_{i=1}^{N_{jitter}} (J_i - J_{mean})^2}{N_{jitter}}} \qquad \text{(Eq 2-9)}$$

Where the J_{RMS} is the RMS value of jitter in such interval time, the J_i is *i-th* jitter value, the J_{mean} is the mean of jitter in such interval time, and the N_{jitter} is the number of jitter in such interval time. Furthermore, the equation of RMS also can be described as other type and the inferential procedure is shown as in Eq2-10.

$$J_{RMS} = \sqrt{\frac{\sum_{i=1}^{N_{jitter}} (J_i - J_{mean})^2}{N_{jitter}}} = \sqrt{\frac{\sum_{i=1}^{N_{jitter}} \left(J_i^2 - 2*J_i*J_{mean} + J_{mean}^2\right)}{N_{jitter}}}$$

$$= \sqrt{\frac{(\sum_{i=1}^{N_{jitter}} J_i^2) - (2*J_{mean} \sum_{i=1}^{N_{jitter}} J_i) + (\sum_{i=1}^{N_{jitter}} J_{mean}^2)}{N_{jitter}}} \quad \text{(Eq 2-10)}$$

$$= \sqrt{\frac{(\sum_{i=1}^{N_{jitter}} J^2) - 2*N_{jitter}*J_{mean}^2 + J_{mean}^2}{N_{jitter}}} = \sqrt{\frac{\sum_{i=1}^{N_{jitter}} J_i^2 - N_{jitter}*J_{mean}^2}{N_{jitter}}}$$

$$= \sqrt{\frac{\sum_{i=1}^{N_{jitter}} J_i^2}{N_{jitter}} - J_{mean}^2}$$

The window size of the proposed improved MV is set to “1024”, and the simulation results compares the difference between the proposed moving average and the overall input as shown in Fig. 2-26.

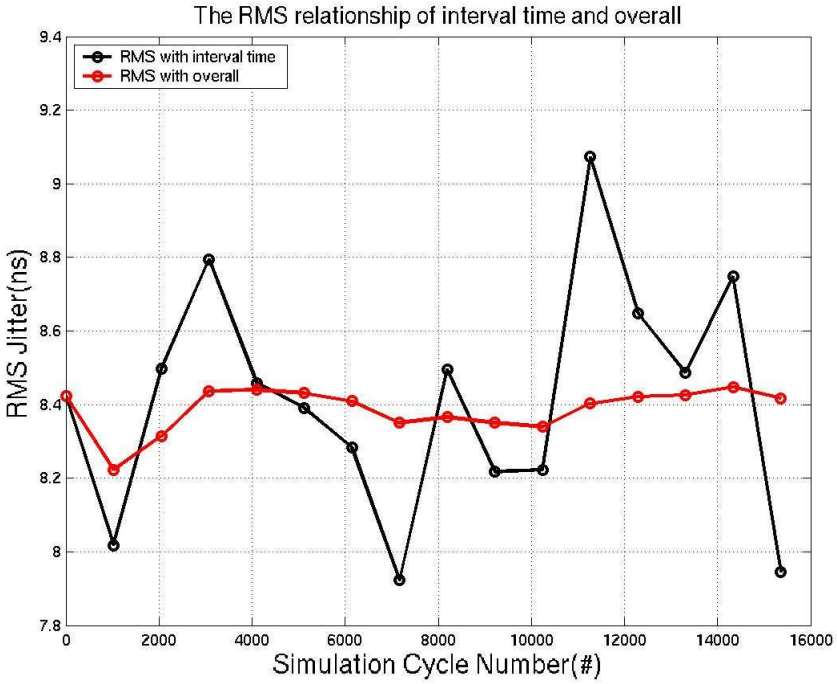


Fig. 2-26 The relationship of the interval time RMS and the overall time RMS

Chapter 3 Built-In Self-Test for ADPLL

3.1. Conventional BIST Circuits

Beside the jitter measurement, there are many other methods to determine the operation of the PLL, and those circuits are called built-in self-test (BIST) circuits [32-41]. In prior approaches, those can be divided into three types, namely non-invasive test [32][33], invasive test [34-38] and open loop test [39-41].

The rest section describes the following. The section 3.1.1 describes the non-invasive test approaches, and the section 3.1.2 describes the invasive test approaches, and the section 3.1.3 discusses the open loop test approaches. Finally, the section 3.1.4 will make the summary.

3.1.1. Non-Invasive Test

In non-invasive test approaches [32][33], those approaches just observe the PLL input and the PLL output to determine the operation of the PLL, and they don't add extra circuits in internal PLL architecture. Therefore, the technique would affect the performance of the PLL slightly.

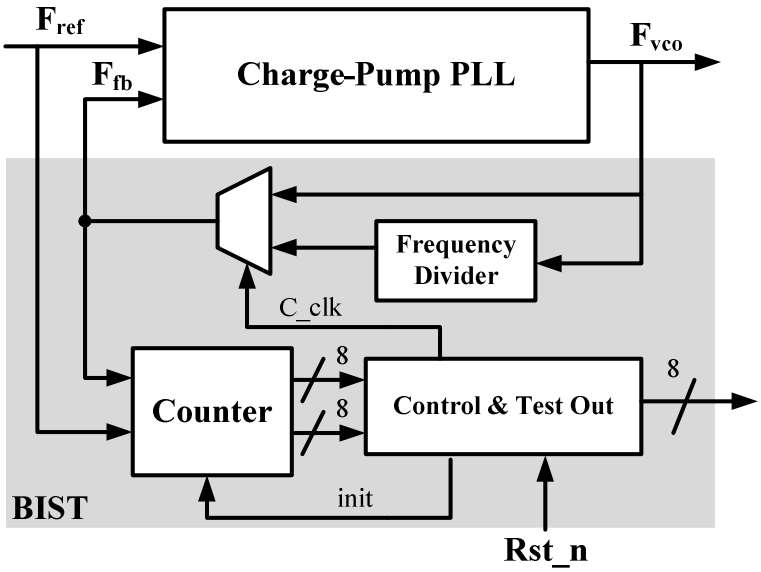


Fig. 3-1 The structure of BIST in non-invasive testing [33]

Fig. 3-1 shows the structure of BIST PLL circuit [33], and it composed of a 2-to-1 multiplexer, a frequency divider circuit, an 8-bit counter circuit, and a controller circuit.

As soon as the PLL is locked, the test circuit starts to determine the operation of the PLL. The thought of the BIST circuit is that altering the frequency divider ratio. When the frequency divider ratio is changed, the PLL needs locked again. Subsequently, the counter records the value, and the controller will compare those results to determine the operation of the PLL.

Moreover, the non-invasive test technique only observes the input and the output of the PLLs, and the test PLL structures are not restricted. However, it is limited for non-invasive testing circuit to measure more parameters.

3.1.2. Invasive Test

The invasive approaches [34-38] observer more signal to determine the performance of the PLLs. In this ways, those can increase the testability.

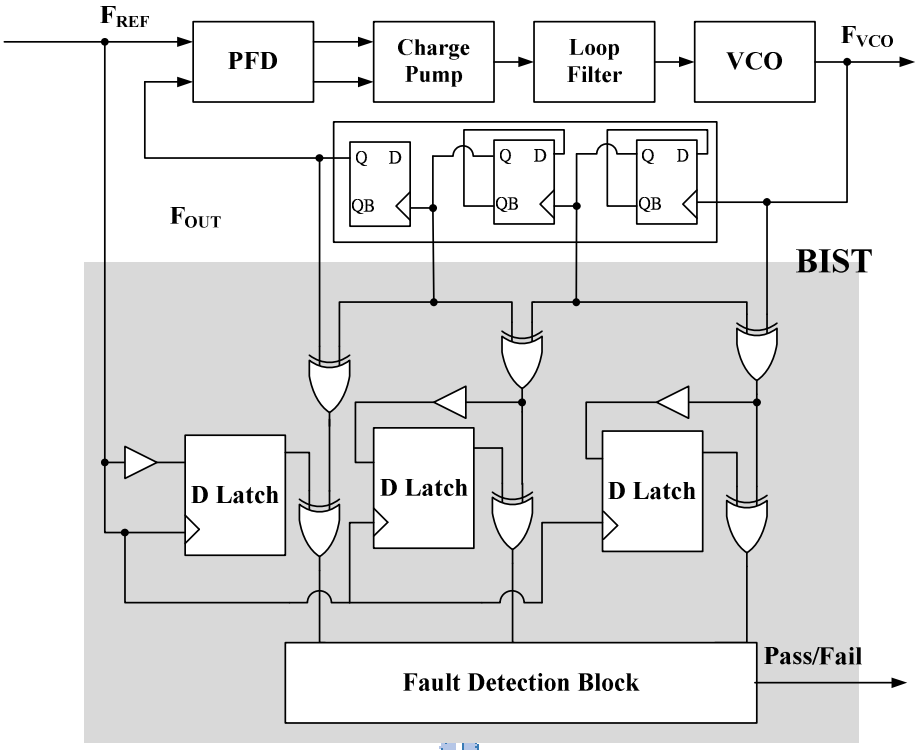


Fig. 3-2 The BIST structure with directly invasive testing [34]

Fig. 3-2 shows the structure of BIST for PLL circuit in invasive test approach [34], and the BIST circuit is composed of some XOR logic gates, some D latch circuits, and a fault detection block.

The internal nodes of the divider-by-N (DBN) circuit are delivered to the BIST circuit, and the relationship of those nodes can be modeled as hamming code. Finally, the fault detection circuit determines the measured results whether matching the hamming code, and outputs the measured results.

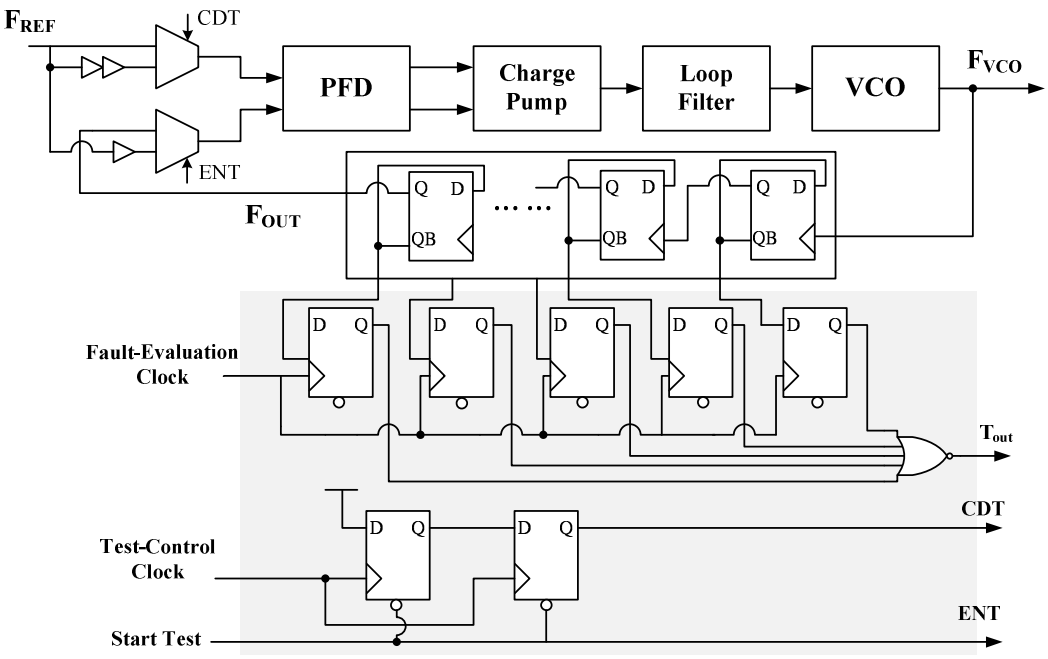


Fig. 3-3 The BIST structure with indirectly invasive testing [35]

Fig. 3-3 shows the structure of BIST PLL in invasive test approach [35], and two 2-to-1 multiplexers and three delay cells are added to test the charge-pump based PLL. The fault-evaluation clock circuit and the test-control clock circuit are added to generate the test-self clock signal.

The test principle is described as following. The test-control circuit produces the charge/discharge test (CDT) signal and the enable test (ENT) signal to control the phase-frequency detector (PFD) inputs. The test operation can be divided into two cases, the charge case and the discharge case. In charge case, the test-control (TC) circuit lets the "IN" signal lead the "FB" signal. Hence, the PFD circuit will still produce the "UP" signal.

In the other case, the TC lets the "IN" lag the "FB" signal in discharge case, and the PFD circuit will generate the "DOWN" signal. Subsequently, the Fault-Evaluation (FE) circuit catches the digital output of divider-by-N (DBN) and diagnoses the test results to determine the operation of the PLL.

Unlike the non-invasive test approaches, the invasive test approaches need add extra circuits in internal PLL, but those approaches still don't need to modify the existing structure of PLL.

3.1.3. Open Loop Test

In open loop test approach [41], the test approach needs to break the PLL loop, and alters the existing PLL circuitry. In [41], it modifies the structure of voltage-controlled oscillator (VCO) as shown in Fig. 3-4. The VCO circuit is added two extra switches to choose the ring oscillator as output clock or a series of inverters. When the Test_Mode value is set to "0", the VCO chooses the output of ring oscillator as output clock, and it chooses as output clock when "Test_Mode" value is set to "1".

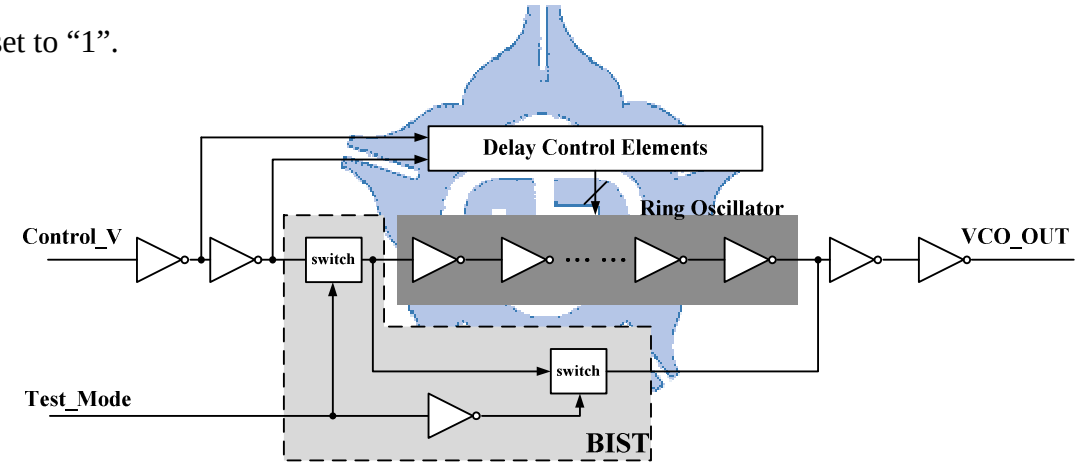


Fig. 3-4 The BIST structure in open loop testing [41]

However, modifying the existing structure would increase the loading of internal nodes, and it also impact the performance of the PLL. In addition, the open loop test approach must design different test circuitry for the different PLL structures.

3.1.4. Summary

The non-invasive test approaches [32][33] determine the operation of PLL only through the PLL input and the PLL output, and this test approach doesn't observe the internal nodes. Moreover, the invasive test approaches [34-38] need to obtain the internal information to determine the operation of the PLL, and the open loop test [41] approaches need to modify the existing structure of the PLL.

Table 3-1 The comparison of the BIST test techniques

	Advantage	Disadvantage
Non-invasive	**Not broken loop**	**Lower testability**
Invasive	**Not broken loop**	**Medium testability**
Open loop	**High testability**	**Broken loop**

Among three types, the non-invasive test approach is the optimal test technique because of it doesn't observe the internal nodes, but it is limited to determine the operation of the PLL. Moreover, even though the open loop testing approach can measure more parameters, but it needs to modify existing structure of the PLL. However, it makes the extra influence of PLL, and impacts the performance of the PLL.

3.2. Proposed BIST Circuit

3.2.1. Structure Overview

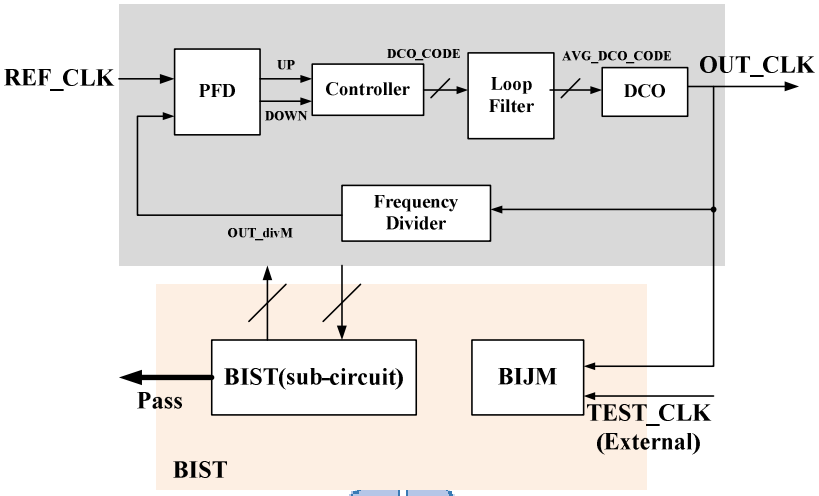


Fig. 3-5 The proposed BIST for PLL structure

Fig. 3-5 presents the simple block of the proposed built-in self-test (BIST) circuit for the all-digital phase-locked loop (ADPLL), and it is composed of a built-in jitter measurement (BIJM) circuit that is mentioned in chapter 2, and a built-in self-test circuit. In this circuit, the BIJM circuit can supply to test the ADPLL output clock frequency and the external test clock frequency. We would introduce the detail description of the BIST sub-circuit.

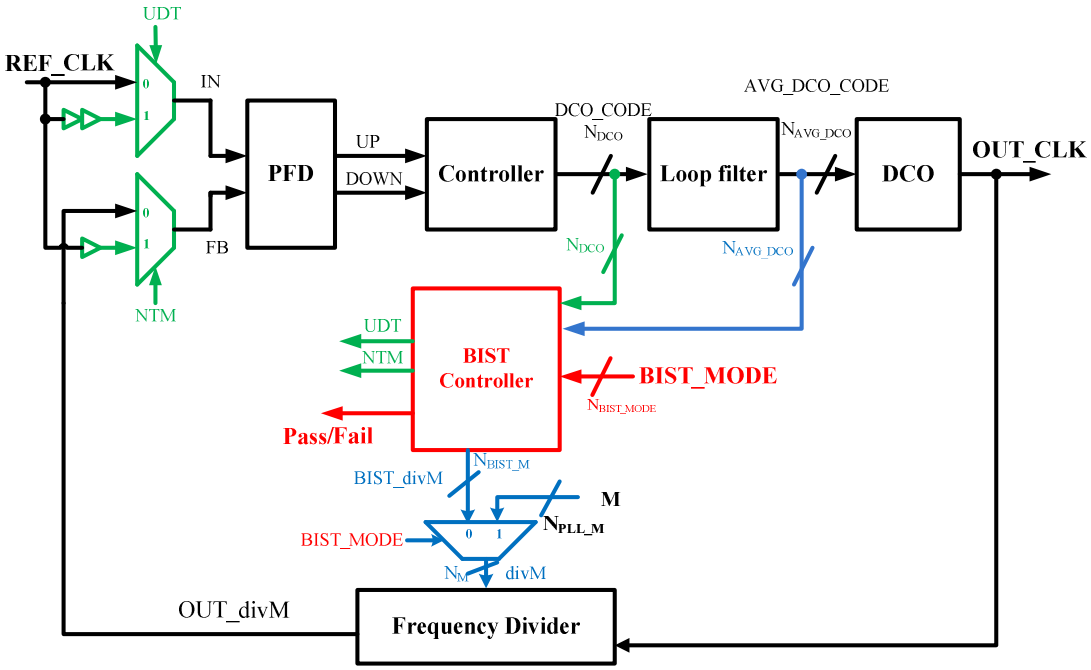


Fig. 3-6 The architecture of the BIST sub-circuit.

Fig. 3-6 presents the structure of the proposed built-in self-test (BIST) circuit, and it is composed of three 2-to1 multiplexers and a BIST controller block. We focus on design an all-digital BIST circuit for the all-digital phase-locked loop in invasive test approach. The proposed BIST circuit supply two test mode to test all-digital phase-locked loop (ADPLL), the test for PFD/Controller and the test for frequency divider and controller, and the mode selection control pins are the "BIST_MODE" and the "BIST_MODE" has 2-bit in the proposed BIST circuit.

When the "BIST_MODE" is set to “01”, the proposed BIST circuit will test the operation of the PFD and the controller. Then, the proposed BIST circuit tests the frequency divider and controller when the "BIST_MODE" is set to “10”.

The section 3.2.2 will describe the proposed BIST for PFD and Controller block, and the section 3.2.3 will describe the BIST circuit for frequency divider and controller, and the section 3.2.4 presents the simulation of those cases.

3.2.2. BIST for PFD/Controller

In proposed PFD/Controller test circuit, we refer to the approach [33] that mentioned in section 3.1.2, and improve its measurement circuit. The proposed BIST circuit observes the relationship between the PFD outputs (UP, DOWN) and the DCO codes (DCO_CODE) to determine the operation of the PFD/Controller by forcing down test and forcing up test.

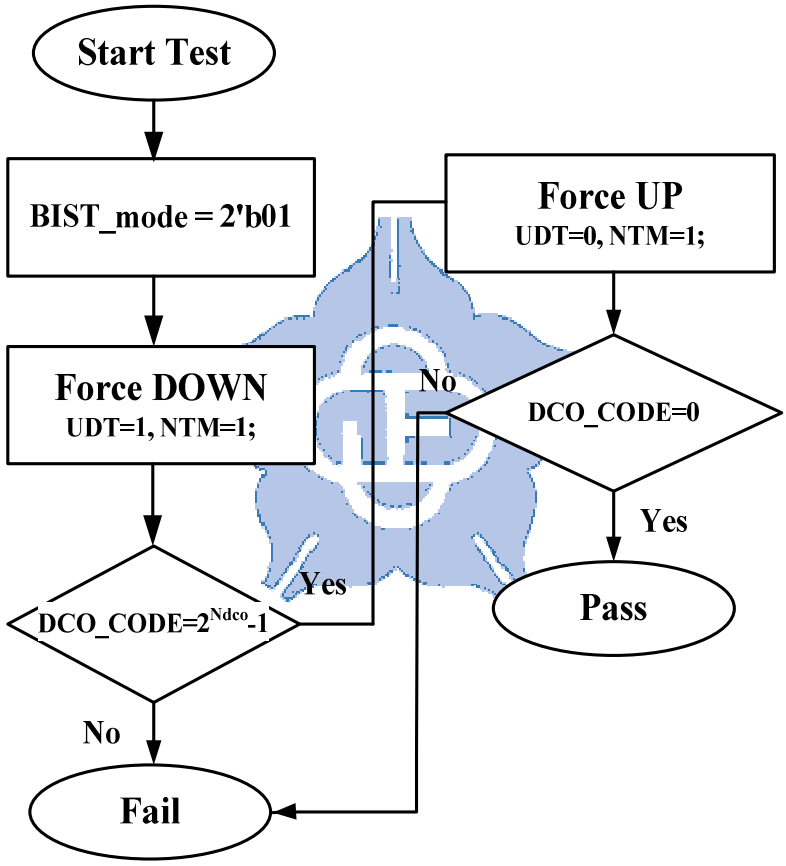
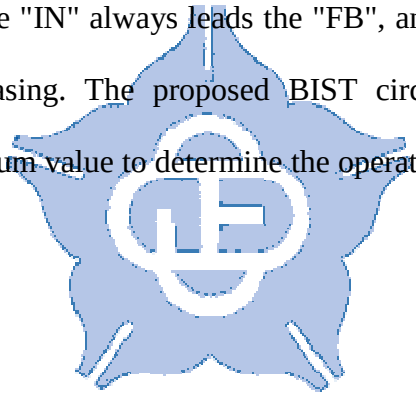


Fig. 3-7 The procedure of the proposed BIST circuit for PFD

The flow chart of PFD/Controller testing as shown in Fig. 3-7, and the working principle is described as following and the N_{dco} is the bit number of the DCO circuit. When the "BIST_MODE" is set to “01”, the BIST control delivers the up-down test (UDT) signal and the normal-test mode (NTM) signal to the former two 2-to-1 multiplexers. When the "UDT" signal is set to “1” and the "NTM" signal is set to “1”,

it means that the "IN" signal is the input clock with two delay cells, and the "FB" clock is the input clock with a delay cell, and the delay cell is the same delay step. Therefore, the "IN" clock always lags the "FB" clock, and the PFD would generate the down signal continuously if the PFD circuit is normal. Then, the down signal makes the controller decrease the DCO codes (DCO_CODE). If the DCO controller doesn’t decrease the "DCO_CODE" into zero, the proposed BIST circuit will finish the test and the Pass/Fail is high.

If the PLL pass in forcing down test, the "UDT" signal will be set to “0” and the "NTM" signal will be set to “1”, and the PFD chooses the input clock without delay and the input clock with a delay cell as the "IN" signal and the "FB" signal, respectively. Therefore, the "IN" always leads the "FB", and the controller will make the "DCO_CODE" increasing. The proposed BIST circuit examine whether the "DCO_CODE" are maximum value to determine the operation of PLL.



3.2.3. BIST for Frequency Divider/Controller

On the other case, the proposed BIST circuit will test the frequency divider (FD) and controller. From the section 3.1.1 discussion, we can determine the operation of the PLL by altering the frequency divider ratio. The proposed BIST circuit observes the change of the output of the loop filter circuit (AVG_DCO_CODE) when the frequency divider ratio is changed.

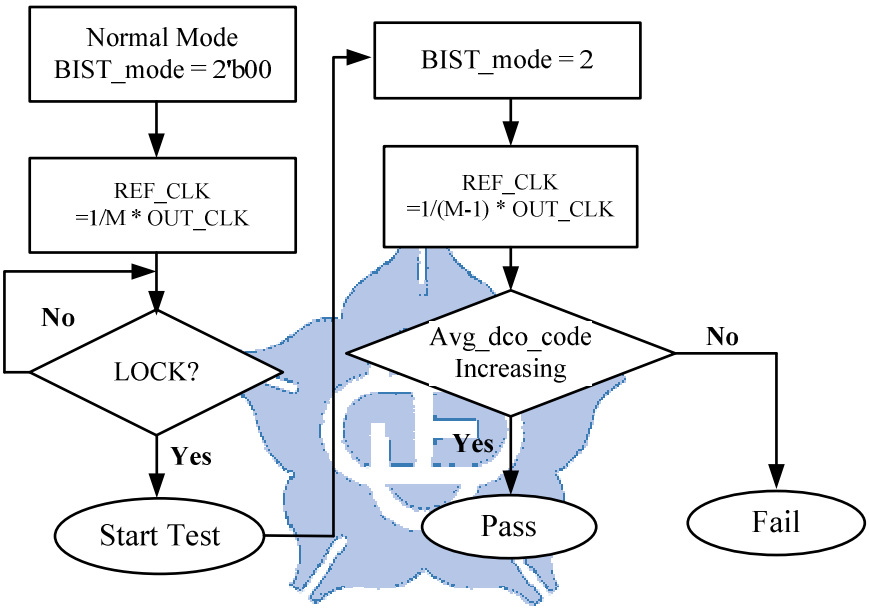


Fig. 3-8 The procedure of BIST for frequency divider

The flow chart of test FD/Controller is shown as in Fig. 3-8, and the detail procedure describes as following. In this case, the proposed BIST circuit needs to wait the PLL state is locked to start test. When the PLL is locked, and the BIST controller changes the frequency divider ratio when the "BIST_MODE" is set to “10”. When the frequency divider ratio (M) becomes less (M-1), the output clock frequency (F_{PLL}) will be faster than the PLL input (F_{REF}) and the average of DCO codes (AVG_DCO_CODE) will be increasing.

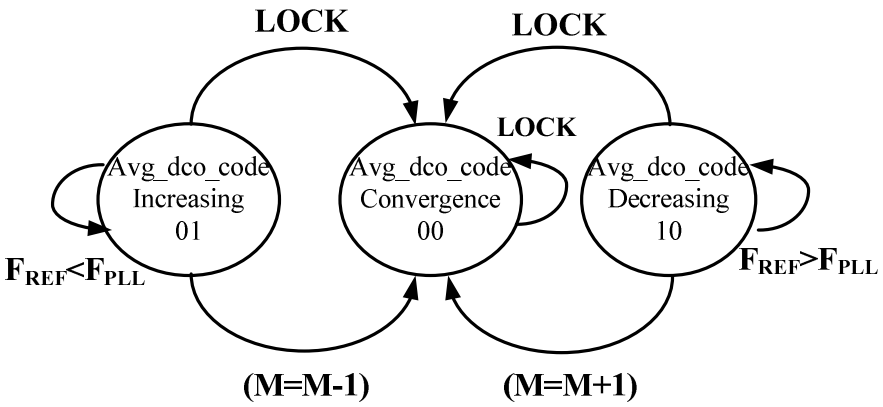


Fig. 3-9 The state machine of PLL locking in BIST for divider testing

Fig. 3-9 shows the state machine of the PLL locking information in testing divider approach. If the input clock frequency (F_{REF}) is faster than the output clock frequency (F_{PLL}), the average of "DCO_CODE" will be decrease, and the state will from state “00” to state “10”. Oppositely, if the input clock frequency is slower than the output clock, the "DCO_CODE" will be increase, and the state would turn to “01”.

3.2.4. Summary

The proposed built-in self-test (BIST) circuit focus on testing the phase-frequency detector (PFD) circuit, the controller circuit and the frequency divider circuit, and this work uses the indirectly input signal to test the function of the blocks, and then observe their operation to test. In this way, the proposed BIST circuit doesn’t add extra circuit to break the internal architecture of the APLL, and doesn’t destroy its loop. Therefore, the proposed BIST circuit belongs to the invasive approach, and it is easy to implement.

3.3. Application Environment

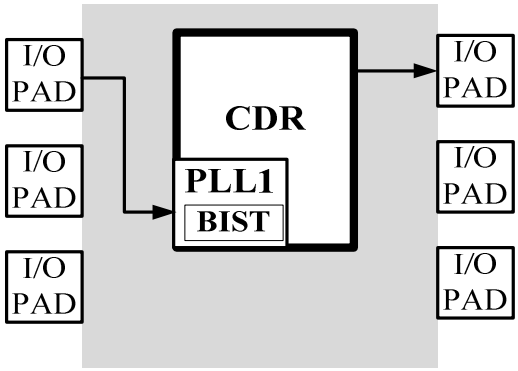


Fig. 3-10 The application environment of single PLL

Fig. 3-10 presents the application environment of single phase-locked loop (PLL). In system-on-chip (SOC) design, the PLL plays an important role for producing various clock rates for different operated requirements. If the PLL doesn't work correctly, it may lead the overall system failure. Therefore, the stability of PLLs is important.

However, the system-on-chip (SOC) design doesn't have only one PLL, and all PLLs should be determined. Therefore, it is difficult to test every PLL by the external instruments. Hence, built-in self-test (BIST) measurement is becoming an attractive and important approach to determine the performance of the PLLs.

Chapter 4 Experimental Results

4.1Chip Implementation

The chips are fabricated by UMC 65nm 1P10M standard performance (SP) CMOS process. We measure the performance of the proposed built-in jitter measurement (BIJM) circuit individually, and we would detail describe in section 4.2. In section 4.2, it shows the simulation results and the chip measurement resolution. Finally, the section 4.3 shows the proposed built-in self-test (BIST) circuit with simulation results.

4.2The Proposed BIJM circuit

4.2.1 Specification

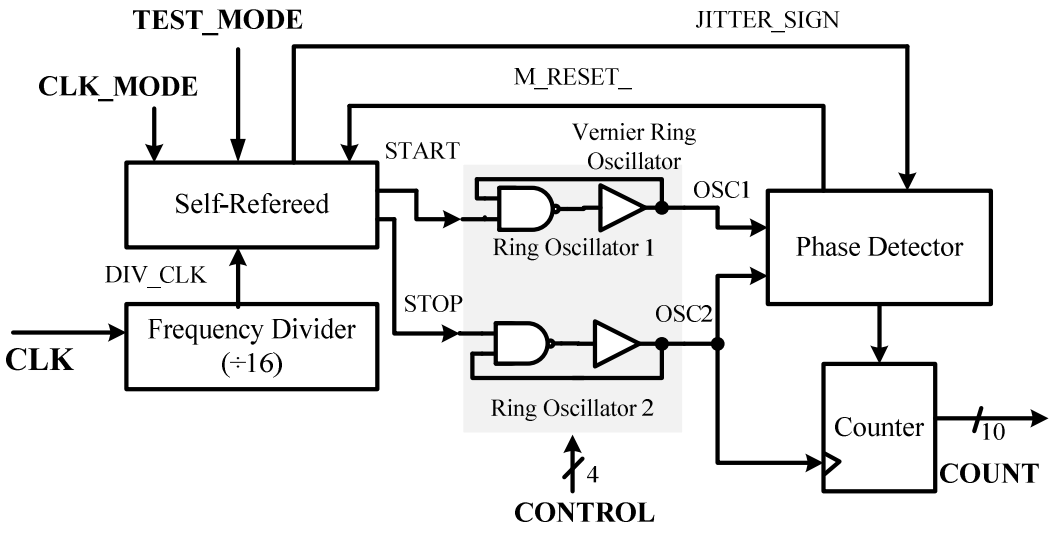


Fig. 4-1 The architecture of the proposed BIJM circuit

Fig. 4-1 shows the architecture of the proposed built-in jitter measurement (BIJM) circuit, and it is composed of five blocks, a Frequency Divider circuit, a Self-Referred circuit, a Vernier Ring Oscillator (VRO) circuit, a Phase Detector (PD) circuit, and a 10-bit counter circuit.

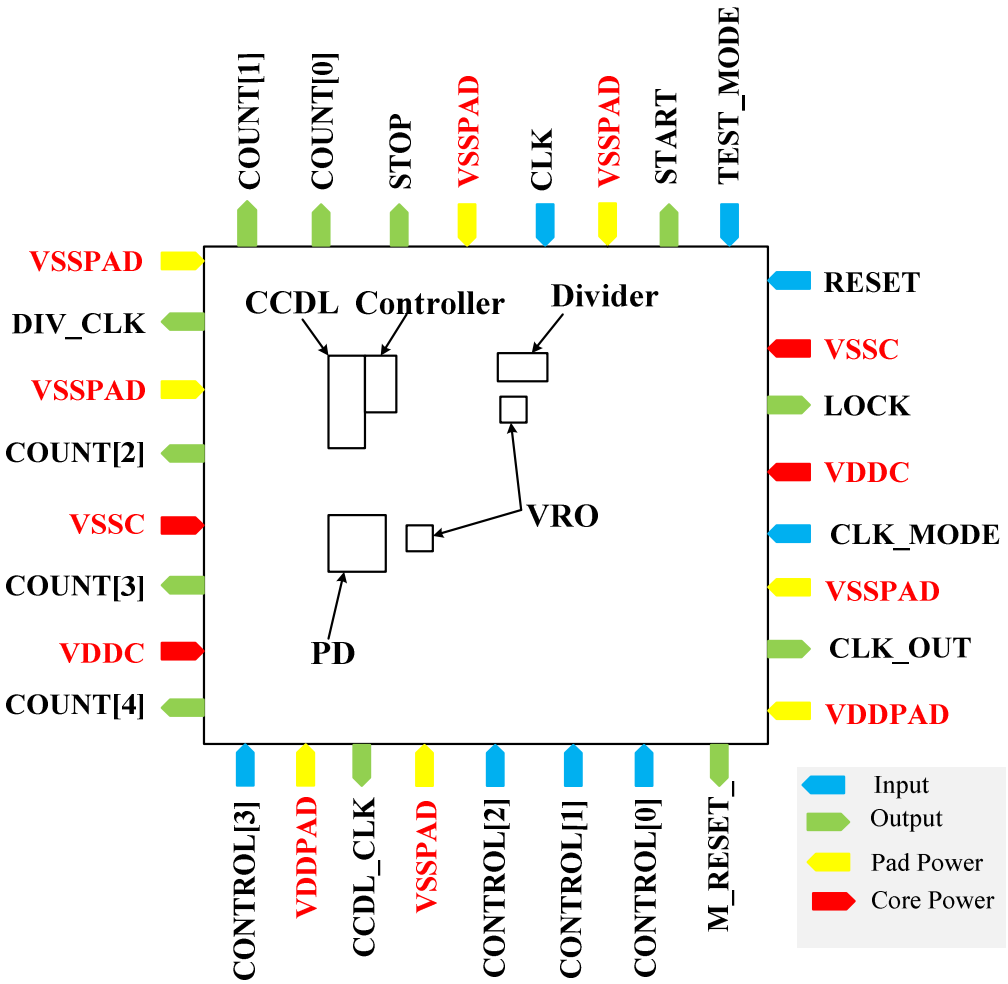


Fig. 4-2 The proposed BIJM chip floorplanning and I/O planning

Fig. 4-2 shows the chip floorplanning and I/O planning of the proposed built-in jitter measurement (BIJM) without mathematics operation block. Then, the detail description of the I/O is shown in Table 4-1.

Table 4-1 Chip I/O PADs description

Input	Bits	Function	
RESET	1	Set chip to initial	
CLK	1	Input test clock	
CLK_MODE	1	Set the test clock	
		Value	**Clock type**
		0	Input clock
		1	Divided clock
TEST_MODE	1	Set the measured mode of BIJM	
		Value	**Mode type**
		0	Calibration mode
		1	Normal mode
CONTROL	4	Adjust the resolution of VRO	
Output	**Bits**	**Function**	
CLK_OUT	1	Input test clock through I/O pad	
DIV_CLK	1	Divided clock with ratio 16	
START	1	The beginning point of measurement	
STOP	1	The end point of measurement	
LOCK	1	CCDL phase lock	
M_RESET_	1	Measured reset	
COUNT	5	Jitter counter	
Power Pad	**Pairs**	**Functions**	
VDDC+VSSC	2	CORE Power Pad	
VDDPAD+VSSPAD	4	Pad Power Pad	

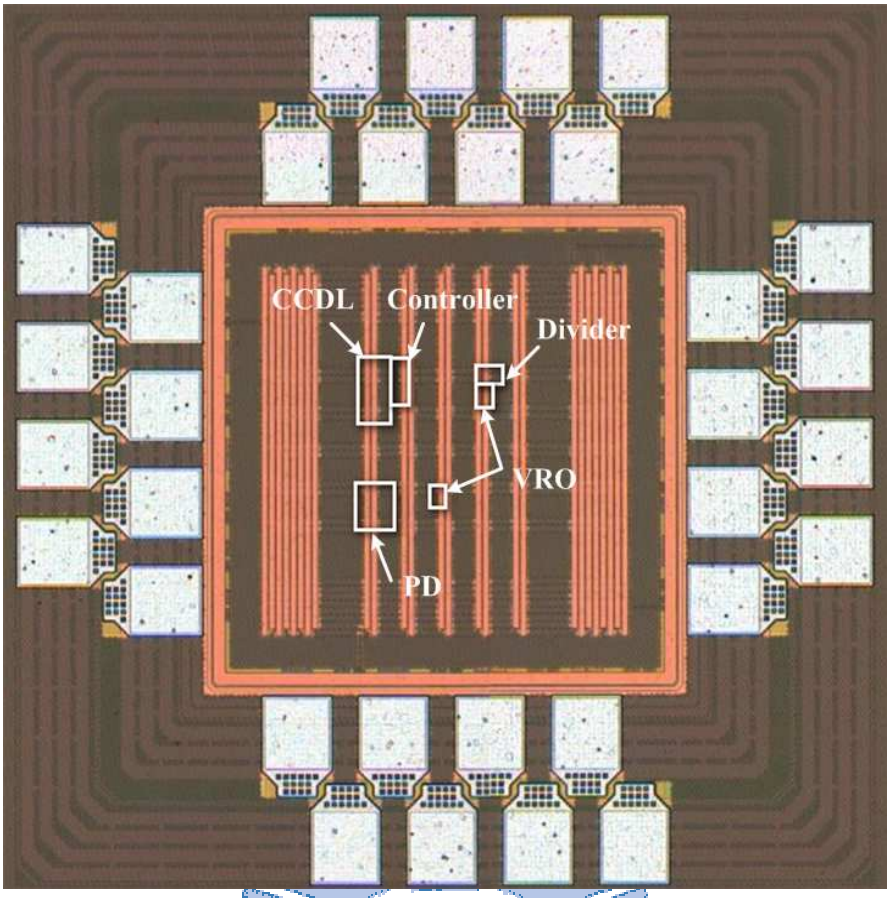


Fig. 4-3 The microphotograph of proposed BIJM circuit

Fig. 4-3 shows the microphotograph the proposed BIJM chip. The chip is fabricated by UMC 65nm standard performance CMOS process. The chip size is 0.644μm × 0.644μm, and the core size is 0.01μm^2. The layout can be divided into CCDL, Controller, Divider, VRO and PD, respectively, and the gate count with a 2-input NAND gate is 1749.

4.2.2 Simulation Results

4.2.2.1 Cycle-Controlled Delay Line

The counter in CCDL circuit has 8-bit, and the period of the ring oscillator is 2.22ns. Then, the delay range that the CCDL circuit can overlap is shown in Table 4-2.

Table 4-2 The step of the CCDL circuit in typical case

	Step	Bits
CCDL	2.22ns	8

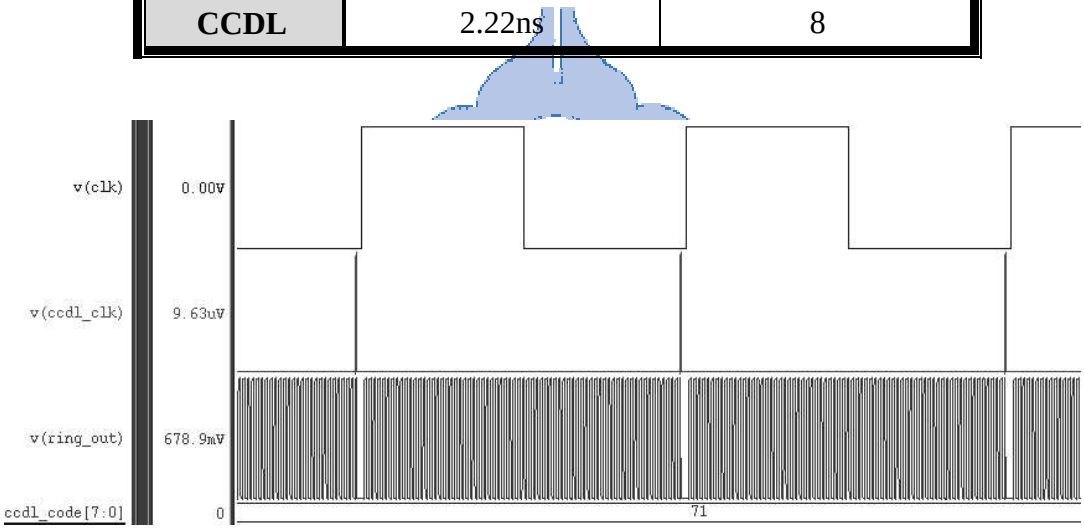


Fig. 4-4 The simulation result of the CCDL circuit.

Fig. 4-4 shows the simulation result of the cycle-controlled delay line (CCDL), and it is simulation in UltraSim MS mode. The period of input clock is 160ns and the frequency of input clock is 6.25MHz, and the input clock injures jitter model. From the period of ring oscillator 2.22 ns and the counter “71”, we can acquire the delay time is “157.62ns”.

4.2.2.2 Vernier Ring Oscillator

The signal CONTROL is used for adjusting the resolution of the vernier ring oscillator (VRO) circuit in calibration process, and the CONTROL has 4-bit.

Table 4-3 The resolution of VRO in typical case

CONTROL	Period of OSC1 (TT)	Period of OSC2 (TT)
00	2.956 ns	2.868ns
01	2.978 ns	2.884 ns
10	3.006 ns	2.906 ns
11	3.022 ns	2.927 ns

Table 4-3 shows the period of the two ring oscillators in TT corner, 1.0V, 25°C, and it is simulated in UltraSim MS mode. The resolution of VRO in process, voltage, and temperature (PVT) variations is shown in Fig. 4-5.

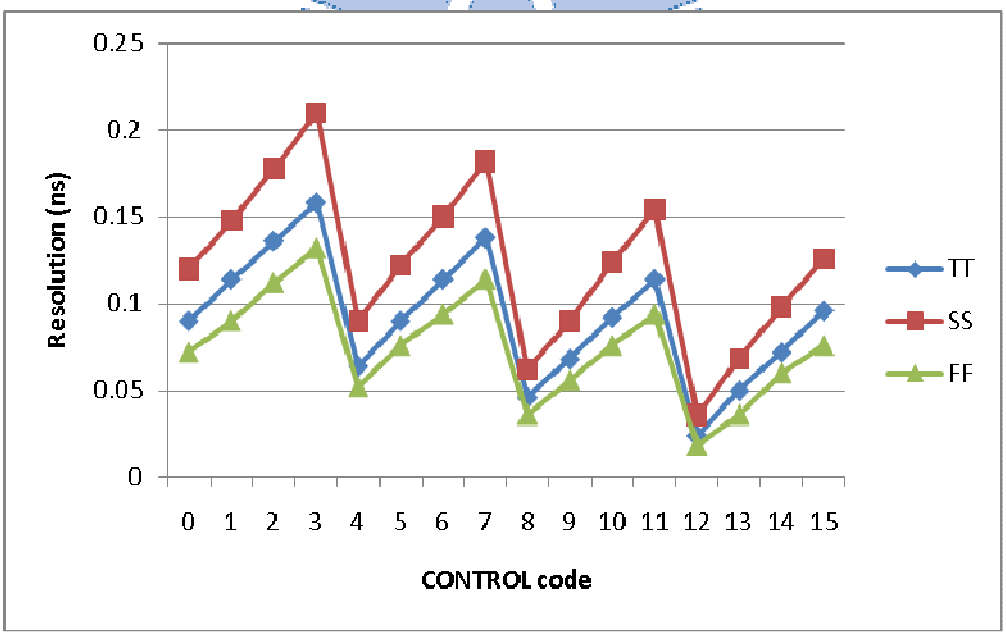


Fig. 4-5 The comparison of the VRO resolution in PVT

Fig. 4-5 presents the comparison of VRO resolution in PVT variations, and it is simulation result in UltraSim SPICE mode. The circle represents the TT corner, 1.0 V, 25°C, the square represents the SS corner, 1.1 V, 0°C, and the triangle represents the

FF corner, 0.9 V, 125°C, respectively.

4.2.2.3 Overall Architecture

The input clock frequency is limited by the cycle-controlled delay line (CCDL), because the period range of one-period delay clock that the CCDL circuit is finite. In addition, the measured range of the proposed built-in jitter measurement (BIJM) circuit restricts the period of the upper ring oscillator (OSC1) in vernier ring oscillator (VRO) circuit. If the jitter is larger than the period of “OSC1”, the BIJM circuit doesn’t measure correctly. In simulation result, the minimum input clock frequency is 1.767 MHz (period is 566ns) if we test the input clock jitter. Then the minimum input clock frequency is 28.26MHz (period is35.38 ns) if we test the divided clock signal with divide ratio (16). Besides, the input and the output clock frequency are restricted by the I/O pad operation frequency, and the maximum input clock frequency is about 333MHz (period is 3ns).

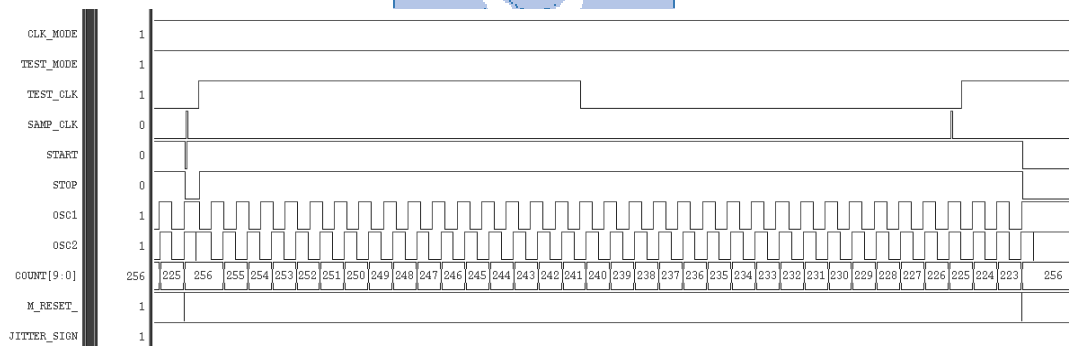


Fig. 4-6 The timing diagram of the proposed BIJM circuit in normal mode

Fig. 4-6 shows the simulation results of the proposed built-in jitter measurement (BIJM) circuit in the normal mode. It is simulated with UltraSIM DF mode at normal case. The input clock period is 4ns, and the divided clock period is 64ns. The average of counter value is “322”, and the resolution of VRO is 60.61ps from Eq2-8 in calibration mode. Moreover, the counter value is record “230” in this case when

"M_RESET_" signal produces a low pulse. The transformation is described as following equation.

$$J_i = |256 - N_i| * R_{VRO} \quad \text{(Eq 4-1)}$$

Where the N_i is *i-th* counter value, the RVRO is the resolution of the VRO in BIJM circuit, and the J_i is *i-th* of the jitter.

Therefore, the jitter value is equal to 1.636ns (=60.61ps*27), and the real jitter time is 1.589ns. Thus, the error of the proposed BIJM circuit is about 3.5%. However, the proposed all-digital BIJM circuit can't measure the jitter of the input clock at every clock cycle. When it starts to measure the jitter, it takes several cycles to calculate the jitter value. Thus, it still needs a long time to collect the jitter characteristic of the input clock.

4.2.3 Chip Measurement Results

The measured instruments have one clock generator, one oscilloscope, two power supplies, and one logic analyzer (LA). The one power supply is used for I/O pad power, and the other one is used for the chip core power. The clock generator offers the test clock frequency, and the oscilloscope records the test clock frequency jitter. Then, the LA instrument is used to collect the counter output of the proposed BIJM circuit, and processes the statistic results to histogram to compare with the record jitter from the oscilloscope.

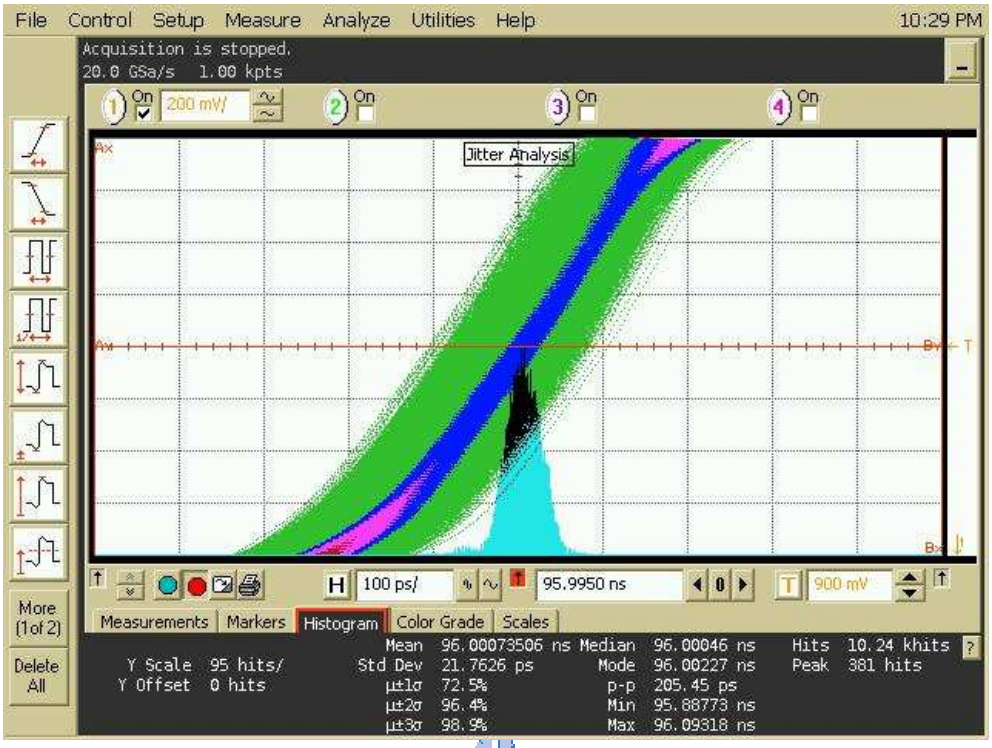


Fig. 4-7 The jitter histogram in oscilloscope

Fig. 4-7 shows the jitter histogram of the measured divided clock frequency, and the core power is 1.0 V and the pad power is 1.8 V. The input clock frequency is 167MHz, and the divided clock frequency with divided ratio "16" is 10.42MHz. The RMS jitter value of the divided clock frequency is 21.7627ps, and the Pk-Pk jitter of the divided clock frequency is 205.45ps.

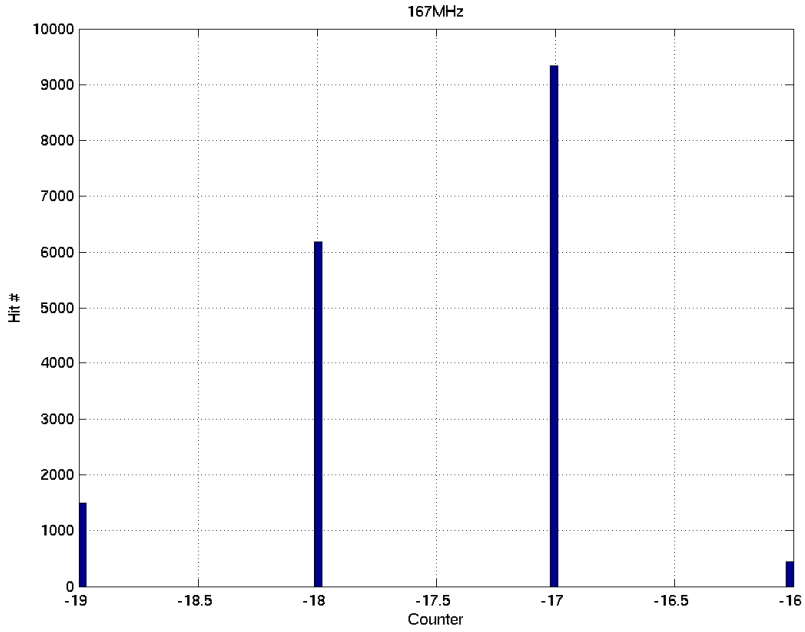
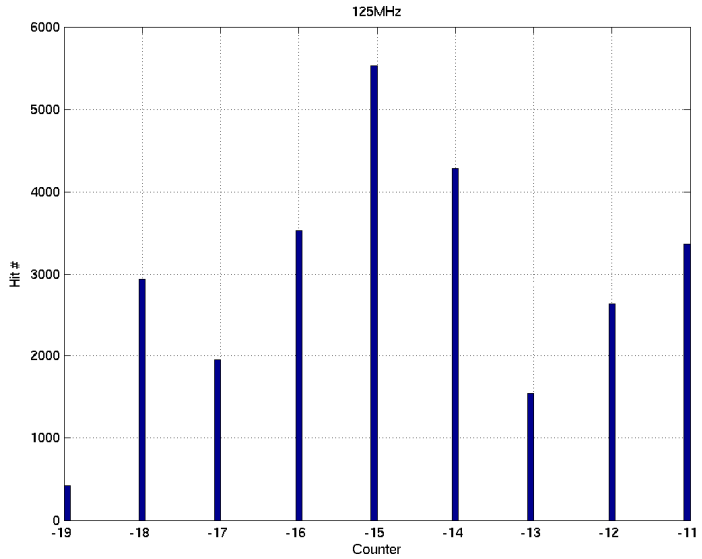


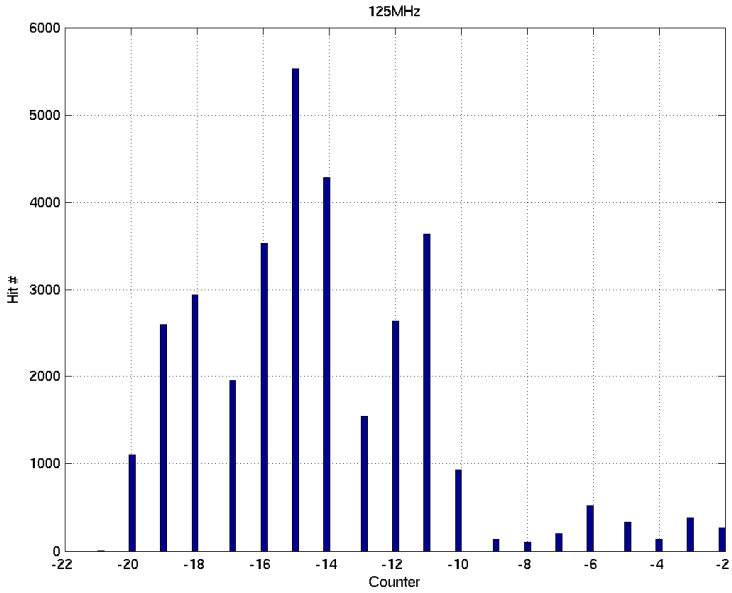
Fig. 4-8 The jitter histogram measured by the proposed BIJM chip

Fig. 4-8 shows the output counter histogram of the proposed BIJM chip and those results are processed by the Matrix Laboratory (MATLAB) software. In our circuit, compare with the input clock jitter, the higher resolution of the VRO in typical case is worse. Additionally, the range of the CCDL circuit is limited.

Moreover, the resolution of the vernier ring oscillator (VRO) and the offset generated by the cycle-controlled delay line (CCDL) would affect the accuracy of the proposed BIJM circuit. In the results, if the jitter is smaller than the resolution of the VRO, it would make the VRO oscillate too many times. On the contrary, if the jitter is longer than the period of the OSC1 that the longer period oscillator of the VRO circuit, it would make the VRO oscillate less cycle times. However, we can adjust the environment to observe our measured results.



(a) Decreasing the core power



(b) Increasing the core power

Fig. 4-9 The improved measured techniques

Fig. 4-9 presents the improved measured results, and those adjust the core power. In Fig. 4-9(a), it decreases the core power to stretching the delay line of the CCDL circuit for producing one-period delay clock signal precisely. In this case, the pad

power is still set to “1.8 V”, and the core power is set to “0.9 V”. It measures other input clock frequency with divided input clock RMS jitter less 50ps. It still can obverse the jitter distribution is normal. However, decreasing core power can stretch the delay line of the CCDL circuit, it also make the resolution of the VRO lower relatively. The most important of parameter is the resolution of the VRO circuit in the accuracy of the BIJM. Therefore, we increase the core power for improving the resolution of the VRO circuit

Fig. 4-9(b) shows the measured result that raising the power to improve the resolution of the VRO circuit, and the pad power is still set to “1.8 V”, and the core power is set to “1.2 V”. It is obvious for increasing the core power to make the resolution higher. However, raising power can improve the resolution of the BIJM circuit, but it would shorten the delay time of the CCDL. It should make a balance between the one-period delay circuit (CCDL) and the quantization circuit (the TDC circuit with VRO structure).

Table 4-4 The comparison table of the proposed BIJM circuit

	Proposed BIJM	ESSCIRC2005[9]	JSSC2006[23]	TVLSI2009[11]	ISVLSI2005[18]	TVLSI2010[17]
Technology	65nm	0.13μm	90nm	90nm	0.18 μm	90nm
Architecture	TA (DIV), TDC (VRO)	TDC(DL)	Interpolate (VDL)	TDC(DL/VDL)	TDC(VRO)	TA, TDC(VRO)
Input frequency	100MHz ~300MHz	100NHz	250MHz	2.5GHz	100MHz	3GHz
Area (mm^2)	0.0027	0.003	0.24	0.075	0.004	0.038
Power (mW)	1.092mW @(250MHz)	N/A	N/A	N/A	N/A	11.4mW (@ 3GHz)
RMS Jitter (oscilloscope /BIJM)	21.76/35.83	4.1/3.2	2.03/2.0	10.1/6.2	42.7/62.7	4.15/3.78
Self-reference	Y	N	N	Y	Y	Y

Table 4-4 lists the comparisons of recent built-in jitter measurement (BIJM) circuits. In [9][23], the external reference clock is needed to measure the jitter performance of the PLL. It is difficult to acquire a jitter-free reference clock, so they are not suitable for the on-chip jitter measurement applications with many PPLs on a single chip. In [11], using the the time-to-digital converter (TDC) with delay line (DL) structure as one-period delay has a very limited input clock range, and the TDC with vernier delay line (VDL) also has limited input clock jitter range. In [18] it doesn't have a timing amplifier (TA) to enlarge jitter, and it has large jitter measurement error. Then, the [17] using the analog timing amplifier (TA) extends the clock jitter, and the linear region of the analog TAs is easily affected by process, voltage, and temperature (PVT) variations.

4.3The Proposed BIST circuit

4.3.1 Specification

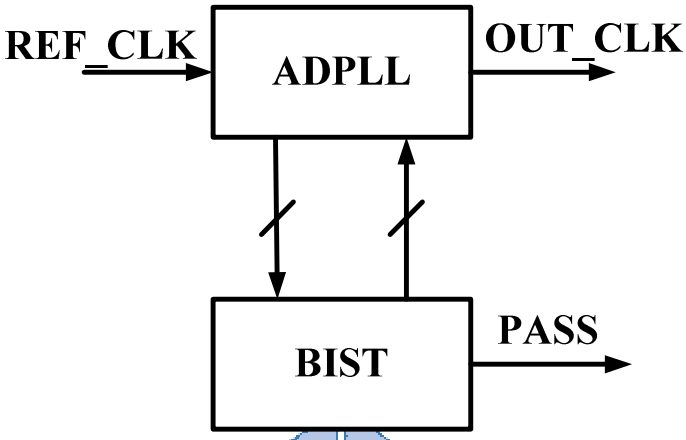


Fig. 4-10 The simple architecture of the proposed BIST circuit with PLL

Fig. 4-10 shows the architecture of the proposed built-in self-test (BIST) circuit and all-digital phase-locked loop (ADPLL) circuit. The detail architecture of the BIST is mentioned in Chapter 3, and the detail architecture of the BIJM with mathematics operation is mentioned in Chapter 2.

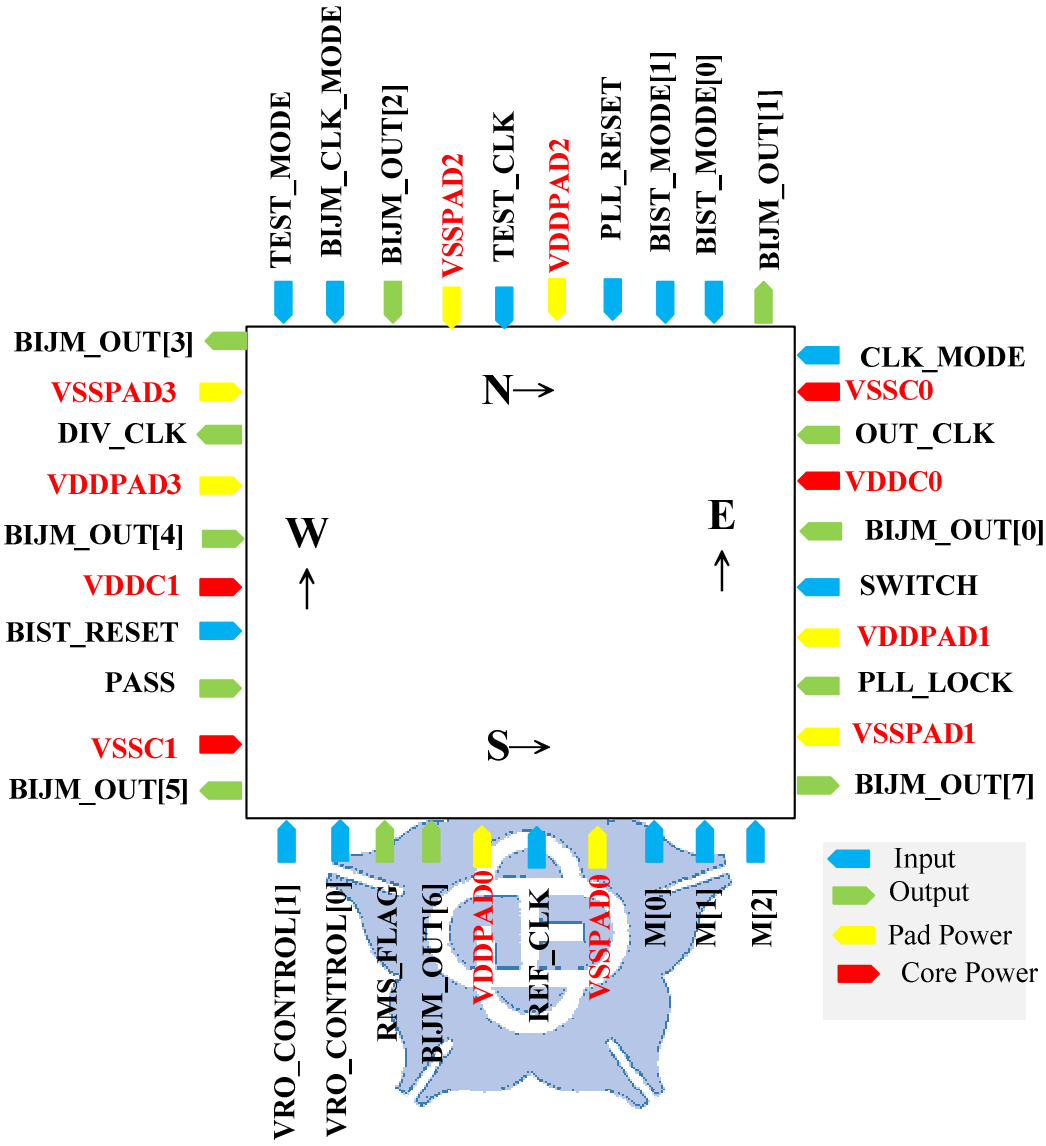


Fig. 4-11 The proposed BIJM chip floorplanning and I/O planning

Fig. 4-11 shows the chip floorplanning and I/O planning of the chip, and it composed ADPLL block, BIST block and BIJM block. Then, the detail description of the I/O is shown in Table 4-5.

Table 4-5 The proposed BIST chip I/O PADs description

Input	Bits	Function	
PLL_RESET	1	Set ADPLL circuit to initial	
BIST_RESET	1	Set BIST circuit to initial	
REF_CLK	1	PLL input clock	
TEST_CLK	1	External test clock	
CLK_MODE	1	Set Test Clock	
		Value	**Clock Type**
		0	Input Clock
		1	Divided Clock
TEST_MODE	1	Set the Measured Mode of BIJM	
		Value	**Mode Type**
		0	Calibration Mode
		1	Normal Mode
BIJM_CLK_MODE	1	Set the BIJM Input Clock	
		Value	**Clock Type**
		0	PLL Output Clock
		1	External Test Clock
BIST_MODE	2	Set the BIST for PLL Operation Mode	
		Value	**Test Mode Type**
		0	PLL Normal Mode
		1	PFD/Controller Test
		2	Jitter Measurement
		3	Frequency Divider Test
SWITCH	1	Set the Output Data	
		Value	**Data Type**
		0	BIJM Counter Value
		1	RMS Counter Value
VRO_CONTROL	2	Adjust the resolution of the VRO	
M	3	PLL frequency divider ratio	

Output	**Bits**	**Function**
OUT_CLK	1	The output of the ADPLL
PASS	1	The test result of the BIST
DIV_CLK	1	Divided clock with ratio 16
PLL_LOCK	1	PLL Lock signal
RMS_FLAG	1	Calculating RMS finished signal

BIJM_OUT	8	Jitter Counter/RMS Counter
Power Pad	**Pairs**	**Functions**
VDDC+VSSC	2	CORE Power Pad
VDDPAD+VSSPAD	4	Pad Power Pad

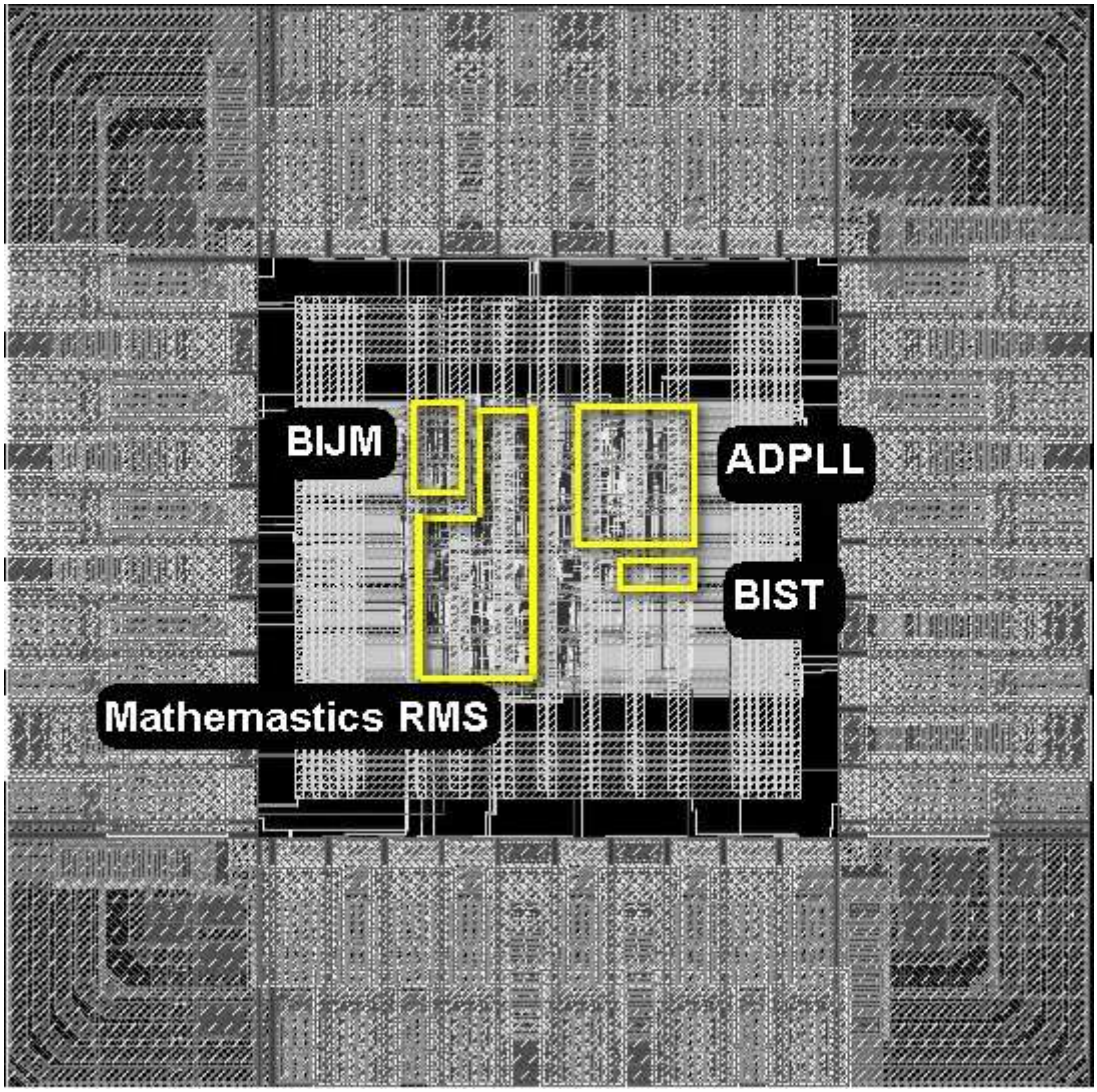


Fig. 4-12 The layout of the proposed BIST circuit

Fig. 4-12 shows the layout of the proposed BIST circuit, and it is composed of a all-digital phase-locked loop (ADPLL) circuit, a built-in jitter measurement (BIJM) circuit, a built-in self-test (BIST) circuit and a mathematics block. The chip is fabricated by UMC 65nm standard performance CMOS process. The chip size is 0.744μm × 0.744μm, and the core size is 0.04μm^2, the Table 4-6 presents the gate count of the sub-circuits.

Table 4-6 The gate count of the proposed BIST block

Circuit	Gate Count (2-input NAND gate)
ADPLL	4158
BIST	361
BIJM	1749
Mathematics Operation	5275

4.3.2 Simulation in Verilog Behavior Model

4.3.2.1 BIST for PFD/Controller

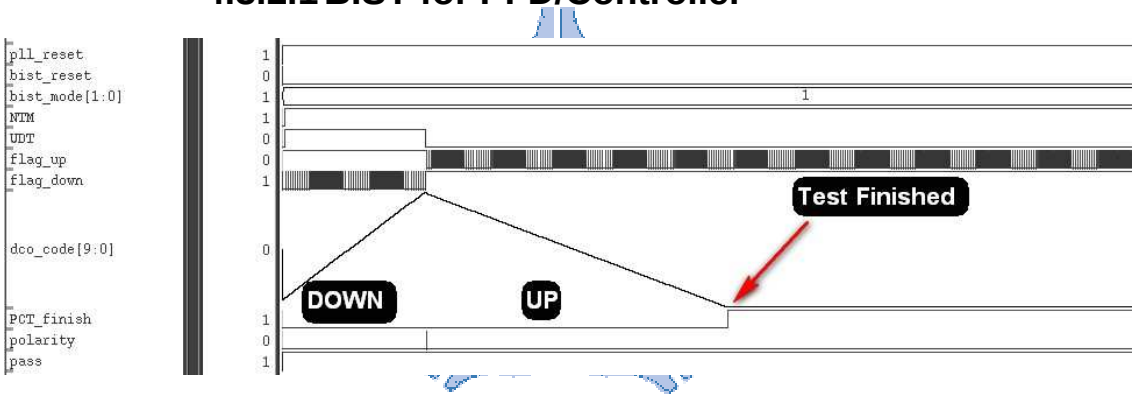


Fig. 4-13 The simulation result of BIST for PFD testing

Fig. 4-13 presents the simulation of proposed BIST for PFD test in verilog behavior model. When "BIST_MODE" is set to “01”, the proposed BIST circuit will implement the operation of PFD test. First, the proposed BIST controller forces the IN signal lags the FB signal, and the PFD will produce the “flag_down” signal and the "DCO_CODE" is increasing. If the PLL doesn’t have fault, the BIST controller will turn the state of PFD into forcing down test. The proposed BIST controller make the "IN" clock signal leads the "FB" clock signal, and the PFD will generate the “flag_up” signal and the "DCO_CODE" is decreasing. The pass/fail signal will announce whether the PLL works correctly, and the PFD/Controller test finish

(PCT_finish) signal will announce the BIST for PFD/Controller test is finished if the forcing down test passes.

4.3.2.2 BIST for Frequency Divider/Controller

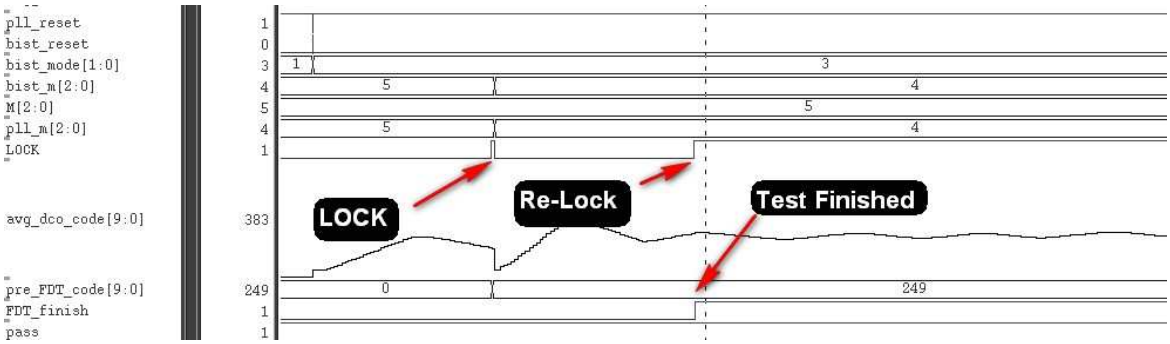


Fig. 4-14 The simulation result of BIST for frequency divider testing

Fig. 4-14 shows the simulation result of BIST for frequency divider testing. After the PLL is locked, the BIST for frequency divider testing circuit is staring. It alters the frequency divider ratio (PLL_M) from input frequency divider ratio (M) to the proposed BIST supplied (BIST_M), and the output clock frequency will be faster. Therefore, the controller will increase to obtain lock state again. The pass/fail signal will announce whether the PLL works correctly, and the frequency divider test finish (FDT_finish) signal will announce the BIST for FD/Controller test is finished.

4.3.3 Summary

No matter the BIST for PFD/Controller circuit or the BIST for Frequency Divider/Controller circuit, they are standard cell library to design. It is programmable for different process.

In this thesis, we use the invasive approach for built-in self-test (BIST) circuit to determine the function of the PLL block. We use the indirectly signal to observe the action of the block, and those extra circuit doesn’t break the loop of the PLL. In addition, the invasive approach is easy to design than the others, and it affects the initial performance of the PLL slightly.

Chapter 5 Conclusion and Future Works

In this thesis, the all-digital built-in jitter measurement (BIJM) is proposed. The circuit uses a frequency divider as timing amplifier, and it can solve the bottleneck of the analog circuits with process, voltage and temperature (PVT) variations. The one-period delay circuit with the cycle-controlled delay line (CCDL) and the time-to-digital converter (TDC) with the vernier ring oscillator (VRO) can reduce the area overhead.

In addition, it also implements a mathematics operation block to calculate the root-mean-square (RMS) of test clock jitter. In general, jitter distribution is normal distribution random variables, and the RMS value and the Pk-Pk value are the important parameters in normal distribution. Therefore, we can calculate the RMS jitter to determine PLL in jitter measurement. The improving moving average method is proposed to reduce the number of registers for decreasing the area overhead.

This thesis also proposes an all-digital built-in self-test (BIST) circuit for an all-digital phase-locked loop (ADPLL) including testing PFD/Controller circuit and testing frequency divider circuit. Although they add extra circuits and catch internal signals, they don’t modify existing circuitry. Thus, the proposed BIST circuit doesn’t break the PLL loop, and slightly affects the performance of PLL.

From the experimental results, we would adjust the resolution of the built-in jitter measurement (BIJM) circuit higher and stretch the delay line of the cycle-controlled delay line (CCDL) circuit to improve the accuracy of the test circuit.

Besides, we would test the others block of the phase-locked loop (PLL) to determine the PLL performance such as digital-controlled oscillator (DCO) circuit.

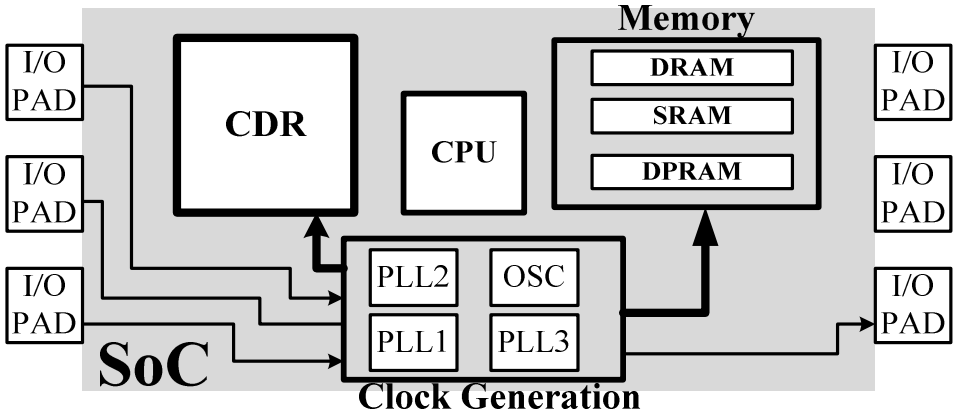


Fig 5-1 The future work for multiple ADPLLs testing

The PLLs are always utilized to generate various clock rates for memory and I/O interfaces, and a chip has more one PLL. However, if each PLL uses own built-in self-test circuit, it would take large area overhead. Therefore, we hope to design a BIST circuit for the multiple PLL application as shown in Fig 5-1.

Reference

[1] Chao-Ching Hung and Shen-Iuan Liu, “A Leakage-Compensated PLL in 65-nm CMOS Technology,” *IEEE Transactions on Circuits and System Ⅱ: Express Briefs*, Vol. 56, pp. 525-529, Jul. 2009.

[2] Chao-Ching Hung and Shen-Iuan Liu, “A Leakage-Suppression Technique for Phase-Locked Systems in 65nm CMOS,” in *Digest of Technical Paper, IEEE Solid-State Circuits Conference*, Feb. 2009, pp. 400-401.

[3] Ching-Che Chung, and Chen-Yi Lee, “An all-digital phase-locked loop for high-speed clock generation,” *IEEE Journal of Solid-State Circuits*, Vol. 38, pp. 347-351, Feb. 2003.

[4] Chia-Tsun Wu; Wei Wang; I-Chyn Wey; An-Yeu Wu, “A scalable DCO design for portable ADPLL designs,” in *Proceedings IEEE International Symposium on Circuits and Systems, (ISCAS)*, July 2005, pp. 5449-5452.

[5] Benoit Nadeau-Dostie, *Design for AT-Speed Test, Diagnosis and Measurement*, Boston: Kluwer Academic Publishers, 2000, Ch. 6, pp. 139-169.

[6] Nelson Soo, “Jitter Measurement Techniques,” Pericom Application Brief AB36, Nov. 2000.

[7] Stephen Sunter, and Aubin Roy, “BIST for Phase-Locked Loops in Digital Applications,” in *Proceedings of the Internal Test Conference*, 1999, pp. 532-540.

[8] Stephen Sunter, and Aubin Roy, “Purely Digital BIST for any PLL or DLL,” in *Proceeding of 12th IEEE European Test Symposium (ETS)*, pp.185-192, May. 2007.

[9] Keith A. Jenkins, Anup P. Jose, and David F. Heidel, “An On-chip Jitter Measurement Circuit with Sub-picosecond Resolution,” in *Proceedings of the European Solid-State Circuits Conference*, Sept. 2005, pp. 157-160.

[10] Jui-Jer Huang, and Jiun-Lang Huang, “A Low-Cost Jitter Measurement Technique for BIST Applications,” in *Proceedings of Asian Test Symposium (ATS)*, Nov. 2003, pp. 336-339.

[11] Shu-Yu Jiang, Kuo-Hsing Cheng, and Pei-Yi Jian, “A 2.5-GHz Built-in Jitter Measurement System in a Serial-Link Transceiver,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, pp.1698-1708, Dec. 2009.

[12] Piotr Dudek, Stanislaw Szczpanski, and John V. Hatfied, “A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line,” *IEEE Journal of Solid-State Circuits*, Vol. 35, pp. 240-247, Feb. 2000.

[13] Chin-Cheng Tsai, and Chung-Len Lee, “An On-Chip Jitter Measurement Circuit

for the PLL", in *Proceedings of Asian Test Symposium (ATS)*, Nov. 2003, pp. 332-335.

[14] Kuo-Hsing Cheng, Shu-Yu Jiang, and Zong-Shen Chen, "BIST for clock jitter measurements, " in *Proceedings of International Symposium on Circuits and Systems*, May 2003, pp. 557-580.

[15] Kuo-Hsing Cheng, Chan-Wei Huang, and Shu-Yu Jiang, "Self-Sampled Vernier Delay Line for Built-in Clock Jitter Measurement," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2006, pp. 1591-1594.

[16] Chan Antonio H. and Roberts Gordon W., "A Jitter Characterization System Using a Component-Invariant Vernier Delay Line," *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, Vol. 12, pp. 79-95, Jan. 2004.

[17] Kuo-Hsing Cheng, Jen-Chien Liu, Chih-Yu Chang, Shu-Yu Jiang, and Kai-Wei Hong, "Built-in Jitter Measurement Circuit with Calibration Techniques for a 3-GHz Clock Generator," *IEEE Transaction on Very Large Scale Integration (VLSI) Systems*, 2010. (IEEE EARLY ACCESS)

[18] Tian Xia, Hao Zheng, Jing Li, and Ginawi. Ahmed, "Self-Refereed on-chip Jitter Measurement Circuit Using Vernier oscillators," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 2005, pp. 218-223.

[19] Wei Tang, Jianhua Feng, and Chundlen Lee, "A Jiiter Measurement Circuit Based on Dual Resolution Vernier Oscillator," in *Proceedings of IEEE international Conference on ASIC*, Oct. 2009, pp.1213-1216.

[20] An-Sheng Chao and Soon-Jyh Chang, "A Jitter Characterizing BIST with Pulse-Amplifying Technique", in *Proceedings of Asian Test Symposium (ATS'08)*, Dec. 2008, pp. 379-384.

[21] Yeong-Jar Chang, Shen-Tien Lin, Kun-Lun Luo, and Wen-Ching Wu, "A Testable BIST Design for PLL," in *Proceedings of International Symposium on VLSI Technology, Systems and Applications*, Oct. 2003, pp. 204-207.

[22] Nai-Chen Daniel Cheng, Yu Lee, and Ji-Jan Chen, "A 2-ps Resolution Wide Range BIST Circuit for Jitter Measurement," in *Proceedings of Asian Test Symposium (ATS'07)*, Nov. 2007, pp. 219-223.

[23] Koichi Nose, Mikihiro Kajita, and Masayuki Mizuno, "A 1ps Resolution Jitter Measurement Macro Using Interpolated Jitter Oversampling" *IEEE Journal of Solid-State Circuits*, Vol. 41, pp. 2911-2920, Dec.2006.

[24] Tian Xia; Jien-Chung Lo; "Time-to-voltage converter for on-chip jitter measurement", *IEEE Transactions on Instrumentation and Measurement*, vol. 52, pp. 1738-1748, Nov. 2003.

[25] Stephen Sunter, and Aubin Roy, "On-Chip Digital Jitter Measurement, from Megaherz to Gigahertz," *IEEE Design & Test of Computer*, Vol. 21, pp. 314-321,

Aug. 2004.

[26] Jen-Chien Hsu and Chauchin Su, “BIST for Measuring Clock Jitter of Charge-Pump Phase-Locked Loops”, *IEEE Trans. Instrum. Mean.*, vol.. 57, no.2, pp.276-284, Feb. 2008.

[27] Kevin Sliech and Martin Margala, “A Digital BIST for Phase-Locked Loops” in *Proceedings of Defect and Fault Tolerance of VLSI Systems (DFTVS)*, Oct. 2008, pp. 134-142.

[28] Karen Taylor, Bryan Nelson, Alan Chong, Hieu Nguyen, Henry Lin, Mani Soma, Hosam Haggag, Jeff Huard, and Jim Braatz, “Experimental Results for High-Speed Jitter Measurement Technique,” in *Proceedings of International Test Conference (ITC)*, Oct. 2004, pp. 85-94.

[29] Abas, M.A., Russell G., and Kinniment D.J., “Embedded high-resolution delay measurement system using time amplification,” *IET Computers & Digital Techniques*, Vol. 1, pp. 77-86, Mar. 2007.

[30] Ishida, M., Ichiyama, K., Yamaguchi, T.J., Soma, M., Suda, M., Okayasu, T., Watanabe, D., and Yamamoto, K., “A Programmable On-Chip Picosecond Jitter-Measurement Circuit without a Reference-Clock Input,” in *Proceedings of IEEE International Solid-State Circuits Conference*, Feb. 2005, pp. 512.

[31] Cazeaux Jose Manuel, Omana Martin, and Metra Cecilia, “Novel On-Chip Circuit for Jitter Testing in High-Speed PLLs,” *IEEE Transactions on Instrumentation and Measurement*, Vol. 54, pp. 1779-1788, Oct. 2005.

[32] Cheng Jia, and Linda Milor, “A BIST Circuit for DLL Fault Detection,” *IEEE Trasactions on Very Large Scale Integration (VLSI) Systems*, Vol. 16, pp. 1687-1695, Dec. 2008.

[33] Junseok Han, Dongsup Song, Hagbae Kim, and Sungho Kang, “An Effective Built-In Self-Test for Chargepump PLL”, in *IEICE Transactions on Electrons, Vol. E88-C*, pp. 1731-1733, Aug. 2005.

[34] Youbean Kim, Kicheol Kim, Incheol Kim, and Sungho Kang, “A New Built-in Self Test Scheme for Phase-Locked Loops Using Internal Digital Signals,” In *IEICE Transactions*, Vol. E91-C, pp. 1713-1716, Oct. 2008.

[35] Chun-Lung Hsu, Yiting Lai, and Shu-Wei Wang, “Built-In Self-Test for Phase-Locked Loops,” *IEEE Transactions on Instrumentation and Measurement*, Vol. 54, pp. 996-1002, Jun. 2005.

[36] Asquini, A.; Badets, F.; Mir, S.; Carbonero, J.-L.; Bouzaida, L.; “PFD Output Monitoring for RF PLL BIST”, in *Proceedings of IEEE Mixed-Signals, Sensors, and Systems Test Workshop(IMS3TW)*, July, 2008, pp. 1-5.

[37] Guo Yu, and Peng Li, “A Methodology for Systematic Built-In Self-Test of Phase-Locked Loops Targeting at Parametric Failures,” in *Proceedings of IEEE*

International Test Conference (ITC), Oct. 2007, pp. 1-10.

[38] Ping-Ying Wang; Hsiu-Ming Chang; and Kwang-Ting Cheng; "An All-Digital Built-In Self-Test Technique for Transfer Function Characterization of RF PLLs", in *Proceedings of Design, Automation & Test in Europe Conference & Exhibition (DATE)*, May, 2011, pp. 1-6.

[39] Seongwon Kim; and Soma, Mani., "An All-Digital Built-In Self-Test for High-Speed Phase-Locked Loops", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, pp. 141-150, Feb. 2002.

[40] Dasnurkar Sachin, and Abraham Jacob, "Closed-Loop Built-in-Self-Test for PLL Production Testing with Minimal Tester Resources," in *Proceedings of International Mixed-Signals, Sensors, and Systems Test WorkShop*, June 2009, pp1-5.

[41] Florence Azais, Yves Bertrand, Michel Renovell, Andre Ivanov, Sassan Tabatabaei, "An All-Digital DFT Scheme for Testing Catastrophic Faults in PLLs," *IEEE Design & Test of Computers*, Vol. 20, pp. 60-67, Feb. 2003.

[42] Chen-Yi Lee, and Ching-Che Chung, "Digital Loop Filter for All-Digital Phase-Locked Loop Design," US patent 7,696,832 B1, Apr.13, 2010.

[43] Ching-Che Chung and Chia-Lin Chang, "A wide-range all-digital delay-locked loops in 65nm CMOS technology," in *Proceedings of International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, Apr. 2010, pp. 66-69.

[44] Hsiang-Hui Chang and Shen-Iuan Liu, "A wide-range and fast-locking all-digital cycle-controlled delay-locked loop," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 661-670, Mar. 2005.

[45] Oulmane, Mourad, and Roberts Gordon W., "A CMOS Time Amplifier for Femto-Second Resolution Timing Measurement," in *Proceedings of the International Symposium on Circuits and Systems (ISCAS)*, May 2004, pp. 509-512.

[46] Ching-Che Chung and Wei-Jung Chu, "An All-digital On-Chip Jitter Measurement Circuit in 65nm CMOS technology," in *Proceedings of International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, Apr. 2011,