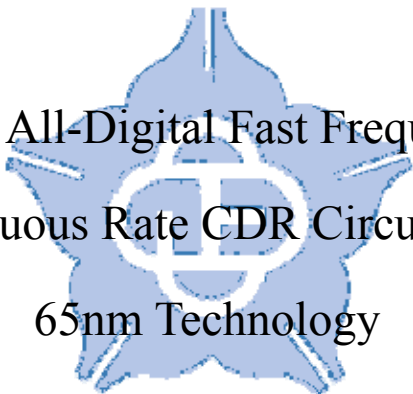


國立中正大學

資訊工程研究所碩士論文

可應用於USB2.0之無參考時脈全數位快速
鎖定之連續速率資料與時脈回復電路

An Referenceless All-Digital Fast Frequency Acquisition
Full-Rate Continuous Rate CDR Circuit for USB 2.0 in
65nm Technology



研究生： 戴偉丞

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中華民國 一 百 年 七 月

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學位考試同意書

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可應用於 USB2.0 之無參考時脈全數位快速鎖定之連續速率資料與時脈回復電路

學生：戴偉丞

指導教授：鍾菁哲 博士

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摘要

有鑑於傳統 USB2.0 傳輸架構之中擁有需要外接石英震盪器來當作參考時脈以及依靠以多相位產生器來完成資料回復等技術會造成額外面積成本以及功率消耗的問題；本論文提出一個不需要外部參考時脈之資料與時脈回復電路，此電路用於 USB2.0 通訊系統之接收端；針對傳送端傳送過來的 USB2.0 封包內之同步訊號區段來完成接收端與傳送端時脈之頻率追蹤及相位鎖定，使得接收端可正確的將傳送端傳送過來的資料重現於接收端之暫存器內；但由於 USB2.0 之同步訊號為一個有限的長度（高速模式下為 32 位元，全速及低速模式中為 7 位元），為了滿足此快速鎖定的需求，本論文提出了內嵌時間至數位轉換器之振盪器使得本電路在頻率追蹤上可在一個同步訊號的時間即可快速的鎖定至接近於資料傳送率的頻率區段，使之加快追蹤過程讓整體鎖定時間可於同步訊號的區段之內完成。本論文也提出一個雙模式相位與頻率偵測器，可於封包中的同步訊號區段使用頻率偵測模式來達成頻率追蹤，於隨機資料的區段中可切換至相位偵測模式，來達成並維護接收端振盪器與輸入資料訊號間相位的對齊。

USB2.0 之中分別提供三種速度模式，分別為高速模式(480MHz)、全速模式(12MHz) 以及低速模式(1.5MHz)；在傳統 USB2.0 傳輸架構之中，每一種速度模式下都需要一個與之對應的時脈與資料回復電路造成成本的提升；本論文提出的

時脈與資料回復電路能達到以一套硬體完成寬頻的工作範圍來涵蓋 USB2.0 中所有速度模式以減少硬體成本。為了支援低頻的模式本論文提出了一個低頻時脈合成器減少傳統上使用延遲單元的作法，減少面積並達成寬頻連續速率時脈與資料回復電路來支援於 USB 2.0 下所有速度模式。

本論文提出之全數位電路使用 65 奈米製程的標準元件庫實現，工作範圍為 700kHz 到 500MHz 可用於連續速率之時脈及資料回復，晶片面積為 $150\mu\text{m}^2$ ，其最高功率消耗為運作於 500MHz 之消耗功率為 2.63mW。



An Referenceless All-Digital Fast Frequency Acquisition Full-Rate Continuous Rate CDR Circuit for USB2.0 in 65nm Technology

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Department of Computer Science and Information Engineering,
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Abstract

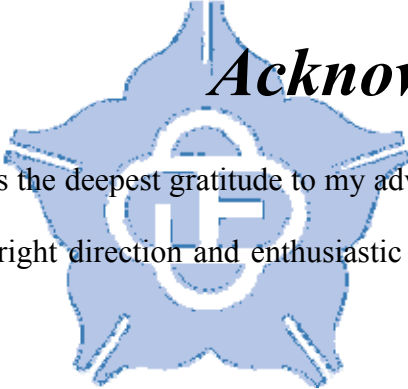
The conventional USB2.0 transceiver usually needs the external reference clock and multi-phase scheme for over-sampling architecture and causes the additional cost. To solve this problem, an all-digital fast frequency acquisition full-rate continuous rate clock and data recovery (CDR) circuit for USB 2.0 applications without a reference clock is presented in this thesis. Lock-in time is constrained by the short USB 2.0 packet synchronization pattern's specifications (32bit for high speed mode and 7bit for full/slow speed mode). Therefore we propose a wide range time-to-digital converter (TDC) embedded digital control oscillator (DCO) to achieve fast frequency acquisition so that the lock-in time can be reduced to satisfy the length of synchronization pattern. A dual mode phase and frequency detector (PFD) is proposed to perform two operating modes in the frequency tracking in the sync pattern region and the phase aligning in the random data pattern region.

In order to support all USB 2.0 speed modes: high speed mode (480MHz), full speed mode (12MHz) and slow speed mode (1.5MHz), the low frequency clock synthesizer is proposed in this thesis. It can achieve the wide range continuous rate

clock and data recovery with reduced area cost and cover all the operation modes of USB 2.0.

The proposed ADCDR is implemented on standard performance 65nm CMOS process. The operating range of proposed ADCDR circuit is from 700kHz to 500MHz which covers all speed modes of USB 2.0. The chip size is $644\mu\text{m}^2$ and the core size is $150\mu\text{m}^2$. The power consumption is 2.63 mW at 500MHz.





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Chapter 1 Introduction

1.1 Conventional CDR circuit survey

1.1.1 Basic concept of CDR circuit

1.1.1.1 Sample CDR Circuit

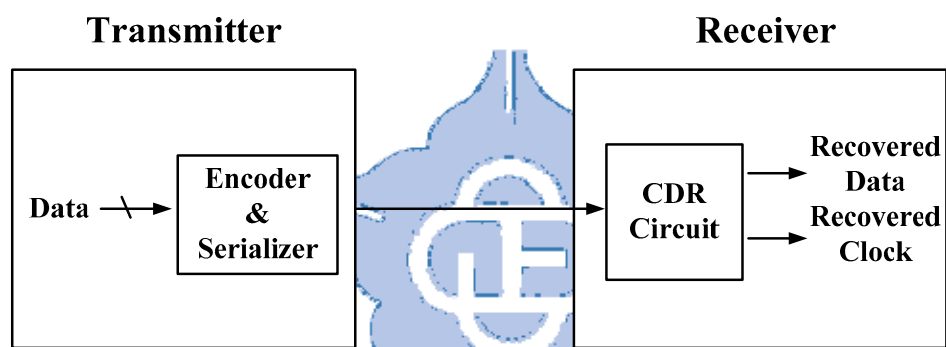


Fig 1.1 The role of CDR circuit in a communication system

Clock and data recovery circuit [8][9] is widely used in high speed serial data link communication system. In Fig. 1.1, the transceiver transmits the encoded serial data to the receiver. The CDR circuit in the receiver recovers the synchronization clock of the incoming serial data and then uses the recovered clock to retiming the received data pattern to as the recovered data.

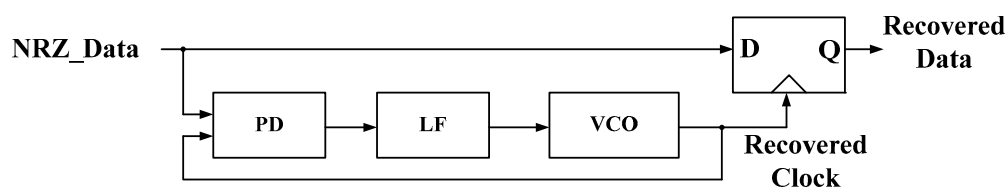


Fig 1.2 Basic example of PLL type CDR circuit

Conventionally, PLL architecture is usually used to construct the CDR circuit. Fig. 1.2 shows the basic architecture of PLL type CDR circuit. The PLL loop is composed of a phase detector (PD), a loop filter (LP), and the voltage controlled oscillator (VCO) to synchronize the VCO clock rate with the input data rate. The VCO clock triggers the D Flip/Flop (DFF) to sample the NRZ data and the input data is retimed as the recovered data. Fig. 1.3 shows the concept of the PLL type CDR circuit. The recovered clock's rising edge should be aligned with the input data transition and then we can sample the input data with its falling edge.

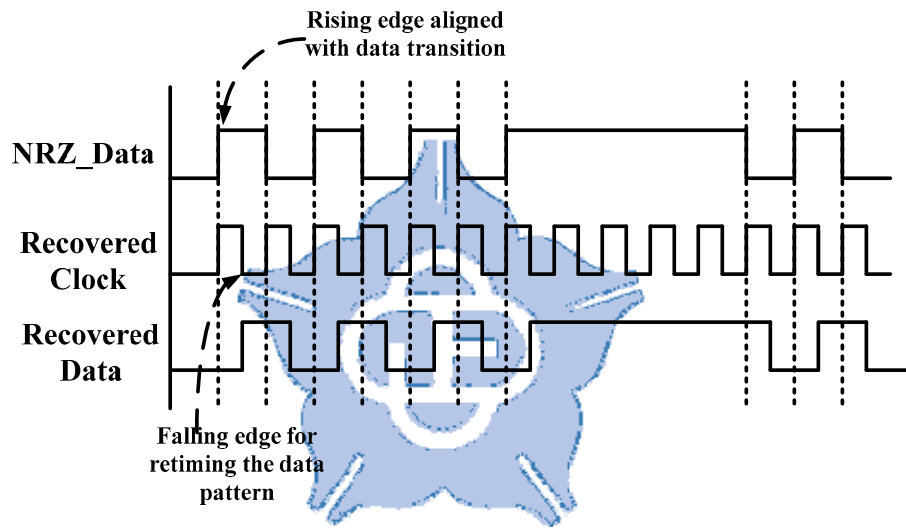


Fig 1.3 Waveform of basic PLL type CDR circuit

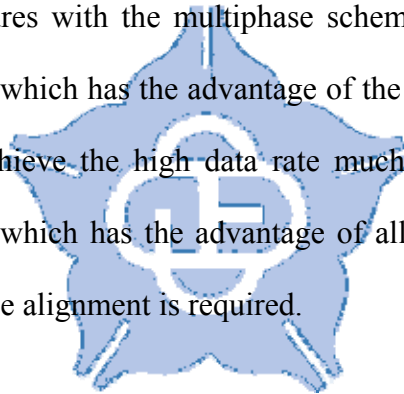
1.1.1.2 Phase Detector in CDR circuit

In order to make the CDR circuit is able to track the random data pattern, several phase detectors (PDs) for random data tracking are published. The linear type Hogge PD [30] and the bang bang type Alexander PD [31] is well-known. Other works like the PD for 3X over-sampling Eye-Tracking [7] or the half rate PD [18] for reduced-rate CDR circuit are proposed to achieve the novel CDR circuit.

1.1.2 Multiphase Scheme for CDR circuit

The traditional PLL type CDR circuit suffers the speed limitation of high speed data rate. In order to track the full rate data, the VCO clock frequency should be operated at a high data rate. Thus the power consumption and design complexity of VCO are increased. In addition, the traditional PLL type CDR circuit has the disadvantage of requiring a 50 % duty-cycle VCO output clock. If the VCO output clock is not the 50% duty cycle the performance of the CDR circuit will be degraded.

In order to overcome these problems and achieve the better performance of clock and data recovery, the multiphase over-sampling scheme is published [19][10]. There are two popular architectures with the multiphase scheme. One is the reduced rate oversampling CDR circuit which has the advantage of the reduced rate of VCO clock to save the power and achieve the high data rate much easier. The other is blind oversampling architecture which has the advantage of all digital nature and the fast lock-in time due to no phase alignment is required.



1.1.2.1 Reduced-rate oversampling CDR circuit

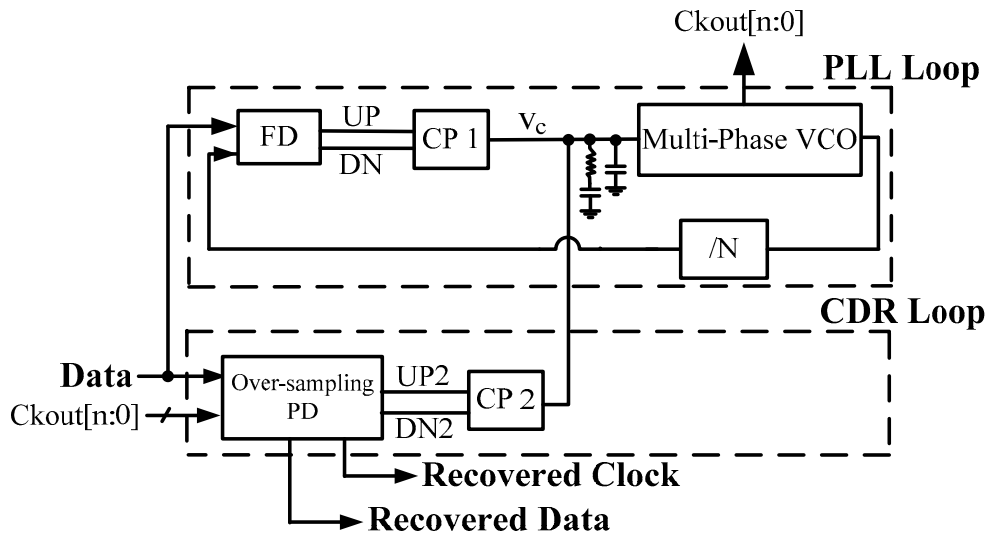


Fig 1.4 Architecture of reduced rate CDR circuit

Fig. 1.4 shows the example of the reduced rate over-sampling CDR circuit. There is a multi-phase VCO oscillates the reduced clock rate (usually half rate or quarter rate) by locking with the divided VCO clock and the data rate in the PLL Loop and generates the multi-phase clocks ($Ckout[n:0]$). The multi-phase clock is used to trigger the Multi-phase PD to generate the up/down pulse to charge/discharge the charge pump to adjust the multi-phase VCO output clock frequency and then output recovered data and recovered clock.

The advantage of this architecture is that the VCO clock is reduced to half or quarter of data rate to save the power consumption from the VCO. However, it suffers the problem of design complexity from multi-phase clock generation and over-sampling circuit.

1.1.2.2 Blind oversampling type CDR circuit

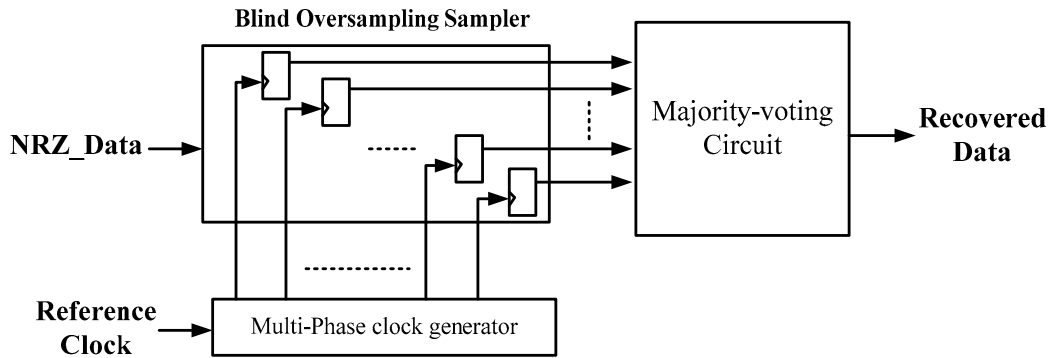


Fig 1.5 Architecture of blind oversampling circuit

Fig. 1.5 shows the example of the blind over-sampling circuit. The multi-phase clock generator's central clock is synchronized with the reference clock which relative to the input data. The multi-phase clocks trigger the blind over-sampling sampler to sample the input data (NRZ_Data). The multi-phase clock sample rate usually is 2X, 3X or 4X higher than data rate. The data sampled by the DFFs in the sampler will be sent to the decision circuit (Majority-voting Circuit) to pick up which data should be the recovered data.

The blind over-sampling architecture has the advantage of the all-digital nature and the short lock-in time, but it suffers the extra power consumption of multi-phase clock generator and usually needs the off-chip reference clock to generate the multi-phase clocks which the central frequency is close to the data rate.

1.1.3 Modern implementation of CDR circuit

1.1.3.1 Single rate CDR circuit

There are three modern implementation of CDR circuit. They are single rate, multi-rate and continuous rate CDR circuit. The single rate CDR circuit is designed for the single data rate. It is used for the specific application which operation speed is specified [2][6][7]. Because of the narrow operation range, the cost of the circuit and design complexity can be reduced. Besides, because of the specified operation speed, the external reference clock is usually used for frequency acquisition [1][3].

1.1.3.2 Multi-rate CDR circuit

The multi-rate CDR circuit has multiple operation speed. It's target for the application with multiple operation modes. The implementation of multi-rate CDR circuit by using multiple reference clocks with automatic bit rate selection is published [12]. However, the cost of multiple reference clock is large, so the architecture of a single external clock and multiple reference generation scheme is proposed in [13]. The other work which do not need a reference clock is presented [14].

1.1.3.3 Continuous rate CDR circuit

The nature of a continuous rate CDR circuit has a wide operation range. The input data rate can be any speed within the operation range [15][16][17][27].

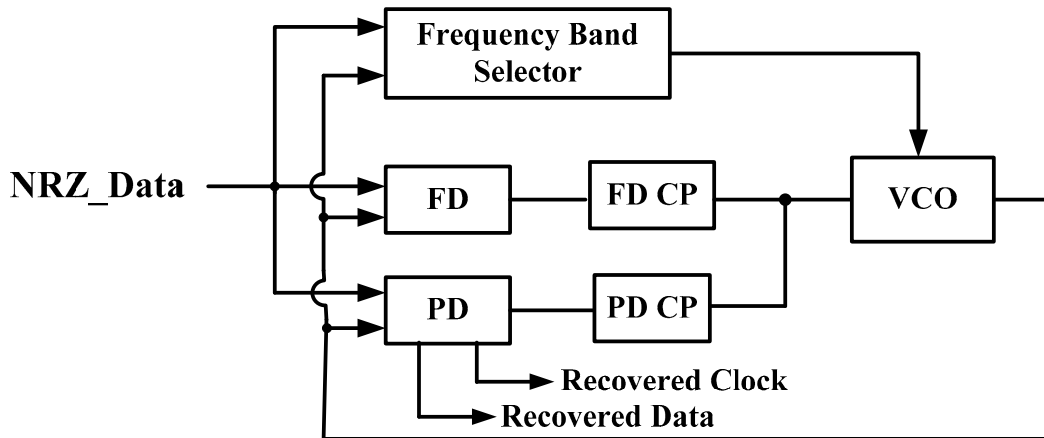


Fig 1.6 Example of continuous rate CDR circuit

Fig. 1.6 shows the example of the continuous rate CDR circuit. The continuous rate CDR circuit usually has the frequency band selector to select which the VCO frequency band is close to the input data rate to speed up the frequency acquisition. The FD is used for frequency tracking. The FD compares the VCO clock and input data rate then adjusts the high gain charge pump to adjust the VCO clock frequency coarsely and achieves the frequency acquisition. The PD is used to compare the VCO phase is leading or lagging to the data transition and adjust the lower gain charge pump to fine tune the VCO and maintain the phase alignment.

1.1.4 Referenceless issue of CDR circuit

An external off-chip reference clock is often needed in a PLL. Therefore, the PLL based CDR circuit [29] is often need the external reference clock. However, the off-chip reference clock increases the deign complexity of the system integration. Besides, the external reference clock has the cost of area occupation and power consumption. To overcome the problem of an external reference clock, the referenceless architecture is more attractive in today's system-on-a-chip era.

However, the referenceless design is usually suffered from the narrow operation range [21] and long lock-in time [22]. In this thesis, the proposed ADCDR can solve these problems.



1.2 Introduction to USB 2.0

1.2.1 USB 2.0 overview

Universal serial bus (USB) is the industrial standard for the communication between computer and electronic device. The USB 2.0 specification [5] is released in April 2000, and it defines the data transfer rate of “Low Speed” (1.5MHz), “Full Speed” (12MHz) and “High Speed” (480MHz).

As shown in Fig 1.7, the USB system specifications define the communication between USB host and USB device (function). There is only one USB host at any USB system. The USB host is used to control the whole communication flow. USB device could have hubs which provide additional attachment point to the USB or the functions which provide capabilities to the system such as a joystick or speakers.

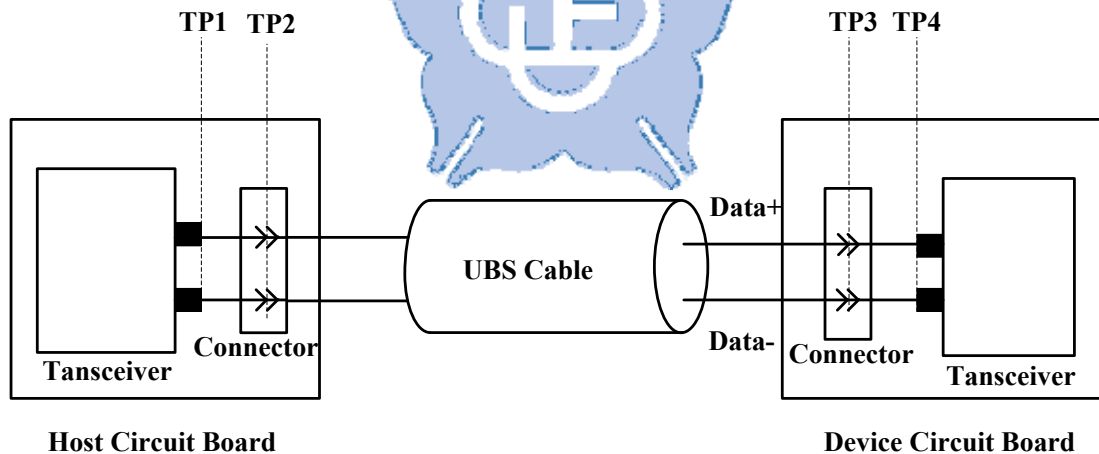


Fig 1.7 USB 2.0 interconnection between host and device

The data is transmitted on the USB cable by the differential signals (Data+ and Data-.) There are difference eye patterns (TP1 to TP4) defined by the USB 2.0 specification. The receiver sensitivity is defined as TP4 which is shown in Fig 1.9.

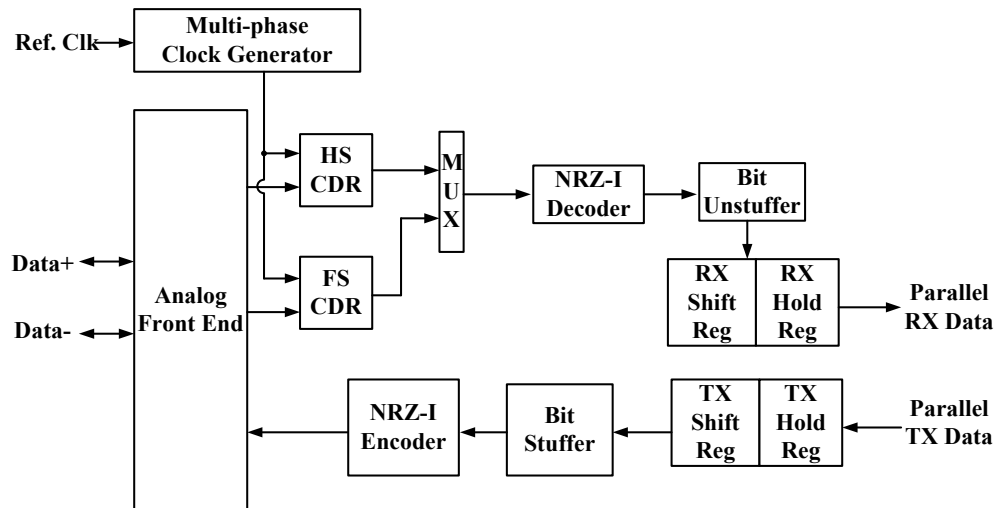


Fig 1.8 System diagram of UTMI

Fig. 1.8 shows the block diagram of the USB 2.0 Transceiver Macrocell Interface (UTMI) [4][23]. UTMI is a transceiver interface of the USB system shown in Fig. 1.7. The Data+ and Data- are the differential signals on the serial bus. The analog front end (Analog Front End) is used to exchange the differential signals with digital signals.

In the transmitter path, the host parallel data (Parallel TX Data) is serialized by the shift register and after bit stuffing and NRZ-I encoding, then is transmitted to the bus. In the receiver path, there are two CDR circuits in the UTMI, HS CDR is for the high speed mode (480MHz) and FS CDR is for the full speed mode (12MHz). Both CDR circuits are locking with the multi-phase reference clock and recover the data. After the NRZ-I decoding and bit unstuffing, the recovered data is sent to the shift register and outputted as the parallel data (Parallel RX Data).

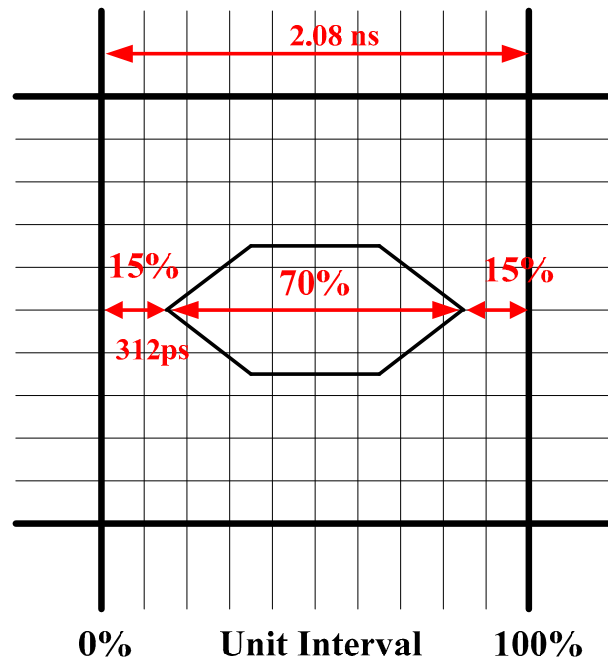


Fig 1.9 Receiver sensitivity requirement of USB 2.0 specification

Fig. 1.9 shows the eye pattern of receiver sensitivity in USB 2.0 high speed mode. The receiver sensitivity of input data should be 70% unit interval (312 ps peak to peak input data jitter) and recommend the BER of recovered data can be less than 10^{-12} .

1.2.2 USB 2.0 protocol layer

In USB 2.0 protocol layer, there are three types of packets: token packet, data packet, and handshake packet. Each transaction must be contained within these three types of packets. The format of these packets is shown in Fig. 1.10.

Token Packet

SYNC	PID 8bit	ADDR 7bit	ENDP 4bit	CRC5 5bit
------	-------------	--------------	--------------	--------------

Data Packet

SYNC	PID 8bit	Data 0-8192 bit	CRC16 16bit
------	-------------	--------------------	----------------

Handshake Packet

SYNC	PID 8bit
------	-------------

Fig 1.10 Packet format of USB 2.0

Each packet has the SYNC field, the length of the SYNC field is 32 bit for high speed mode and 7 bit for full/slow speed mode. The PID field is used to define each packet meaning. Table 1.1 shows PID types and detail functions. The Data field is the transmit data. The ADDR and ENDP field is used to address the device number. The CRC field is for error detection within the transaction. The example of the USB 2.0 transaction is shown in Fig. 1.11.

Table 1.1 PID Types

PID Type	PID Name	PID<3:0>*	Description
Token	OUT	0001B	host-to-function transaction.
	IN	1001B	function-to-host transaction.
	SOF	0101B	Start-of-Frame marker and frame number.
	SETUP	1101B	host-to-function transaction for SETUP to a control pipe.
Data	DATA 0	0011B	Data packet PID even.
	DATA 1	1011B	Data packet PID odd.
	DATA2	0111B	Data packet PID high-speed, high bandwidth isochronous transaction in a microframe.
	MDATA	1111B	Data packet PID high-speed for split and high bandwidth isochronous transactions.
Handshake	ACK	0010B	Receiver accepts error-free data packet.
	NAK	1010B	Receiving device cannot accept data or transmitting device cannot send data.
	STALL	1110B	Endpoint is halted or a control pipe request is not supported.
	NYET	0110B	No response yet from receiver.
Special	PRE	1100B	Host-issued preamble. Enables downstream bus traffic to low-speed devices.
	ERR	1100B	Split Transaction Error Handshake (reuses PRE value).
	SPLIT	1000B	High-speed Split Transaction Token.
	PING	0100B	High-speed flow control probe for a bulk/control Endpoint.
	Reserved	0000B	Reserved PID.

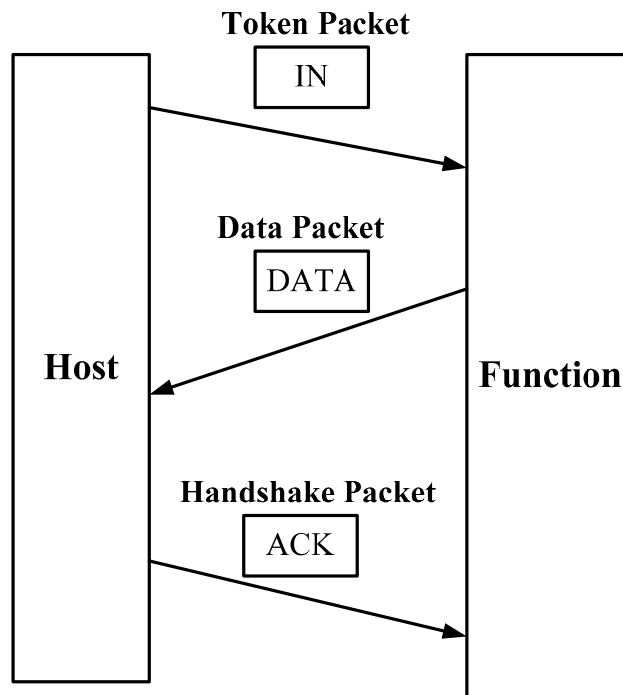


Fig1.11 Example of USB2.0 transaction

The Fig. 1.11 shows the sample example of USB 2.0 transaction. The host sends a token packet IN to request the data. The function receives the token packet and the function is now ready to do the data transmission. Then, the function starts to transmit the data packet. When the data packet is transmitted without error, the host will send a handshake packet ACK to the function and whole transmission is complete successfully.

1.3 Design challenges of CDR circuit in USB2.0

As the former description, before the packet transmit to the bus, the packet will be bit stuffed in any six consecutive “1” (Consecutive Identical Digit) to avoid a long period without data transition, then each bit is encoded with non-return to zero, inverted (NRZI) encoder. The NRZI signal has a transition if the bit being transmitted is “0”, and does not have a transition if the bit being transmitted is “1”. Finally, the packet is transmitted on the bus.

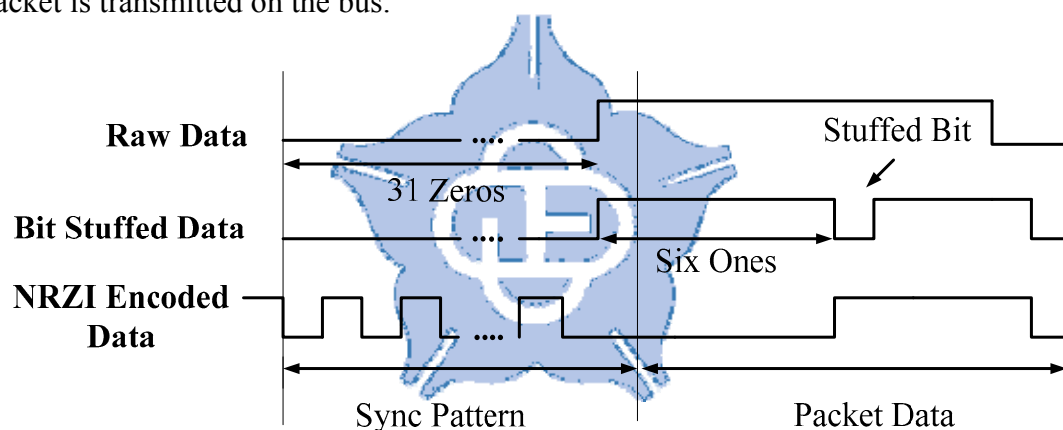


Fig 1.12 Waveform of USB 2.0 packet

Fig. 1.12 shows the encoded NRZI waveform of USB 2.0 packet, the first 32 bit is the SYNC field and after NRZI encoding, there are 31 continuous data transition in the SYNC pattern. That means the frequency and phase acquisition should be completed within the 31 cycles.

However, the conventional analog approaches have difficulty to satisfy this fast lock-in requirement. Because the charge pump type VCO loop suffers the problem of long unilateral frequency acquisition time. The Fig. 1.13 shows the locking procedure

of conventional analog approach frequency tracking. In the beginning, the VCO is discharged to the minimum frequency. In the coarse-tuning phase, the VCO would be charged with high gain charge pump to speed up the frequency acquisition. After frequency acquisition is completed. In the fine tuning phase the VCO is charged with low gain charge pump for the finer tracking, and then it achieves the phase acquisition. The lock-in time from the minimum frequency to the target frequency usually takes several micro seconds.

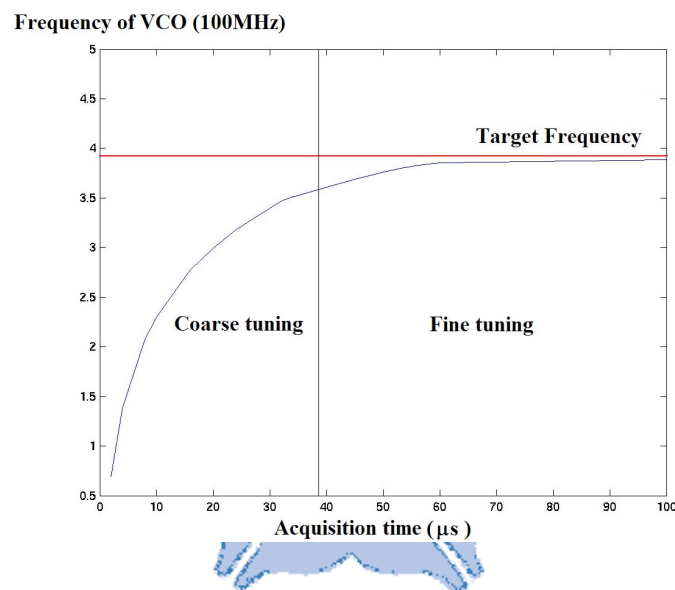


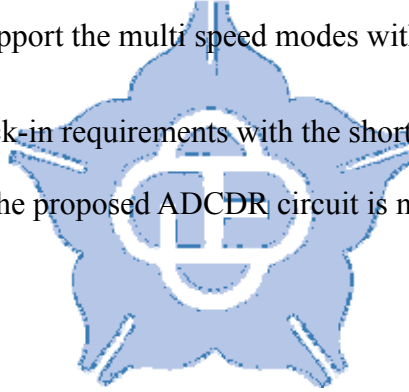
Fig 1.13 Tracking time of charge pump VCO loop

1.4 Summary

Due to the additional cost with an external reference clock and the multi-phase clock generation of over-sampling architecture, in this thesis, we design an ADCDR circuit without an external reference clock and over-sampling scheme. Thus the off-chip crystal and the multi-phase generator shown in Fig. 1.8 can be eliminated to save the power consumption and the area occupation.

In order to support three speed modes of USB 2.0 specification, we design an ADCDR circuit to the wide range continuous rate type CDR circuit. Therefore, instead of using multiple CDR circuits to support the multi speed modes of USB 2.0, our ADCDR circuit can support the multi speed modes with reduced hardware costs.

To satisfy the fast lock-in requirements with the short SYNC pattern of USB 2.0, the fast lock-in feature in the proposed ADCDR circuit is necessary.



Chapter 2 Referenceless CDR

Circuit for USB2.0 High Speed Mode

2.1 System Architecture Overview

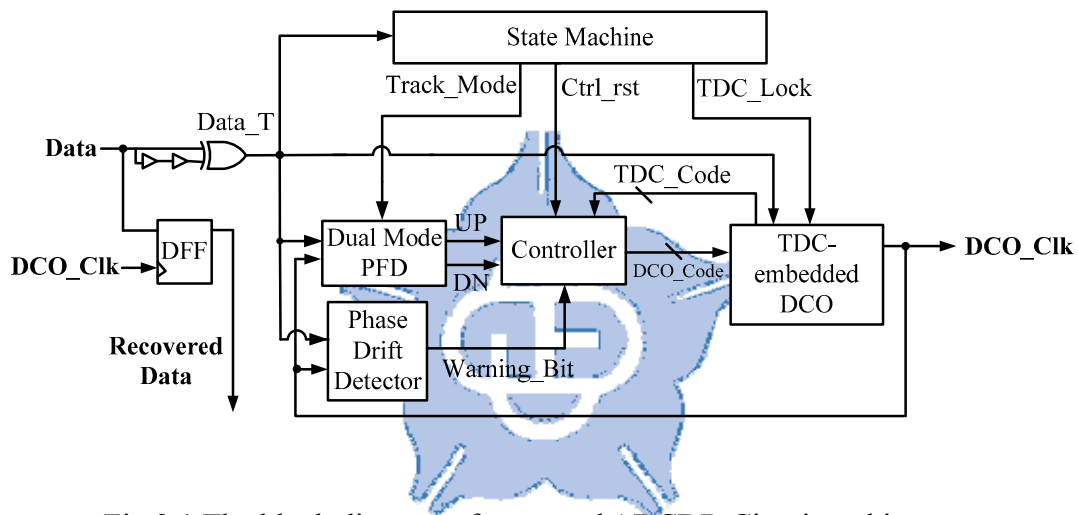


Fig 2.1 The block diagram of proposed ADCDR Circuit architecture

Fig. 2.1 shows the block diagram of proposed ADCDR Circuit architecture. The proposed ADCDR Circuit is composed of a dual mode phase frequency detector (PFD), a TDC-embedded digitally controlled oscillator (DCO), a phase drift detector, a CDR Controller (Controller), and a lock-in procedure control state machine (State Machine).

The data transition (**Data_T**) is extracted from the delayed input data and exclusive-OR with the original input data. Every data transition of input data would generate a small pulse shown as Fig. 2.2.

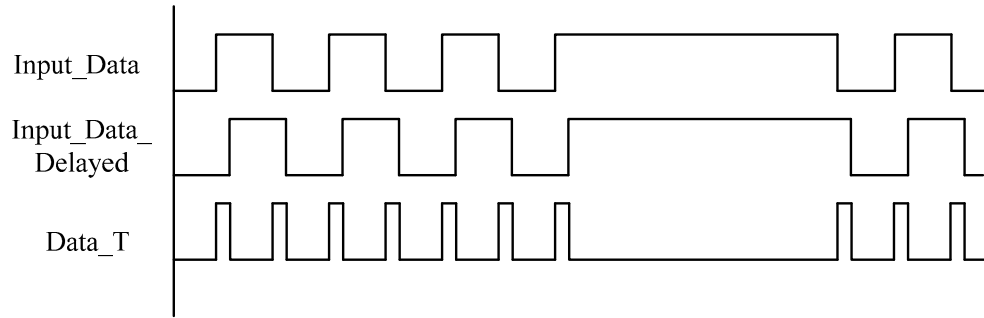


Fig 2.2 The waveform of data transition extraction

The lock-in procedure control state machine triggered by the Data_T is used to control the whole lock-in procedure.

The whole lock-in procedure has three phases: TDC-locking phase, coarse-tuning phase and fine-tuning phase. In the TDC-locking phase, the period of the first two data transition (Data_T) will be measured by TDC-embedded DCO and then it generates the TDC_Code. The TDC_Code is encoded as the Initial DCO_Code in the Controller. After this phase, the DCO output frequency (DCO_Clk) would be very close to the input data rate.

After TDC-locking phase the state machine would turn off the TDC function to save power by setting the TDC_lock signal to “1”. Then it enters the coarse-tuning phase within the SYNC patterns. In coarse-tuning phase, state machine sets the operating mode of dual mode PFD by setting signal Track_Mode to “1”. In this mode, the dual mode PFD works as the common PFD. In this mode, the PFD compares the frequency between DCO output clock (DCO_Clk) and data transition signal (Data_T) which is the input data rate. When DCO output clock (DCO_CLK) is faster than input data rate, the UP signal is generated. Then the controller reduces the DCO_Code to slow down the DCO output clock. Otherwise, if DCO output clock is slower than input data rate, the DN signal is generated. Then the controller would increase the

DCO_Code to speed up the DCO output clock. In coarse-tuning phase the DCO output clock is adjusted with the coarse-tuning cells to speed up the lock-in time.

After two phase polarity changes of UP and DN signals in the coarse-tuning phase, the state machine switches the CDR circuit to the fine-tuning phase. In this phase, the dual mode PFD is switched to the PD mode by setting the Track_Mode signal to “0”. The dual mode PFD can generate the correct UP/DN signals to tracking the random data. In addition, the DCO output clock would be adjusted with fine-tuning cells to achieve finer tuning. So that the CDR circuit can keep the phase alignment between the DCO output clock and the data transition until the end of packet.



2.2 Dual Mode Phase and Frequency Detector

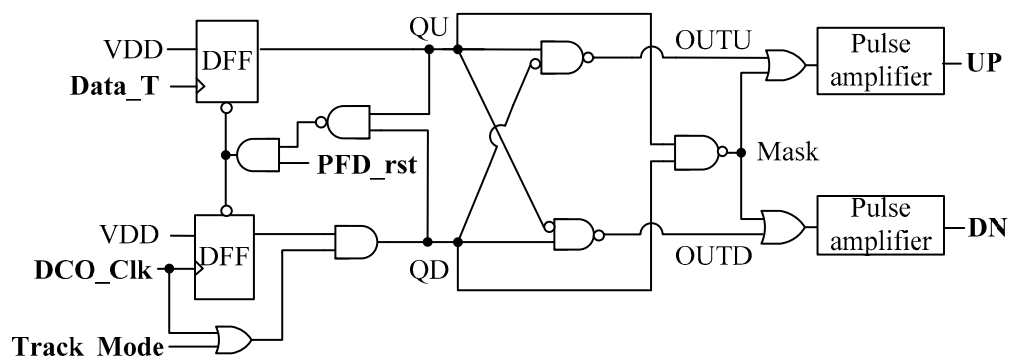


Fig 2.3 Proposed dual mode PFD architecture

Fig. 2.3 shows the proposed dual mode PFD architecture. It supports two tracking mode to achieve the frequency and phase acquisition with the USB 2.0 packet format.

When the Track_Mode is setting to “1”, the proposed dual mode PFD is in the PFD mode. In this mode it works just like other common conventional Bang-Bang PFDs to achieve frequency tracking within the SYNC pattern. If frequency of the DCO output clock (DCO_Clk) is faster/slower than the input data rate, then the proposed dual mode PFD outputs the UP/DN signal to the CDR controller to adjust the frequency of the DCO output clock. The waveform of PFD mode is shown in the left side of Fig 2.4

When the Track_Mode is setting to “0”, the proposed dual mode PFD is switched to the PD mode. In this mode, it can be used to achieve the phase acquisition with the random data pattern of the USB2.0 packet.

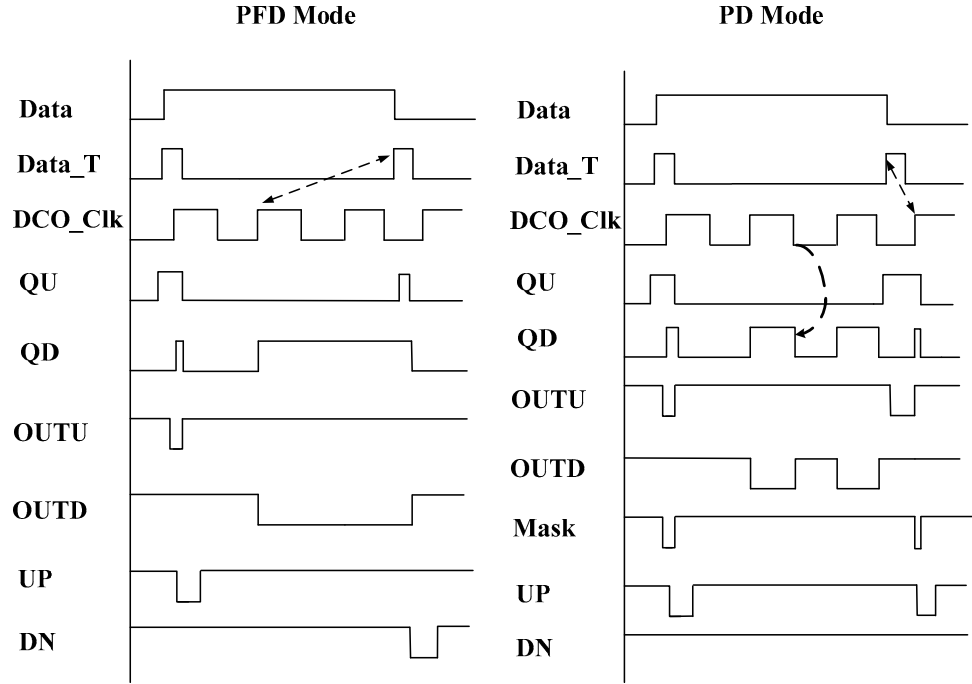


Fig 2.4 Waveform of the proposed dual mode PFD

In the right side of Fig. 2.4, QD reset by the negative edge of DCO_Clk, that means if there is no data transition arrives within the half period of the DCO_Clk, the comparison of this time is discarded. Furthermore, because of the reset of QD, there is an irregular down pulse of OUTD is generated, and thus if constructs the irregular UP/DN signals. The mask signal is created by the NAND operation between QU and QD. So that the irregular down pulse of OUTD can be masked by the AND operation, and PFD can remain output the correct UP/DN signal.

2.3 Time-to-Digital Converter

Embedded DCO

2.3.1 Structure

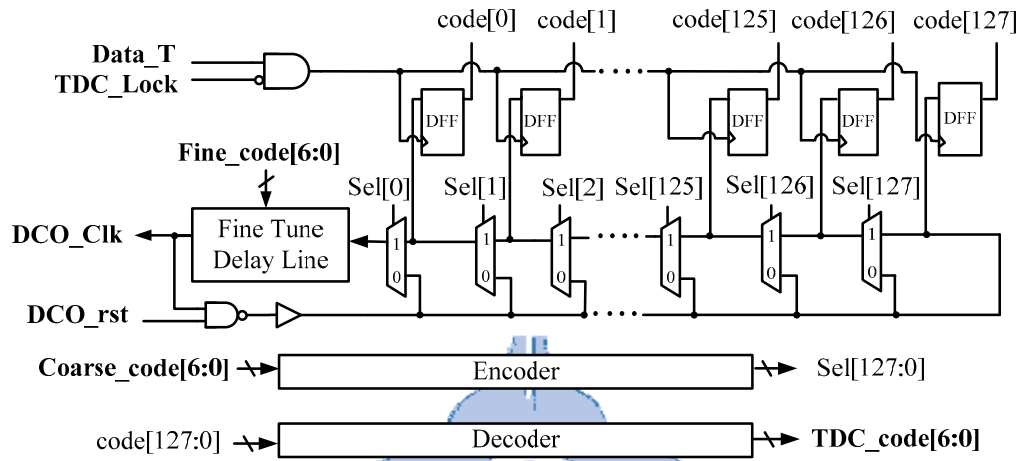


Fig 2.5 The TDC-embedded DCO architecture

As shown in Fig. 2.5 is shown, the TDC-embedded DCO is constructed by DCO part and TDC part. The DCO part is a ring type DCO constructed by a coarse-tuning delay line and the fine-tuning delay line. The coarse-tuning delay line composed with the chain of 2-to1 multiplexers (MUXs). The fine-tuning delay line which is composed with the digital-controlled varactors (DCV) [11][20][24][26] to achieve the finer resolution. The TDC part is constructed by deploying the D-Flip/Flops (DFFs) on every node between any two MUXs. The Decoder decodes the 128-bit thermal meter code to the 7-bit binary TDC_code and outputs to the CDR controller. The Encoder encodes the input 7-bit code from the CDR controller's 7-bit control code to the 128 bit DCO code (Sel[127:0]) to adjust the DCO output clock (DCO_Clk).

2.3.2 MUX Type DCO structure

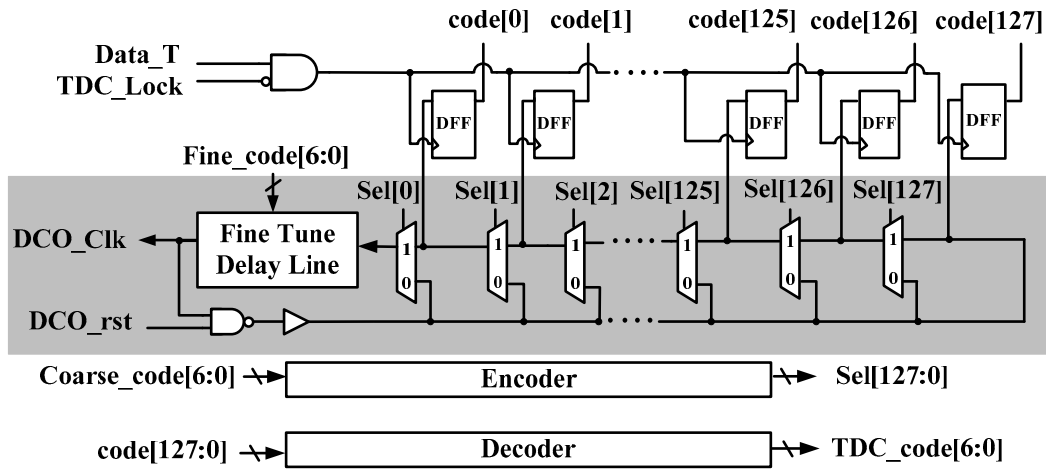


Fig 2.6 DCO part of proposed TDC-embedded DCO

The gray region in Fig. 2.6 is the DCO part of the proposed TDC-embedded DCO. In the proposed ADCDR circuit, there are 127 cascaded MUXs as the coarse-tuning delay line. The Coarse_code[6:0] is the digital dco code output from CDR controller. After encoding, Coarse_code[6:0] is encoded to Sel[127:0] to select the delay path to control the DCO output clock (DCO_Clk). As shown in Fig. 2.7, after encoding the Coarse_code “125”, the Sel[125] is setting to “0”, the others are setting to “1”, then the delay path is passing through 125 MUXs. The resolution of the coarse-tuning delay line is about 34ps.

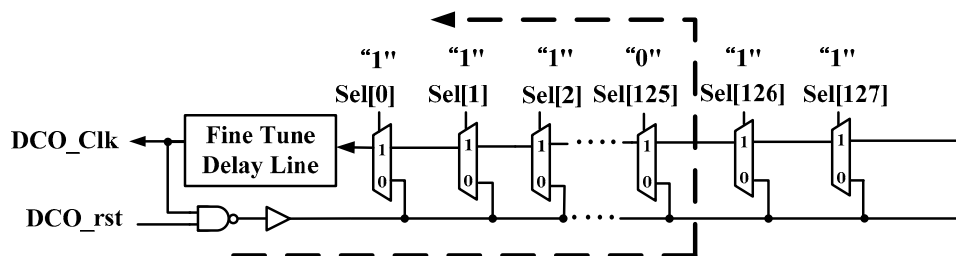


Fig 2.7 Delay path selection of proposed MUX Type DCO

2.3.3 DCV fine-tune delay line

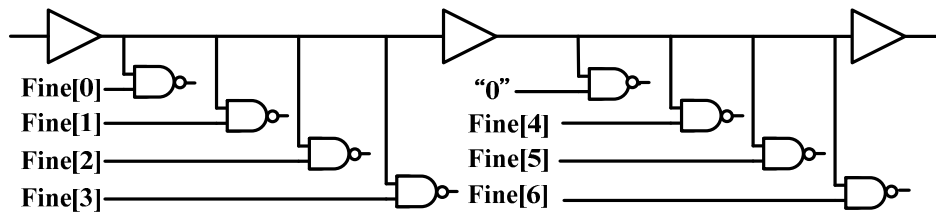


Fig 2.8 The fine-tune delay line of proposed MUX Type DCO

Fig. 2.8 shows the architecture of fine-tuning delay line of the proposed MUX Type DCO. To achieve a finer resolution, the digital-controlled varactors (DCVs) [11] are used. In proposed ADCDR circuit, the thermal meter code Fine[6:0] controls the nodal capacitance between each two buffers to adjust the delay timing on the delay line. This architecture can achieve a high resolution to about 8ps, and total delay range is about 56ps that can cover the one step of coarse-tuning delay line.

2.3.4 Time-to-Digital Converter

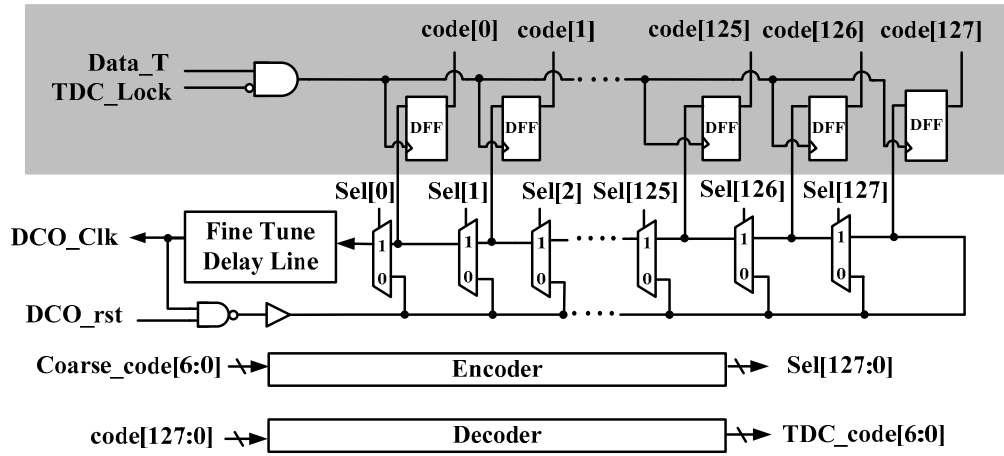


Fig 2.9 The TDC part of proposed TDC-embedded DCO

The gray region of Fig. 2.9 is the TDC part of proposed TDC-embedded DCO. When TDC_Lock is setting to “0” the small pulse (Data_T) which generated from data transition would trigger the DFFs deployed on the DCO delay line to quantize the data rate of input data to a digital code to achieve the fast frequency acquisition.

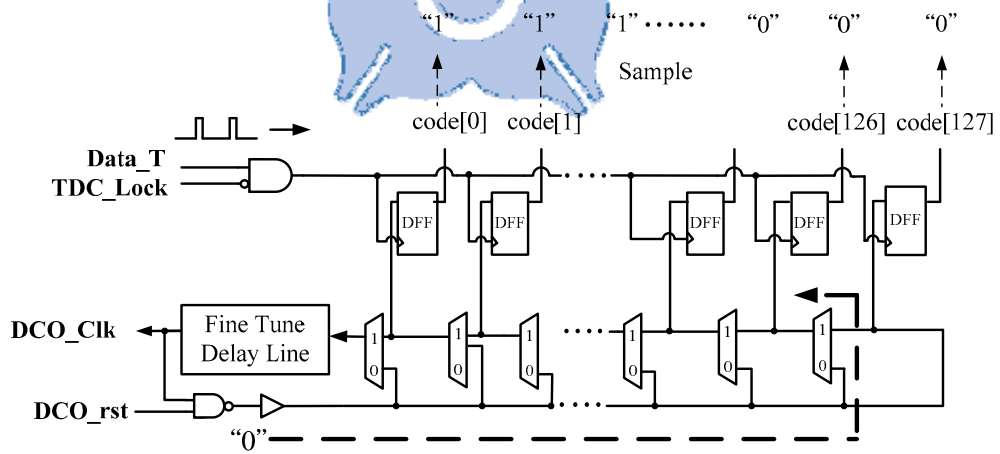


Fig 2.10 Operation of TDC-embedded DCO

Fig. 2.10 shows the operation of proposed TDC-embedded DCO. When the CDR is reset, DCO_rst is “0”. In addition, in the beginning, the coarse-tuning code is set to the maximum value to select the longest delay path of the delay line in the beginning. Then, when the first positive edge of the small pulse of the data transition

arrives, the DCO_rst is setting to “1” by the state machine. Then the “0” is beginning pass through the delay line. When the second positive edge of the small pulse of the data transition arrives, the DFFs are triggered to sample the value on the delay line. The number of “0” which the DFFs sampled is the number of the MUXs that the “0” pass through during the period of one bit time. After encoding the TDC code, the value would be the initial value of DCO_code so that the initial DCO clock frequency could be very close to the input data rate to speed up the frequency acquisition within the short SYNC pattern in USB 2.0. Finally, when the TDC measurement is finish, the TDC_lock is setting to “1” to turn off the TDC to save power.



2.4 Adaptive Gain in Consecutive Identical Digit

In the region of Consecutive identical digit (CID) the PD is not operating. Thus, there is no frequency adjustment in this region. The frequency error between DCO output clock (DCO_Clk) and input data rate (Data_T) will accumulate phase error and causing the phase drift and the data recovery error. The Fig. 2.11 shows the example. If the initial frequency is $\Delta P1$ and the period difference between data transition (Data_T) and DCO output clock (DCO_Clk) is X . In the right side of Fig. 2.11, we turn off the frequency tracking. The phase error is accumulated with period difference X in each cycle. After 3 cycles, the phase error is increase to $\Delta P1 + 3X$. In 3 consecutive identical digits region, the quantity of phase error is the same as turn off the frequency tracking for 3 cycles shown as the left side of Fig. 2.11

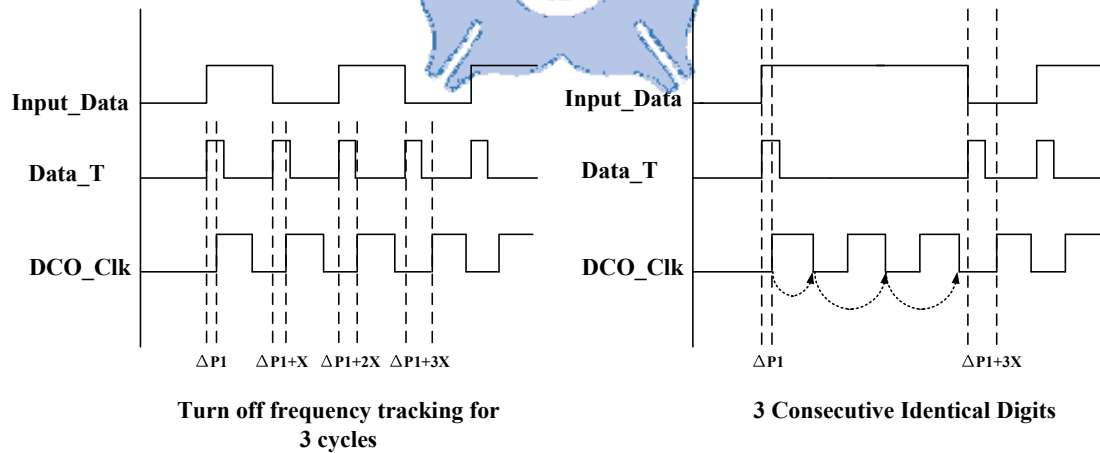


Fig 2.11 Phase error accumulation

To solve the problem of data recovery error from phase error accumulation, we proposed a tracking scheme of adaptive gain in consecutive identical digit (AGCID) in the CDR controller. We count the number of negative edge between any data

transition. The value of the counter will be used to increase the gain of the DCO clock frequency adjustment. As shown in Fig. 2.12, in the first of comparison between Data_T and DCO_Clk, Data_T is leading DCO_Clk and DCO_code is reduced with one step. Then, after the 3 consecutive identical digits, the Data_T is still leading DCO_Clk and DCO_code is reduced with a increased gain of 3*step.

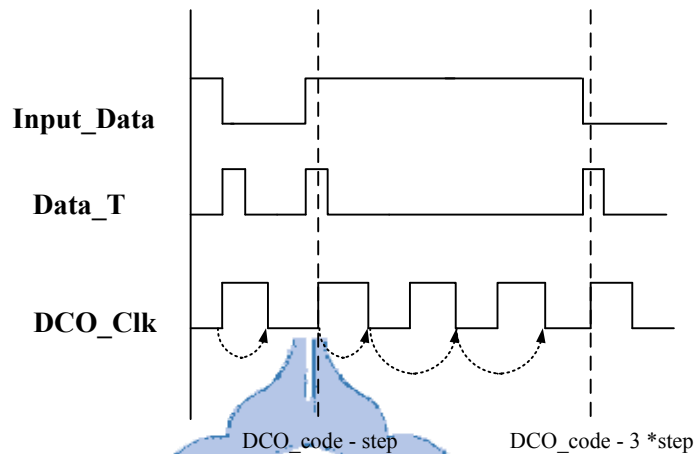


Fig 2.12 Increased gain in the 3 consecutive identical digit

Chapter 3 Wide Range Improvement of Supporting USB2.0 Full/Low Speed Mode

3.1 System Architecture with Wide Operating Range Improvement

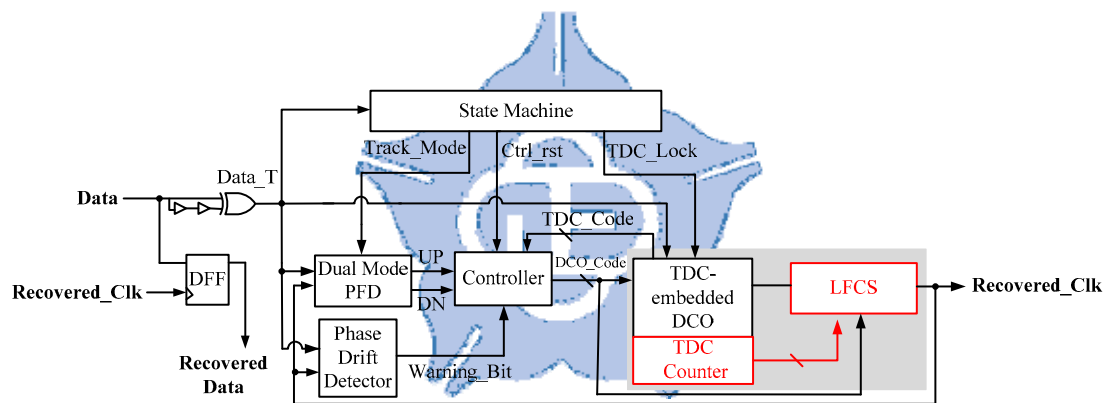


Fig 3.1 System architecture of wide operation range improvement

Fig. 3.1 shows the system architecture of the second version of CDR circuit proposed in this thesis. The CDR circuit of previous version only supports the single operating rate of USB 2.0 at high speed mode. In the second version, it has the improvement of wide operating range from 700kHz to 500MHz that can cover all speed mode (High Speed, Full Speed and Low Speed mode) of the USB 2.0 specification.

There are two added components in 2nd version of proposed ADCDR circuit, the low frequency clock synthesizer (LFCS) to achieve the low area cost and wide operation range, and the TDC Counter combined with the TDC-embedded DCO to achieve the wide range TDC measurement.



3.2 Wide Range Cyclic TDC-embedded DCO

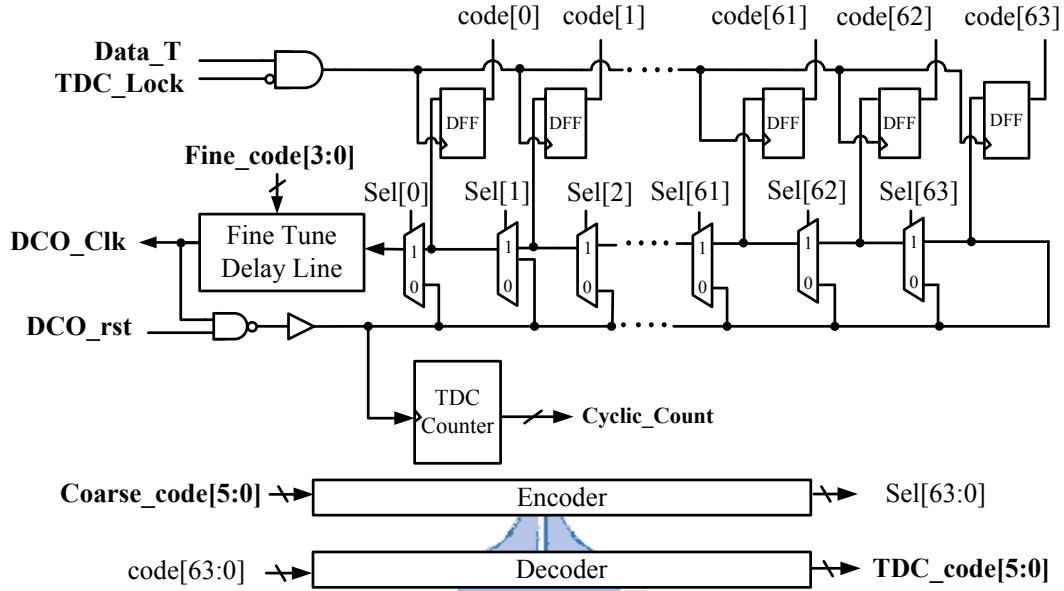


Fig 3.2 Proposed wide range cyclic TDC-embedded DCO architecture

The proposed wide range cyclic TDC-embedded DCO architecture is almost the same with the former version except the number of MUXs and DFFs is reduced to 63 to save the chip area occupation, and there is an additional counter (TDC Counter) connected on the DCO, and it is used to achieve the wide range TDC measurement.

The difficulty of wide range TDC implementation is the number of DFFs is not enough to quantize the long pulse width. To achieve the wide range TDC, the cyclic concept is combined into the original TDC-embedded DCO. The TDC measurement is completed within the first two data transition (Data_T). When the first positive edge comes, the “0” beginning pass through the delay. If the input data rate is slower than the minimum DCO frequency, then the “0” will pass through the entire delay line and DCO begin oscillating. The TDC Counter deployed on the DCO is trigger by the negative edge. Then, when the second positive edge arrives, DFFs samples the

remained digit on the delay line which can not reach to trigger the TDC Counter. Then TDC measurement is completed. The TDC measurement result is separated to two parts, Cyclic_Count which output from TDC Counter and TDC_code which encoded from DFFs' value (code[63:0]).

Assume that “ K ” is the value of Cyclic_Count, “ M ” is the value of the TDC code, T_f is the delay of fine-tuning delay line (Fine Tune Delay Line), and T_{mux} is a delay time of unit MUX. The input data rate can be quantized to two cases:

If LSB of code[63:0] is “0”

$$DataRate = (K - 1) * (128T_{mux} + 2T_f) + (64T_{mux} + T_f) + M * T_{mux} \quad (3.1)$$

If LSB of code[63:0] is “1”

$$DataRate = (K - 1) * (128T_{mux} + 2T_f) + 2 * (64T_{mux} + T_f) + M * T_{mux} \quad (3.2)$$

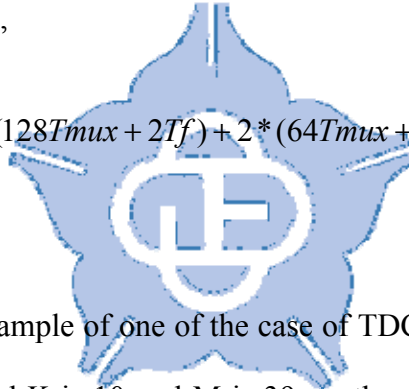


Fig. 3.3 shows the example of one of the case of TDC measurement. In this case the LSB of code is “0” and K is 10 and M is 39, so the proposed TDC quantize the period of two data transition to the delay of

$$9 * (128 + 2T_f) + 2 * (64T_{mux} + T_f) + 39T_{mux}.$$

Fig. 3.4 shows the other case of TDC measurement. In this case the LSB of code is “1” and the K is still 10 and M is 52. That the proposed TDC quantize the period of two data transition to the delay of

$$9 * (128 + 2T_f) + 64T_{mux} + T_f + 52T_{mux}.$$

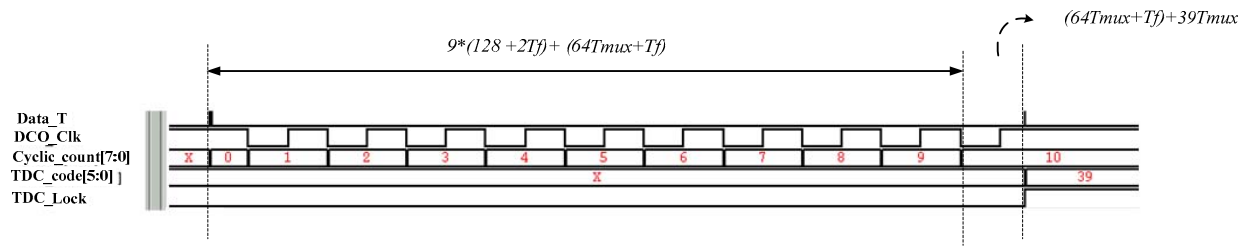


Fig 3.3 Operation waveform of proposed cyclic TDC-embedded DCO

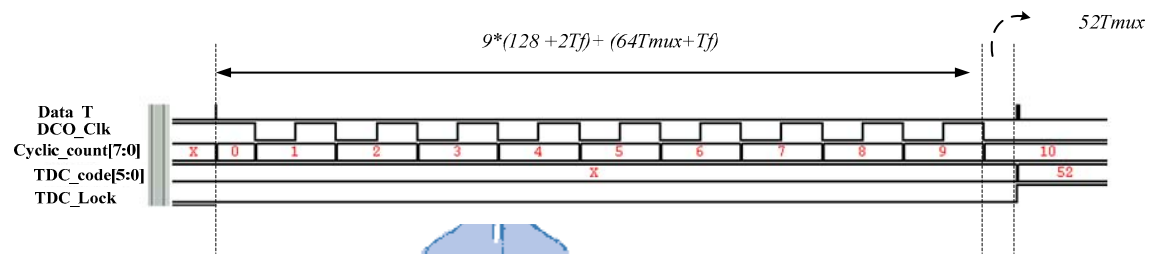


Fig 3.4 Another case of TDC measurement

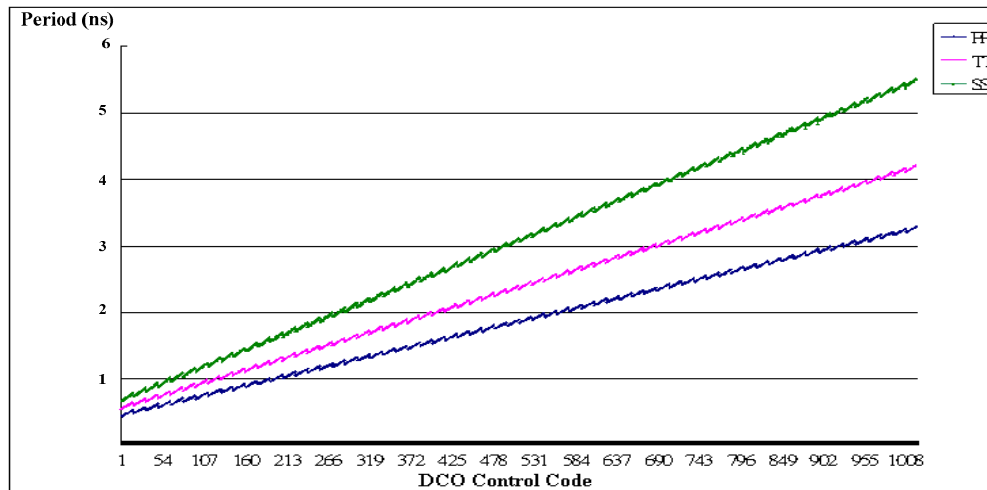


Fig 3.5 DCO delay line simulation with PVT variations

Table 3.1 Coarse/Fine stage range and step in PVT variations

PVT corner	Slow Case		Typical Case		Fast Case	
	Step	Range	Step	Range	Step	Range
Coarse tune stage	68 ps	4854 ps	52 ps	3665 ps	57 ps	2850 ps
Fine tune stage	7.6 ps	124 ps	6.8 ps	103 ps	5.9 ps	89 ps

Fig. 3.5 shows the DCO delay line of the Cyclic TDC-embedded DCO's control code versus period simulation with PVT variations, and the range and step of each stage is shown in Table 3.1.

3.3 Low Frequency Clock Synthesizer

3.3.1 Cyclic Delay of low frequency clock

synthesization

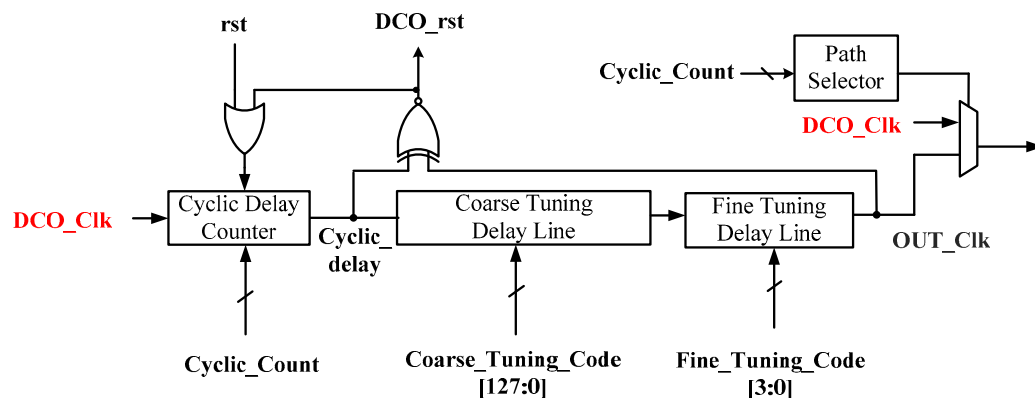


Fig 3.6 The proposed low frequency clock synthesizer architecture

Fig. 3.6 shows the proposed low frequency clock synthesizer (LFCS). There is a Cyclic Delay Counter triggered by DCO_Clk as the cyclic delay cell and output the Cyclic_delay signal. The Cyclic_delay passes through the Coarse Tuning Delay Line and Fine Tuning Delay Line and generates the output clock (OUT_Clk). Therefore, by combining the delay of the cyclic delay and the coarse and fine delay line's delay, the low frequency clock can be synthesized. The Path Selector can choose which path should be select to be a recovery clock (Recovery_Clk). Because if the input data rate which is faster than the minimum frequency of the DCO_Clk, that the LFCS is not necessary. Then the DCO_Clk is output as the recovery clock directly.

The proposed LFCS can use the TDC measurement result to set the initialization output clock (Recovery_Clk) which is very close to the target data rate and can achieve the fast frequency acquisition. As the former description, the input data rate is quantized as the (3.1) and (3.2). So the recovery clock period should be:

$$\text{Recovered_Clock} = (K - 1) * (64T_{\text{mux}} + T_f) + (32T_{\text{mux}} + T_f / 2) + M * T_{\text{mux}} / 2 \quad (3.3)$$

or

$$\text{Recovered_Clock} = (K - 1) * (64T_{\text{mux}} + T_f) + 2 * (32T_{\text{mux}} + T_f / 2) + M * T_{\text{mux}} / 2 \quad (3.4)$$

Fig. 3.7 shows the waveform of low frequency clock synthesization. The Cyclic Delay Counter generates the transition of Cyclic_delay for X delay time. The DCO_rst which is constructed by the operation XNOR between Cyclic_delay, and the low pulse of the DCO_rst can reset and restart the DCO within several periods. Assume Y is the low pulse of DCO_rst, that we can adjust the Coarse_Tuning_Code and Fine_Tuning_Code to adjust its width and adjust the OUT_Clk period. Then the period of OUT_Clk can be synthesized to X+Y.

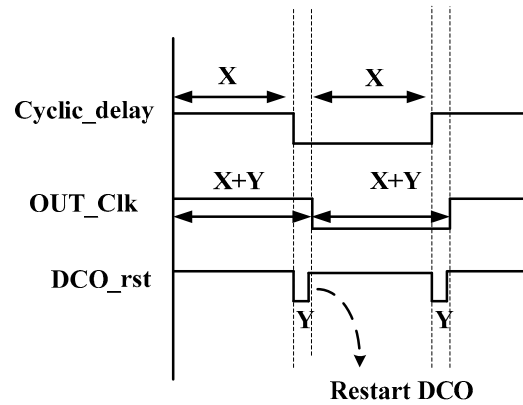


Fig 3.7 Waveform of low frequency clock synthesize

Assume that the Cyclic TDC-embedded DCO output value Cyclic_count is K and TDC_code is M , T_{mux} is the unit delay of MUX, and T_f is the delay of fine-tuning delay line. In the operation of low frequency clock synthesis, the period of DCO_Clk is setting to half of the maximum period. Therefore, when the Cyclic Delay Counter is counting to K , a transition of Cyclic_delay signal is generated, then the delay time of X can be:

$$X = (k - 1) * (64T_{mux} + T_f) + 32T_{mux} + T_f / 2 \quad (3.5)$$

Then the value of the $M/2$ or $M/2+32$ is used to be the $\text{Coarse_Tuning_Code}$, and the delay time of Y can be:

$$Y = M * T_{mux} / 2 + T_f \quad (3.6)$$

or

$$Y = 32T_{mux} + M * T_{mux} / 2 + T_f \quad (3.7)$$

The period of OUT_Clk ($X+Y$) can be:

If LSB of code[63:0] is “0”:

$$X + Y = (K - 1) * (64T_{mux} + T_f) + 32T_{mux} + M * T_{mux} / 2 + 1.5 * T_f \quad (3.8)$$

If LSB of code[63:0] is “1”:

$$X + Y = (K - 1) * (64T_{mux} + T_f) + 64T_{mux} + M * T_{mux} / 2 + 1.5 * T_f \quad (3.9)$$

Finally, the OUT_Clk initial output clock frequency can be close to the input data rate to achieve the fast frequency acquisition. In addition, there is a little mismatch between (3.8) and (3.3). The mismatch also appears between (3.9) and (3.4). However, the mismatch is quite small enough that can be eliminated with the flowing frequency tracking of the lock-in procedure easily.

3.3.2 Fast Reset Scheme on DCO

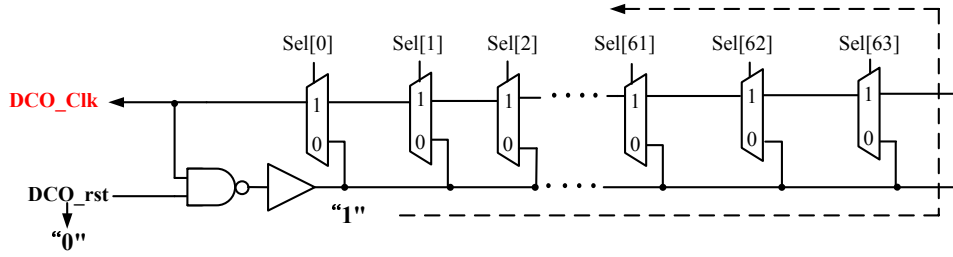


Fig 3.8 Long reset time for original DCO architecture

Because the proposed LFCS has the requirement of short reset time for the DCO. So the DCO with fast reset scheme is proposed, and it will not worsen the resolution of delay line. This architecture is combined into the Cyclic TDC-embedded DCO.

The conventional work like is shown in Fig. 3.8 shows. When the DCO_rst is setting to “0”, the reset time that value “1” reach DCO_Clk is the half of the period relative with current control code. It spend a lot of time to wait the value “1” pass through the delay line in the conventional architecture.

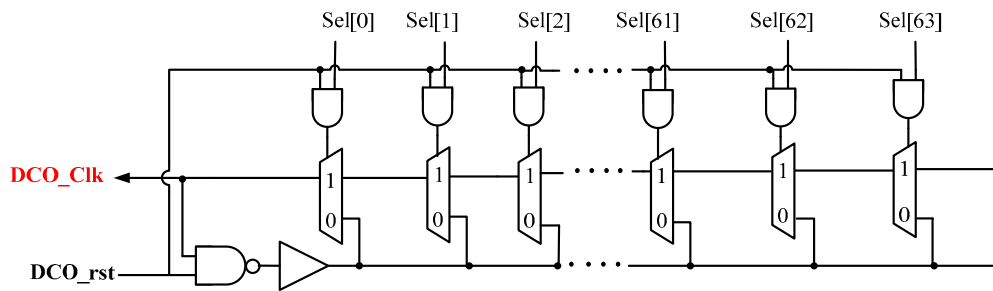


Fig 3.9 Fast Reset DCO architecture

Therefore, in this paper we proposed a fast reset scheme that is not need waiting for the reset signal pass through the delay line. Fig. 3.9 shows the proposed fast reset scheme implemented on the DCO part of TDC-embedded DCO.

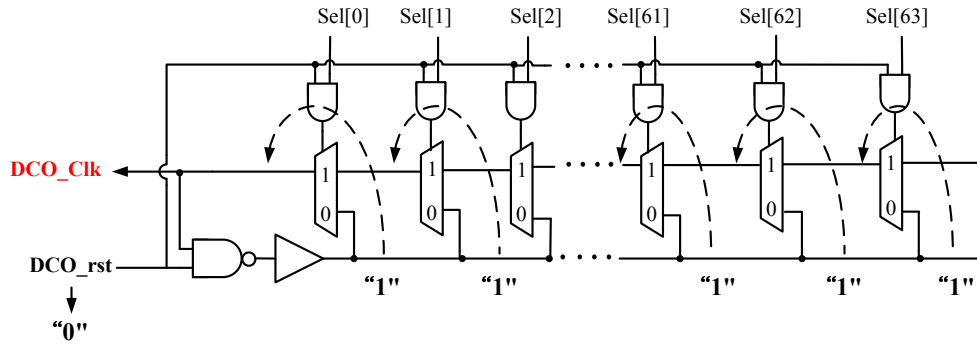
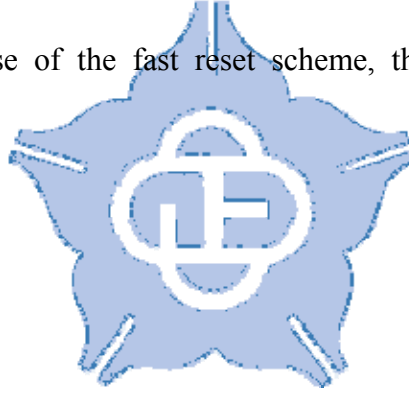


Fig 3.10 Operation of fast reset scheme

Fig. 3.10 shows the operation of the fast reset scheme. When the reset signal (DCO_rst) is setting to “0”, then the output node of the NAND gate is setting to “1”. In addition, the MUXs are enforced to select the path which the value “1” can pass through to their output. So that the fast reset scheme can reset the DCO entire delay line very quickly. Because of the fast reset scheme, the proposed LFCS can be achieved.



Chapter 4 Experimental Results

4.1 Test Chip Implementation

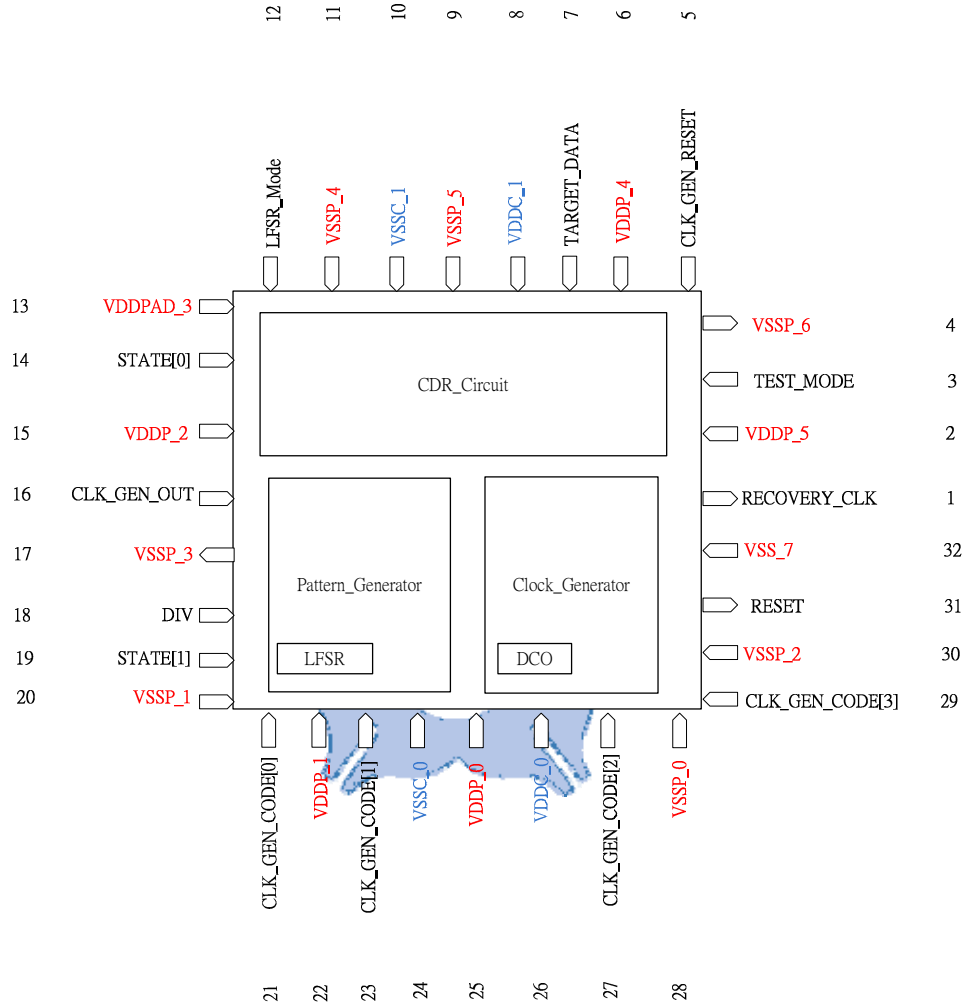


Fig 4.1 Test chip floorplaning and I/O planning

Fig. 4.1 shows the proposed ADCDR circuit floorplaning and I/O planning. There are 14 I/O PADs and 18 power PADs. The detail I/O description is shown in Table 4.1. The test chip contains the first version of the proposed ADCDR circuit and there is a on-chip clock generator (Clock_Generator) to generate the 480MHz clock to trigger the pattern generator (Pattern_Generator) and output the USB 2.0 format data

pattern to the proposed ADCDR circuit. The clock generator which implemented with the DCO has the range of 300MHz to 500MHz to cover the USB2.0 high speed mode operation frequency (480MHz), and the DCO is controlled by the off-chip input (CLK_GEN_CODE[3:0]) that can adjust the clock generator output clock coarsely. The pattern generator (Pattern_Generator) generates the 32 bit SYNC pattern and data pattern with stuff bit in every 6 consecutive identical digits data by using the linear feedback shift register (LFSR) with 2^7-1 pseudo random binary sequence (PRBS).

Table 4.1 I/O PADs discription

Output	Bits	Function	
CLK_GEN_OUT	1 bit	Clock of USB 2.0 data pattern generator	
RECOVERY_CLK	1 bit	CDR Circuit recovery clock	
STATE	2 bit	State of Circuit Condition	
TARGET_DATA	1 bit	CDR Circuit's input data generated by USB 2.0 data pattern generator	
Input	Bits	Function	
CLK_GEN_CODE	4 bit	Adjust the on chip clock generator to 480MHz clock provide to USB 2.0 data pattern generator	
LFSR_MODE	1 bit	Value	Mode
		0	Normal Case
		1	Worst Case
TEST_MODE	1 bit	0	Output the CLK_GEN_OUT and RECOVERY_CLK
		1	Output the RECOVERY_CLK and TARGET_DATA
DIV	1bit	0	Output normal RECOVERY_CLK
		1	Output RECOVERY_CLK/8
RESET	1 bit	System reset	
CLK_GEN_RESET	1 bit	On chip clock generator reset	

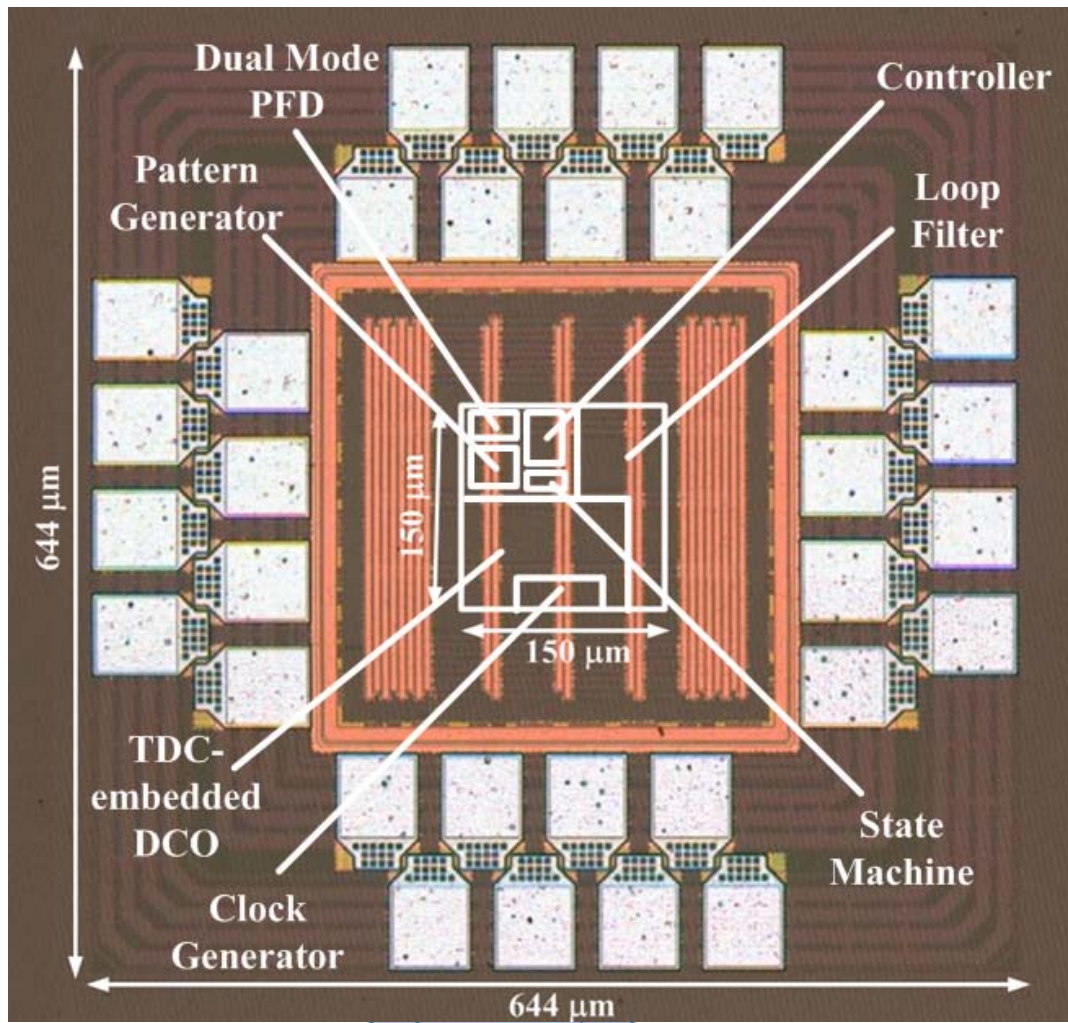
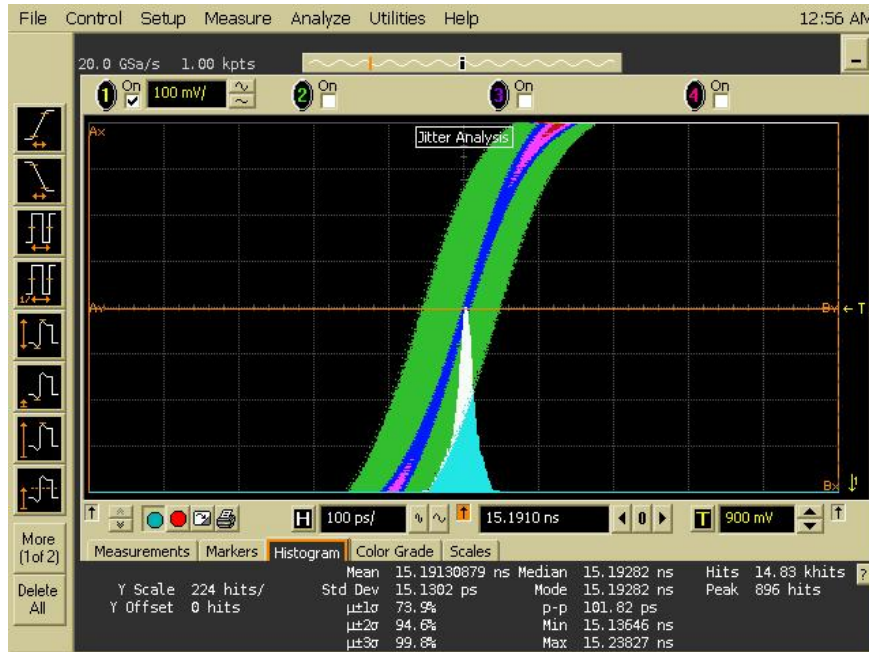


Fig 4.2 microphotograph of the test chip of proposed ADCDR circuit

Fig. 4.2 shows the microphotograph of the test chip. The test chip is fabricated on the standard performance 65nm CMOS process. The chip size is $644\mu\text{m}^2$ and the core size is $150\mu\text{m}^2$. Whole chip is composed of the testing part and proposed ADCDR part. The testing part contains the Pattern Generator and the Clock Generator. The ADCDR part contains TDC-embedded DCO, Dual Mode PFD, Controller, State Machine and Loop Filter [28].

4.2 Test Chip Measurement Result



(a) Jitter histogram of the recovered clock in 526MHz and output is divided by 8



(b) Jitter histogram of the on-chip clock generator clock at 526MHz and output is divided by 8

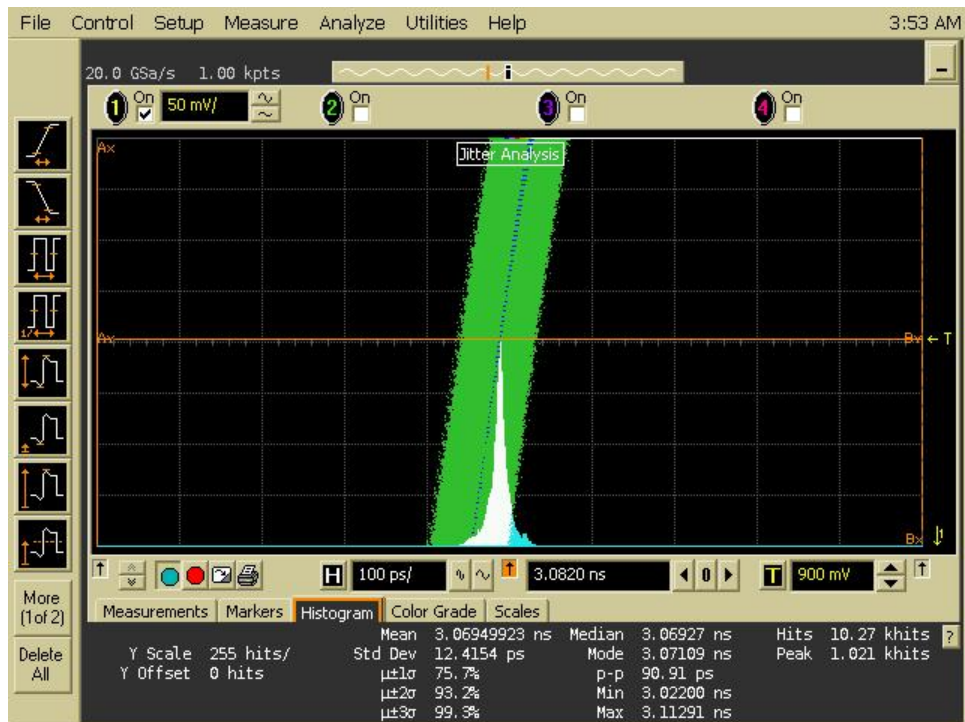
Fig 4.3 The jitter histogram of proposed ADCDR circuit

Fig. 4.3 (a) show the jitter measurement result of recovered clock of proposed ADCDR circuit recovered clock at 526MHz. Because of the speed limitation of I/O PADs, so the recovered clock is divided by 8 then outputs. The rms jitter is 15.13ps, and the peak to peak jitter is 101.82ps. Fig. 4.3 (b) is the jitter measurement result of on-chip clock generator, and it's also divided by 8. The rms jitter is 7.47ps and peak to peak jitter is 63.64ps. The proposed ADCDR circuit can tolerance for input jitters and still operates correctly.

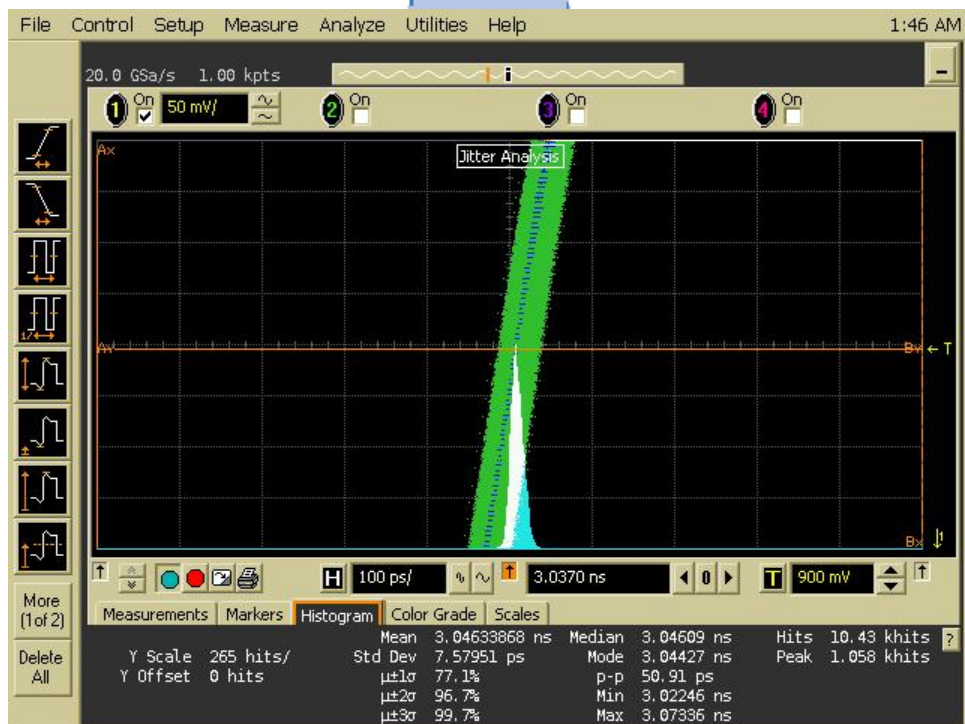
Because of the divider would influence the jitter performance, so the jitter performance of recovered clock and on-chip clock generator in 325MHz which is without the clock divider is tested, and the result is shown in Fig 4.4. Fig 4.4 (a) shows the rms jitter of proposed ADCDR circuit recovered clock is 12.41ps and peak to peak jitter is 90.91ps. Fig 4.4 (b) shows the on-chip clock generator output clock rms jitter is 7.57ps and peak to peak jitter is 50.91ps.

The divider influence is shown in Fig. 4.4 (c) and (d). The case of jitter performance of the 325MHz ADCDR circuit recovered clock and on-chip clock generator output clock divided by 8 is tested. Fig. 4.4 (c) shows the recovered clock with rms jitter is increased to 25.25ps and peak to peak jitter is increased to 167.27ps. Fig. 4.4 (d) shows the on-chip clock generator output clock, the rms jitter is increased to 10.6ps and peak to peak jitter is increased to 80ps.

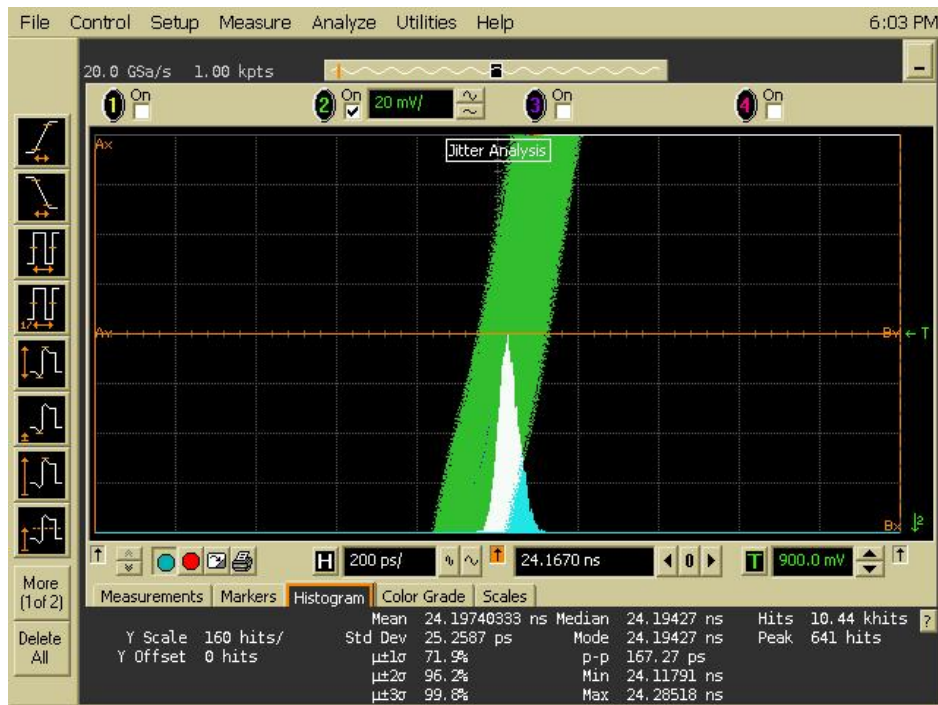
As the measurement result is shown, the operation range of proposed ADCDR circuit is 325MHz to 526MHz, and its cover the operating frequency of the USB2.0 high speed mode at 480MHz.



(a) Jitter histogram of the recovered clock in 325MHz without the output divider



(b) Jitter histogram of the on-chip clock generator output clock 325MHz without the output divider



(c) Jitter histogram of recovered clock in 325MHz and output is divided by 8



(d) Jitter histogram of on-chip clock generator output clock 325MHz and output is divided by 8

Fig 4.4 The jitter histogram of proposed ADCDR circuit

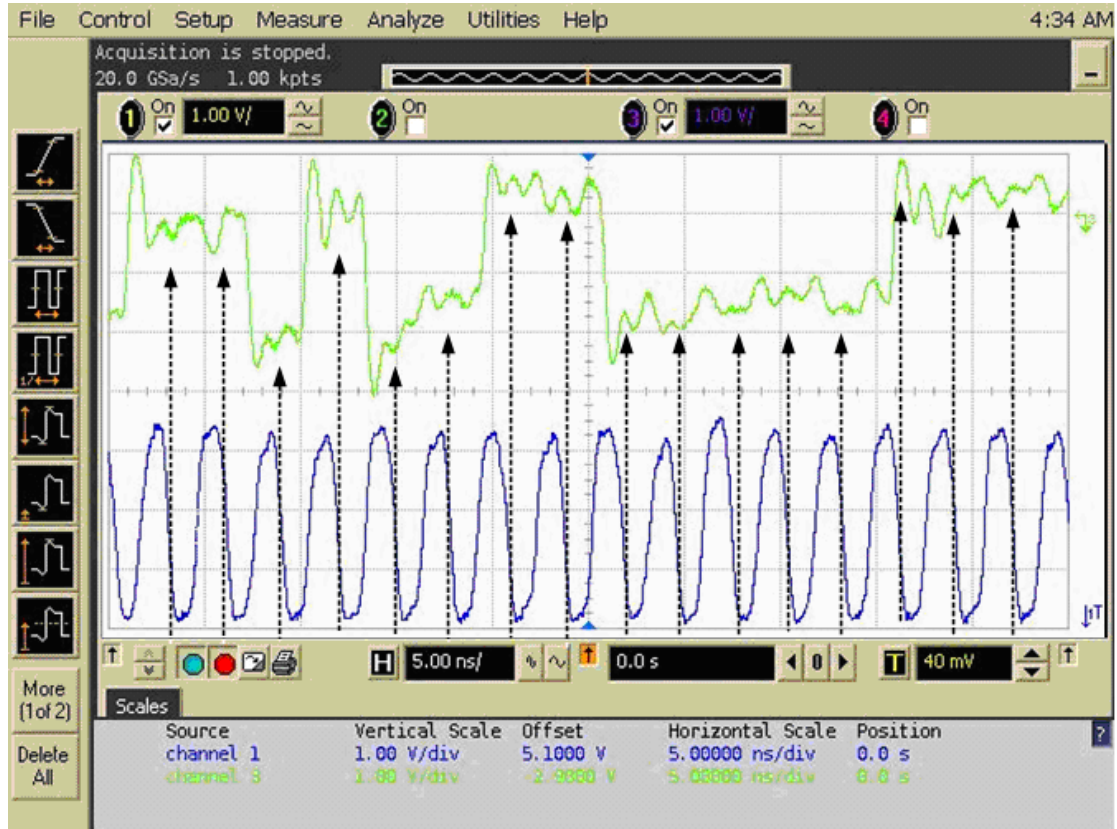


Fig 4.5 Waveform of recovery clock and data pattern

Fig. 4.5 shows the waveform of recovery clock and data pattern in 325MHz

The 325MHz recovery clock is directly output from I/O PADS directly. In the proposed ADCDR, the negative edge of recovery clock is used to trigger the DFF to retime the input data as the recovery data. In Fig. 4.5, the arrow is point out the sample node of input data that the negative edge of recovery clock sampled.

4.3 Final Chip Implementation

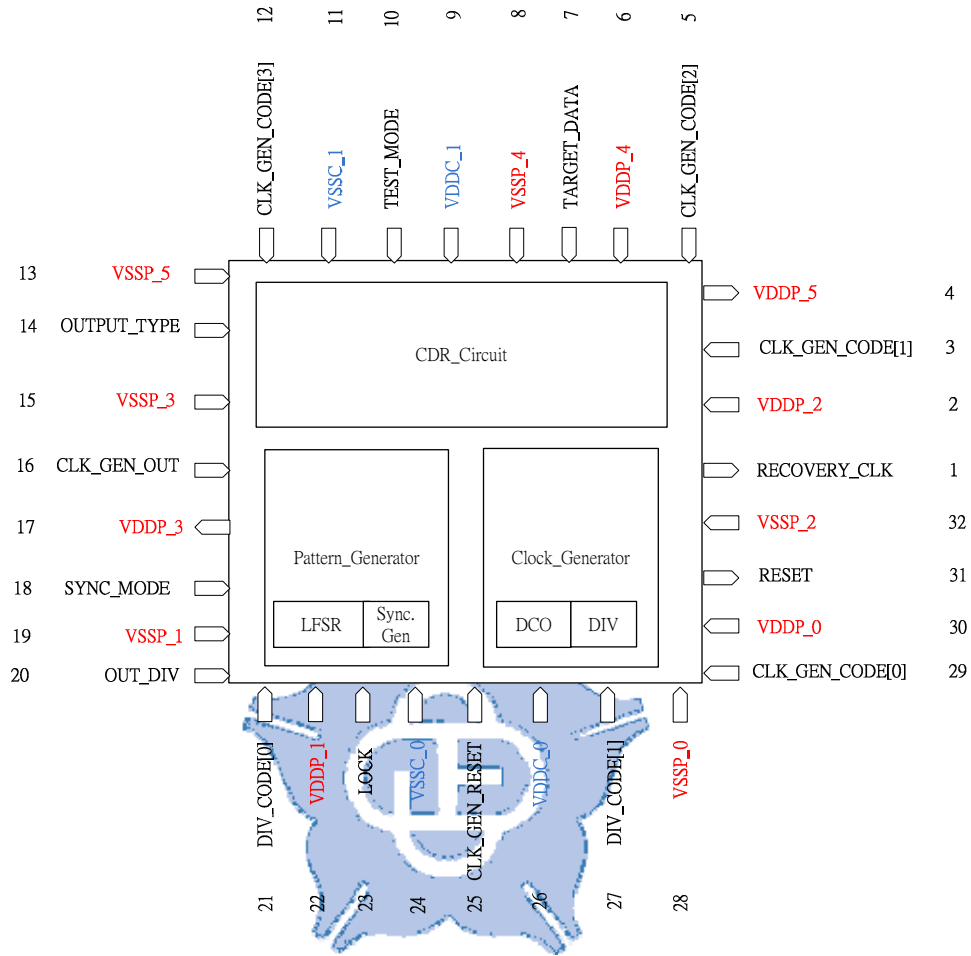


Fig 4.6 second version chip floorplaning and I/O planning

Fig. 4.6 shows the floorplaning and I/O planning of final chip of 2nd proposed ADCDR circuit. There is an additional programmable divider to supply the low frequency clock to achieve the wide range testing. The DCO will supply the 1GHz clock and divided by the programmable divider to generate the 500MHz, 100MHz, 10MHz, 1MHz clocks. The programmable divider supply the mode for divide by 2, 10, 100 or 1000 controlled by the off-chip input DIV_CODE[1:0]. The other detail I/O PADs descriptions are shown in Table 4.2.

Table 4.2 I/O PADs description of 2nd chip

Output	Bit	Function	
CLK_GEN_OUT	1 bit	Clock of USB 2.0 data pattern generator	
RECOVERY_CLK	1 bit	CDR Circuit recovery clock	
LOCK	1 bit	System lock in	
TARGET_DATA	1 bit	CDR Circuit's input data generated by USB 2.0 data pattern generator	
Input	Bit	Function	
DIV_CODE	2 bit	Adjust the on chip clock generator frequency for 500MHz to 1MHz by adjusting the divider counter.	
CLK_GEN_CODE	4bit	Control code of on-chip clock generator	
TEST_MODE	1 bit	Value	Mode
		0	Random Mode
		1	Worst Case/USB Test Mode (SPEED_MODE = 1)
SYNC_MODE	1 bit	0	SYNC Pattern = 7
		1	SYNC Pattern = 32
OUTPUT_TYPE	1 bit	0	Gated TARGET_DATA
		1	Gated CLK_GEN_OUT
OUT_DIV	1 bit	Turn on the divider for RECOVERED_CLK/8 and CLK_GEN_OUT/8 for high speed mode measurement	
RESET	1 bit	System reset	
CLK_GEN_RESET	1 bit	On chip clock generator reset	

4.4 Full Chip Overall Simulation

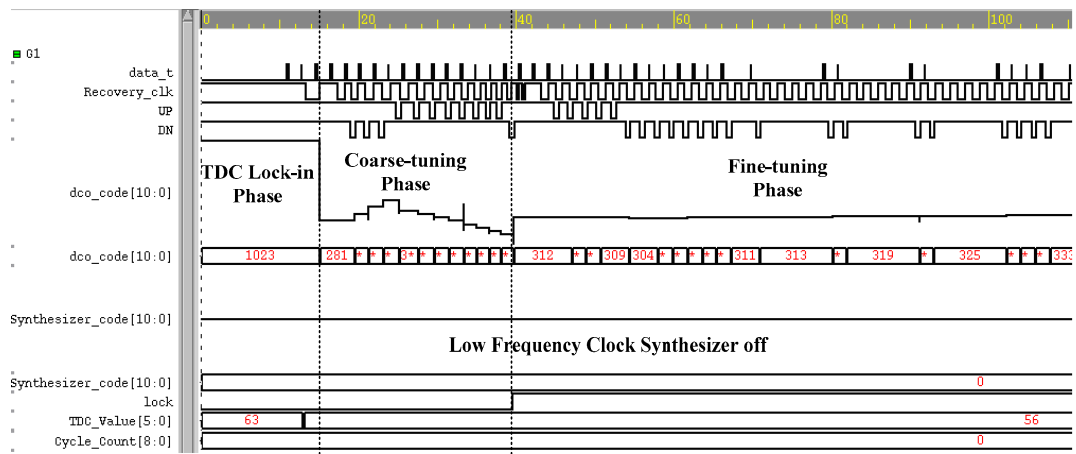


Fig 4.7 System simulation of proposed ADCDR circuit in 480MHz

Fig. 4.7 shows the post layout simulation waveform of the proposed ADCDR circuit in operation speed of USB2.0 high speed mode. Because of the data rate (480MHz) is faster than the minimum frequency of Cyclic TDC-embedded DCO, so the Cyclic_Count is 0 and the LFCS is not operating (so the synthesizer_code[10:0] is 11'b0) and the TDC-embedded DCO clock is output as the recovery clock directly. The TDC_Value is 56 and after encoding and sending to the ADCDR controller as the dco_code initial value 281. The UP/DN pulse is sending to the ADCDR controller to adjust the dco_code and adjust the TDC-embedded DCO clock frequency for frequency tracking in the 32 continuous data transitions (data_t) of the USB2.0 SYNC pattern. Finally, the frequency and phase acquisition is completed and lock-in within 40ns.

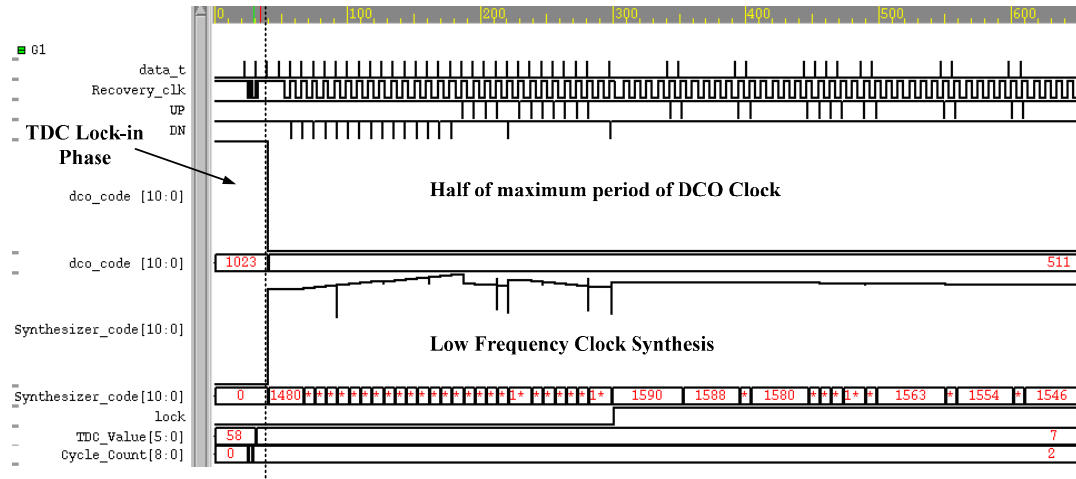


Fig 4.8 System simulation of proposed ADCDR circuit in 100MHz

Fig. 4.8 shows the post layout simulation waveform of proposed ADCDR circuit in operation speed of 100MHz. After the TDC measurement the Cyclic_count is 2, greater than 0. That means the LFCS must be used to synthesize the recovery clock. Then, the dco_code is reduced to the half of the maximum and the synthesizer_code is used to control the LFCS to adjust the recovery clock. Finally whole system is lock-in within 310ns.

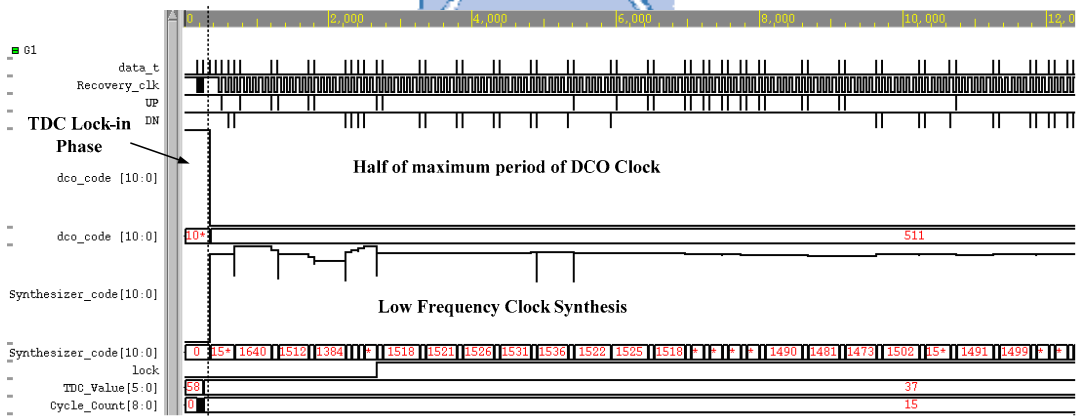
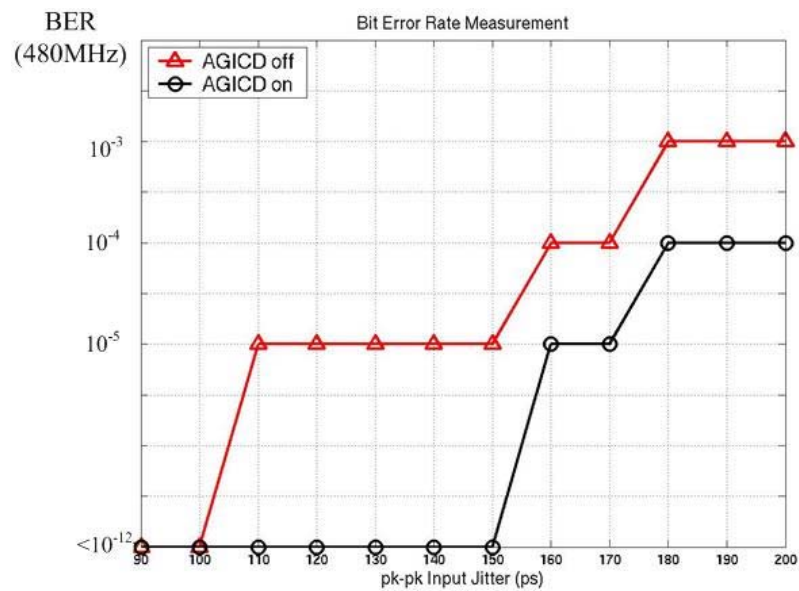


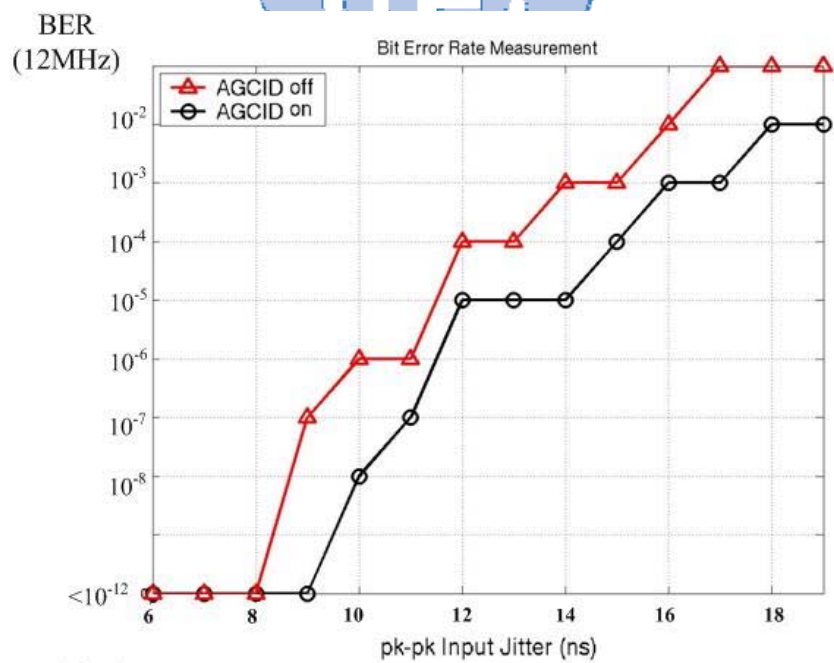
Fig 4.9 System simulation of proposed ADCDR circuit in 12MHz

Fig. 4.9 shows the post layout simulation waveform of proposed ADCDR circuit in operation speed of USB2.0 full speed mode. The Cyclic_count is 15 measured by TDC and the lock-in time is 2.4μs.

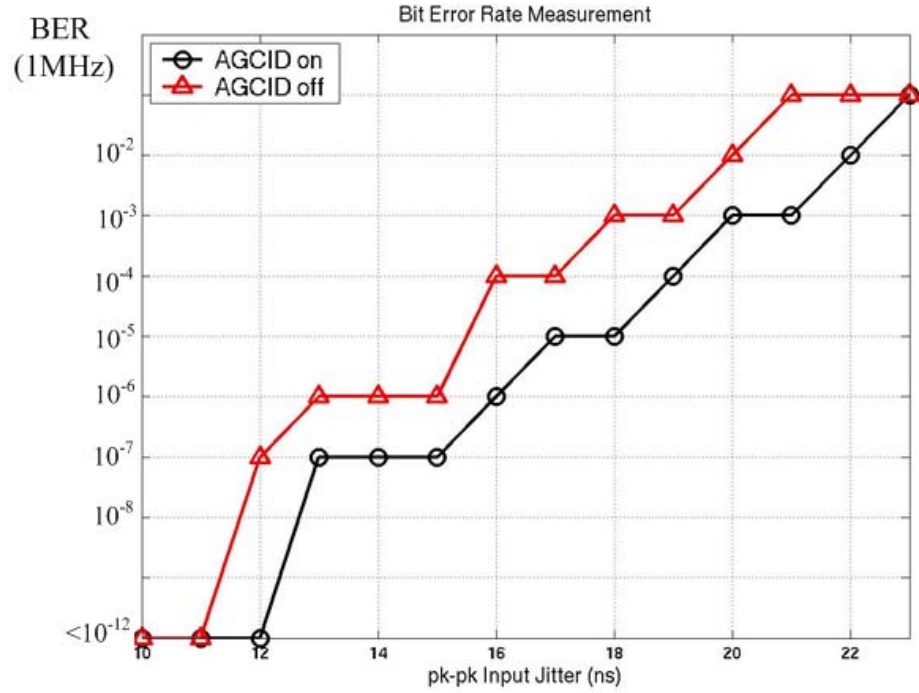
4.5 Bit Error Rate measurement in RTL Behavior Model Simulation



(a) BER performance of AGCID in 480MHZ



(b) BER performance of AGCID in 12MHZ



(c) BER performance of AGCID in 1MHz

Fig 4.10 Input jitter tolerance of BER performance with AGCID scheme

As shown in Fig. 4.10 (a), when the proposed ADCDR circuit operates in the USB2.0 high speed mode, and the AGCID scheme is turned off, BER (Bit Error Rate) is less than 10^{-12} until the input data jitter is larger than 100ps. When the input data jitter is larger than 100ps, BER performance is beginning get worse. However, when the proposed ADCDR turns on the AGCID scheme, the jitter tolerance is improved, when the input jitter is 150ps, and the BER is still less than 10^{-12} . The Fig. 4.10 (b) shows the proposed ADCDR circuit operates in the operation speed of USB2.0 full speed mode of 12MHz. The input jitter tolerance of BER performance is improved from input jitter 8ns to input jitter 9ns by turning on the AGCID. The Fig. 4.10 (c) shows the proposed ADCDR circuit at 1MHz achieves the input jitter 11ns and the BER is less than 10^{-12} . The AGCID scheme turns on and the input jitter is improved to 12ns and the BER is still less than 10^{-12} .

4.6 Chip Summary and Comparison Table

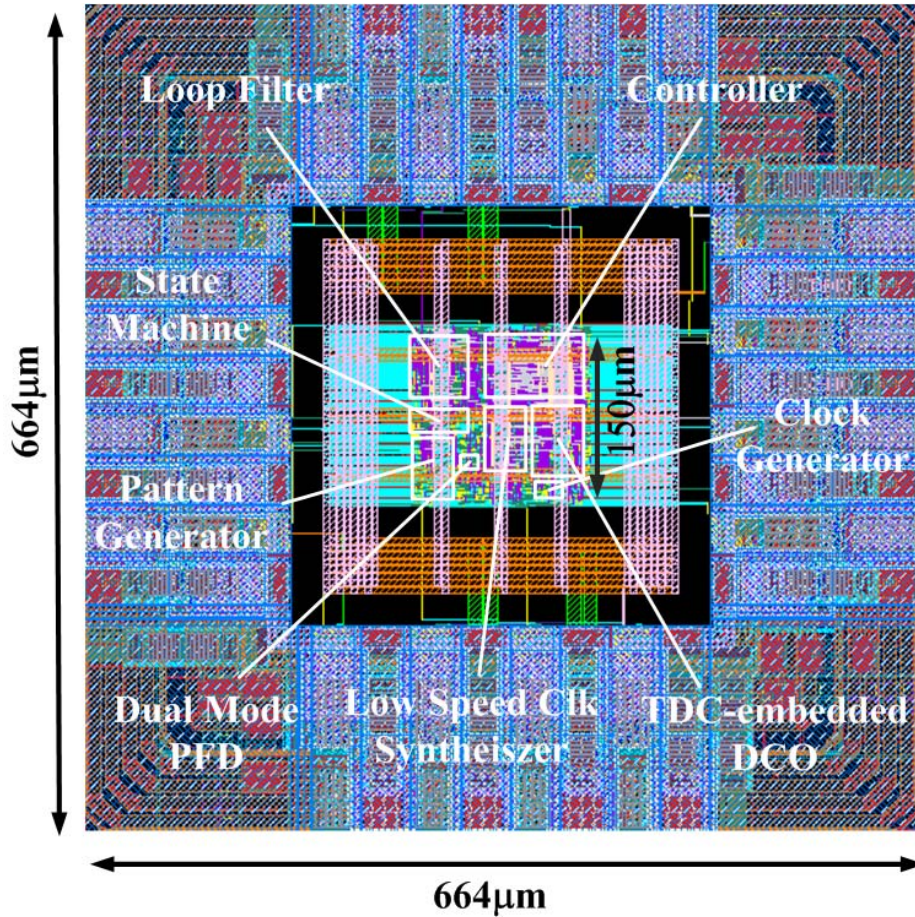


Fig 4.11 Layout of 2nd version of proposed ADCDR circuit

Fig. 4.11 shows the layout of the 2nd version of proposed ADCDR circuit. The chip is implemented on standard performance 65nm CMOS process. The chip size is $664\mu\text{m}^2$ and the core size is $150\mu\text{m}^2$. Except the proposed ADCDR, there are additional testing circuits in this circuit. The pattern generator (Pattern Generator) occupies $1479\mu\text{m}^2$ and the clock generator (Clock Generator) occupies $230\mu\text{m}^2$, respectively. In addition, the power consumption of the testing circuit by the pattern generator is 0.213mW in 500MHz, and the clock generator is 0.155mW in 500MHz.

The operation range of proposed ADCDR is from 700kHz to 500MHz, that can cover all speed modes of USB 2.0 specification.

The lock-in time of proposed CDR is less than 32 cycles in 480MHz that means the lock-in procedure can be completed within the SYNC pattern of USB 2.0 packet in high speed mode. In addition, the resolution of the wide range cyclic TDC is small enough to the USB 2.0 full speed mode (12MHz) and slow speed mode (1.5MHz) that the initial phase error between data transition and recovered clock is less than 90° , thus the proposed ADCDR circuit can recover data correctly within the short SYNC pattern in full speed mode and slow speed mode of USB 2.0.

The input jitter tolerance of proposed ADCDR is already achieved the pk-pk 150ps (86% UI), in USB 2.0 high speed mode, 9ns (80% UI) in USB 2.0 full speed mode and 12ns (96% UI) in USB 2.0 slow speed mode. The component inside the transceiver analog front shown in Fig. 1.8 such like equalizer can be used with the proposed ADCDR and achieve the receiver sensitivity requirement of input data eye pattern of 70% UI which is shown in Fig. 1.7.

The performance of proposed ADCDR and comparison with related works of clock and data recovery circuits are shown in Table 4.3.

Table 4.3 Comparison table

	[16] ASSCC'07	[17] TCAS-I'06	[26] JSSC'06	[15] TCAS-II'09	[2] TCAS-II'08	[25] Version 1.	Version 2.
Process	0.13- μm	0.35- μm	0.18- μm	0.25- μm	0.18- μm	65nm	65nm
Data Rate	180Mb/s~ 3.2Gb/s	200Mb/s~ 2Gb/s	155Mb/s~ 3Gb/s	140Mb/s~ 1.8Gbs	480MHz	480MHz	700Kb/s~ 500Mb/s
Operation Rate	Continuous Rate	Continuous Rate	Continuous Rate	Continuous Rate	Single Rate	Single Rate	Continuous Rate
CDR Type	4X Multi-phase	4X Multi-phase	4X Multi-phase	14X Multi-phase	Blind Over-sampling	Full Rate	Full Rate
Area	0.55mm ²	0.4mm ²	0.88mm ²	2mm ²	0.185mm ²	0.0255mm ²	0.0255mm ²
Supply	1.2V	3.3V	1.8V	2.5V	1.8V	1.0V	1.0V
Power	140 mW (3.2Gb/s) 75 mW (180Mb/s)	170 mW (2Gb/s)	95 mW (3Gb/s)	342.5 mW (Receiver)	8.2 mW (480MHz)	1.73 mW (480MHz)	2.63 mW (500MHz) 1.73 mW (150MHz) 0.54 mW (1MHz)
Jitter rms	14 ps (3.2Gb/s) 138 ps (180MHz)	5.86 ps (2Gb/s) 18.8 ps (200Mb/s)	64 ps (3Gb/s) 80 ps (155Mb/s)	14.96 ps (1.8Gb/s)	N/A	15 ps (526MHz) 12.41 ps (325MHz)	N/A
Jitter pk-pk	116 ps (3.2Gb/s) 700 ps (180Mb/s)	41.8 ps (2Gb/s) 120 ps (200Mb/s)	48.9 ps (3Gb/s) 467 ps (155Mb/s)	N/A	N/A	101 ps (526MHz) 90.91 ps (325MHz)	N/A
Lock-in Time	12 μs (3.2Gb/s) 9.5 μs (200Mb/s)	30 μs (1Gb/s)	50 μs (3Gb/s)	7.5 μs (1.8Gb/s) 8 μs (140Mb/s)	Zero lock time	40 ns (500Mb/s)	40 ns (500Mb/s) 310 ns (100Mb/s) 2.4 μs (12Mb/s) 25 μs (1Mb/s)
Reference Clock	No	No	No	No	Yes	No	No

Chapter 5 Conclusion and Future Works

In this thesis, the referenceless continuous rate ADCDR with the short lock-in time and wide operation range is proposed

The Cyclic TDC-embedded DCO is used to measure the input data rate that the initial recovered clock frequency can be close to the target data rate to achieve the fast frequency acquisition within the SYNC pattern of USB 2.0 packet.

The proposed cyclic concept of the TDC makes the DFFs on the delay line can be reused and achieve the wide range TDC measurement. Besides, the cyclic delay concept of the low frequency clock synthesis makes the wide operation can be achieved and not increasing the area occupation.

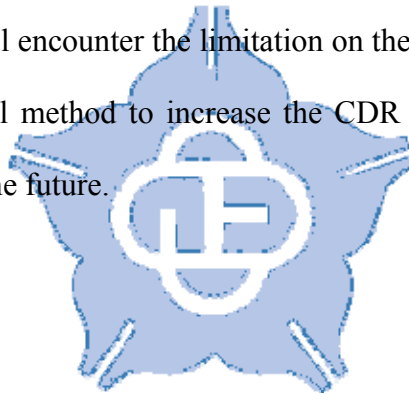
The proposed ADCDR doesn't need the multi-phase over-sampling scheme. The design complexity and the cost are both reduced.

The dual mode phase detector achieve both of the SYNC pattern phase and frequency tracking and random data pattern phase tracking. The scheme of adaptive gain in consecutive identical digit improves the input jitter tolerance and the bit error rate performance.

For this ADCDR, the test chip of version 1 is taped out to verify the proposed methods. This version is designed only for the operation speed of USB2.0 High Speed Mode (480MHz). The test chip is fabricated in UMC 65nm standard performance CMOS process and the core area is $150\mu\text{m} \times 150\mu\text{m}$.

CDR circuit is widely used in the high speed serial data link. However, there is a problem of Electromagnetic Interference (EMI) exist. The EMI would cause the disturbance of the transmission data. The conventional solution is the metal shielding, but this solution is requires a high cost. Therefore the technique of spread spectrum is proposed [32] for the EMI reduction.

Therefore, if the transmitter uses the triangle modulation to generate the spread spectrum clock, the output data rate would be continuous changed with a regularly pattern. The tracking ability of CDR circuit must be enhanced to tracking the changing data rate and keep the robustness and the bit error rate performance. At the present stage the proposed AGCID scheme can be used to enhance the CDR circuit tracking ability, but it's still encounter the limitation on the high modulation frequency. We hope to find the novel method to increase the CDR circuit performance on the spread spectrum issue in the future.



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