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資訊工程學系研究所

碩 士 論 文

全數位自動校正智慧型溫度偵測晶片

All-Digital Smart Temperature Sensor with Self-Calibration in 65nm CMOS Technology

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摘要

在此論文中，我們針對全數位智慧型溫度偵測晶片的設計，提出了討論以及架構的改進，更進步一步在溫度計的校正部份加入了自動校正的新方法，使我們溫度偵測晶片成為一個擁有自動校正能力的溫度計，稱之為全數位自動校正智慧型溫度偵測晶片。

論文中包含傳統慧型溫度偵測晶片中的重要元件介紹，並對各種元件架構的優缺點來做分析，討論是否適合使用在我們的晶片設計中。此外會介紹傳統溫度計校正的方法與缺點，以及為什麼我們需要擁有自動校正能力的溫度偵測晶片；而在介紹自動校正的部份，分為溫度本身的校正以及製程漂移的補償兩個部份，並會依次介紹其架構以及流程。

論文最後的部份統整了我們三個設計的成果：全數位智慧型溫度偵測測試晶片、完整版的全數位智慧型溫度偵測晶片和在可编程邏輯閘陣列上設計全數位智慧型溫度偵測器；由於論文中部份的技術並沒有包含在第一個設計中，所以經由比較第一與第二個設計的數據，可以很明顯看出效果。最後第三個設計主要是針對系統單晶片的整合來做開發，我們將設計好的溫度偵測電路燒錄到可编程邏輯閘陣列，並透過匯流排和 ARM 中央處理器來做整合與溝通，並利用開發版上的介面來做溫度呈現。

在這項研究中，我們在 65 奈米製程下呈現了具有小面積、低功率消耗的全數位智慧型溫度偵測晶片，而且完全不需要手動的校正，大幅降低了全數位智慧型溫度偵測晶片製作上的成本。

Abstract

In this thesis, we make a discussion and architecture improvements that focus on the design of all-digital smart temperature sensor. Additionally, the method of auto-calibration has been joined into our design to make the sensor to be automatic in calibrating operations. And so we call it an all-digital smart temperature sensor with auto-calibration.

This thesis will introduce the critical components in smart temperature sensor and analysis the advantages or disadvantages of each architecture. Besides, we talk about the conventional calibration method of smart temperature sensor and why auto-calibrating method is in need, and we present the architecture and operation flows of the temperature calibration and the process variations compensation.

Finally, we summarize our three designs in the thesis: the all-digital temperature sensor test chip, the full-fledged version all-digital smart temperature sensor and the all-digital smart temperature sensor on FPGA board. Because the first test key did not include all the techniques in the thesis, by comparing the first and second designs, we can clearly see the improvement of our novel method of calibration and compensation. The last design is focus on the integration with SoC system. We implement a simpler all-digital smart temperature sensor with the FPGA board and integrate the sensor with ARM CPU by the AHB, and then use the device on FPGA board to display the temperature information.

In this research, we have presented a novel fully digital CMOS smart temperature sensor with 65nm CMOS technology. It has tiny chip area and low power consumption, and the traditional two temperature points calibration can be eliminated to reduce the testing cost of sensor in mass production.

Acknowledgments

I would like to express my gratitude to my supervisor, Prof. Ching-Che Chung for his valuable guidance and advices. Moreover, his supports and encouragement always helped me to keep positive in this research.

I would also like to thank my graduate mates in Silicon Sensor and System (S3) Lab of National Chung Cheng University for many fruitful discussions and supports during my two years graduate live.

Finally, I want to appreciate my family and my girlfriend for their concerns and toleration when I was dejected, and this really makes me to be optimistic every time.

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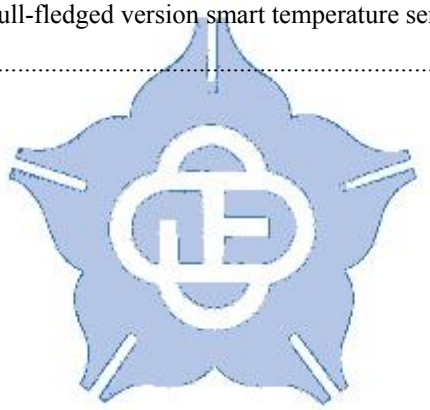


Chapter 1

Introduction

1.1 Introduction to Smart Temperature Sensor

Thermal sensor is an instrument which uses the characteristic of physics to measure the temperature or temperature gradient. There are lots of thermal sensors today, and the most popular thermal sensor in our live is the Mercury-in-glass thermometer [1]. However, after the thermometers have been manufactured, they have to be calibrated to optimize the sensor accuracy. To be a good thermometer, the temperature gradients of a thermal sensor should be as linear as it can for easy calibrating with common two-point calibration. Otherwise, we will need to calibrate every temperature points of a thermometer and that's impossible for mass production.

In 19th century, the computer and IC design were booming and start to play an important role in human life. Because the conventional thermal sensors generally have large area and they are difficult to be integrated with digital interface. Even though the conventional thermal sensors have a long development time, they are still unsuitable for integration with VLSI or system-on-chip (SoC) design. Therefore, the smart temperature sensors came out.

1.2 Motivation

In recent years, the advanced CMOS process makes it possible to integrate many designs into a single chip. The number of central processing units on a single embedded system chip

is also extended to 8 cores or even more [2]. When multiple chips are integrated and fabricated on the single chip, the power consumption wasted on the I/O buffers and the board-level interconnection parasitic RCs can be saved. However, system integration also increases design complexity and power density. Additionally, because the area of chip is increased, the on-chip variations will become significant in local process corner differentiation. As a result, on-chip thermal sensing or monitoring is very important for system reliability and dynamic thermal management [3-[6].

Traditionally, designer must to design for worst case to make sure that the chip can work normally under process, voltage and temperature (PVT) variations. However, design for worst case could be too pessimistic and it also increases the design complexity [7]. Thus not only the design time but also the area and power of chip are increased. Additionally, when the chip is working close to the critical point (ex: hot spot), the system will do some operations like dynamic frequency scaling (DFS) [8-[9] and make the chip away from critical point.

Thermal monitoring on a chip is a way to measure the temperature variations. It uses on-chip thermal sensors to provide the run-time thermal profile of a system. When hot spot occurs, the thermal management circuit can send request to the system controller to stop the current operation or to slow down the system clock frequency, so that the chip temperature can be kept below the specified temperature limitation, and therefore the reliability of the system can be improved.

In generally, we can use simulation result to analyze the power consumption of each module on a chip, and then disturb the high power consumption modules in chip floorplanning to prevent overheat [10-[12]. Nevertheless, prevention is not enough. We still have to uniformly place many temperature sensors on the chip to detect the local temperature variations of the chip in run-time. The requirements for these temperature sensors are small area, low-power consumption, and easy to calibration. Temperature sensors should have

extreme low-power consumption to avoid self-heating effects to the system. Moreover, temperature sensors must be easy to perform absolute temperature calibration and have sufficient conversion rate (> 1000 samples/sec) to monitor the run-time thermal profile of a system.

Traditionally, the BJT-based smart temperature sensors [13] are widely used in many applications. The BJT-based smart temperature sensor converts the measuring temperature into a voltage or current firstly, and then the analog-to-digital converter (ADC) converts voltage or current information into digital codes. However, the BJT-based smart temperature sensor usually has large chip area and high power consumption due to the ADC circuit and the band gap reference voltage circuit. And the BJT-based smart temperature sensor also needs the second order curvature correction circuit and post-silicon transistor trimming to improve the accuracy of temperature measurement. Since there are many temperature sensors on the chip, it is not possible to perform absolute temperature calibration and postsilicon transistor trimming for every temperature sensors. And it also takes more efforts to integrate the analog circuits with the digital circuits. As a result, the BJT-based smart temperature sensors are not suitable for dynamic thermal management in system-on-a-chip (SoC).

The all-digital time-domain smart temperature sensor which uses the time-to-digital converter (TDC) to quantize the delay pulse into temperature information is proposed in [14-[16]. The all-digital architecture make can be easy to be ported to different processes in a short time, and it is also easy to be integrated into the digital systems. However, the temperature sensors [14[16] still need to perform two temperature points calibration before the temperature sensors can be used. Since there are many temperature sensors on the chip, and therefore how to reduce the calibration cost of the temperature sensor array becomes very important now.

Thus the temperature sensor with dual DLLs to perform one temperature point

calibration is proposed in [17]. The reference clock with a multi-phase delay line can generate a fixed delay in PVT variations to calibrate the temperature errors. However, the temperature sensor with dual DLLs occupied too much chip area with high power consumption at milli-watt level.

1.3 Thesis Organization

In this thesis, we discuss about the implementations of all-digital smart temperature sensor in 65nm technology and the proposed algorithms for auto-calibration. The proposed auto-calibration method can greatly reduce the cost of sensor's calibration. The rest of the thesis is organized as follows.

In chapter 2, we discuss about several Proportional to Absolute Temperature (PTAT) circuit architecture that used in smart temperature sensor and explain how they work. Because all-digital circuit is easy for integration with SoC design, we will mainly focus on digital PTAT circuit architecture.

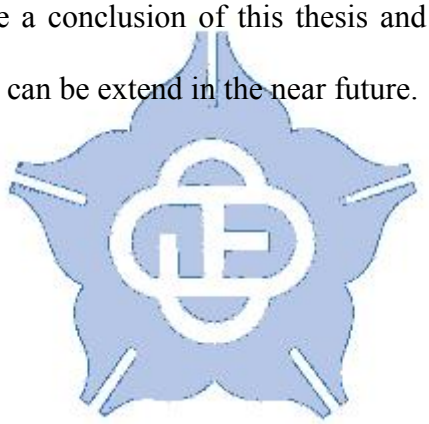
In chapter 3, the design for all-digital smart temperature sensor circuit is presented. Here we will split the main sensor circuit into two parts, the PTAT pulse generator and the Time-to-Digital Converter (TDC). In the part of TDC, we will introduce several types of TDC in detail and discuss about their advantages or disadvantages that used in our smart temperature sensors.

In chapter 4, the proposed algorithm for thermal sensor auto-calibration is presented. Our smart temperature sensor can perform auto-calibration in room temperature when system is reset. After the auto-calibration, the run-time thermal profile of a system can be monitored. Another part in chapter 4 is the compensation to process variations and this operation can greatly reduce the effects of process variations, and it is also automatic when the system is

reset.

In chapter 5, the specification, measurement and simulation results of the smart temperature sensors are shown. The first smart temperature sensor test key only includes the auto-calibration of temperature with single slope. The second test key is the full-fledged version all-digital smart temperature sensor, unlike the first test key has some modifications in TDC architecture, and the auto-calibrating method in this design includes the auto-calibration of temperature with dual slope and the process variations compensating. The third design is a special corresponding design with ARM CPU system for system-on-chip integrating achievement.

In chapter 6, we make a conclusion of this thesis and describe the further work about several design issues which can be extend in the near future.



Chapter 2

Proportional to Absolute Temperature (PTAT) Circuit

2.1 Bipolar Junction Transistor (BJT) Based PTAT Circuit

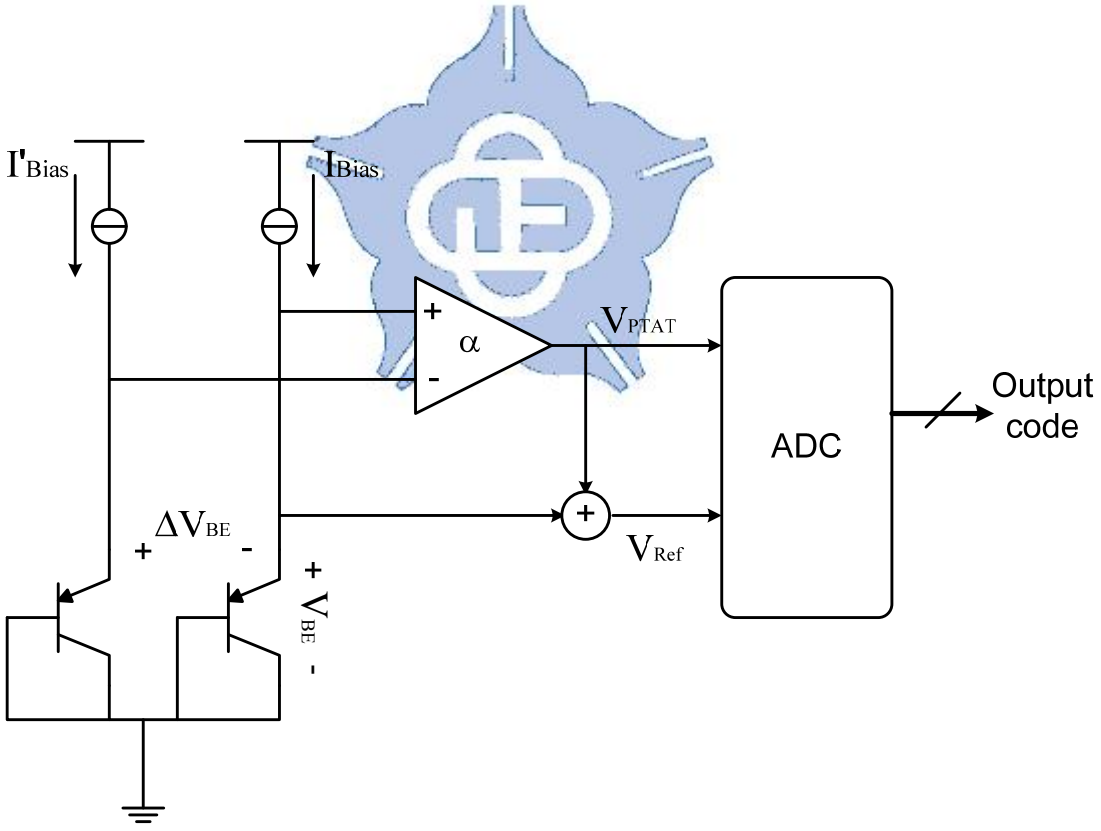


Fig. 2.1: The architecture of the conventional BJT based thermal sensor.

Traditionally, the BJT-based PTAT circuit is regularly used to design the on-chip thermal

sensor in conventional CMOS technology (i.e. > 0.35μm) [13]. The Fig. 2.1 shows the architecture of the conventional BJT based thermal sensor.

In Fig. 2.1, the ΔV_{BE} which is the difference between V_{BE} of the two BJTs can be expressed as

$$\Delta V_{BE} = \frac{KT}{q}\ln(p) \qquad (2.1)$$

Where p is the ration of BJT bias current I_{Bias} and I'_{Bias}.

In the equation 2.1, we can see that ΔV_{BE} is proportional to the temperature. Therefore, the conventional BJT-based sensor can use an analog-to-digital converter (ADC) to convert the voltage information into digital temperature data.

However, the reference voltage of ADC will be affected by the temperature variations. Even though the BJT based PTAT circuit has good linearity in temperature and voltage converting, the mismatch of the ADC's reference voltage will still restrain the accuracy.

2.2 Delay-Line Based PTAT Circuit

Besides the BJT circuit, the delay time of logic gate cells also can be used to measure the temperature variations [14]. When a signal pass through a logic gate, there will have a propagation delay between the input and output of the gate, and that's what we call a gate delay.

The propagation time for a NOT gate can be expressed as

$$T_P = \frac{T_{PLH} + T_{PHL}}{2} \tag{2.2}$$

Where T_{PLH} and T_{PHL} are the high-to-low and low-to-high propagation time.

In [19], we can see that the high-to-low and low-to-high propagation time of a NOT gate can be expressed as

$$T_{PLH} = \frac{2C_L V_{TN}}{k_N (V_{DD} - V_{TN})^2} + \frac{C_L}{k_N (V_{DD} - V_{TN})} \times \ln\left(\frac{1.5V_{DD} - 2V_{TN}}{0.5V_{DD}}\right) \tag{2.3}$$

$$T_{PHL} = \frac{-2C_L V_{TP}}{k_P (V_{DD} + V_{TP})^2} + \frac{C_L}{k_P (V_{DD} + V_{TP})} \times \ln\left(\frac{1.5V_{DD} + 2V_{TP}}{0.5V_{DD}}\right) \tag{2.4}$$

Where $k_N = \mu_N C_{OX} (W/L)_N$, $k_P = \mu_P C_{OX} (W/L)_P$ are the trans-conductance parameters and C_L is the effective load capacitance of the NOT gate.

By Eq. 2.3 and Eq. 2.4, the Eq. 2.2 can be derived as

$$T_P = \frac{(L/W)C_L}{\mu C_{OX} (V_{DD} - V_T)} \times \ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right) \tag{2.5}$$

In [21] and [22], we know that

$$\mu = \mu_0 \left(\frac{T}{T_0} \right)^{km}, \quad km = -1.2 \sim -2.0 \tag{2.6}$$

$$V_T(T) = V_T(T_0) + \alpha(T - T_0), \quad \alpha = -0.5 \sim -3.0 \; mV/°K \tag{2.7}$$

So we can see that if the temperature rises, the mobility μ and threshold voltage V_T will both decrease. Additionally, V_{DD} is much larger than the threshold voltage of a CMOS gate, so the propagation time for the NOT gate will be dominated by the mobility. In other words, the propagation time for the NOT gate will be increased when the temperature is rising.

Generally, the support voltage V_{DD} is much lower in 65nm than 0.35μm (i.e. 1.0V in 65nm and 3.3V in 0.35μm) and the threshold voltage also has a decreasing (i.e. about 400mv in 65nm and 600mv in 0.35μm). If we take those parameters into Eq. 2.5, we can see that the affection of V_T become more significant in 65nm. However, the simulation result shows that the linearity is good enough for temperature monitoring. The delay line we used in our simulation in 65nm CMOS technology was composed of 100 delay cells. We simulated the delay line with different temperature to observe the variations of propagation time, and the result is shown in Fig. 2.2.

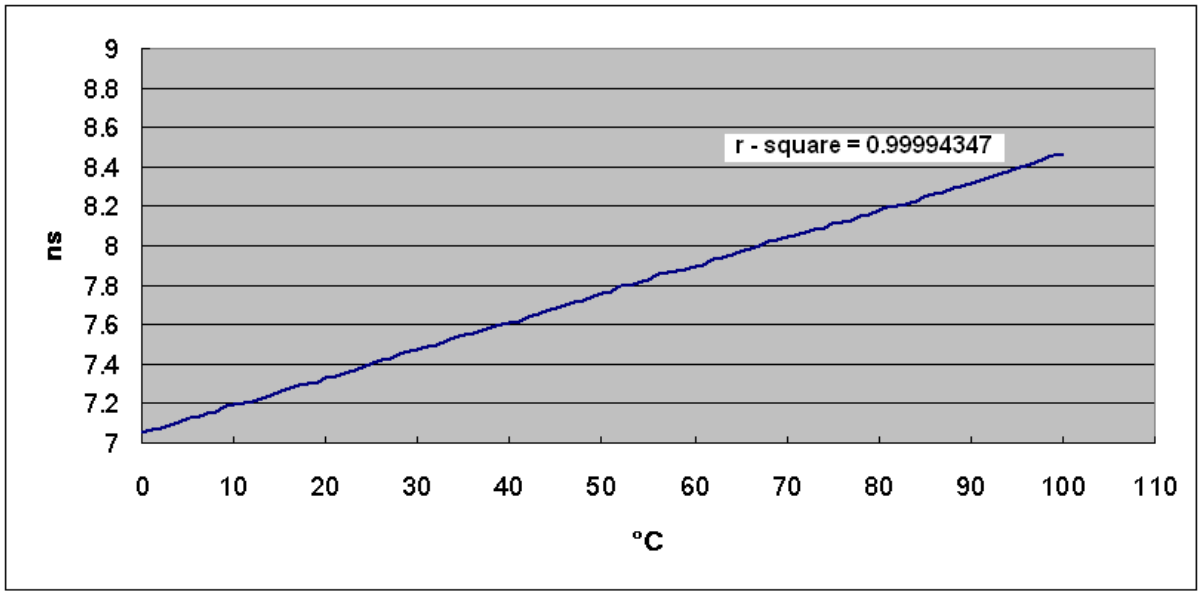


Fig. 2.2: The simulation result of the delay line's propagation time vs. temperature.

In Fig. 2.2, the delay line's propagation delay has a good linearity with temperature (i.e. r-square is 0.99994347). Therefore, the delay line which is composed of delay cells in 65nm CMOS technology is feasible to be a thermal meter. All we have to do just to quantify the change of propagation delay information.

2.3 Oscillator Based Inverse PTAT Circuit

As we discuss in the above section, the delay cells' delay is proportional to absolute temperature. If we design a ring oscillator constructed by delay cells, the oscillating frequency will be

$$f = \frac{1}{T} \tag{2.8}$$

Where T is the period of the ring oscillator. And by Eq. 2.2 and Eq. 2.5, the Eq. 2.8 can be derived as

$$f = \frac{1}{T_{PLH} + T_{PHL}/2} = \frac{\mu C_{OX}(V_{DD} - V_T)}{(L/W)C_L}\left[-\ln\left(\frac{1.5V_{DD} - 2V_T}{0.5V_{DD}}\right)\right] \qquad (2.9)$$

With Eq. 2.6 and Eq. 2.7 we can see that the frequency *f* should be inverse proportional to absolute temperature. The Fig. 2.3 present the oscillator based IPTAT circuit, the counter is used to count the oscillating pulse in a fix time. Because the oscillating frequency is IPTAT, we can expect that the code generated from the counter is also IPTAT.

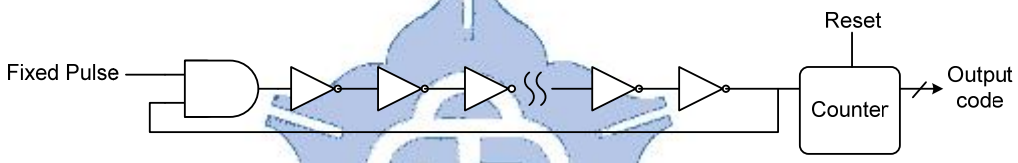


Fig. 2.3: The oscillator based IPTAT circuit.

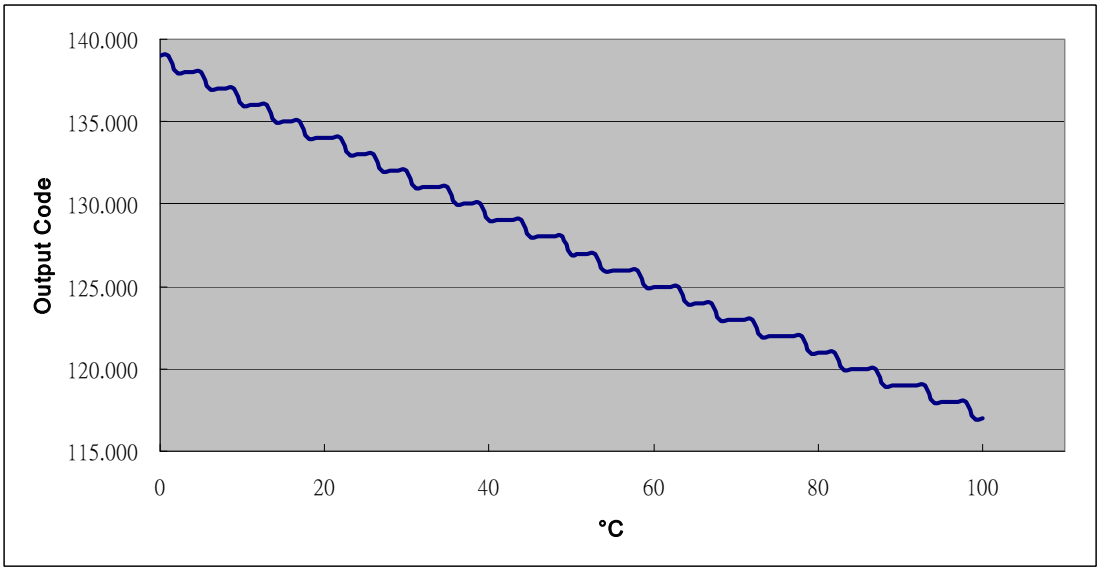


Fig. 2.4: the simulation result of the oscillator based IPTAT circuit vs. temperature.

Fig. 2.4 shows the simulation result of the oscillator based IPTAT circuit output code with different temperature. In this design, the resolution is limited by the oscillating frequency. If we reduce the number of delay cells in the delay ring, the oscillating frequency becomes higher, and the resolution can be improved. However, if the frequency is too fast, it is hard to design the counter.

2.4 Summary

The proportional to absolute temperature circuit is a basic building block in all-digital smart temperature sensor. Just likes mercury-in-glass thermometer refer the expansion and contraction of mercury to reflect the temperature variations, the smart temperature sensor also needs to refer something to measure the change of temperature. Because the difficulties in the oscillator-based IPTAT circuit design, the proposed smart temperature sensor uses the delay line for temperature referring. In the following chapter, we will discuss about the proposed sensor architecture and how it uses the PTAT information then converts into digital code to become a real thermal meter.

Chapter 3

All-Digital Smart Temperature Sensor Circuit

3.1 The Proposed All-Digital Smart Temperature Sensor Overview

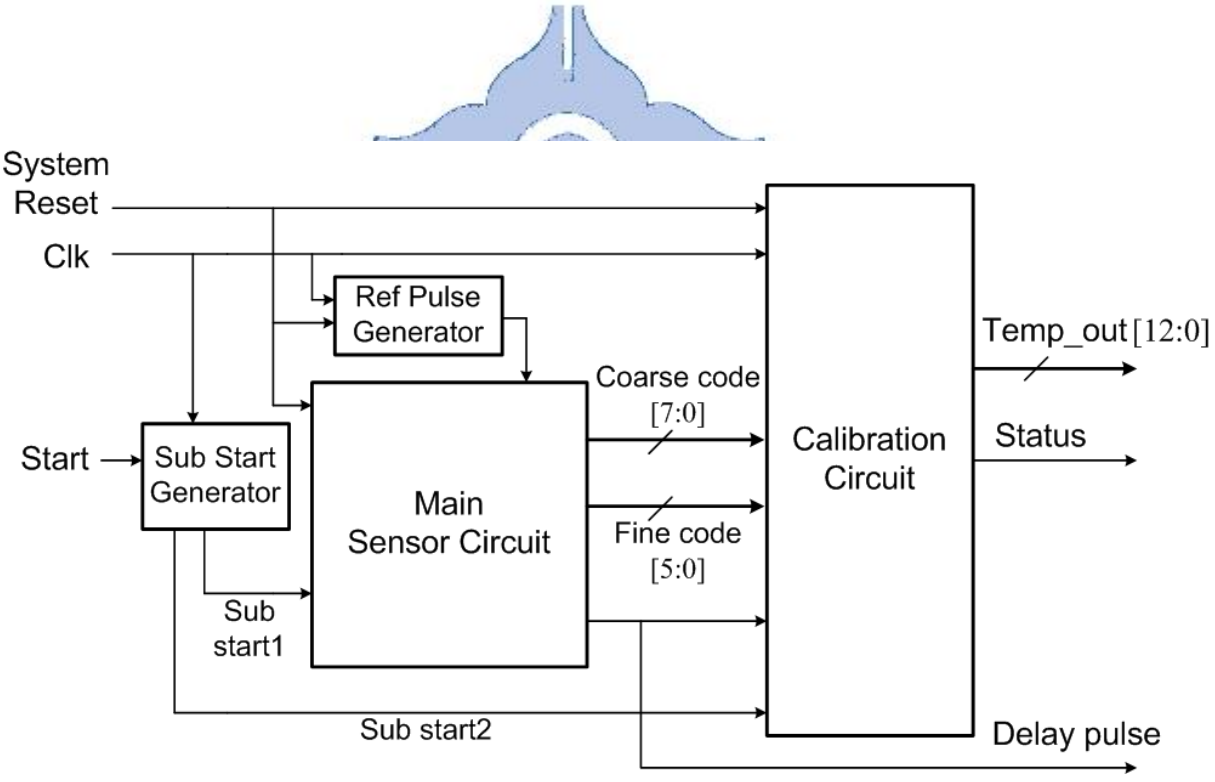


Fig. 3.1: The block diagram of the proposed smart temperature sensor.

The block diagram of the proposed smart temperature sensor with auto-calibration circuit is shown in Fig. 3.1. It has four blocks: Sub start generator, reference pulse generator, main

sensor circuit and the calibration circuit. Sub start generator for start signal triggering controlling. Reference pulse generator is for sensor's process variation calibrating. The main sensor circuit and the calibration circuit are used to measures the temperature variations and auto-calibrate the measurement result. In detail, the main sensor circuit measures current temperature information and outputs digital codes (coarse_code[7:0], fine_code[5:0]) to the calibration circuit to calculate the temperature in the neighborhood of the on-chip temperature sensor. We will discuss the algorithm in calibration circuit and its operation flow in the next chapter.

The architecture of the proposed main sensor circuit is shown in Fig. 3.2. It is composed of the propagation to absolute temperature (PTAT) delay pulse generator and the time-to-digital converter (TDC). The following sections will describe the components of the main sensor circuit in detail.

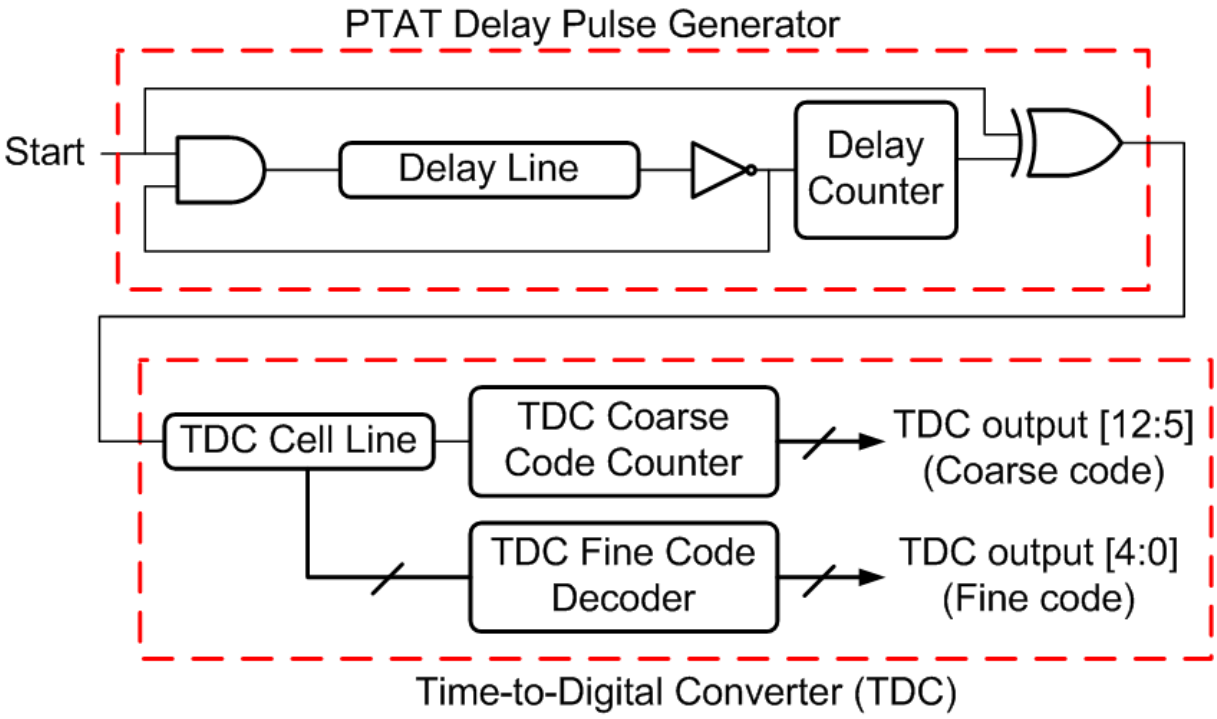


Fig. 3.2: The main sensor circuit in our all-digital smart temperature sensor.

3.2 Proportional to Absolute Temperature (PTAT) Pulse Generator

To reduce the chip area, the delay line used in PTAT delay pulse generator is a cyclic delay line [23] which is shown in Fig 3.3. The cyclic delay line used a XOR logic gate with the external signal "Start Signal" to generate a pulse and the pulse width is proportional to the absolute temperature (PTAT). The cyclic delay line will start to oscillate after the signal "Start Signal" is enabled. The delay counter counts the number of positive edges of the signal "oscillating_pulse". When the delay counter reaches the specified number, the signal "delay_pulse" will be enabled. Then the signal "Start" and the signal "delay_pulse" are inputted to the XOR gate to generate the signal "PTAT_pulse" for the TDC. Fig. 3.4 shows the timing diagram of the cyclic delay line.

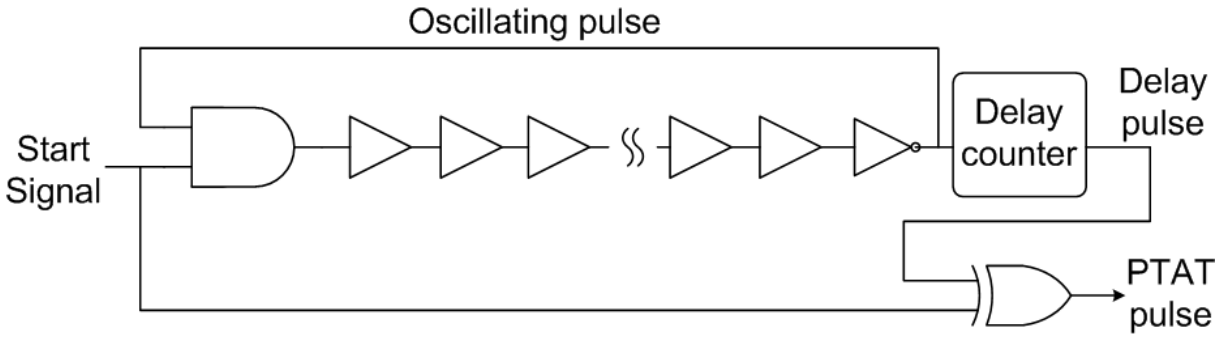


Fig. 3.3: The cyclic delay line.

The pulse width of the signal "PTAT_pulse" can be controlled by the delay counter, and the pulse width should be wide enough for the next stage TDC to quantize it into digital codes. In addition to the above viewpoint, more delay cells used in the cyclic delay line means that the "oscillating_pulse" output frequency is reduced, and the power consumption of the cyclic

delay line is reduced, too. But if the number of delay cells is increased, the area of the cyclic delay is also increased. Thus we need to trade-off the area and the power of the PTAT pulse generator circuit.

Another viewpoint is that the sensor resolution to temperature is dependent on the width of PTAT pulse. The wider the pulse is, the higher resolution we will have. However, if we want to make the PTAT pulse to be wider, we have to either increase the length of delay line or expand the bits of delay counter. Moreover, those methods will both increase the power consumption. This tradeoff also affects the TDC design in resolution. If we want our sensor to have a 0.1 °C resolution to temperature and the width of PTAT pulse will be increased 100ps with 0.1 °C rising, then our TDC behind PTAT pulse generator must have a limitation of resolution with 100 ps. In other words, the resolution of PTAT pulse width to temperature is interlocking with the resolution of TDC to pulse width.

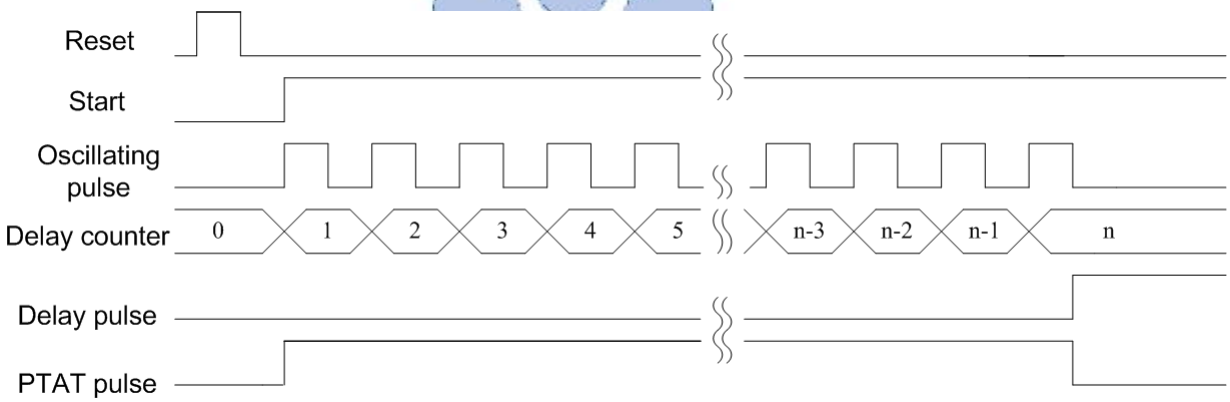


Fig. 3.4: The timing diagram of the cyclic delay line.

3.3 Time-to-Digital Converter

After the PTAT pulse is generated by the cyclic delay line. The time-to-digital converter (TDC) is used to quantize the pulse width information into digital codes. The following subsections introduce four different types of TDC: the clock sampling TDC and veriner delay line based TDC are for survey and comparing to our design. The ring based TDC and PVT compensated ring based TDC are novel architecture we present, and the ring based TDC is the mainly using architecture in our proposed all-digital temperature sensors.

3.3.1 Clock Sampling TDC

Fig. 3.5 shows the clock sampling TDC with pulse and reference clock input.

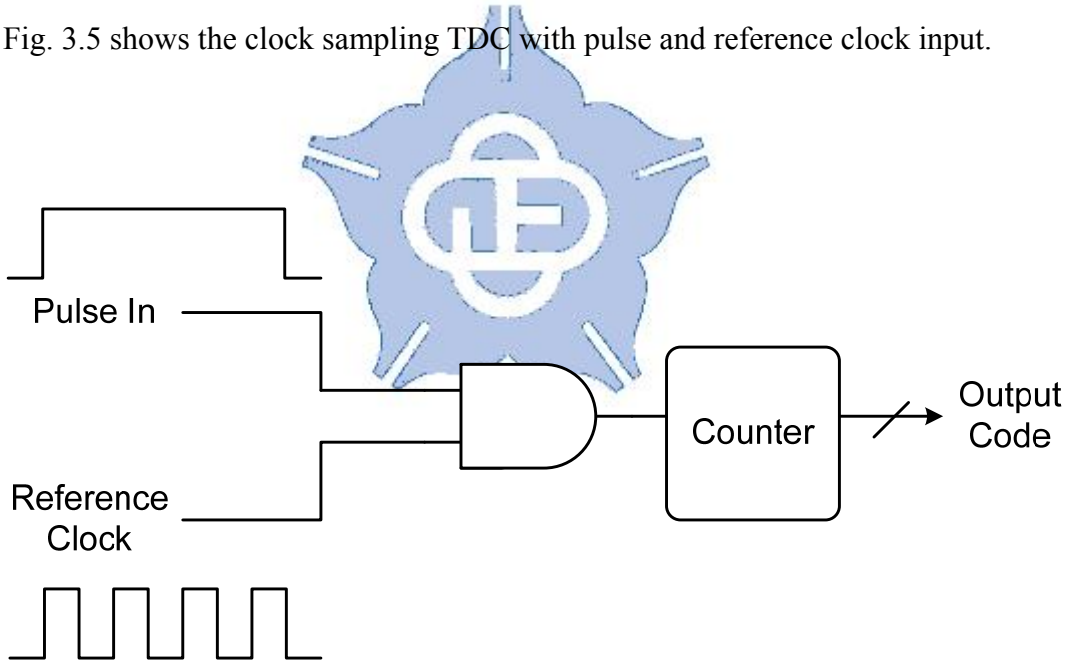


Fig. 3.5: The architecture of clock sampling TDC.

The TDC used the reference clock to sample the input pulse and counts its width. This architecture has good linearity and is almost PVT independent. Additionally, the TDC resolution is directly determined by the reference clock frequency. The higher the frequency

input, the better the resolution we will have. However, the high-speed reference clock frequency will force us to design a high speed logic gate and counter, and thus the design complexity is also increased.

3.3.2 Vernier Delay Line Based TDC

The vernier delay line based TDC has a very fine resolution [24[25] because the sub-gate-delay technique. It uses two different delay lines, one with delay α and the other with delay β, and the resolution of the TDC can be (α - β). The Fig. 3.6 shows the vernier delay line circuit.

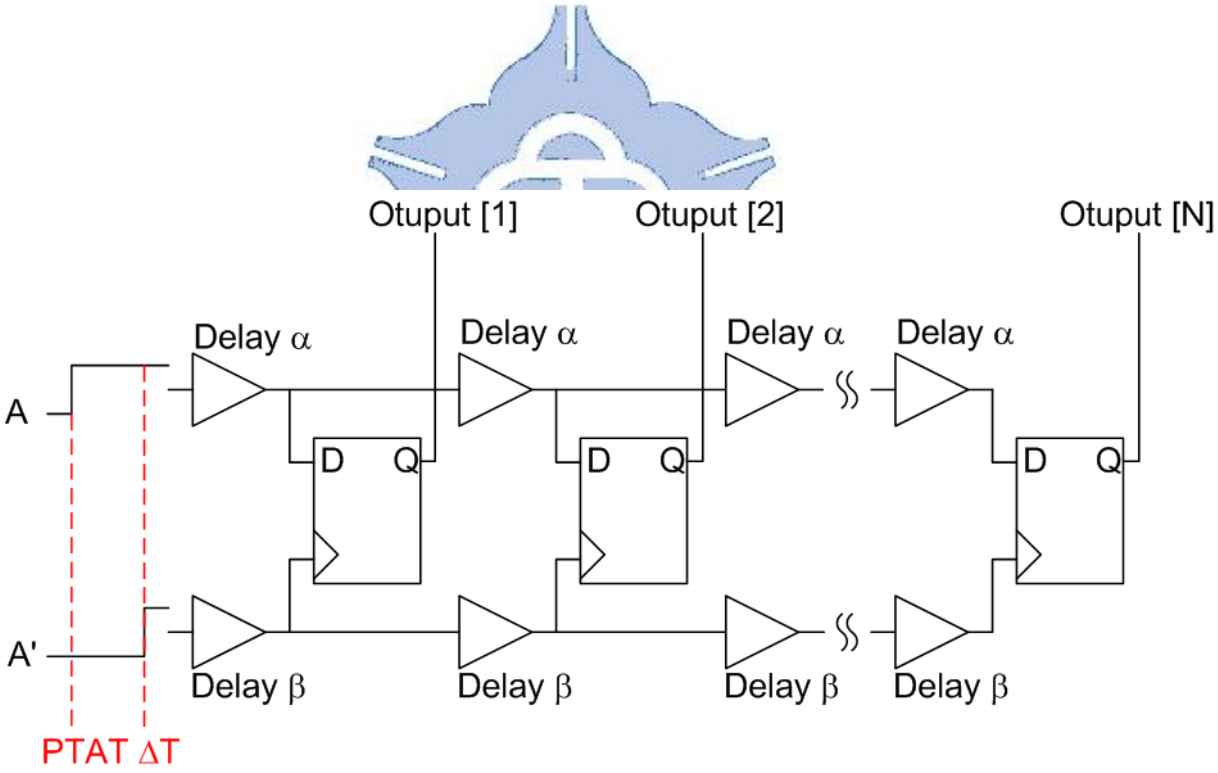


Fig. 3.6: Vernier delay line.

Even though the vernier delay line has a fine resolution in quantization, the input pulse range is limit by the length of delay line. However, the timing-domain smart temperature

sensor must extend the PTAT pulse for higher resolution in temperature measurement. So the limitation of the input pulse range makes the vernier delay line to be unsuitable in thermal applications or may need to extend the delay line and thus the chip area become very large.

3.3.3 Ring Based TDC

To have a small chip size of TDC, the cyclic TDC was present in [26]. Even though the cyclic TDC reduce the consumption of area, the resolution is limited by the oscillating frequency of the cyclic delay line. However, if the oscillating frequency is too fast, the counter behind the delay line will be very difficult to implement.

The proposed ring based TDC is composed of the TDC cells ring, the coarse counter and the fine code decoder to achieve high resolution quantization for wide range input pulse width. The Ring Based TDC is shown in Fig. 3.7.

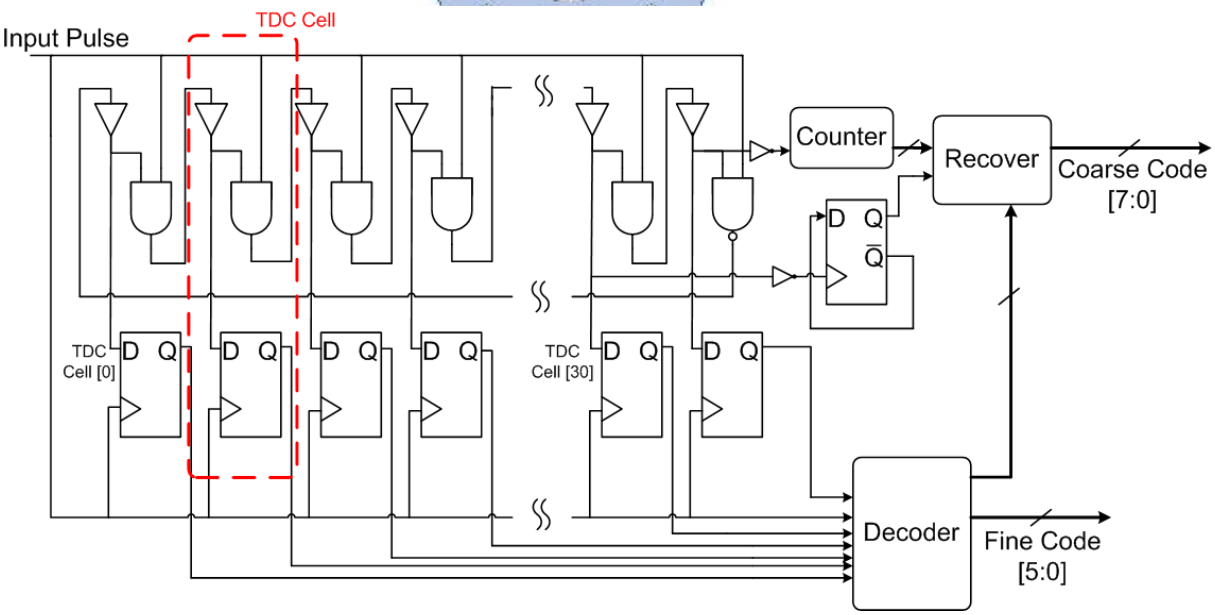


Fig. 3.7: The ring based time-to-digital converter (TDC).

In the proposed ring based TDC, 32 TDC cells are used to compose the TDC cells ring. For signal counting, only the last TDC cell has a NAND gate instead of a AND gate. When the signal "input_pulse" is enabled, then all cells in the TDC cells ring will pass the signal from the previous cell, and the TDC cell line starts to oscillate. The TDC coarse counter counts the arrival positive edges to generate the TDC coarse code. This operation is continued until the signal "input_pulse" is disabled. Then the residual pulse width information can be generated by the fine code decoder. The timing diagram of the ring based TDC is shown in Fig 3.8.

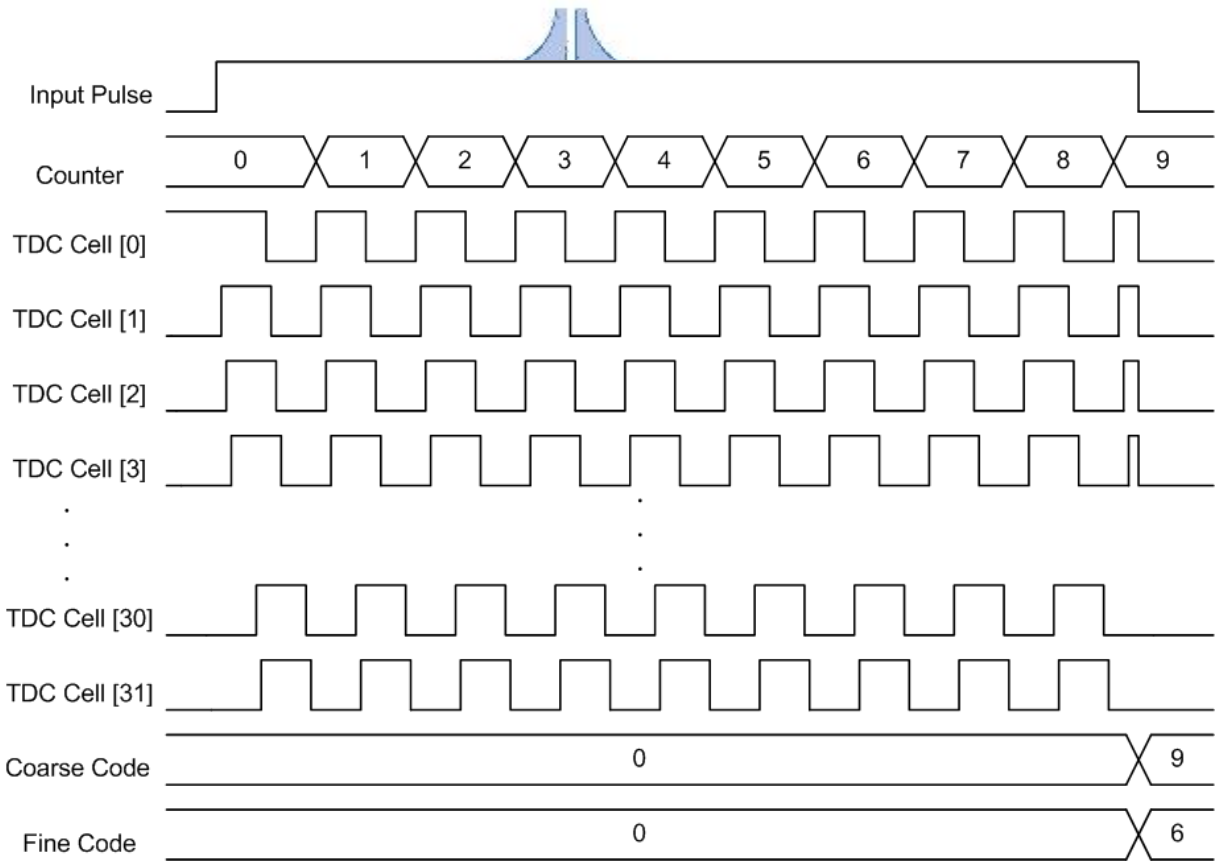


Fig. 3.8: The timing diagram of the ring based TDC.

An ambiguous condition exists in this ring based TDC architecture. If the "input_pulse"

falling when the positive edges of the oscillating signals arriving the counter, there will be a counting error. So we need an additional recovery circuit to compensate the counting errors. The recovery circuit uses a recovery latch to latch the signal passing information and compare with the counter's LSB. The condition could appear when the value of recovery latch and counter's LSB are different, and then the recovery circuit uses the residual pulse width information which has been latched to compensate the coarse code.

Eventually, the output of the TDC coarse counter (recovered) and the fine code decoder are combined as the TDC_output[13:0].

3.3.4 PVT Compensated Ring Based TDC

The variations of process, voltage and temperature (PVT) will cause a non-negligible effect on TDC resolution and make a mismatch in TDC result [27] such as two similar TDC quantization results correspond to two pulses with different pulse width. To compensate the effects which are caused by PVT variations, the PVT compensated ring based TDC has been presented. The architecture of the PVT compensated ring based TDC is shown in Fig. 3.9. We modify the ring based TDC in above section and make the delay buffers in each TDC cells can be "compensated". In other words, the gate delay of delay buffers is adjustable, and then we can fix the mismatch caused by PVT variation.

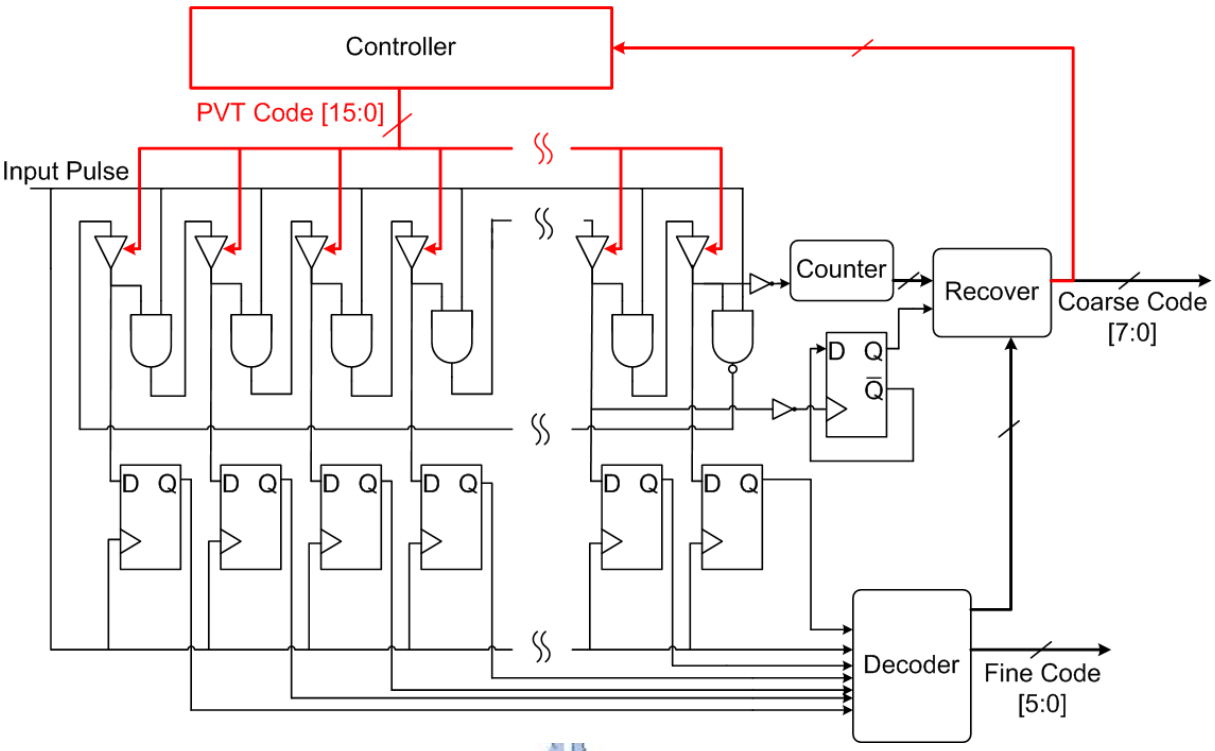


Fig. 3.9: The architecture of PVT compensated ring based TDC.

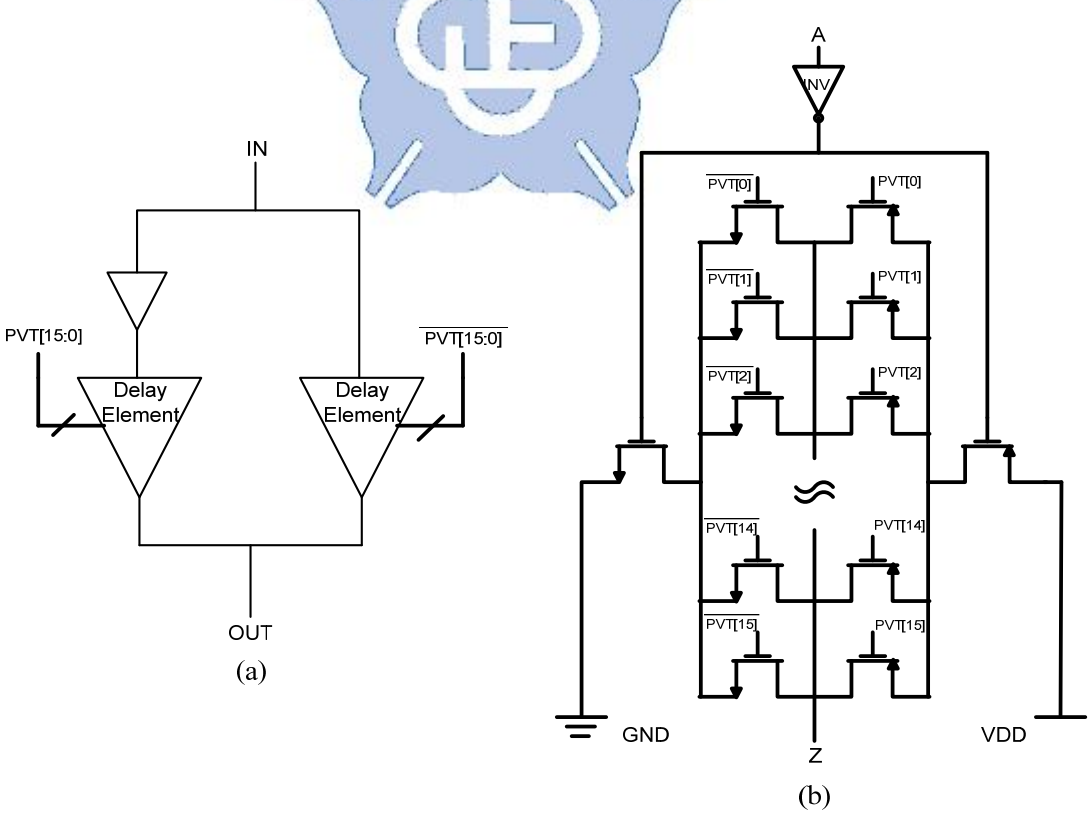


Fig. 3.10: The (a) architecture of the delay buffer, and (b) schematic of the delay element in each delay buffer.

For higher tuning resolution and better linearity, we use the interpolation-based delay cell [28] to be the delay buffer in each TDC cells. Fig 3.10 shows the architecture of the delay buffer in the PVT compensated ring based TDC.

The reference pulse generator produces a pulse with fixed pulse width and feeds it into TDC, and then the TDC will quantize the pulse width into digital codes. Without PVT variations, theoretically, the TDC will make no mismatch and the fixed pulse will be converted into a fixed code. Under PVT variations, if we can control the delay buffer's delay and make the fixed pulse always be quantized to a fixed code, then the mismatch of the TDC can be eliminated. Fig. 3.11 shows the operation flow of the TDC compensating.

The PVT compensating TDC will start self-testing and adjust the delay buffer's delay until the TDC code of the fixed reference pulse matches the TDC reference code which we have stored in the controller. The TDC reference code is from the simulation of the TDC quantization result for the fixed reference pulse under typical case (TT, 1.0V, 25°C).

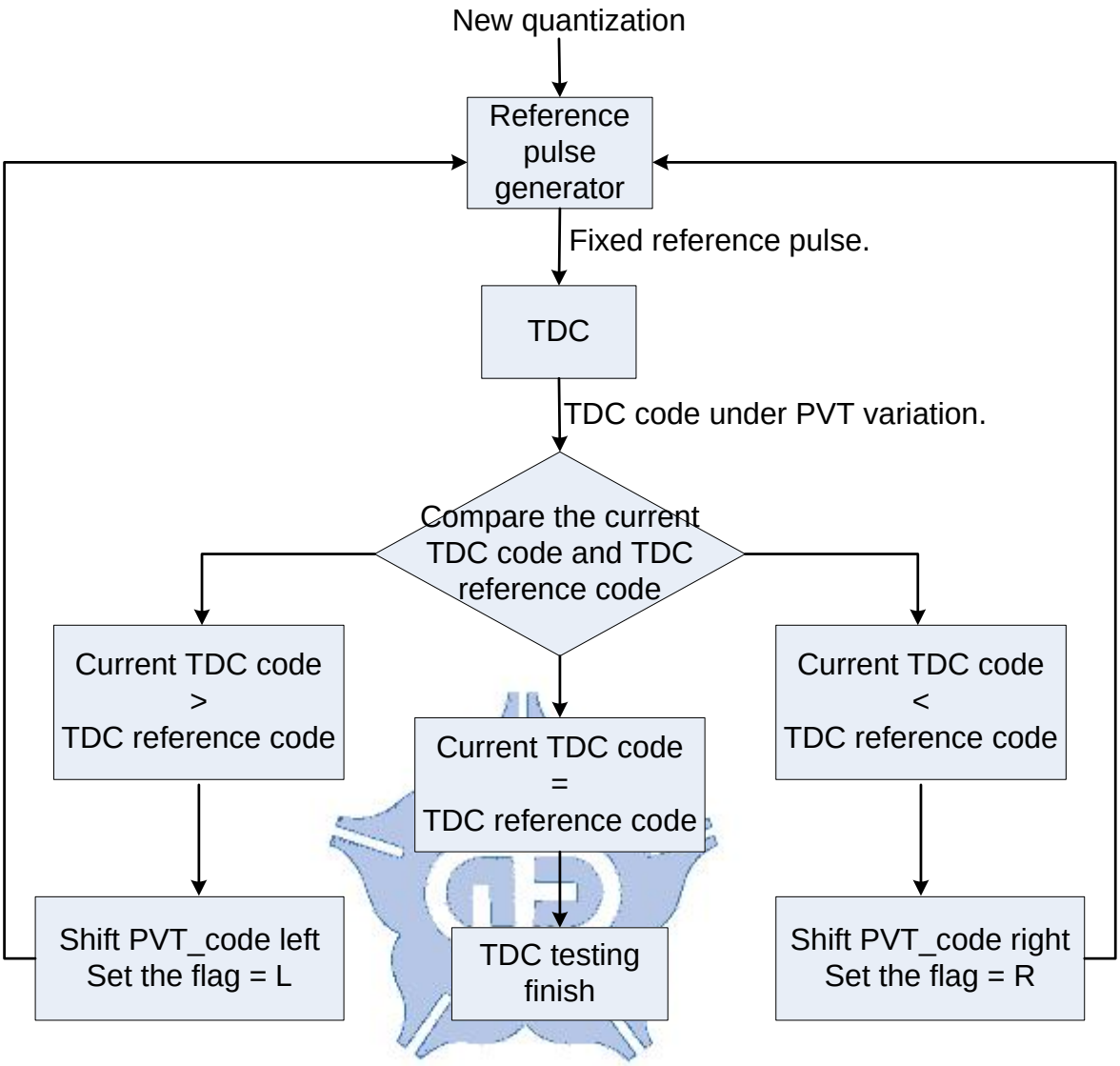


Fig. 3.11: Operation flow of the TDC's PVT compensating.

The main problem of the proposed PVT compensated TDC used in the smart temperature sensor is that the compensated delay range and resolution. Under the process and voltage (PV) variations, we need a wide range to compensate the delay shifts. But under the temperature (T) variations, we are desirous of better resolution.

3.4 Summary

Time-to-Digital Converter is one of the most important components in time-domain all-digital smart temperature sensor with timing-domain. The TDC's resolution and mismatch will have influence on the final output of the temperature sensor. Additionally, area, power and conversion time of TDC also need to be considered. So choosing a suitable TDC architecture is very significant.

Chapter 4

Auto-Calibration Technology in Smart Temperature Sensor

4.1 Thermometer Calibration

Thermometer calibration provides a way to regulate the temperature quantization uncertainties and mismatch which are caused by PVT variations and make the same value of two sensors correspond to different temperatures. In other words, the thermometer calibration is in order to optimize the sensor accuracy.

4.1.1 Conventional Calibration Method

The normal calibrating method to smart temperature sensor is using a thermometer with high accuracy and comparing the sensor output with the absolute temperature, and then trimming the sensor to correct the mismatch caused by process and voltage (PV) variations.

The calibration procedures are usually be performed at two levels, the die-level [29] and package level. Here we mainly discuss about the calibrating method after the die is packaged.

All smart temperature sensors need to be calibrated individually. In a widely use calibrating method like two-point calibration, we have to make the environment around the senor to be thermal equilibrium and comparing the sensor output to a thermometer which has been calibrated to finish the calibration for one point, and then repeat the above operation to

finish the other calibration for another point. A significant cost in the above calibrating method is that it will take a long time more than 15 minutes to make the environment to be thermal equilibrium. Additionally, the time for thermal equilibrium need to be doubled because every sensor needs to do this twice to complete the two-point calibration.

Another calibration method for smart temperature sensor is the reference voltage calibration [30]. However, the reference voltage calibrating method can only be used in smart temperature which is composed of voltage PTAT circuit like BJT based smart temperature sensor. Even though the reference voltage calibration does not need a temperature-stabilized environment [31], the BJT-based temperature sensor is still not suitable for dynamic thermal management applications. Therefore, for product cost reducing and dynamic thermal management, an all-digital smart temperature sensor with self -calibration or auto-calibration [*] is in need.

4.1.2 Auto-Calibration Method

The calibration circuit in our all-digital smart temperature sensor includes the temperature calibration circuit and the process compensating circuit. We will discuss process compensating circuit in the next section.

The main sensor circuit is composed of the cyclic delay line and the TDC. Although the temperature information is already converted into the digital codes, these digital codes must be calibrated before output. This because the process, voltage, and temperature variations make it impossible to create a fixed mapping between the absolute temperature values (°C) and the TDC's output codes. The timing diagram and operation flow of the temperature calibration circuit is shown in Fig. 4.1 and Fig. 4.2.

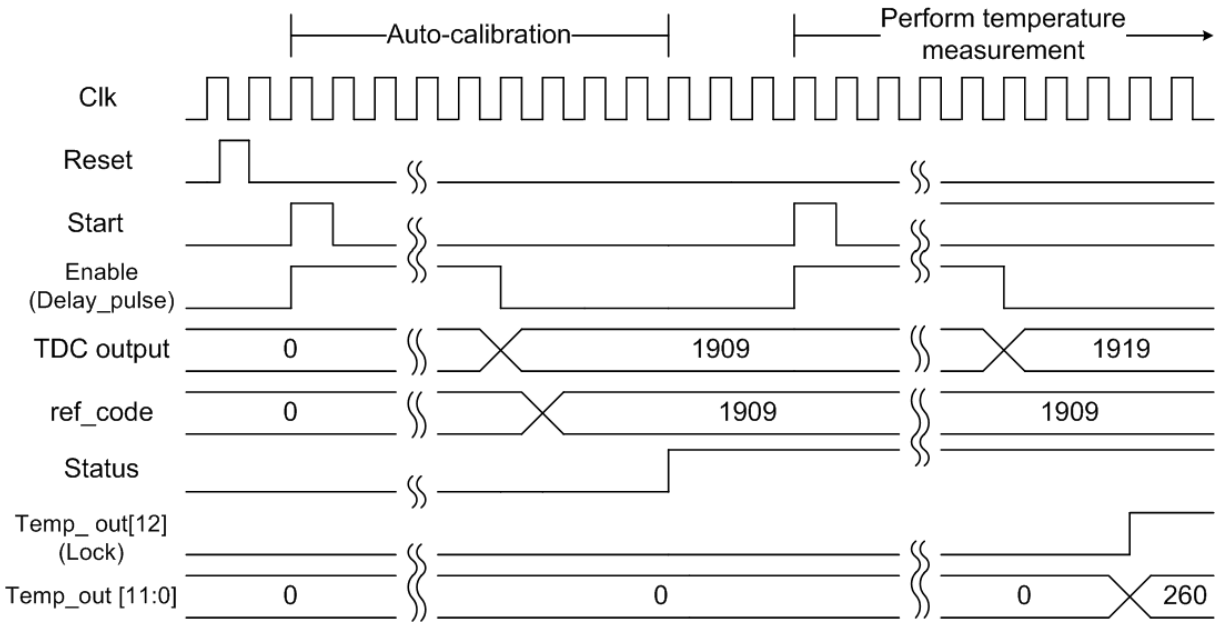


Fig. 4.1: Timing diagram of the temperature calibration circuit.

When system is reset, the on-chip temperature is assumed to room temperature at 25°C. Thus the reference code for room temperature can be generated. In Fig. 4.2, when the signal "Start" is enabled in auto-calibration phase, the first output of the main sensor circuit is stored as reference code for the temperature calibration circuit. After the reference code has been stored, the signal "Status" is pulled up to indicate that the sensor is ready for temperature measurement. Then when the temperature of the smart temperature sensor is changed, the new temperature value can be calculated from the difference between reference code and current TDC output code.

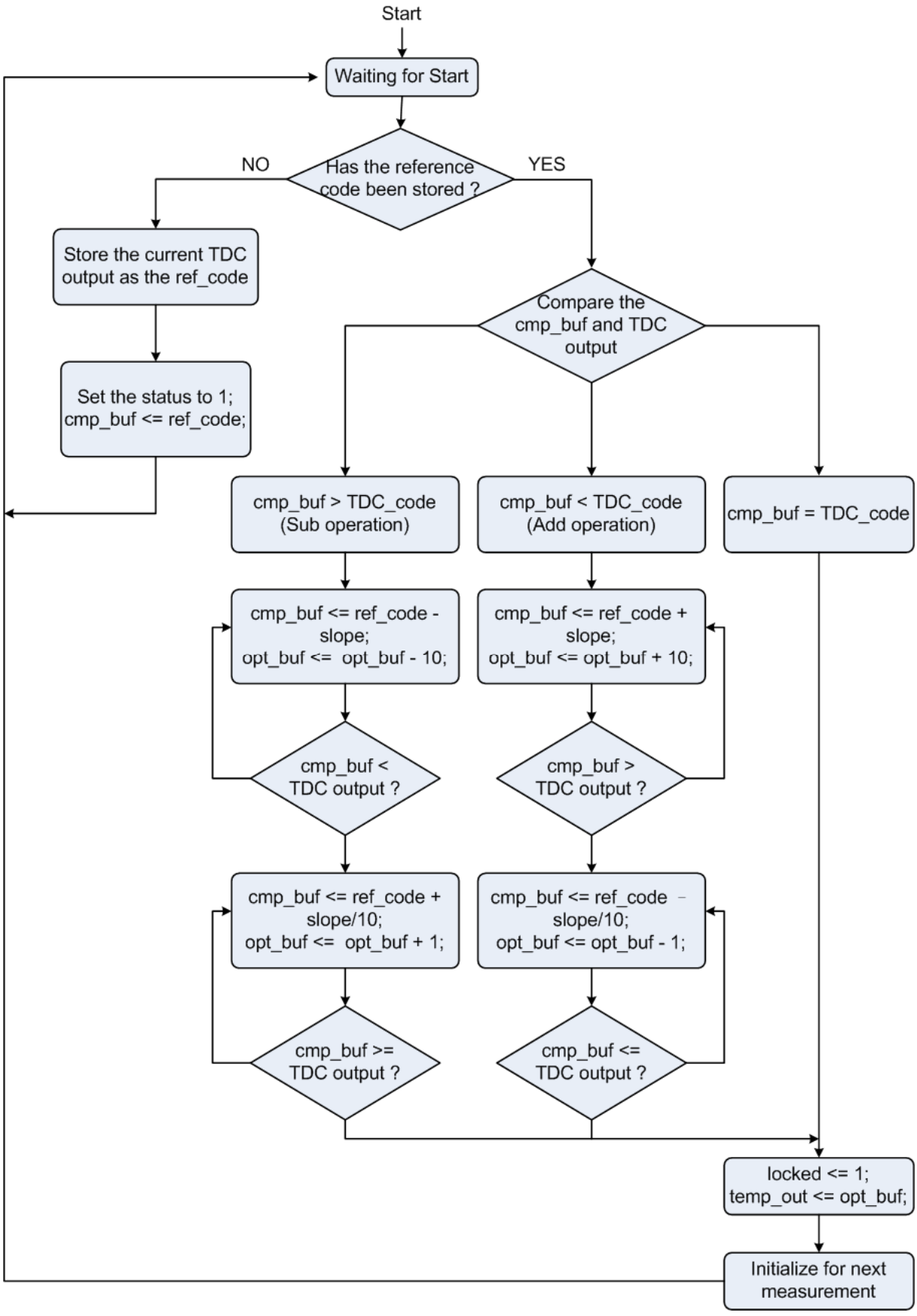


Fig. 4.2: Operation flow of the temperature calibration circuit.

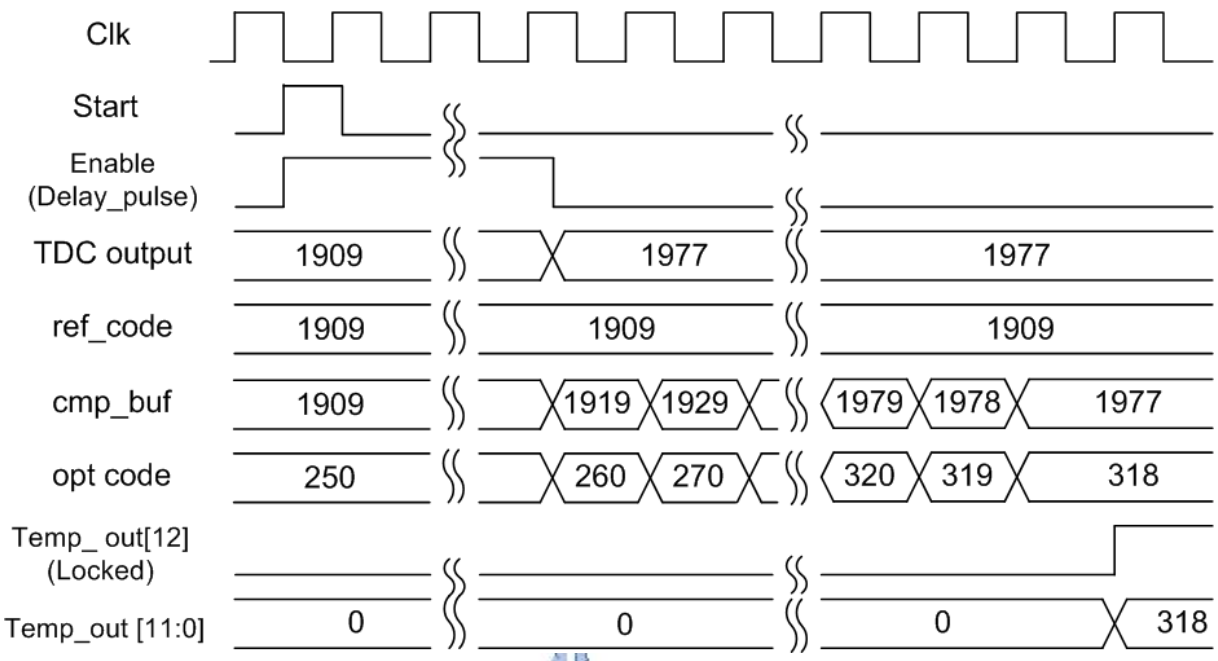


Fig. 4.3: the timing diagram of the temperature calculation.

To calculate the current temperature by the difference between reference code and current TDC output code, first we have to compare the code in "cmp_buf" and TDC output. The value in "cmp_buf" will be initialized to "ref_code" which was the TDC code we stored at 25°C. If "cmp_buf != tdc_code", then we use the slope (i.e. "10" in Fig 4.2) that has already been store in the smart temperature to add or sub to the "cmp_buf" until "cmp_buf = tdc_code". In this stage, there is a register call "opt_buf" and its value is been initialized to "250" (the origin point at 25°C). Incidentally, the unit digit of the value "250" is for decimal calculation (i.e. 25.0°C). Following the calculation of "cmp_buf", the "opt_buf" will also be added or subtracted by "10". After the "cmp_buf" is bigger than "TDC_code" with add operation or smaller than "TDC_code" with subtract operation, the slope will set to be tenth and the number we add or subtract to "opt_buf" will be changed form "10" to "1", and then repeat the temperature calculation above to approach the final temperature output. Finally,

when the "cmp_buf" is equal to the "TDC_code", the value in "opt_buf" will be the temperate value that we calculated and output. Fig 4.3 shows the timing diagram of the temperature calculation, and the final output is 31.8 °C.

After the calculation is finished, the lock signal "Temp_out[12] (Locked)" will be pulled up to indicate that the temperature output is valid. In practical applications, one of the on-chip temperature sensors can use the traditional two temperature point calibration. And the temperature at system reset can be determined from this calibrated sensor. As a result, the reference code generation is more accurate in other non-calibrated temperature sensors. Additionally, since the smart temperature sensor eliminates the two temperature points calibration on every temperature sensors, it is very suitable for current thermal management applications in SoC era.

4.1.3 Auto-Calibration Method with Dual-Slope

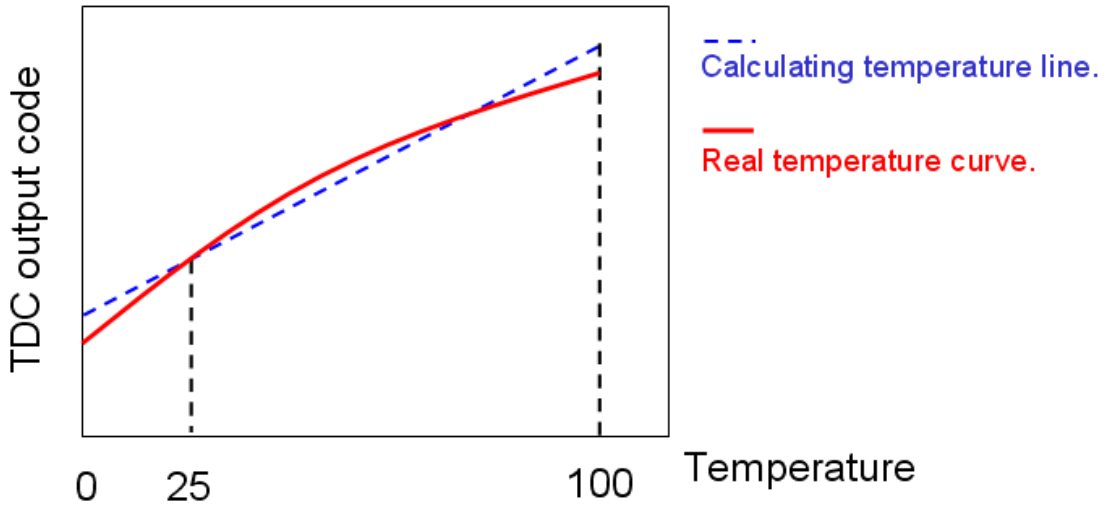
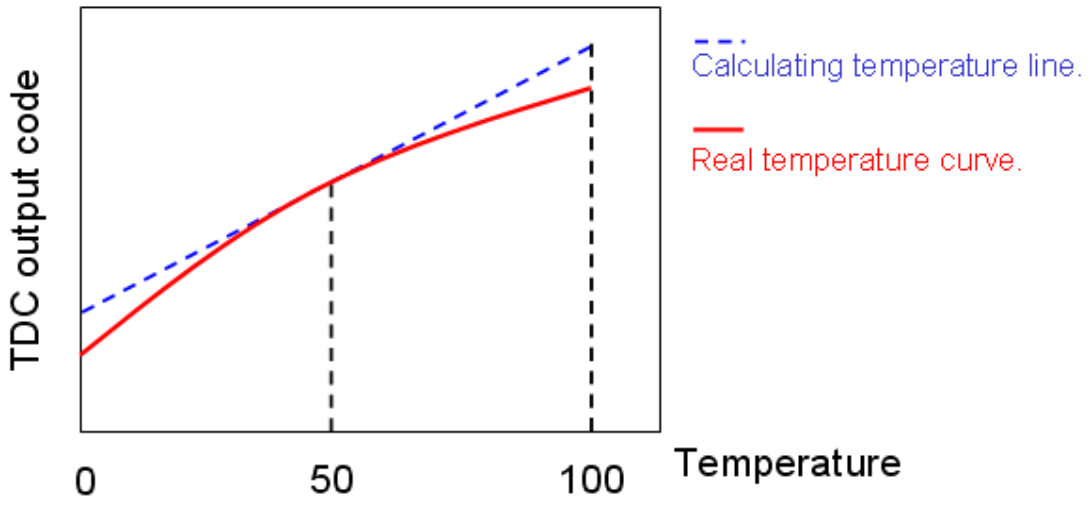


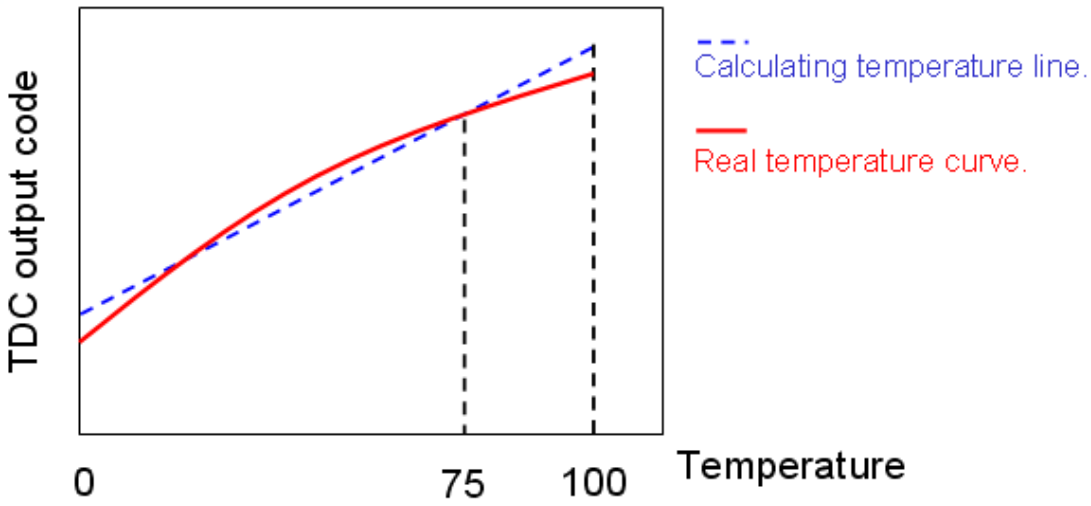
Fig. 4.4: The mismatch between the real temperature and the calculated temperature.

The temperature rising (flowing) tendency corresponds to the TDC output codes is not a straight line. Actually, it is a curve, and this will make some mismatches in our temperature

calculations which are based on slopes. The Fig. 4.4 shows the mismatch between the real temperature curve and the calculated temperature line with one slope. For easy understanding, the curvature of the real temperature curve in this figure is much bigger than it really is.



(a)



(b)

Fig. 4.5: The change for choosing temperature calculating origin, (a) 50 °C and (b) 75 °C

There is another problem we found that the choosing for temperature calculating origin. In section 4.1.2, the origin we assume for temperature calibrating is 25 °C. If we change the origin, the temperature calculating mismatch should be different, just like the Fig. 4.5.

Fortunately, the origin we chose is a good position for mismatch reducing between calculating temperature line and real temperature curve. Furthermore, if we choose the origin point at 75°C, the effect seems similar to the origin point has been set at 25 °C, and that's why the two-point calibration for temperature sensor usually takes this proportion of the two calibration points.

In Fig. 4.4, we can see that the large errors occur at the two extreme points, 0 °C and 100 °C. For further errors elimination, we use the dual slope temperature calculating method. The Fig. 4.6 shows the concept of the dual-slope temperature calculating method.

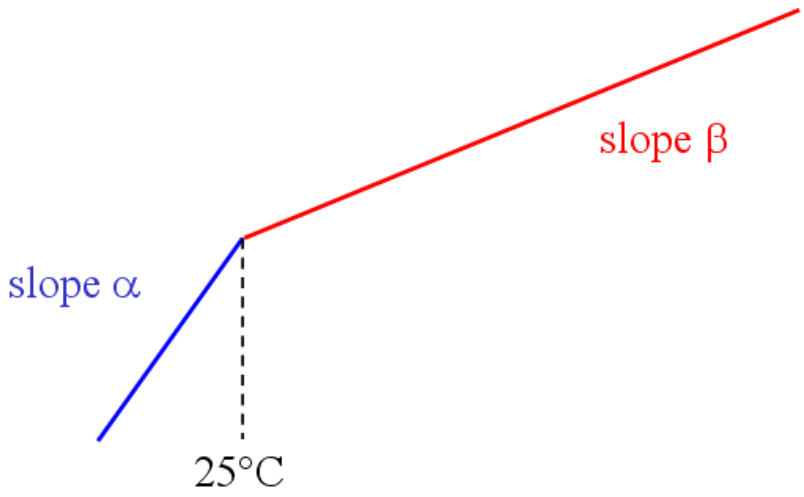


Fig. 4.6: The dual-slope temperature calculating method.

We spilt the original slope into two parts, the slope α and slope β, where the slope α is used for temperature calculating between 0 °C to 25 °C and the slope β is used between 25 °C

to 100 °C. In our temperature calculation in the above section, the slope will be change when the calculation is passing through 25°C (top down or bottom up). The simulation result in Fig. 4.7 shows that the max measurement error of the proposed temperature sensor can be reduced to -1.2 ~ 2.2 °C by the dual-slope temperature calculating method.

In fact, if we have more segments of different slopes, the accuracy will be increased in our temperature calculation. Nevertheless, more segments and slopes mean more storage.

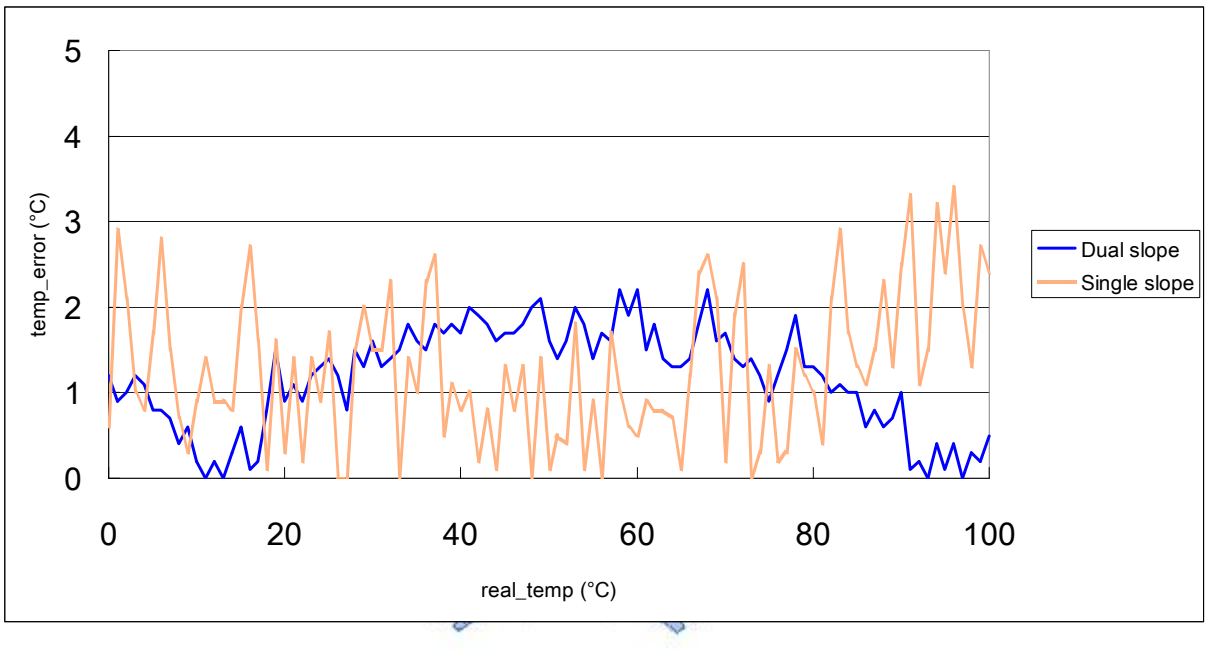


Fig. 4.7: The comparison of simulation result between dual slope temperature calculating and single slope temperature calculating.

4.2 Compensation for Process Variations

In the above section, we have discussed about the calibration for temperature. The other part of the calibration circuit, is the process compensating circuit. In Chapter 1, we saw that process variations in smart temperature sensor can be compensated by dual delay lock loops [17]. However, the consumption of area and power are very large.

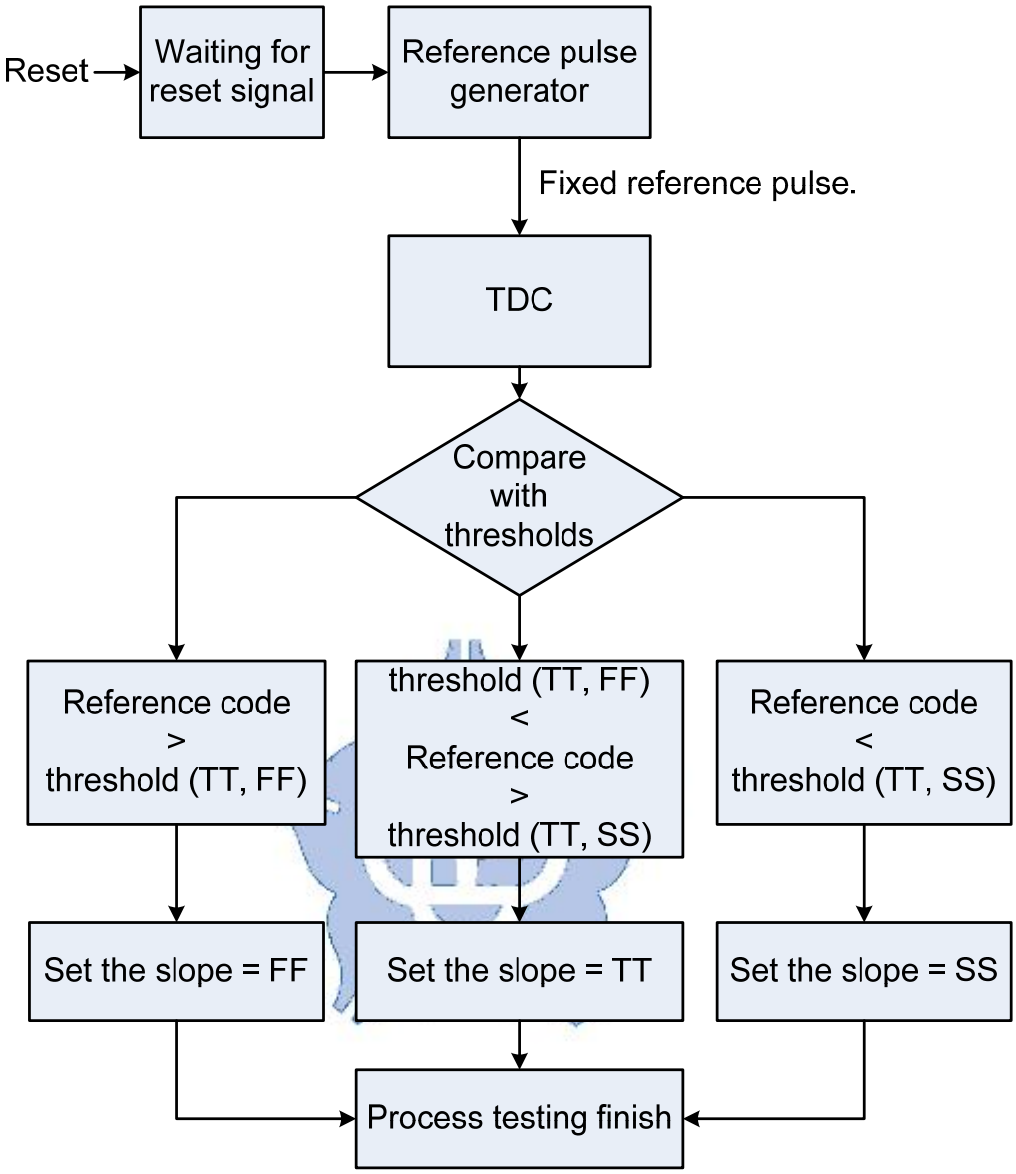


Fig. 4.8: The operation flow of the process compensating circuit.

The presented process compensating circuit in full-fledged version smart temperature sensor uses the quantization result of the pulse with fixed width to choose the slope which is been used in temperature calibrating calculation to compensate the process variation. The operation flow of the process compensating circuit is shown in Fig. 4.8.

Every time when system is booting or resetting (we assume that the booting environment

is 25°C), the reference pulse generator will produce a pulse with fixed pulse and feed it into TDC, and then output a reference code. After the reference code has been generated, it will compare to the two thresholds which are threshold (TT, FF) and threshold (TT, SS), where the first threshold (TT, FF) is the average of the TDC code by simulation at (TT, 1.0v, 25°C) and (FF, 1.0v, 25°C) and the second threshold (TT, SS) is the average of the TDC code by simulation at (TT, 1.0v, 25°C) and (SS, 1.0v, 25°C). If the reference code is higher than the threshold (TT, FF), then the smart temperature sensor is operated at fast case and the slope will be set to FF. If the reference code is lower than the threshold (TT, SS), the smart temperature sensor is operated at slow case and the slope will be set to SS. Otherwise, the sensor is at the typical case, so the slope will be set to TT. The slope which has been selected will be used in temperature calibrating calculation in the temperature calibration circuit.

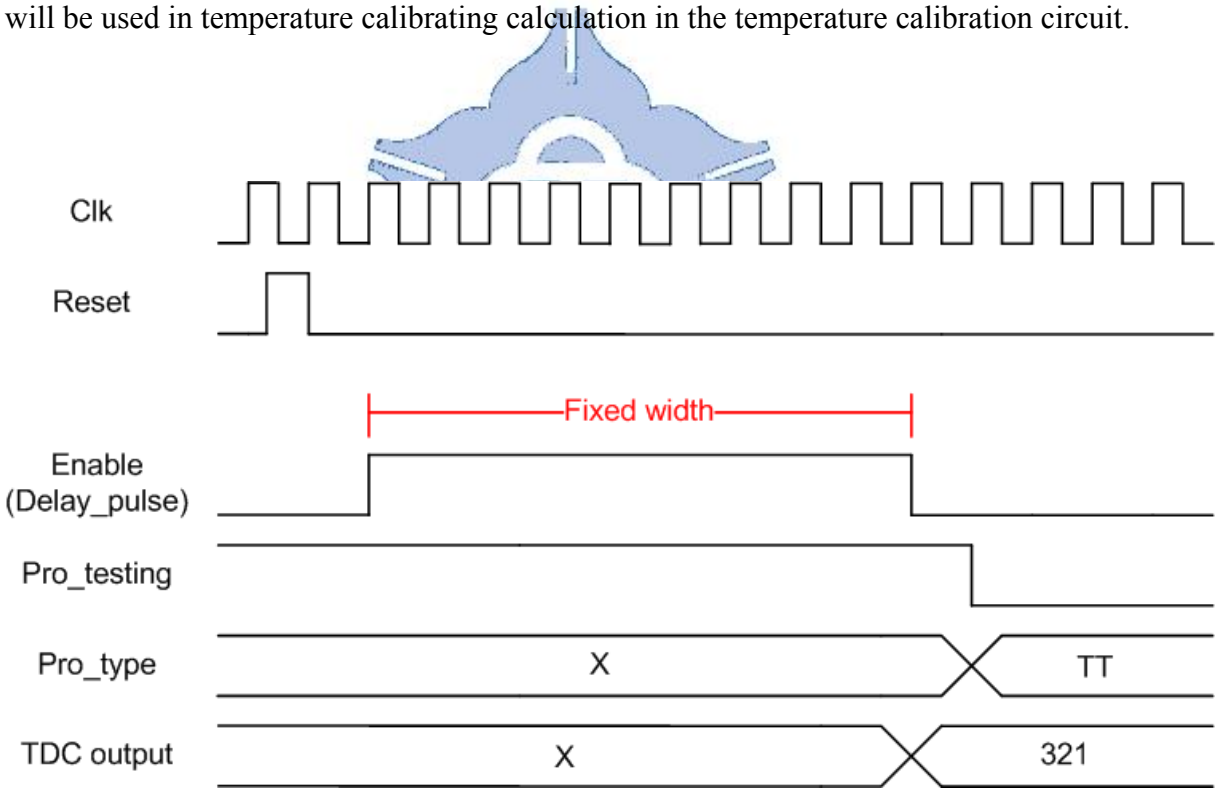


Fig. 4.9: The timing diagram of the process compensating circuit

Fig. 4.9 shows the timing diagram of the process compensating circuit. The delay pulse with fixed width is generated by the reference pulse generator, and then the TDC output the

quantization result of the delay pulse for comparing to threshold (TT, FF) and threshold (TT, SS). Here we assume that threshold (TT, FF) = 400 and threshold (TT, SS), so the TDC output "321" is smaller than threshold (TT, FF) and bigger than threshold (TT, SS). As a result, the process type "Pro_type" will be decided to typical and so will the slope.

4.3 Summary

In this chapter we discuss about the calibration circuit in our smart temperature sensor. The conventional method of temperature sensor calibrating like two-point calibration can be eliminated. Additionally, the calibration of temperature and compensation of process are both automatic at the chip (system) is booting or resetting, the calibration efforts of temperature sensor can be significantly reduce.

Chapter 5

Implementations and Measurement Results

5.1 All-Digital Smart Temperature Sensor Test Chips

5.1.1 Specification

The proposed all-digital smart temperature sensor test chip is fabricated on a standard performance (SP) 65nm CMOS process. The specifications and characteristics are shown in table 5.1 and table 5.2, and the microphotograph of the test chip is shown in Fig. 5.1.

Table 5.1: The features of the proposed all-digital smart temperature sensor test chip.

Components	Type
Delay line	Cyclic Delay line.
TDC	Ring Based TDC.
Calibrating Method	One-point auto-calibration with single slope.

Table 5.2: The features of the proposed all-digital smart temperature sensor test chip.

Parameter	Value	Unit
Resolution	0.143	°C
Power Consumption	55 (@10KHz)	μW
Area	644 x 644 (with IO pad)	μm^2
Temperature range	0 ~ 100	°C

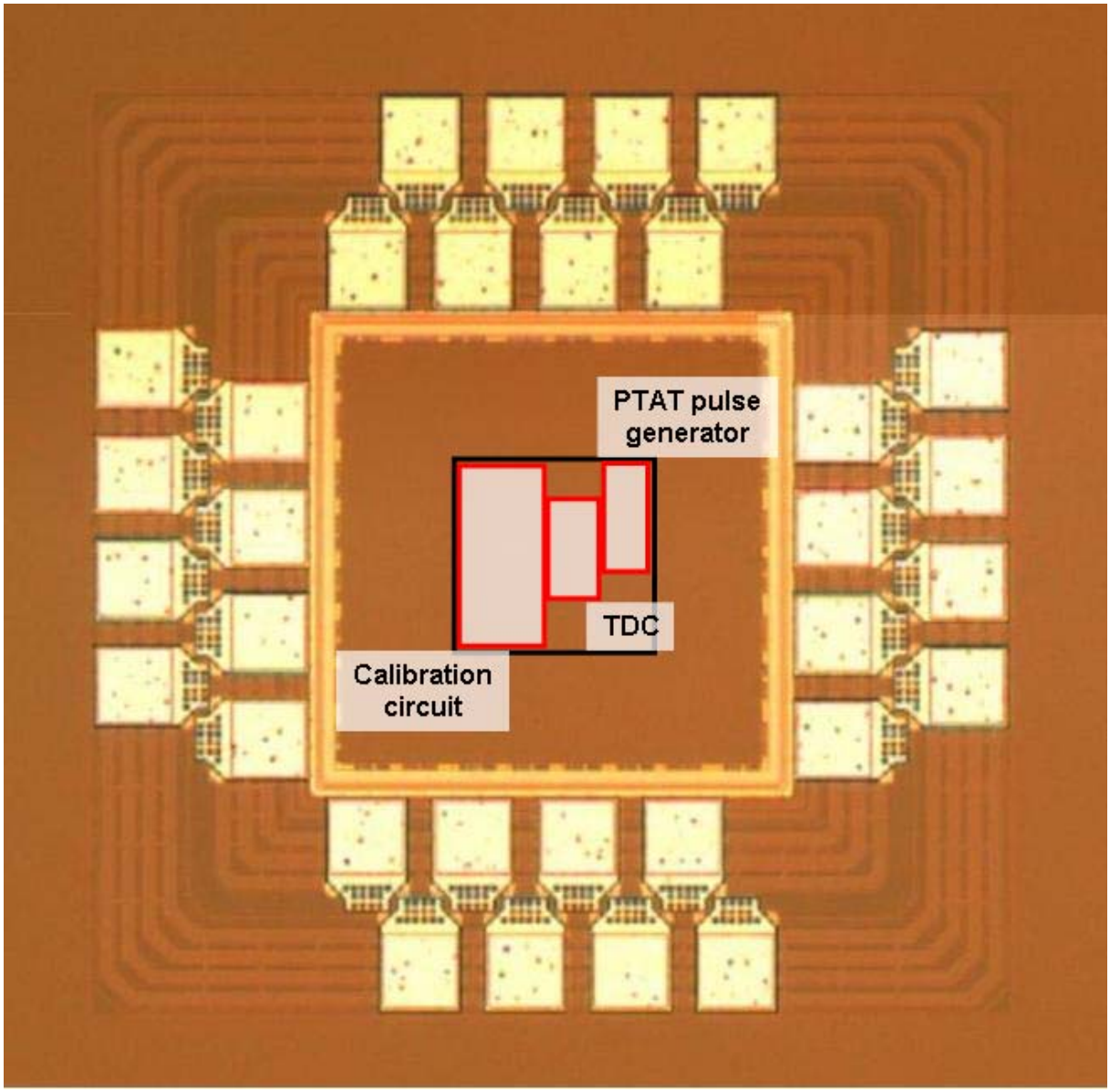


Fig. 5.1: The microphotographic of the all-digital smart temperature sensor test chip.

5.1.2 Simulation Result

Fig. 5.2 shows the simulation results of the all-digital smart temperature sensor test chip in different temperatures ranges from 0°C to 100°C under typical process.

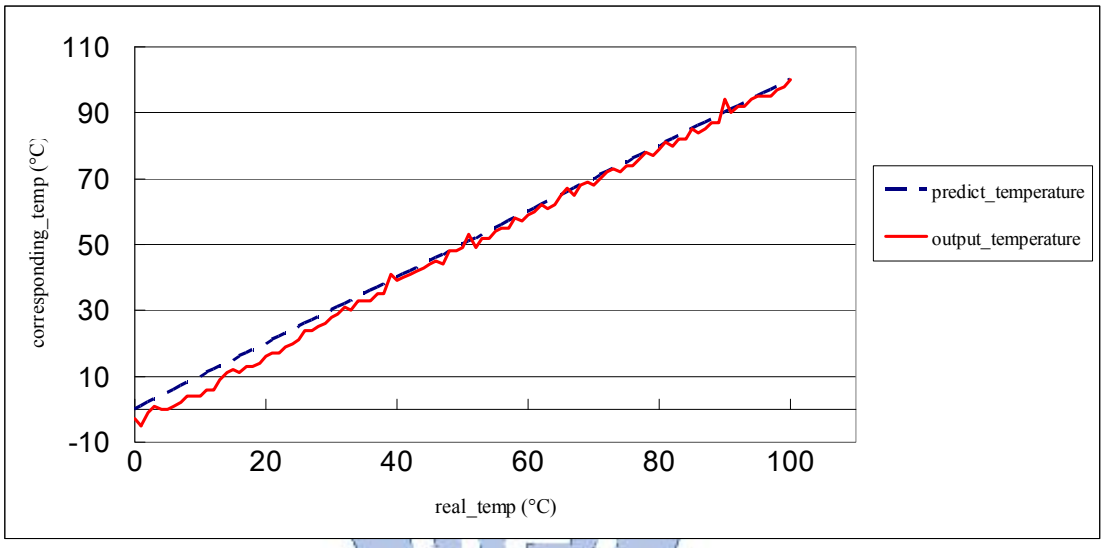
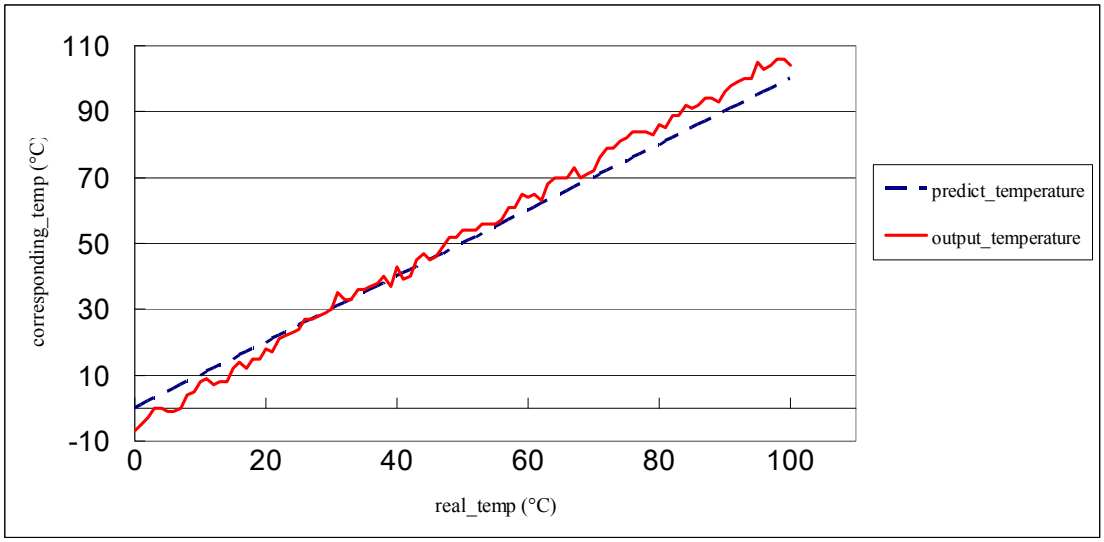
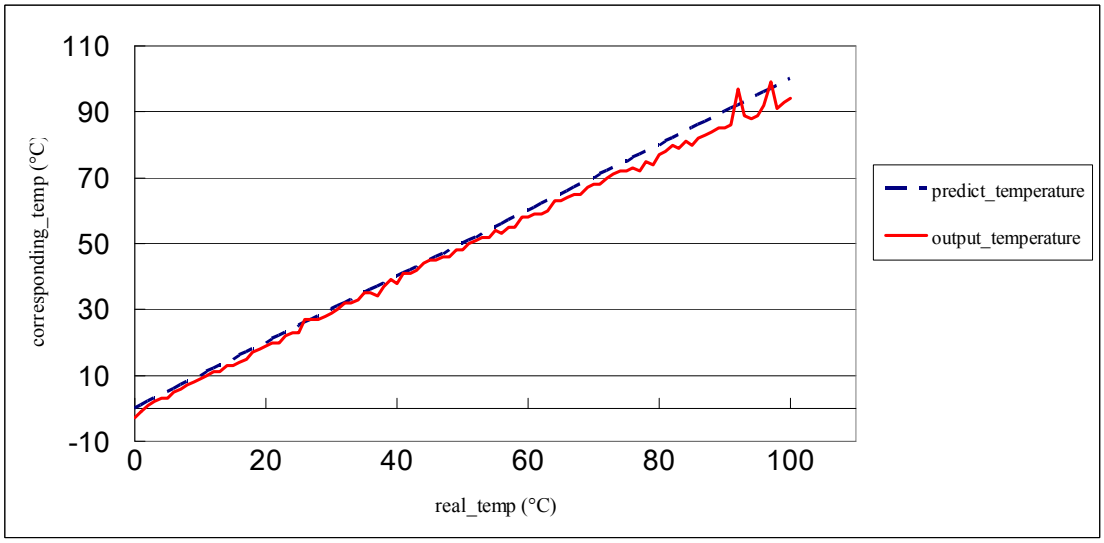


Fig. 5.2: The simulation results of the all-digital smart temperature sensor test chip from 0 °C to 100 °C under typical process.

The line "predict_temperature" means the ideal temperature predictor, and the line "output_temperature" means the real output temperature value of the smart temperature sensor circuits. The difference between these two lines is often caused by nonlinearity of the delay line in smart temperature sensor, the bit resolution in calibration circuit, and the TDC resolution limitation. Additionally, the simulation results of the all-digital smart temperature sensor test chip under different process variations are shown in Fig. 5.3.



(a)



(b)

Fig. 5.3: The simulation results of the all-digital smart temperature sensor test chip from 0 °C to 100 °C under process variations, (a) FF and (b) SS.

Because the process variation will affect the slope of temperature rising/falling trend, the accuracy of the temperature sensor become worse. Fig. 5.4 and table 5.3 show the accuracy of the all-digital smart temperature sensor test chip.

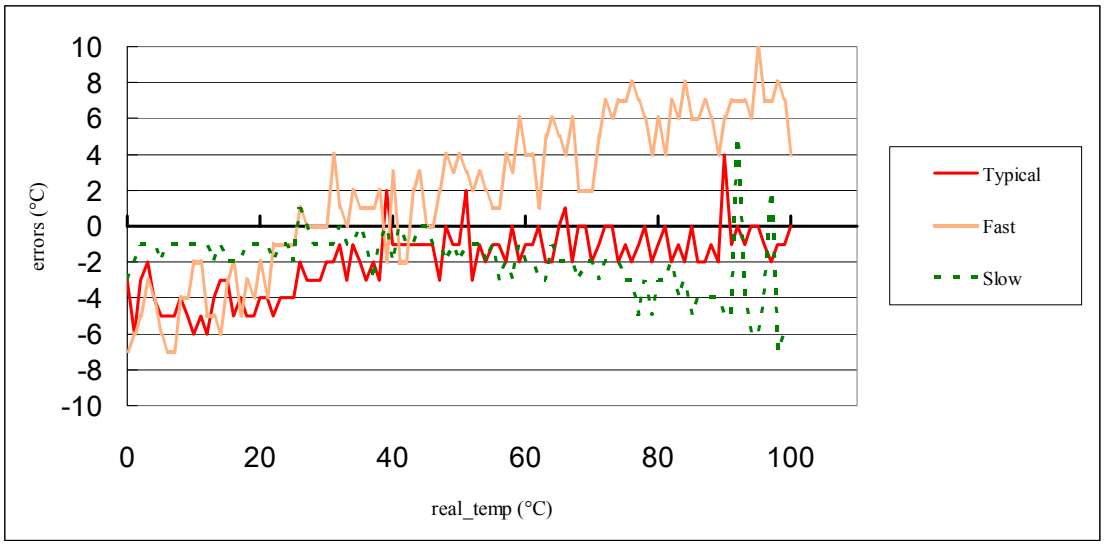


Fig. 5.4: The accuracy of the all-digital smart temperature sensor test chip simulation results.

Table 5.3: The accuracy of the all-digital smart temperature sensor test chip.

	Max.	Min.	Avg.	Unit
Errors	4.0	- 6.0	± 2.13	°C
Errors (w/ process variations)	10.0	- 7.0	± 2.75	°C

5.1.3 Measurement Result

The measurement environment of the all-digital smart temperature sensor test chip is shown in Fig. 5.5.

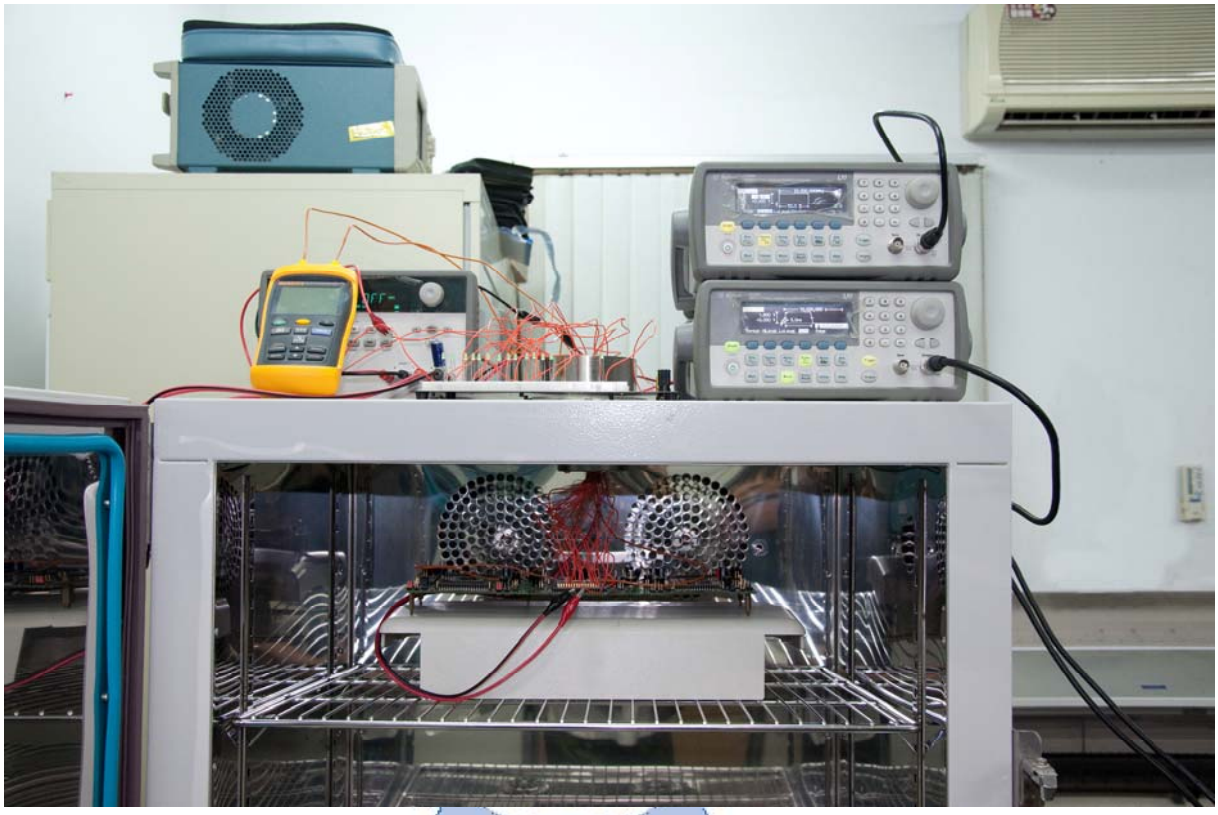


Fig. 5.5: The measurement environment of the all-digital smart temperature sensor test chip.

The installations on the Oven temperature incubator from left to right are thermometer for absolute temperature measurement, power supply for pad power and core power, light emitting diodes (LEDs) for chip output displaying and two Agilent 33220A waveform generators for the "start" signal triggering and the reference clock (20MHz). Fig. 5.6 shows the measurement results of three chips.

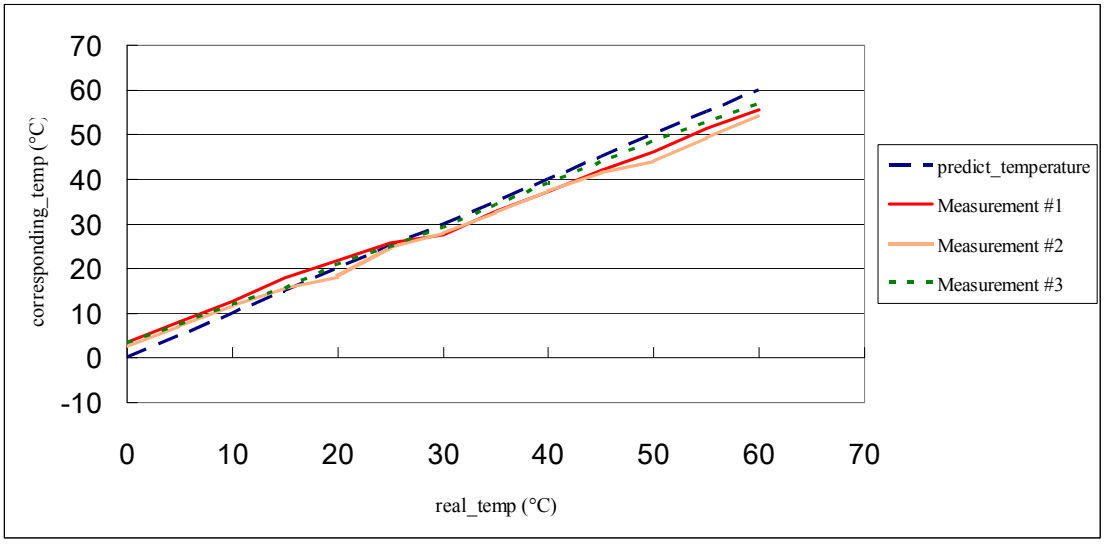


Fig. 5.6: The measurement results of three all-digital smart temperature sensor test chips.

The interval in temperature measurement is 5°C and the measurement range is 0°C to 60°C because the printed circuit board (PCB) is not heat-resistant. In the three measurements we can see that the slopes of temperature rising/falling trend are smaller than the slope in typical and hence we can say that the three measured chips are all trending to slow case. Fig. 5.7 and table 5.4 show the accuracy of the three chips measurement results.

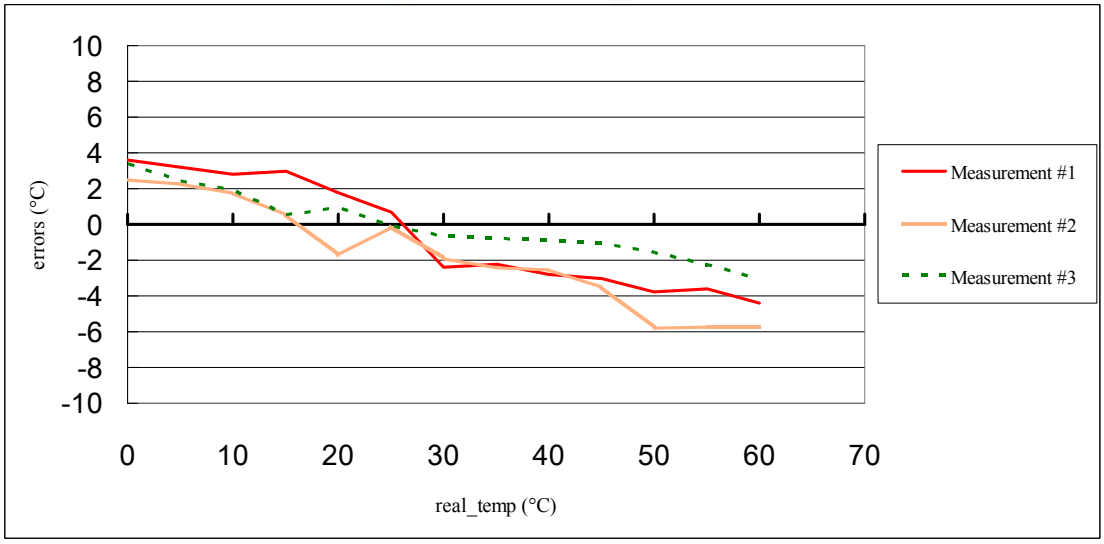


Fig. 5.7: The accuracy of three all-digital smart temperature sensor test chips measurement results.

Table 5.4: The accuracy of three all-digital smart temperature sensor test chips measurement results.

	Max.	Min.	Avg.	Unit
Errors	3.6	- 5.8	± 2.39	℃

5.1.4 Comparisons of Recent Smart Temperature Sensors

Table 5.5: Comparisons of the all-digital temperature sensor test chip with recent smart temperature sensors.

	Resolution (°C)	Error (°C)	Calibration	Power	Area (mm^2)	Conversion Rate (samples/s)	Range (°C)	CMOS Tech.
[13]	0.01	±0.1 (3σ)	One-point with post-silicon trimming	247μW @ 3.3V	4.5	10	-55~125	0.7μm
[14]	0.16	-0.7~0.9	Two-point	0.49mW @ 3.3V	0.175	1K	0~100	0.35μm
[15]	0.058	-1.5~0.8	Two-point	8.4μW @ 2.5V	N/A	2	0~75	FPGA
[16]	0.0918	-0.25~0.35	Two-point	36.7μW @ 3.3V	0.6	2	0~90	0.35μm
[17]	0.66	-1.8~2.3	One-point with dual DLL	12mW @ 1.2V	0.16	5K	0~100	0.13μm
Test chip	0.143	±10	Auto calibration	55 μW @ 1.0V	0.01	10K	0~100	65nm

Table 5.5 lists the comparisons of the smart temperature sensor test chip with recent smart temperature sensors. In all-digital smart temperature sensors [14], [15] and [16], the all-digital smart temperature sensor test chip can achieve higher conversion rate with low power consumption. And the two-point temperature calibration is eliminated in the proposed smart temperature sensor design with auto-calibration. Although the temperature error is very small (± 0.1°C) in [13], this BJT-based temperature sensor is not suitable for dynamic thermal management applications. And in [17], the high power consumption and large chip area makes it is also not suitable for dynamic thermal monitoring.

5.2 The Full-Fledged Version All-Digital Smart Temperature Sensor

5.2.1 Specification

The all-digital smart temperature sensor test chip is fabricated on a standard performance (SP) 65nm CMOS process. The specifications and characteristics are shown in table 5.6 and table 5.7, and the chip layout is shown in Fig. 5.8.

Table 5.6: The features of the proposed full-fledged version all-digital smart temperature sensor.

Components	Type
Delay line	Cyclic Delay line.
TDC	Ring Based TDC.
Calibrating Method	One-point auto-calibration with dual slope and Process variation compensating.

Table 5.7: The specifications of the full-fledged version all-digital smart temperature sensor.

Parameter	Value	Unit
Resolution	0.139	°C
Power Consumption	150 (@10KHz)	μW
Area	644 x 644 (with IO pad)	μm^2
Temperature range	0 ~ 100	°C

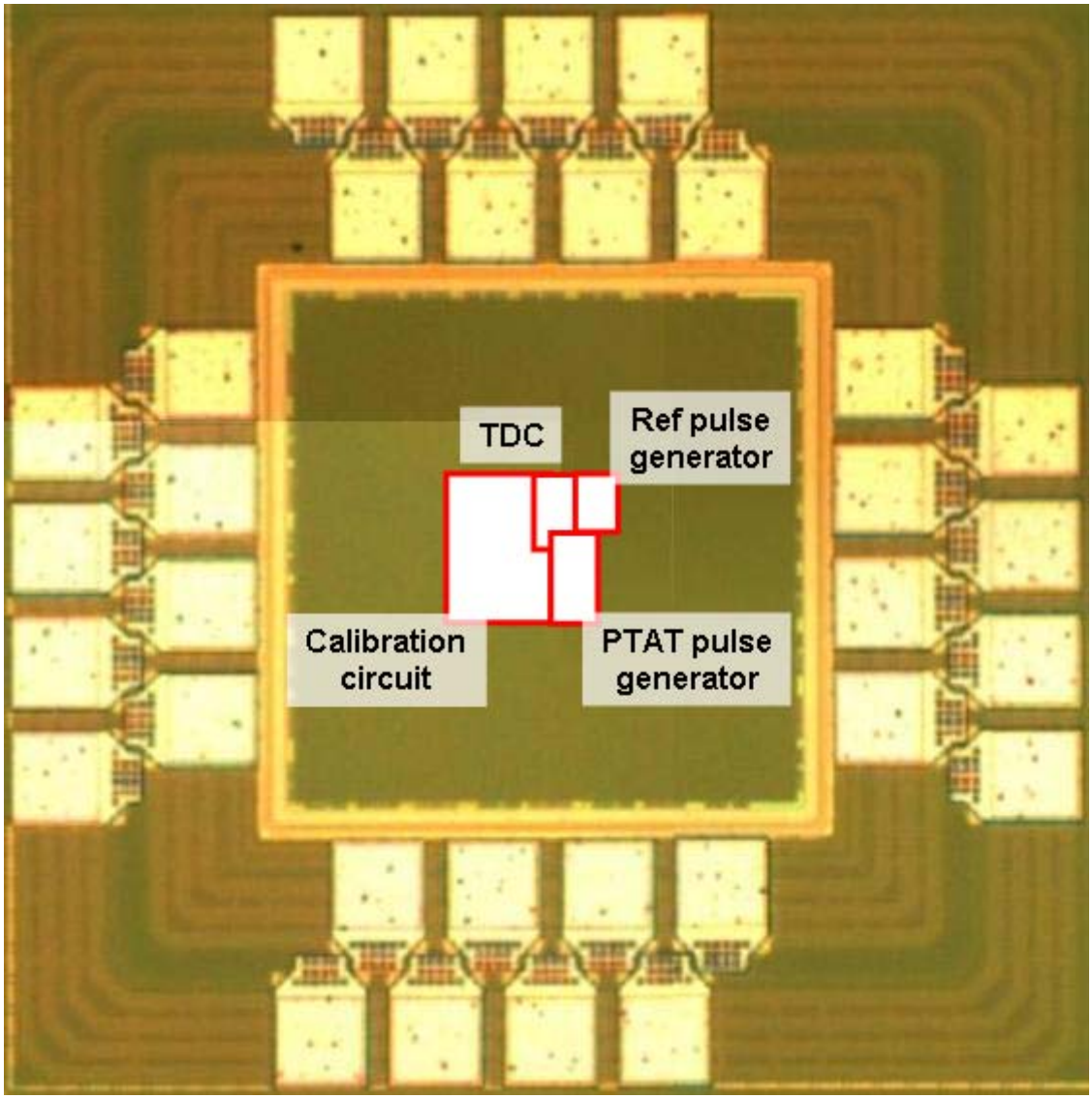


Fig. 5.8: The microphotographic of the full-fledged version all-digital smart temperature sensor test chip.

5.2.2 Simulation Result

Fig 5.9 shows the simulation results of the full-fledged version all-digital smart temperature sensor in different temperatures ranges from 0°C to 100°C under typical process.

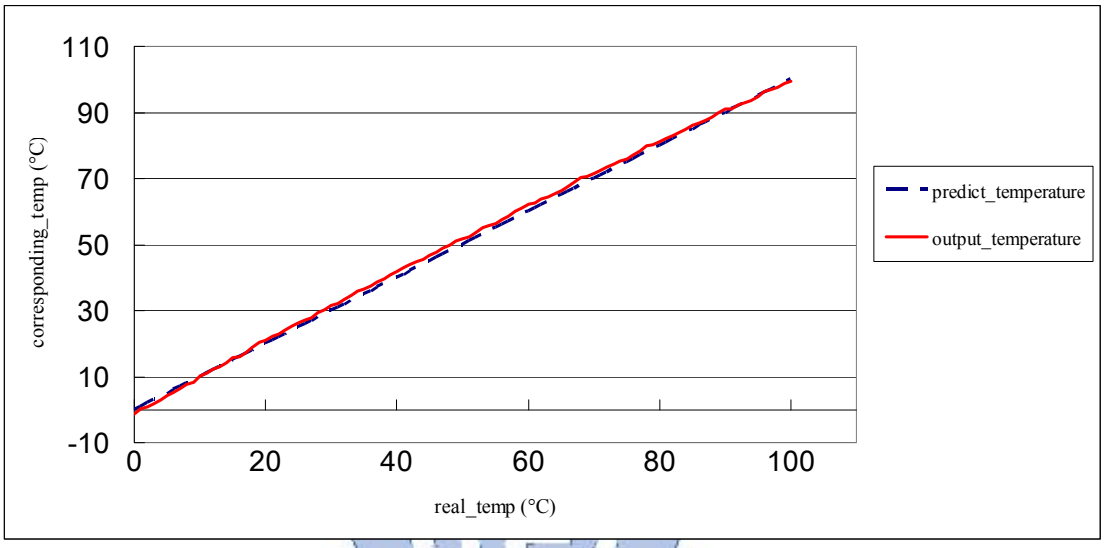
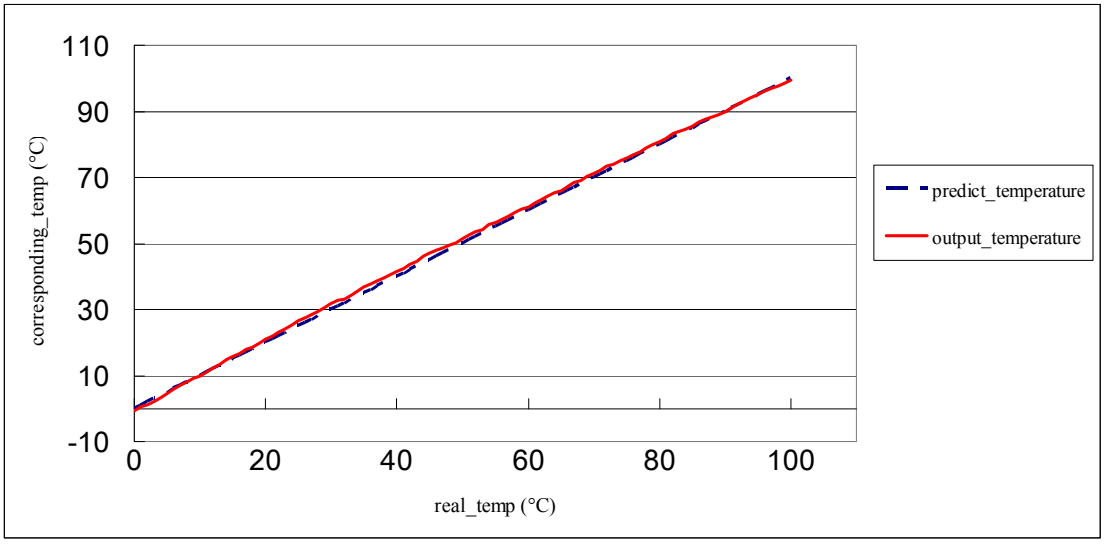
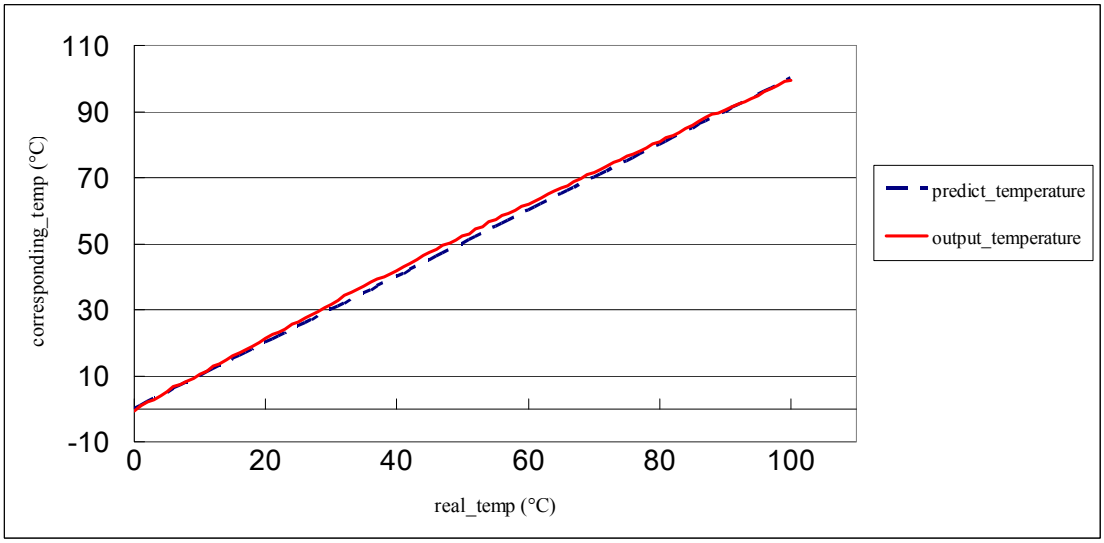


Fig. 5.9: The simulation results of the full-fledged version all-digital temperature sensor from 0 °C to 100 °C under typical process.

Just like the above section, the line "predict_temperature" means the ideal temperature predictor, and the line "output_temperature" means the real output temperature value of the all-digital smart temperature sensor circuits. The difference between these two lines has been reduced by the TDC with delay cells as the delay buffers instead of latches and the dual slope calibrating method. The simulation results of the all-digital smart temperature sensor under process variations are shown in Fig. 5.10.



(a)



(b)

Fig. 5.10: The simulation results of the full-fledged version all-digital temperature sensor from 0 °C to 100 °C under process variations, (a) FF and (b) SS.

We can find that the process variation effects have been reduced significantly with the proposed process compensation. Fig. 5.11 and table 5.8 show the accuracy of the full-fledged version all-digital smart temperature sensor. Compared to previous all-digital smart

temperature sensor test chip, the accuracy has been improved.

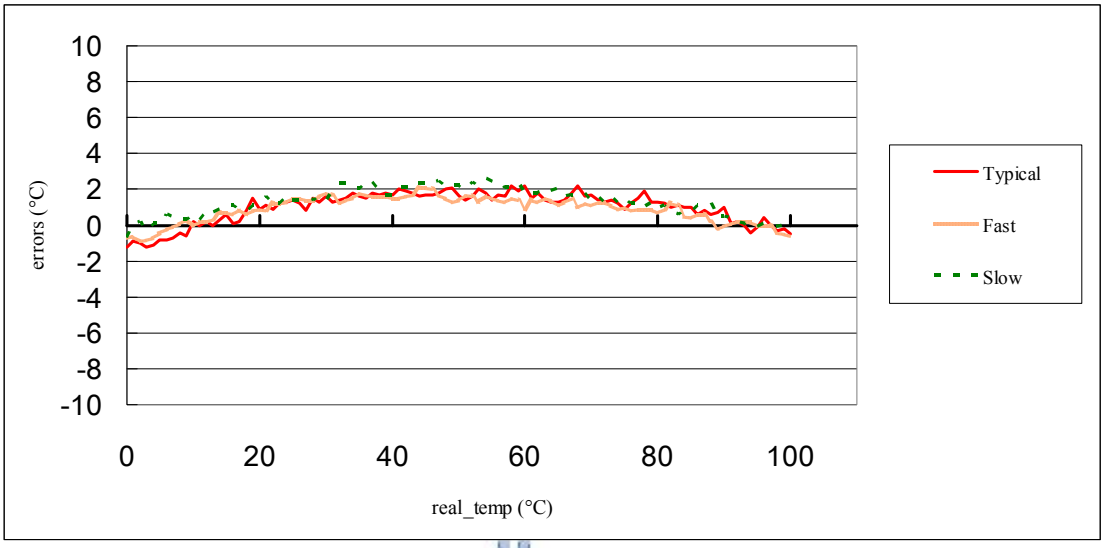


Fig. 5.11: The accuracy of the full-fledged version all-digital temperature sensor under process variations.

Table 5.8: The accuracy of the full-fledged version all-digital temperature sensor under process variations.

	Max.	Min.	Avg.	Unit
Errors	2.2	-1.2	± 1.17	°C
Errors (w/ process variations)	2.6	-1.2	± 1.17	°C

5.2.3 Measurement Result

The measurement environment of the full-fledged version all-digital smart temperature sensor is similar to the all-digital smart temperature sensor test chip which is shown in Fig. 5.5. The Fig. 5.12 shows the measurement results of three full-fledged version all-digital

smart temperature sensor chips.

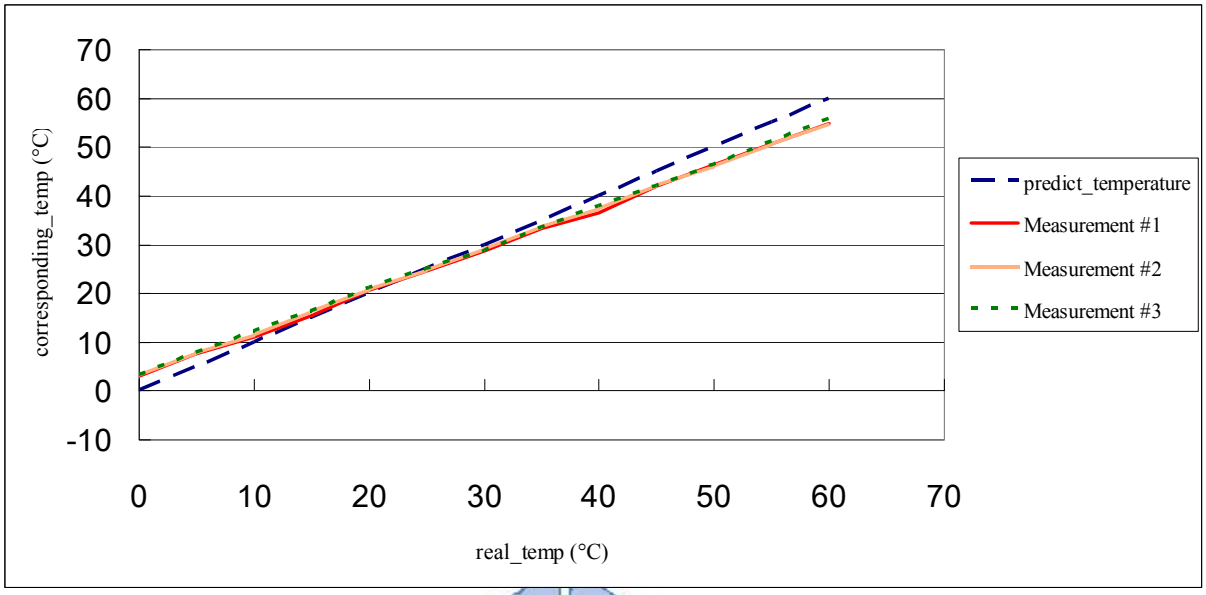


Fig. 5.12: The measurement results of three full-fledged all-digital smart temperature sensor chips.

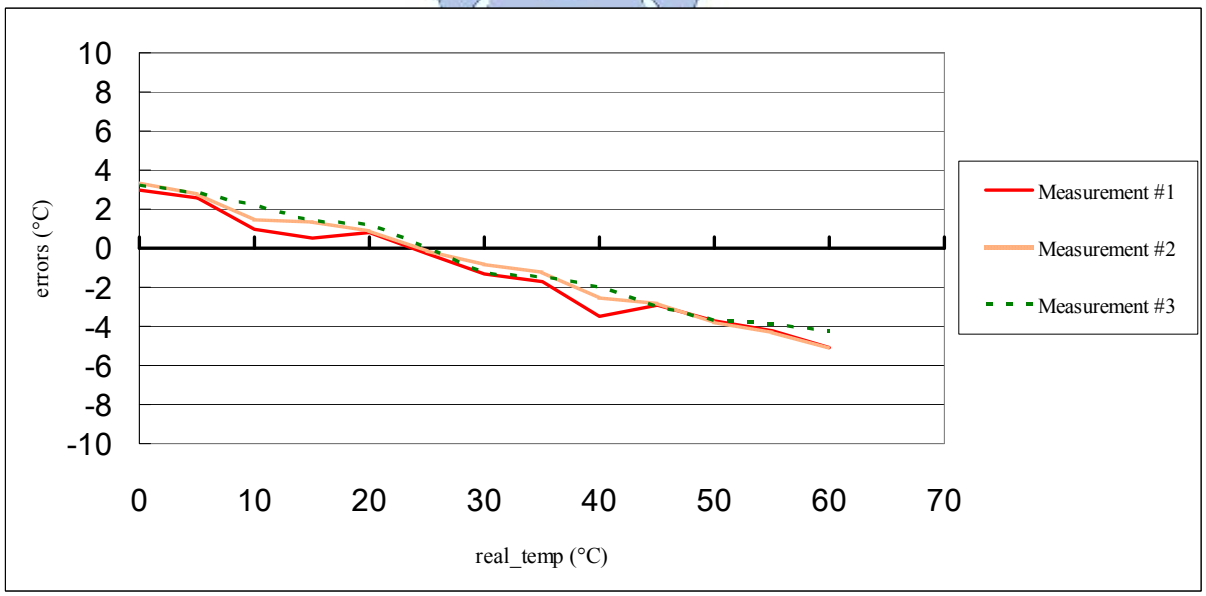


Fig. 5.13: The accuracy of three full-fledged version all-digital smart temperature sensor chips measurement results.

The interval in temperature measurement is 5°C and the measurement range is 0°C to 60°C because the printed circuit board (PCB) is not heat-resistant. In the three measurement results we can see that the slopes of temperature rising/falling trend are smaller than the slope in typical and from this we can say that the three measured chips are all trending to slow case. Fig. 5.13 and table 5.9 show the accuracy of the three chips measurement results.

Table 5.9: The accuracy of three full-fledged version all-digital smart temperature sensor chips measurement results.

	Max.	**Min.**	**Avg.**	**Unit**
Errors	3.4	-5.1	± 2.35	°C

5.2.4 Comparisons of Recent Smart Temperature Sensors

Table 5.5 lists the comparisons of the full-fledged version smart temperature sensor with recent smart temperature sensors. The proposed design keeps the characteristic in all-digital and auto-calibration of the smart temperature sensor test chip above. Additionally, the full-fledged version all-digital smart temperature sensor improves the accuracy of temperature measuring with a little power consumption rising.

Table 5.10: Comparisons of the full-fledged version smart temperature sensor with recent smart temperature sensors.

	Resolution (°C)	**Error (°C)**	**Calibration**	**Power**	**Area (mm^2)**	**Conversion Rate (samples/s)**	**Range (°C)**	**CMOS Tech.**
[13]	0.01	±0.1 (3σ)	One-point with post-silicon trimming	247μW @ 3.3V	4.5	10	-55~125	0.7μm
[14]	0.16	-0.7~0.9	Two-point	0.49mW @ 3.3V	0.175	1K	0~100	0.35μm
[15]	0.058	-1.5~0.8	Two-point	8.4μW @ 2.5V	N/A	2	0~75	FPGA
[16]	0.0918	-0.25~0.35	Two-point	36.7μW @ 3.3V	0.6	2	0~90	0.35μm
[17]	0.66	-1.8~2.3	One-point with dual DLL	12mW @ 1.2V	0.16	5K	0~100	0.13μm
Test chip	0.143	±10	Auto calibration	55 μW @ 1.0V	0.01	10K	0~100	65nm
Full fledged version	0.139	-5.1~3.4	Auto calibration	150 μW @ 1.0V	0.01	10k	0~60	65nm

5.3 All-Digital Smart Temperature Sensor Implemented with FPGA.

5.3.1 All-Digital Smart Temperature Sensor in CCU SoC Criti-Core Integration Project

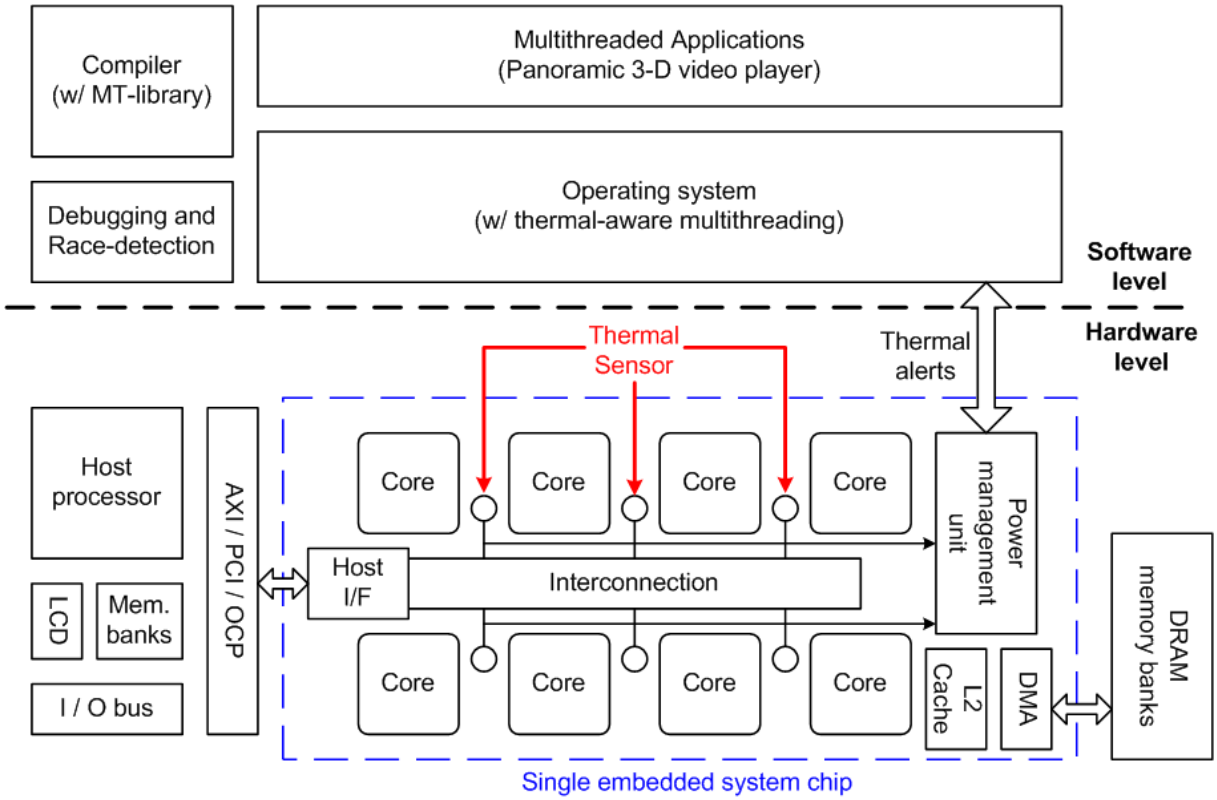


Fig. 5.14: The Cirticore computer system architecture.

This work was supported in part by the National Science Council of Taiwan, R.O.C., under Grant NSC98-2220-E-194-013. In this project, we will design an on-chip all-digital thermal sensor and integrate the sensor into Cirticore architecture for thermal information supporting to raise the reliability of the whole computer system. The Cirticore computer

system is a multi-core CPU system and its architecture is shown in Fig. 5.12.

5.3.2 Implementations on FPGA

In the first year demo of the National Science Council (NSC) project, the Criti-Core CPU will be implemented on FPGA to present the performance of multi-core CPU. Therefore, we have to port a smart temperature sensor which is completely all-digital for Criti-Core integrating onto the FPGA board.

Because the propagation delay of logic gates on FPGA is so large, the ring based TDC in section 3.3 can not have a fine resolution. Therefore, the TDC in this smart temperature sensor is the clock sampling TDC. Additionally, the proposed auto-calibrating method can not be used on the FPGA, we use the two-point calibration and simpler smart temperature sensor architecture to port onto FPGA board [15] and the smart temperature sensor is shown in Fig. 5.13.

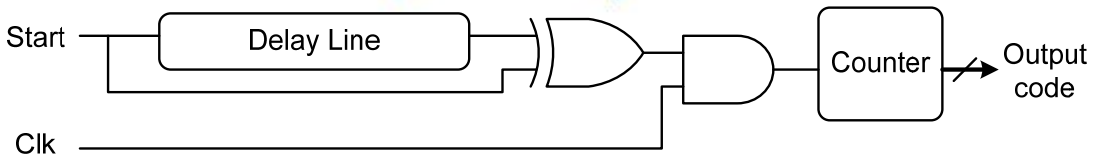


Fig. 5.15: The smart temperature sensor for FPGA porting.

The signal "Start" is controlled by the external I/O on FPGA board, and the reference clock "Clk" is the internal clock of FPGA board [33]. Every temperature measuring will start when the signal "Start" rising. After every measurement, the output code will be written to the memory address where the ARM CPU continually polling.

5.3.3 Corresponding Design with ARM CPU

For corresponding design with ARM CPU, we must make our temperature sensor become a peripheral device of the ARM CPU. Therefore, we have to build the Advanced microcontroller bus architecture High-performance Bus (AHB) for interconnection between the ARM CPU and the peripheral device (i.e. smart temperature sensor) [34].

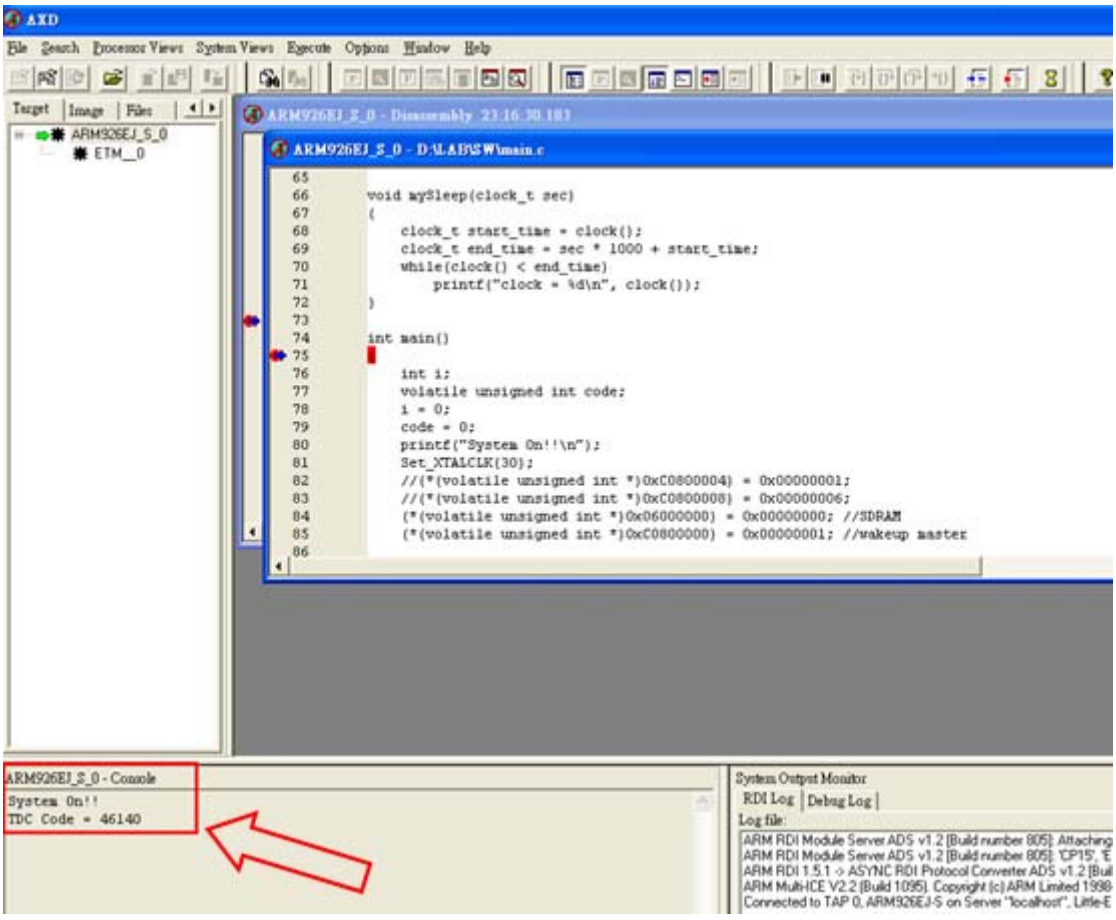


Fig. 5.16: The output of the smart temperature sensor on the FPGA board.

After the measurement is finished, the temperature information will be written to the memory address which the ARM CPU is continually polling. Every time the data of the memory address has been changed, the ARM CPU will read the new data just as shown in

specified Fig 5.14 (by AXD Debugger for ARM Developer Suite 1.2).

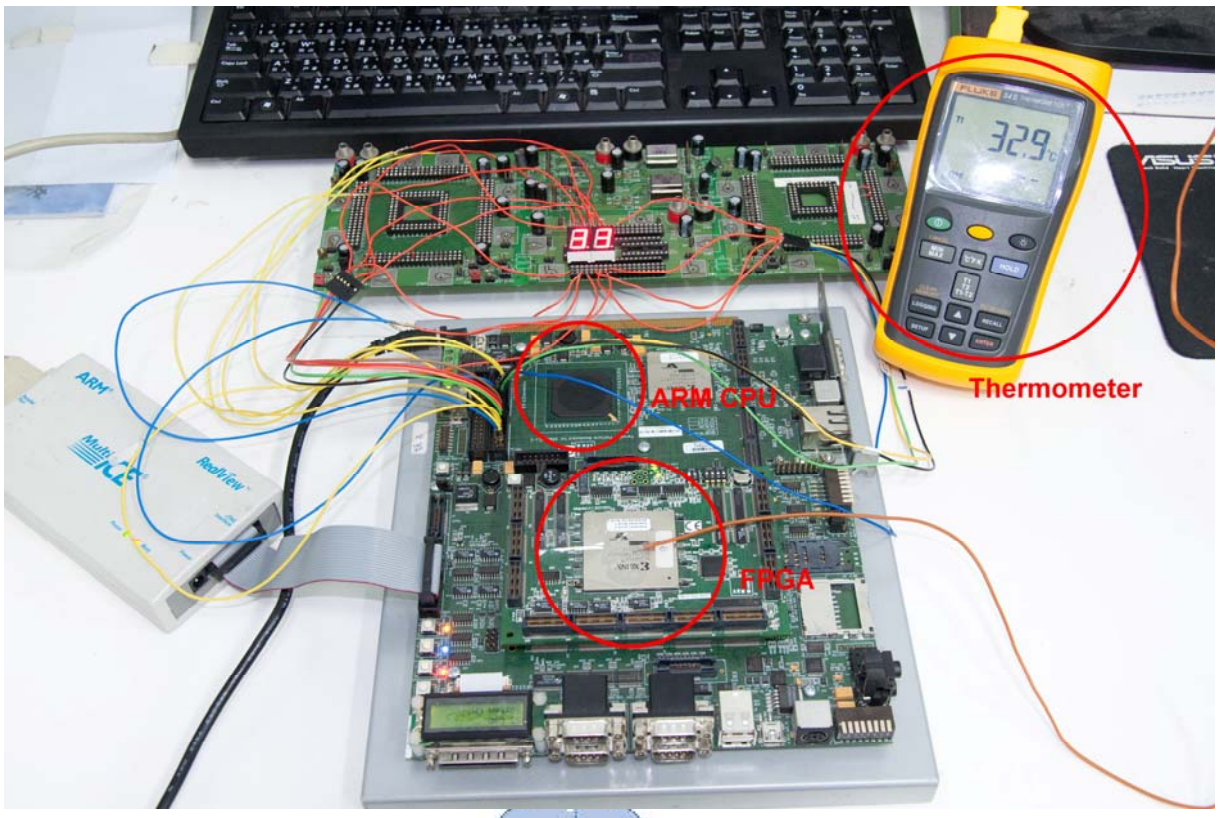
Because the auto-calibration can not be used on FPGA, we must do the two-point calibration for the temperature sensor. The two-point calibration can be implemented in a ARM executable file with C code, so the output result form the smart temperature sensor circuit can be calibrated by the ARM CPU and display the temperature information in Celcius degree (°C).

To display the temperature information which was outputted from the smart temperature sensor on FPGA, we use the ARM CPU to control the general purpose input/output (GPIO) of the FPGA board, and then use GPIO to output signals to control two external seven-segment display for thermal displaying.

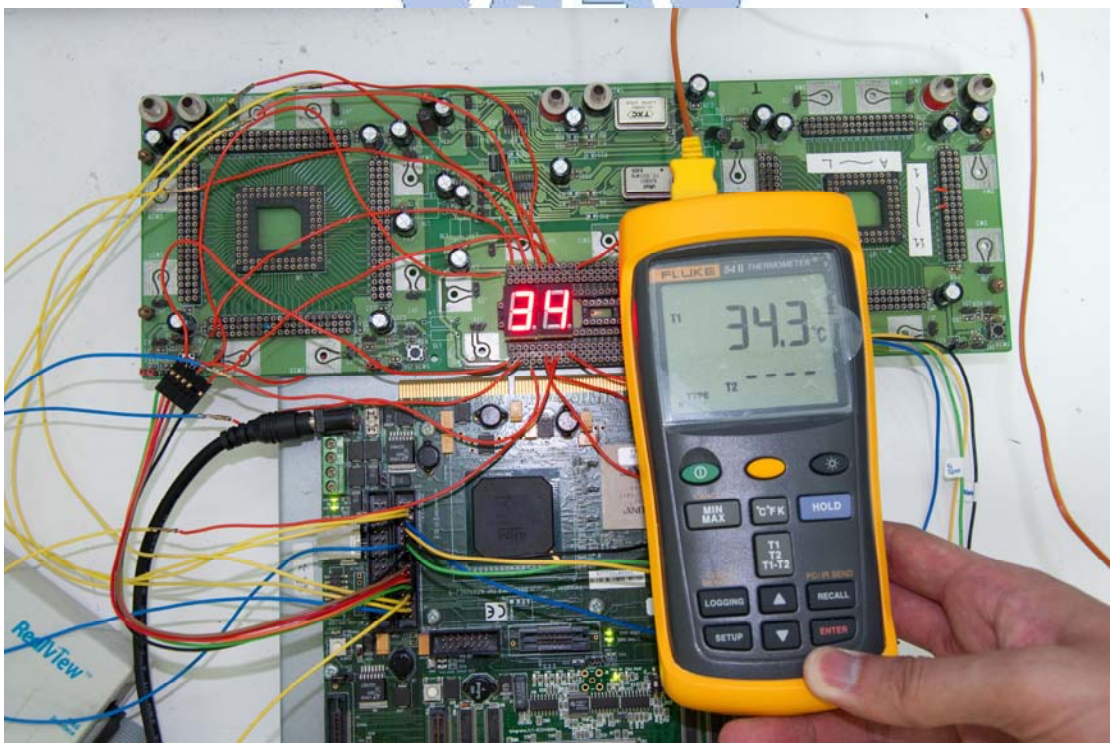
5.3.4 Criti-Core Project Demo

This demo of Criti-Core project is at May 7, 2010, in National Chung Cheng University and the installations of the demo environment are listed below:

- ARM RealView ® Versatile/PB926EJ-S Board.
- AXD Debugger for ARM Developer Suite 1.2
- FLUKE 54II Thermometer.
- TATUNG THD-90J hair dryers.



(a)



(b)

Fig. 5.17: The (a) demo environment and (b) thermal information displaying from the smart

temperature sensor on FPGA board.

At first, we show the temperature measuring result (on 7-seg display) of the smart temperature sensor at room temperature (about 25°C), and there is a thermometer for absolute temperature measurement to measure the temperature on the FPGA board. After a while, we use the hair dryer to rise the temperature around the FPGA, and then the presents of the thermometer and 7-seg display were both increasing with the temperature rising. The Fig. 5.15 shows the demo environment and thermal information displaying from the smart temperature sensor on FPGA board.

5.4 Summary

In this chapter we have shown the performance of all-digital smart temperature sensor with auto-calibration. The accuracy and temperature range is acceptable for normal SoC devices. Moreover, we also ported a smart temperature sensor onto a FPGA board and built the interconnection between central processing unit (CPU) and smart temperature sensor. So the CPU can read the sensor's output codes and do calibration, and then display the temperature information by the peripheral devices.

Chapter 6

Conclusions and Future Work

In this thesis, we have presented several solutions to build up an all-digital smart temperature sensor with self-calibration. Additionally, for the critical components in smart temperature sensor like the PTAT circuit and TDC, we have surveyed many architectures and analyzed their advantages or disadvantages in our design. The two chips, the all-digital smart temperature sensor test chip and the full-fledged version all-digital smart temperature sensor use the cyclic delay line as the PTAT circuit to save the area, and the ring based TDC to achieve long width pulse quantifying with fine resolution. And the last corresponding design with ARM uses the clock sampling TDC for easy porting and integration.

The calibration of temperature in the all-digital smart temperature sensor test chip is with one slope, the error is 3.6 ~ -5.8 °C in measurements of three chips between temperature range from 0 to 60 °C. However, the simulation result shows that the error will be -7.0 ~ 10 °C under process variations and this is really not an acceptable mismatch. The full-fledged version all-digital smart temperature sensor uses the calibration with dual-slope of temperature. Comparing the simulation result with the all-digital smart temperature sensor test chip, we can see that without process variations, the errors has been reduced form -6.0 ~ 4.0 °C to -1.2 ~ 2.2 °C. Additionally, the process compensation method can greatly reduce the errors of full-fledged version all-digital smart temperature sensor under process variations. By simulation result, the errors only increase from -1.2 ~ 2.2 °C (w/o process variations) to -1.2 ~ 2.6 °C (w/ process variations).

The smart temperature corresponding design with ARM uses the two-point calibration. However, this design focus on the integration and interconnection with Criti-Core system, so the sensor architecture and calibrating algorithm are much simpler than the above two all-digital smart temperature sensors. By this viewpoint, if we can hand over the calibration works to CPU then we can save the area, power and design complexity of the smart temperature senor. But this could raise an extra overhead to CPU loading when the number of sensor is very large on a singe chip.

The performance and accuracy of a chip design will be affected by the process, voltage and temperature (PVT) variations. In this thesis, our calibration and compensation methods can reduces the influence from process and temperature variations, but the voltage variations have not been compensated yet. Normally, the dependency of cell delay on voltage variations is much stronger than the dependency on temperature variations [35] and will cause a significant mismatch in sensor‘s accuracy.

Another problem of smart temperature sensor is the hysteresis effect [36] which has been discussed extensively in recent years. Hysteresis effect is a condition that appears in temperature sensor’s measuring through a sequential temperature range. If a temperature sensor is measuring from cold to hot, it will follow a particular curve, and then if we reverse the measurement from hot to cold follow the above operation, the particular curve should be the same in theory. Nevertheless, there will be an offset between the two curves. The influence of hysteresis effect on smart temperature sensor is very hard to observe because the simulation can not be presented.

From the above problems, we can see that there still has many difficulties in all-digital smart temperature sensor design and they should be investigated for the further research.

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