國立中正大學

資訊工程研究所碩士論文

抗電壓與製程飄移之全數位溫度感測器

An All-Digital Temperature Sensor with Process and Voltage Variation Tolerance for IoT Applications

研 究 生 ： 黃信翰

指導教授 ： 鍾菁哲 博士

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一個適用於物聯網應用並可抵抗製程與電壓變異的全數位溫度感測器 An all-digital temperature sensor with process and voltage variations tolerance for IoT applications

經本委員會審查，符合 碩 士學位論文標準。

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摘要

現今的晶片設計都以高整合度為主，晶片處理的問題日益複雜，但晶片的包裝卻沒有突破性的革命，也因此在設計晶片的過程中也需要考慮到散熱的問題，在目前的系統晶片上，會內嵌許多溫度感測器來監控晶片有無過熱的情形。

而一般的溫度感測器都未考量到電壓漂移的影響，但電壓飄移可能會帶給溫度感測器有上百度的誤差影響，而要消除電壓飄移的影響，通常都是以類比的穩壓電路或是開發低電壓敏感度的電路來克服，但因兩者都需要客製化設計，設計的複雜度也較高，本論文提出的全數位溫度感測器可估計目前的工作電壓，並根據工作的電壓不同，來補償溫度感測器的輸出，並透過校正來消除製程變異的影響，讓溫度感測器可以同時抵抗電壓、製程飄移。

本論文中的低電壓敏感度全數位溫度感測器，利用三個環形震盪器來建立相對參考模型，並開發出 1. 低溫度敏感度的工作電壓估測電路 2. 低電壓敏感度的溫度感測電路，並利用多點校正來將建立輸出與實際溫度的關係。並改善先前建立相對參考模型中需要大量時間來找尋標準元件庫中適合的元件，改以一較有理論根據且較省時的方法。

在這篇論文中，我們提出的低電壓敏感度全數位溫度感測器，採用 90 奈米製程實現，並可在 0.9 ~ 1.1 伏特的電壓及 20 – 80 度的溫度範圍內工作，在下線版本中，最大誤差為−4.3℃~4.3℃.，在低成本版本中，我們會犧牲 12 倍的轉換率來降低電路所需的參考時脈速度以及功耗和成本，最大誤差為−1.6℃~1.8℃，並適合內嵌在電池供電或物聯網裝置等較易受到電壓飄移的應用上。

關鍵字 :全數位，溫度計，抗電壓與製程飄移，相對參考模型

Abstract

Due to more circuits integrated on a single chip, but the IC package technology does not catch up the speed of chip growing. Therefore, the cooling problem should be considered during the design process. As a result, embedded temperature sensors on a system-on-a-chip (SoC) to monitor the hot spots becomes more popular.

Most of the temperature sensors can't resist the influence of voltage variations and will cause hundreds of degrees Celsius errors. Some of temperature sensors may use a bandgap reference or low voltage sensitivity circuits to eliminate the influence of voltage variations which need to full-custom design and can't be portable to different process in a short time. In this thesis, the proposed all-digital temperature sensor can estimate the current supply voltage and compensates for the temperature sensor's output based on the supply voltage information to resist the voltage variations. Addition, the process variations can be removed by three-point calibration.

The proposed temperature sensor uses three ring oscillators to build up the relative reference modeling (RRM) and proposed 1. Low-temperature sensitivity voltage classifier. 2. Low voltage sensitivity PTAT (Proportional to Absolute Temperature). The relationship between the sensor output and the actual temperature value are determined after three-point calibration. The proposed negative voltage coefficient and zero temperature difference ratio design is theoretical basis and save the time in searching cell combinations in previous method.

In this thesis, the proposed all-digital temperature sensor with process and voltage variation tolerance is implemented in TSMC 90nm CMOS technology. The temperature sensor can operate at 0.9 ~ 1.1V supply voltage and 20 – 80 Celsius with a maximum temperature error $-4.3℃\sim4.3℃$ in the tape-out version. In the cost-down version, the

proposed temperature sensor will reduce the conversion to one-twelfth to lower the area , power consumption and the speed of reference clock. The maximum temperature error $-1.6℃\sim1.8℃$ in the cost-down version.

Keyword: all-digital, temperature sensor, process and voltage variation tolerance, Relative reference modeling

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Chapter 1 Introduction

1.1 Smart Temperature Sensor for IoT applications and Battery Operated Systems

As the technologies scale down, more and more transistors are integrated on a compact size chip, which causes the power density being higher and higher in each generation. High power density causes the hot spot occurring more frequently which may affect the chip performance seriously.

Modern CPUs and DRAMs utilize several on-chip temperature sensors for thermal monitoring which can provide temperature information and detect the hot spots. With the increase of cores in processor, the complemental number of temperature sensors on the processor will continuously grow. Of course, these temperature sensors require low power consumption and with compact size.

Temperature sensors usually embedded in the wireless network for IoT applications and battery operated system, which often require power management. As shown in Fig. 1.1, IoT applications or battery operated systems use Dynamic Voltage Frequency Scaling (DVFS) technique to lower the power consumption and extend the battery life as mentioned above.

In IoT applications or battery operated system, the temperature sensors are easily suffered from voltage variation because of operating under different supply voltage or frequency, and power supplied by battery is inherently less stable than the power

supplier. However, most of the previously published temperature sensors[1][4][6][10-11] can't resist voltage variation or need a voltage regulator which occupied a large chip area[28]-[30] and not suitable for IoT applications or battery operated system.

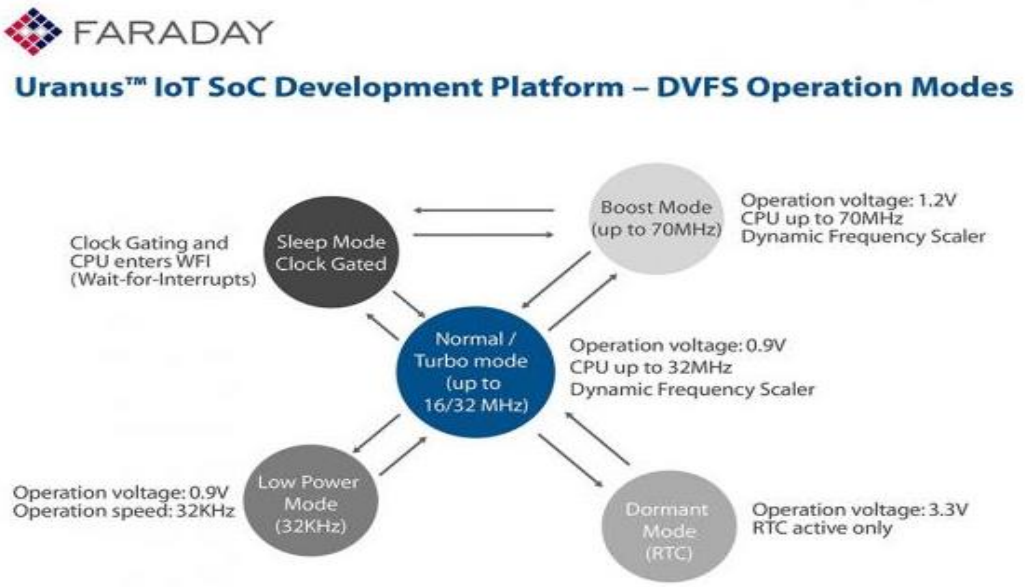


Fig. 1.1. Faraday IoT SoC development platform demonstrates DVFS modes (www.eenewseurope.com/news/soc-development-platform-ultra-low-power-iot-0)

1.2 Architecture of Common Temperature Sensor

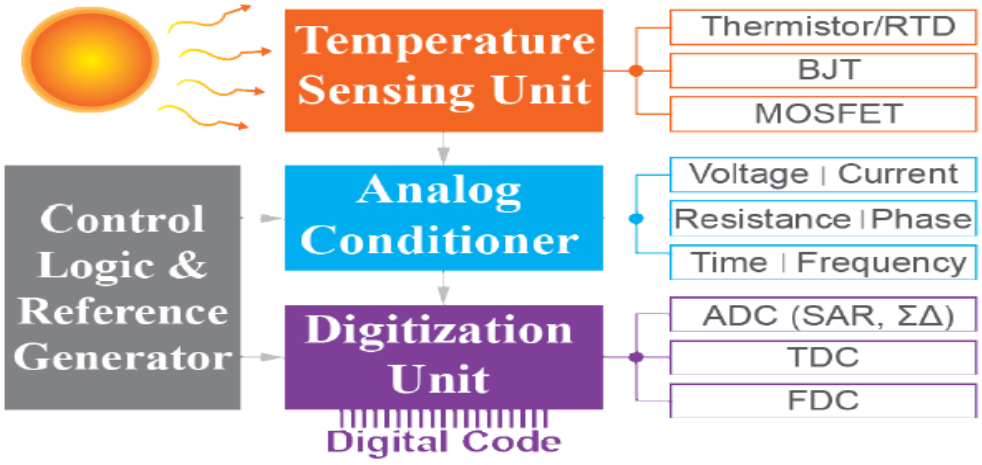


Fig. 1.2. Architecture of common temperature sensor [1]

As shown in Fig. 1.2, the design of the temperature sensor need to find out the component which is sensitive to the absolute temperature value, such as high-temperature sensitive resistors, bipolar junction transistors (BJT), and metal-oxide-semiconductor-field-effect-transistors (MOSFET). After designing a temperature sensing unit, measurable parameter (e.g., voltage, current, resistance or digital pulse width) which is proportional to the absolute temperature(PTAT) is selected. Subsequently, the digitization unit like an analog to digital converter (ADC) or a time to digital converter (TDC) can be used to obtain the digital output.

1.2.1 BJT-Based Temperature Sensor

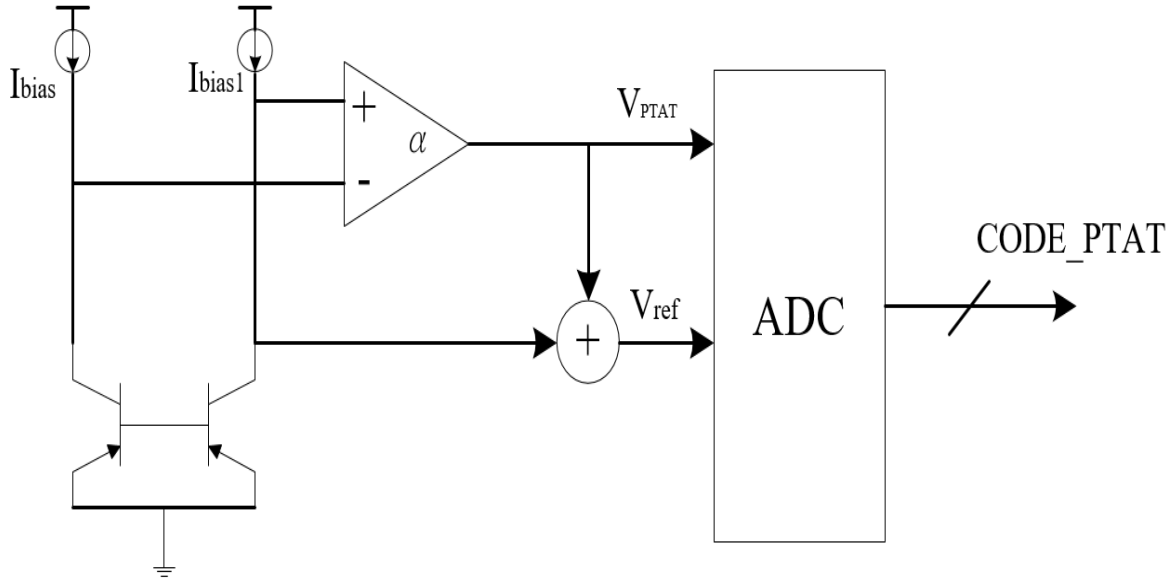


Fig. 1.3. The BJT-based temperature sensor [2]

Fig. 1.3 shows the temperature sensor which has been designed using bipolar junction transistors, the proportional to absolute temperature (PTAT) characteristic of the difference of two base-emitter voltages is used to measure the temperature information as explained in Fig.1.4. In the equations of (1.1) and (1.2) [2], the PTAT voltage ΔV_{be} can be obtained and then the digitization unit is used to convert the voltage into a digital output.

$$V_{be} \approx \frac{kT}{q}\ln\left(\frac{I_{bias}}{I_s}\right) \tag{1.1}$$

$$\Delta V_{be} \approx \frac{kT}{q}\ln\left(\frac{nI_{bias}}{I_s}\right) - \frac{kT}{q}\ln\left(\frac{I_{bias}}{I_s}\right) = \frac{kT}{q}\ln n \tag{1.2}$$

The BJT-based temperature sensors can achieve a high linearity, high accuracy, and wide temperature range and low calibration cost [3]. However, it requires a high supply voltage in order to bias BJT in the active region with the high power consumption. Addition, in advanced CMOS technology, the performance of BJT device is not good which make the BJT-based temperature sensor rare used.

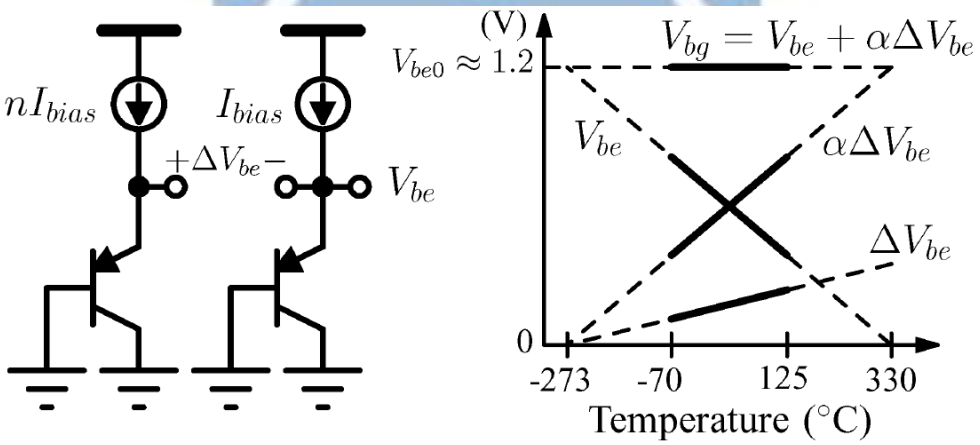


Fig. 1.4. The conventional BJT-based PTAT reference voltage [2]

1.2.2 Resistor-Based Temperature Sensor

The resistor-based temperature sensor, as shown in Fig. 1.5, utilizes the positive (or negative) temperature characteristic of the resistor which implemented by the ceramic, the poly or the metal and it needs a stable current or voltage to get the proportional to absolute temperature voltage or current. After getting the proportional to absolute temperature voltage or current, digitization units like an analog-to-digital converter (ADC) is used to get the output.

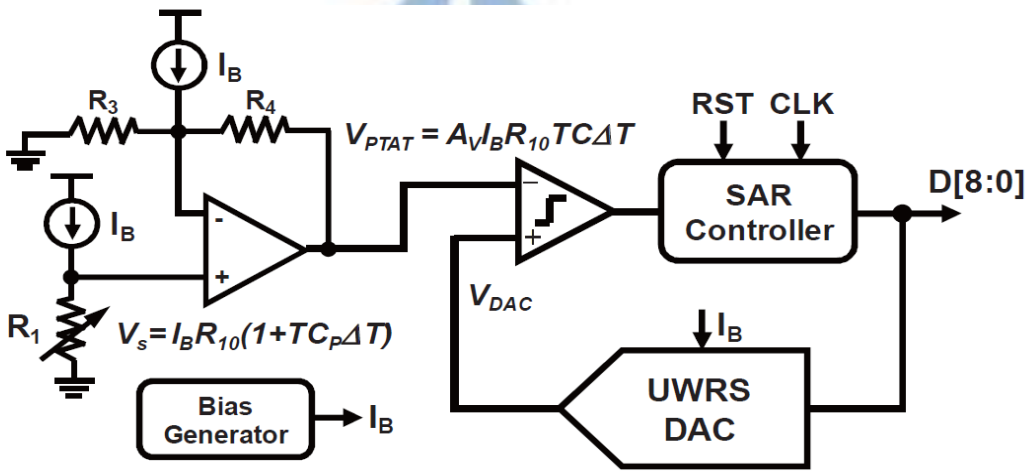


Fig. 1.5. Resistor-based temperature sensor made by the p+-diffusion resistor [4]

Table 1.1 shows the different resistor type and the characteristics which available in TSMC 0.18-um CMOS technology [5]. High resolution, high accuracy, high linearity, low calibration cost, and with large temperature coefficient and low 1/f noise is the first priority when choose the material. N-well is not suitable to be the material for temperature sensor design although N-well has a large temperature coefficient. N-well resistor has a large 2^{nd}-order temperature coefficient and needs high calibration cost and with strong supply dependency which means the voltage variation will influence the accuracy drastically.

Table 1.1. Different material of resistors and its characteristics [5]

Resistor type	Metal	Diffusion	N-well	Poly	Silicided diffusion	Silicided poly
Temperature coefficient	Large	Medium	Large	Medium or Small	Large	Large
2^{nd}-order Temperature coefficient	Medium	Medium	Large	Medium	Small	Small
Sheet resistance	Very Small	Large	Large	Large	Medium	Medium
Supply dependency	Small	Medium	Large	Small	Small	Small
$1/f$ noise	No	No	No	Large	Small	Small
Stress sensitivity	Small	Large	Large	Medium	Small	Small

Silicided diffusion and Silicided poly both have a large temperature coefficient, small 2^{nd}-order temperature coefficient, low supply dependency and small 1/f noise, and are more suitable to be the material of temperature sensor. However, resistor-based temperature sensor needs to custom design and find out the suitable material, which is not portable under different CMOS process.

1.2.3 CMOS Temperature Sensor

CMOS technology is the most widely used in nowadays, MOSFET temperature sensor can integrate with other CMOS circuit more easily. Therefore, MOSFET temperature sensors are more widely used than BJT-based and resistor-based temperature sensor. Measuring the temperature is easy by using the temperature characteristic of drain current. Fig. 1.6 shows the four MOSFET temperature sensor with a voltage output [6] and the temperature characteristic of the V_{GS} which needs a

high-resolution ADC to converter the voltage output into a digital output. However, the high-resolution ADC is hard to design and occupied a large area and power.

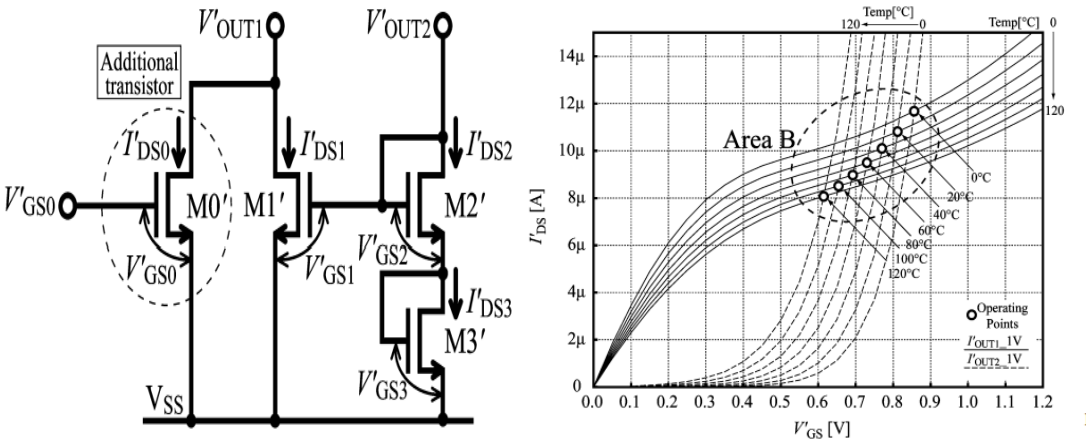


Fig. 1.6. The four MOSFET architecture temperature sensor [6]

Compared to the voltage domain temperature sensor, time-domain temperature sensor uses a digital quantization unit like a stable reference clock or a time-to-digital converter which has relatively low power, small area, and low design complexity than an ADC. As mentioned above, time domain sensors are more often used than voltage domain sensors in advanced CMOS processes. Fig. 1.7 shows the delay line based temperature sensor, common delay cells like, NOT, NAND, AND gate…. are suffered by temperature variations which means the delay time is proportional to the absolute temperature, and the temperature coefficient of the delay cells can use to measure the temperature by quantifying the delay time of the delay cells.

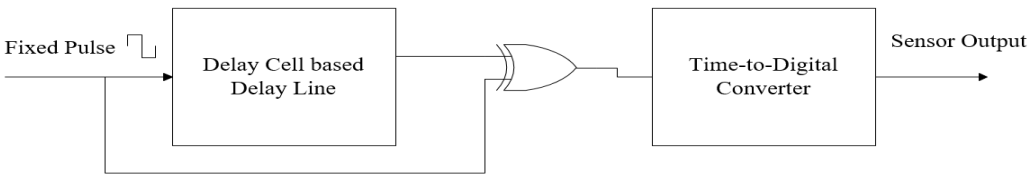


Fig. 1.7. Delay line based temperature sensor

$$T_P = \frac{T_{PLH} + T_{PHL}}{2} \tag{1.3}$$

$$T_{PLH} = \frac{2C_L V_{TN}}{k_N(V_{DD}-V_{TN})^2} + \frac{C_L}{k_N(V_{DD}-V_{TN})} \times ln\left(\frac{1.5V_{DD}- 2V_{TN}}{0.5VDD}\right) \tag{1.4}$$

$$T_{PHL} = \frac{-2C_L V_{TP}}{k_P(V_{DD}+V_{TP})^2} + \frac{C_L}{k_P(V_{DD}+ V_{TP})} \times ln\left(\frac{1.5V_{DD}+ 2V_{TP}}{0.5VDD}\right) \tag{1.5}$$

$$k_N = u_N C_{ox}(\frac{W_N}{L_N}) \ , \ k_P = u_p C_{ox}(\frac{W_P}{L_P}) \tag{1.6}$$

The propagation delay of a NOT gate is discussed in [7], as shown in (1.3), where the T_{PLH} and T_{PHL} shown in (1.4) and (1.5), respectively.

From (1.4), (1.5) and (1.6), (1.7) can be derived.

$$T_P = \frac{\left(\frac{L}{W}\right)C_L}{uC_{ox}(V_{DD}-V_T)} \times \ln\left(\frac{1.5V_{DD}- 2V_T}{0.5V_{DD}}\right) \tag{1.7}$$

$$u = u_0\left(\frac{T}{T_0}\right)^{km} , km = -1.2 \sim -2.0 \tag{1.8}$$

$$V_T = V_{T0} + \alpha(T - T_0) \ , \ \alpha = -0.5 \sim -3.0\text{mV/°K} \tag{1.9}$$

In equation (1.8) and (1.9) [8][9], the mobility u and the threshold voltage V_T are sensitive to the temperature especially the mobility u. As mentioned above, the propagation delay of a NOT gate has a temperature dependency which is proportional to the absolute temperature. The Delay-line based temperature sensor can achieve high linearity [10] but needs a long delay line to generate the pulse with sufficient pulse width for the time-to-digital converter (TDC) to lower the quantization error and then usually result in a chip large area.

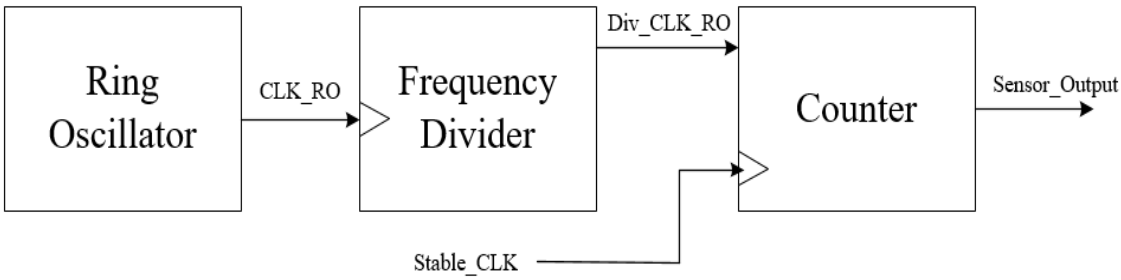


Fig. 1.8. Oscillator-based temperature sensor

Fig. 1.8 shows an oscillator-based temperature sensor which can be implemented by the delay cells of the standard cell library or custom design.

$$\text{Sensor Output} = \frac{Period_{CLK\_RO}}{Period_{Stable\_CLK}} \times Div\_Coef \tag{1.10}$$

The output of the oscillator-based temperature sensor can be expressed as (1.10), where Div_Coef is the divided ratio of the frequency divider, and the $Stable\_CLK$ is the external reference clock.

The $Period_{CLK\_RO}$ in (1.10) can be replaced by using (1.7) and (1.11) can be derived, where n is the stage number of the delay cells in the ring oscillator

$$\text{Sensor Output} = \frac{1}{Period_{Stable\_CLK}} \times n \times \frac{\left(\frac{L}{W}\right)C_L}{uC_{ox}(V_{DD}-V_T)} \times \ln\left(\frac{1.5V_{DD}-2V_T}{0.5V_{DD}}\right) \times Div\_Coef \tag{1.11}$$

As seen in from (1.11), the sensor output will have temperature dependency, which is proportional to absolute temperature. Although oscillator-based temperature sensor does not need a high-resolution TDC but it still requires a high-speed clock which inputs from the signal generator or a phase locked loop (PLL).

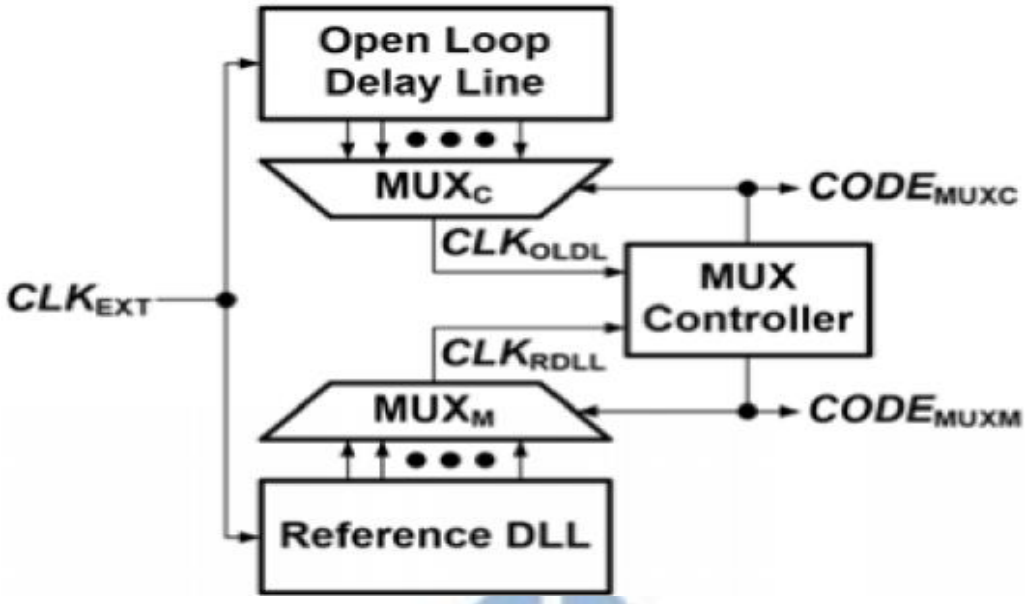


Fig. 1.9. Dual DLL-based temperature sensor [11]

Another time-domain sensor is the dual DLL-based temperature sensor, as shown in Fig 1.9. The purposed architecture measures the temperature using two delay lines, one of them, the open loop delay line(OLDL) is suffered from temperature variation, the other one, the reference DLL(RDLL) is not. The dual DLL-based temperature sensor needs to calibrate at a known temperature T_C in order to eliminate process variations.

In the calibration mode, the open loop delay line need to be tuned until the CLK_{OLDL} is phase aligned with CLK_{RDLL} by tuning the multiplexer of open loop delay line. After calibration, the temperature changes from T_C to an unknown temperature T_U, the lock state of DLL will be released because the phase of the CLK_{OLDL} is changed with temperature variations. Therefore, the MUX controller needs to change the $CODE_{MUXC}$ under different temperature in order to let the CLK_{OLDL} is phase aligned with CLK_{RDLL}, and the $CODE_{MUXC}$ will have the temperature dependency.

1.3 Calibration of the Temperature Sensor

Process variation may cause delay cells of temperature sensors have the different delay. After getting the output from a temperature sensor which has not been calibrated, the relationship between temperature sensor's output digital code and the absolute temperature value is not established. Fig. 1.10 shows an oscillator-based temperature sensor under different process corners. At 50℃, the sensor output has quite different results under different process corners. In order to eliminate process variations, the temperature sensor should be calibrated in a temperature chamber at known temperature value.

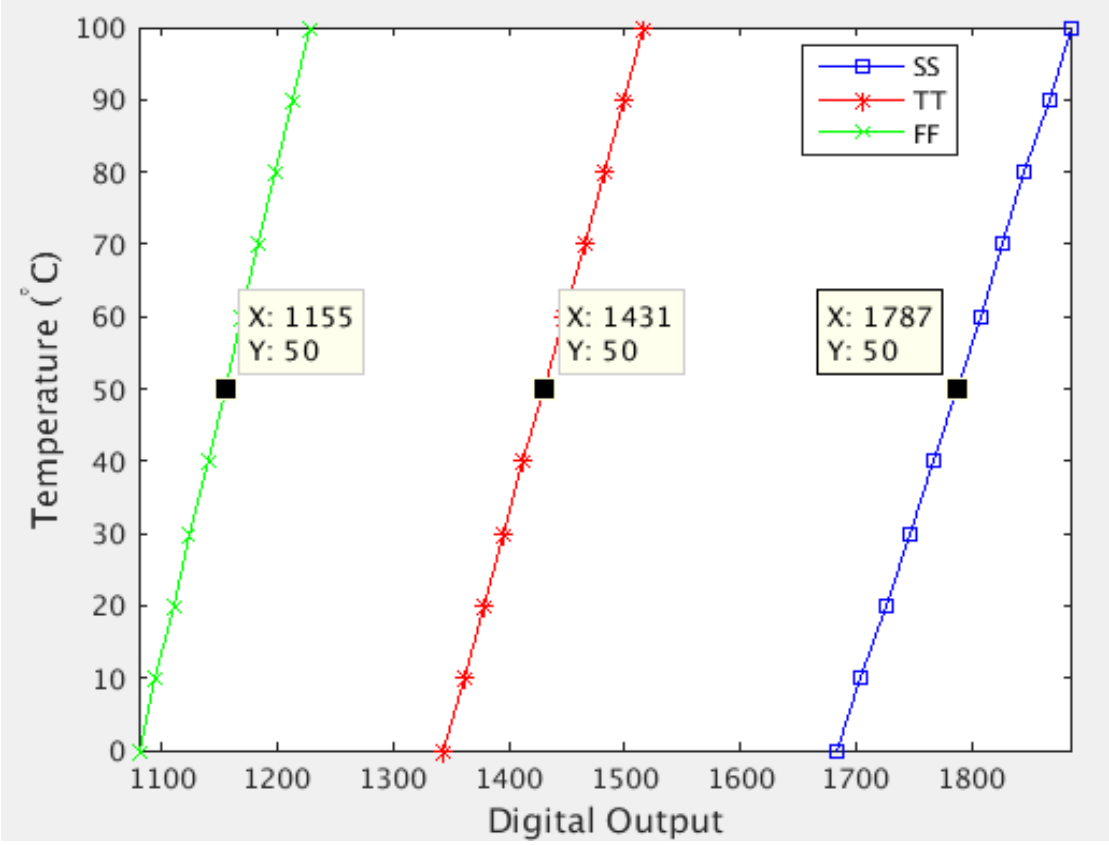


Fig. 1.10. Oscillator-based temperature sensor's output under different corners

The purpose of calibration process is to find the relationship between the output of the temperature sensor and the absolute temperature value. In (1.12), a n- th order polynomial equation is used.

$$\text{Temp\_code} = coef_0 + coef_1 T_{out} + coef_2 {T_{out}}^2 + \cdots + coef_n {T_{out}}^n \quad (1.12)$$

Where $coef_n$ is the n-th order modeling coefficient, T_{out} is the temperature value in ℃ or ℉. High order modeling equation needs more calibration points, but it can fit more close to the actual output. The fitting results will reflect the error of the temperature.

1.4 Influence of Voltage Variation on Temperature Sensor

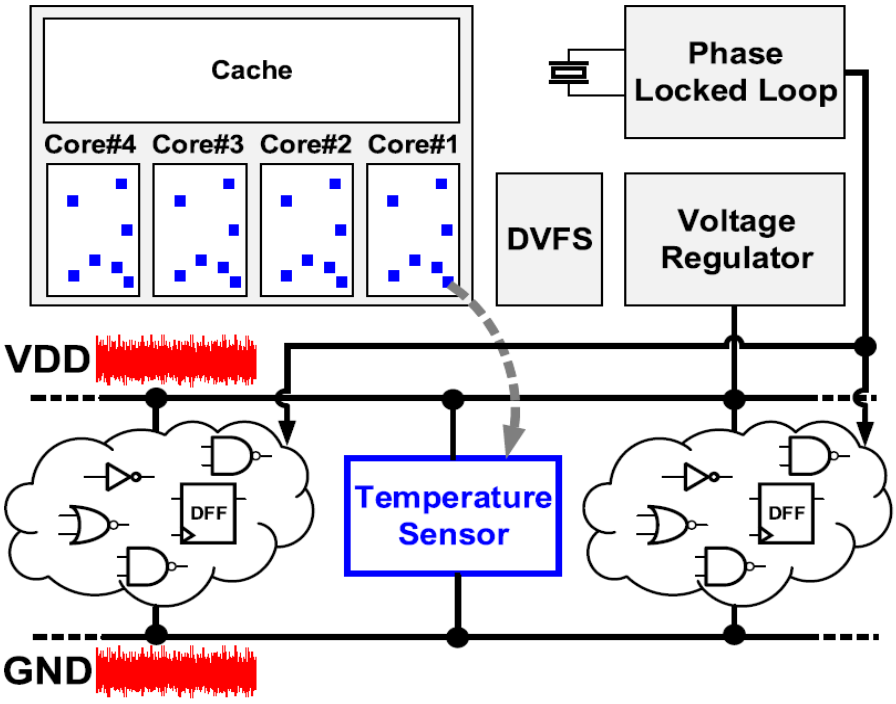


Fig. 1.11. Temperature sensors integrated with the processor [12]

As the consideration of lowering the power consumption, most of the systems use dynamic voltage and frequency scaling. The temperature sensor integrated inside these systems will operate under different supply voltage as shown in Fig. 1.11. The propagation delay of the delay cells (NOT, AND or NAND gate) will be different under different voltage. The delay time of delay cells under the same temperature but with different voltage will not be the same. After getting a digital output from the delay-line based temperature sensor, the digital output may not represent the real temperature under voltage variation as shown in Fig. 1.12.

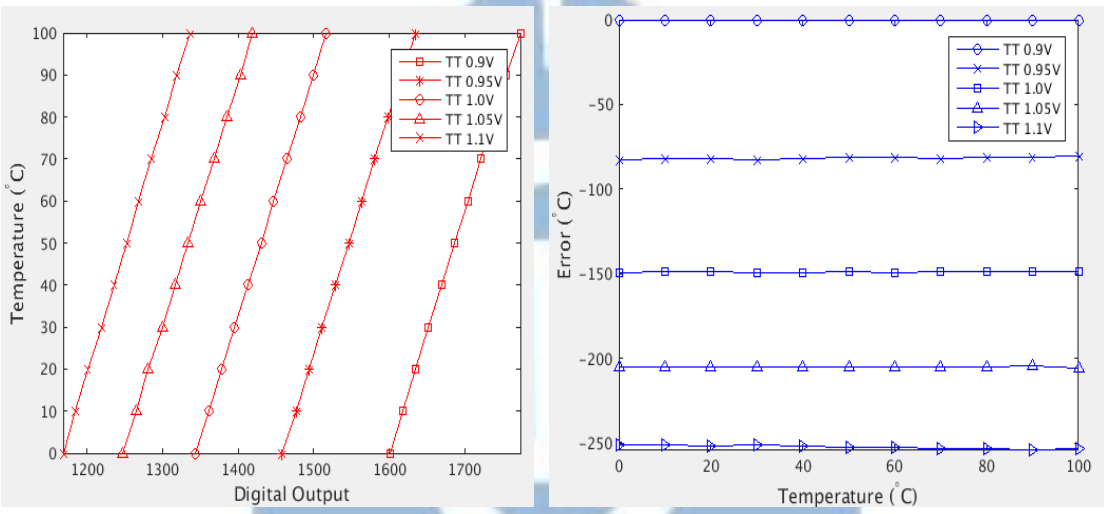


Fig. 1.12. The digital output and error of delay-line based temperature sensor under different voltage at TT corner.

Most of the architectures as described in section 1.2 will be suffered from voltage variations which have > 100℃ error with 10% supply voltage variations, as shown in Fig. 1.12. A voltage regulator can be added to the temperature sensor as shown in Fig. 1.13. The voltage regulator can provide a supply voltage V_R which is stable under voltage variation. However, in advanced CMOS process, the supply voltage V_{DD} lower than 1.0V make it's hard to design the voltage regulator. Addition, the voltage regulator occupies a large area and has large power consumption.

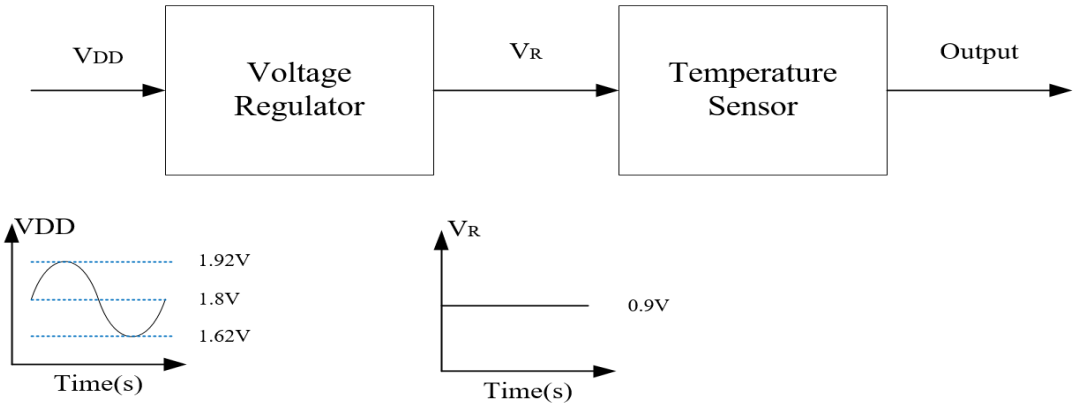


Fig. 1.13. Temperature sensor with a voltage regulator

Another solution to resist voltage variation on the temperature sensor is to design a voltage insensitivity delay cell [13] [14]. However, it is more difficult than design a voltage regulator and is usually not portable to different processes. Fig. 1.14 shows a ring oscillator composed of voltage insensitivity delay cells and the simulation result, the period T_{OSC} of the ring oscillator has a low voltage dependency [13].

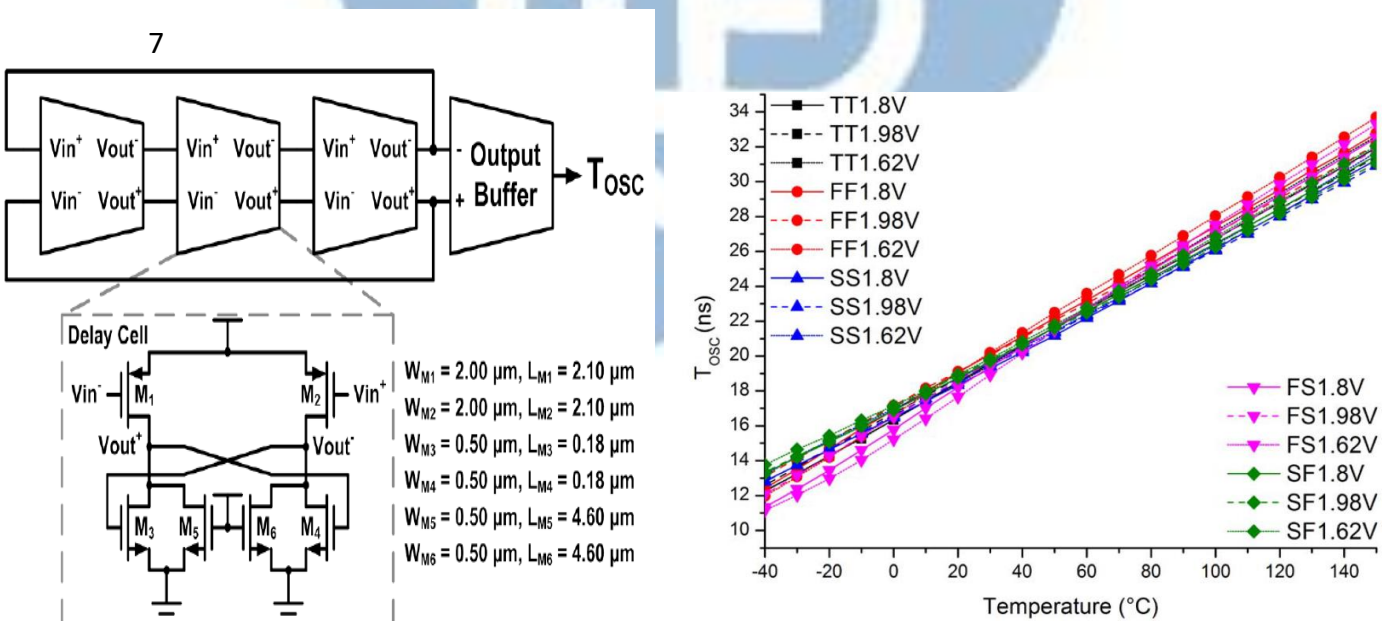


Fig. 1.14. Voltage Insensitivity and simulation result [13]

The two voltages (V_H and V_L) will both increase or decrease with voltage

variations, but the voltage difference between them will be almost the same under voltage variations. Using the characteristic of the voltage difference can create a stable supply voltage to resist voltage variations, as shown in Fig. 1.15 [15].

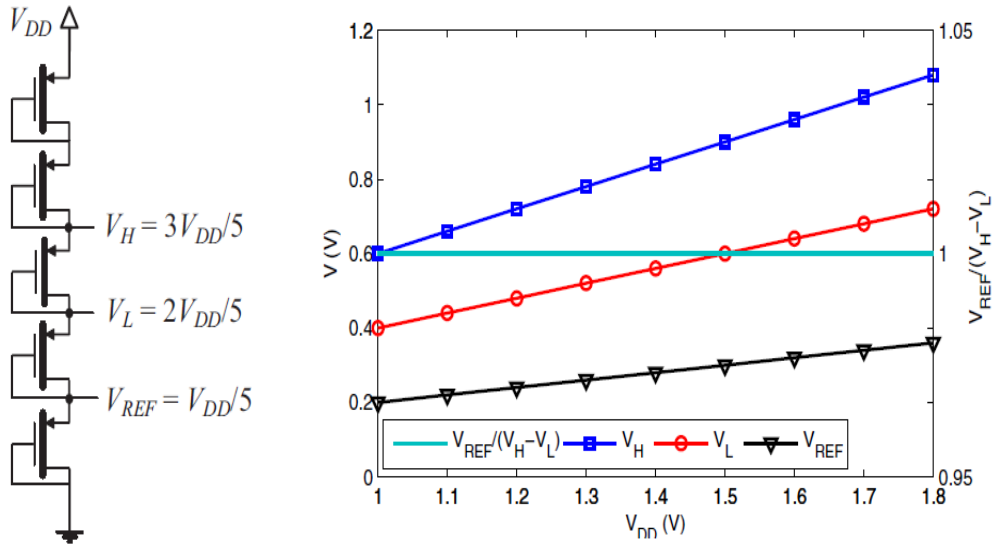


Fig. 1.15. (a) Voltage generation schematics (b) Supply voltage dependence

The above methods are analog circuit design, which needs to full-custom the circuit and have relatively long design time. Compared with digital circuits, analog circuits are difficult to design under advanced processes and usually not portable to different processes.

1.5 Summary

In this chapter, different kinds of the temperature sensor are introduced. BJT-based can reach a high-resolution and accuracy but need a large area, power consumption and hard to integrate with CMOS[2][16] -[20]. Resistor-based need to find out the suitable material and a high-resolution ADC, analog type designs are not suitable for design automation with the poor portability[4][5][21]-[23]. CMOS time-domain temperature

sensors are more suitable for the modern system, which have a lower consumption, area, high portability and easy to integrate with other circuits[6]-[15]. The shortcomings of CMOS time-domain temperature sensors is the high voltage sensitivity, which is not suitable for IoT applications or battery operated system.

1.6 Motivation

As mentioned in chapter 1.4, most of the method to resist voltage variation is analog type design, which needs a large area, power consumption and hard to design on advanced CMOS process. In order to let the temperature sensor can operate on IoT or battery operated system under different supply voltage, which required a compact size, low power consumption, and high portability. Therefore, we hope to find an all-digital method to resist the voltage or temperature variation instead of analog type design.

1.7 Organization

In this thesis, we discuss the design of a temperature sensor in TSMC 90nm CMOS technology. The proposed temperature sensor can operate under 10% voltage variation. The rest of the thesis in organized as follows.

In chapter 2, we discuss the all-digital method, relative reference modeling (RRM), which can resist the voltage variation on temperature sensor and the temperature variation on voltage sensor, and analyze the advantage and the shortcoming of RRM. Subsequently, we discuss the purposed method to separate the temperature and voltage variation from each other. Here we will spill the main circuit into two part, one is the voltage classifier, which can detect the current supply voltage under different temperature, the other is the PTAT circuit which is not suffered from voltage variation

a lot.

In chapter 3, we presented the simulation results and the calibration flow of the purposed temperature sensor. In this version, we improve the shortcoming of RRM with a new method to pick the cell combination.

In chapter 4, we discuss the cost-down version of the proposed temperature sensor which is more suitable for IoT applicaitons. In chapter 5, we make a summary and the future work of the purposed temperature sensor.

Chapter 2 Temperature Sensor with Process and Voltage Variation Tolerance for IoT Applications

2.1 Introduction to Relative Reference Modeling

An all-digital method to separate the influence of voltage and temperature variation is proposed in [24]-[27] which uses the characteristics of the division to cancel out the temperature or voltage variations. The propagation delay of standard delay cells is easily affected by process, voltage, and temperature variations. A simple model to represent the propagation delay of delay cells is shown in (2.1).

$$D_{cell} = D_0 * P^{\alpha} * V^{\beta} * T^{\gamma} \tag{2.1}$$

Where D_0 represent the propagation delays of delay cells, P^{α} is the process coefficient, V^{β} is the voltage coefficient, T^{γ} is the temperature coefficient of the delay cell. The delay ratio of two delay cells, referenced delay cell (RDC) and compared delay cell (CDC) can be expressed in (2.2).

$$\frac{D_{RDC}}{D_{CDC}} = \frac{D_1 * P^{\alpha 1} * V^{\beta 1} * T^{\gamma 1}}{D_2 * P^{\alpha 2} * V^{\beta 2} * T^{\gamma 2}} \tag{2.2}$$

Where D_1 represents the propagation delays of the referenced delay cell, $P^{\alpha 1}$, $V^{\beta 1}$ and $T^{\gamma 1}$ represent the process, voltage and temperature coefficient of the referenced delay cell, respectively. D_2 represent the propagation delays of the compared delay cell, $P^{\alpha 2}$, $V^{\beta 2}$ and $T^{\gamma 2}$ represents the process, voltage and temperature coefficient of the compared delay cell, respectively.

$$\frac{D_{RDC}}{D_{CDC}} = \frac{D_1 * V^{\beta 1} * T^{\gamma 1}}{D_2 * V^{\beta 2} * T^{\gamma 2}} \tag{2.3}$$

The process coefficient can be eliminated by the calibration flow. Therefore, (2.2) can be simplified into (2.3).

If the two delay cells RDC and CDC have similar temperature coefficients but have different voltage coefficients, the ratio of Eq. (2.3) will not be affected by temperature variations but will be affected by voltage variations. As mentioned above, if the temperature coefficient between two delay cell $T^{\gamma 1} \approx T^{\gamma 2}$, (2.3) can be simplified into (2.4).

$$\frac{D_{RDC}}{D_{CDC}} \approx \frac{D_1 * V^{\beta 1}}{D_2 * V^{\beta 2}} \tag{2.4}$$

The ratio of Eq. (2.4) will only be affected by voltage variations. Therefore the ratio of Eq. (2.4) can be used to detect the supply voltage variations, and the result will not be suffered from temperature variations.

$$\frac{D_{RDC}}{D_{CDC}} \approx \frac{D_1 * T^{r1}}{D_2 * T^{r2}} \tag{2.5}$$

Similarly in Eq. (2.3), if the two delay cells have the similar voltage coefficients $V^{B1} \approx V^{B2}$, (2.3) can be simplified into (2.5). The ratio of Eq. (2.5) will be affected by temperature variations, but will not be affected by voltage variation, and the Eq. (2.5) can be used to detect the temperature variations.

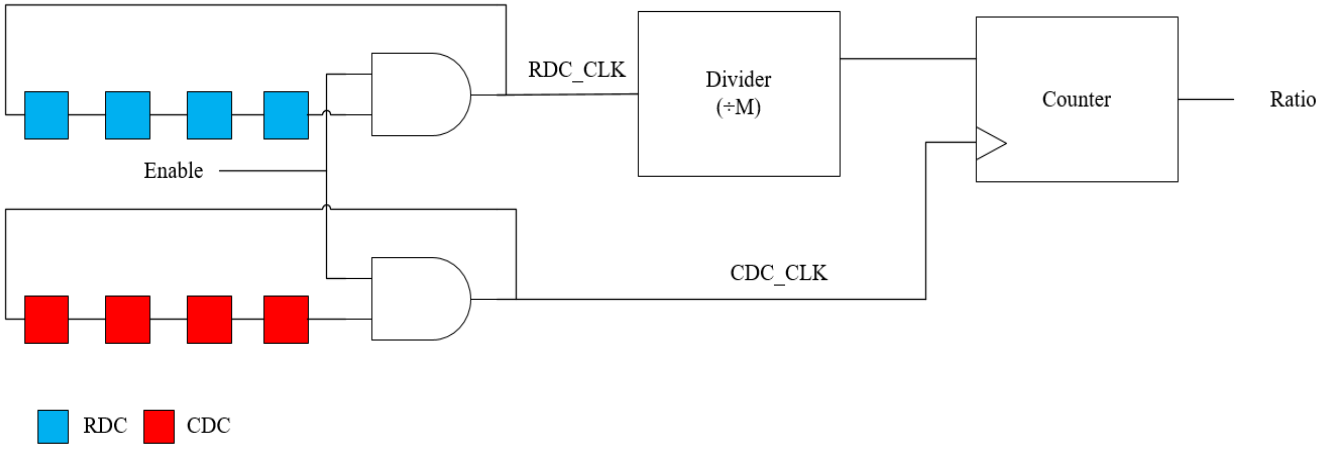


Fig. 2.1 Architecture of the delay ratio estimator

$$Ratio = \frac{Period_{RDC\_CLK}}{Period_{CDC\_CLK}} * M \tag{2.6}$$

Fig. 2.1 shows the architecture of the delay ratio estimator when the input of the counter is 1, the output will be counted up, the output of delay ratio estimator, Ratio can be expressed in (2.6), where $Period_{RDC\_CLK}$ represents the period of the ring oscillator composed by the RDC, $Period_{CDC\_CLK}$ represent the period of the ring oscillator composed by the CDC, and M represents the coefficient of the divider. The period of ring oscillator depends on the propagation delays of the delay cells and the number of delay cells. Therefore, (2.6) can be rewritten into (2.7).

$$Ratio = \frac{N_1 * D_{RDC}}{N_2 * D_{CDC}} * M \tag{2.7}$$

Where N_1 represents the stages of the RDC, N_2 represents the stages of the CDC, D_{RDC} represents the propagation delay of the RDC, D_{CDC} represents the propagation delay of CDC. As shown in (2.7), the equation (2.3) can be implemented into circuit level as shown in Fig. 2.1.

2.2 Design of Voltage Variation Tolerance Temperature Sensor Using Delay Ratio Estimator

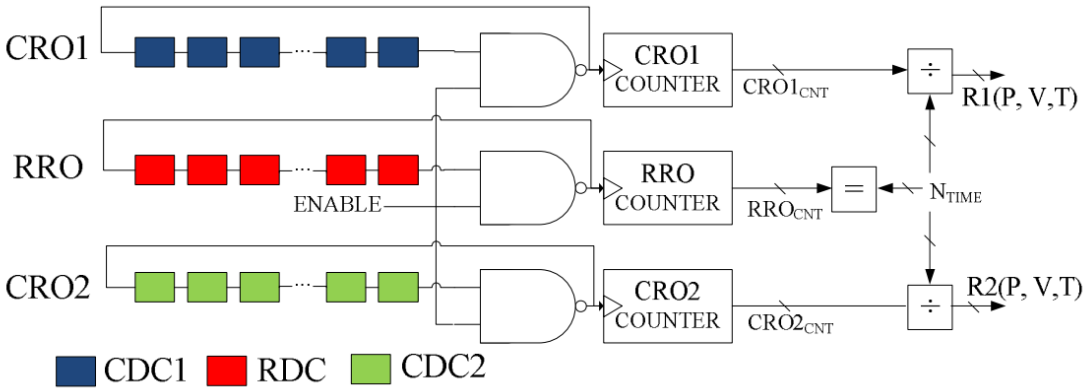


Fig. 2.2 The two delay ratio estimators [24]

Fig. 2.2 shows the two delay ratio estimator [24]. Three ring oscillators CRO1, RRO, and CRO2 are composed of three standard logic cells, RDC, CDC1, and CDC2, respectively. The three ring oscillators trigger three counters, when the RRO COUNTER is count to 16,383, all the ring oscillators will be shut down. Subsequently, the output value of these counters can be used to compute the delay ratio R1(P,V,T) and R2(P,V,T) as expressed in (2.8) [24].

$$R1_{(P,V,T)} = \frac{CRO1_{CNT}}{RRO_{CNT}} \ , \ R2_{(P,V,T)} = \frac{CRO2_{CNT}}{RRO_{CNT}} \qquad (2.8)$$

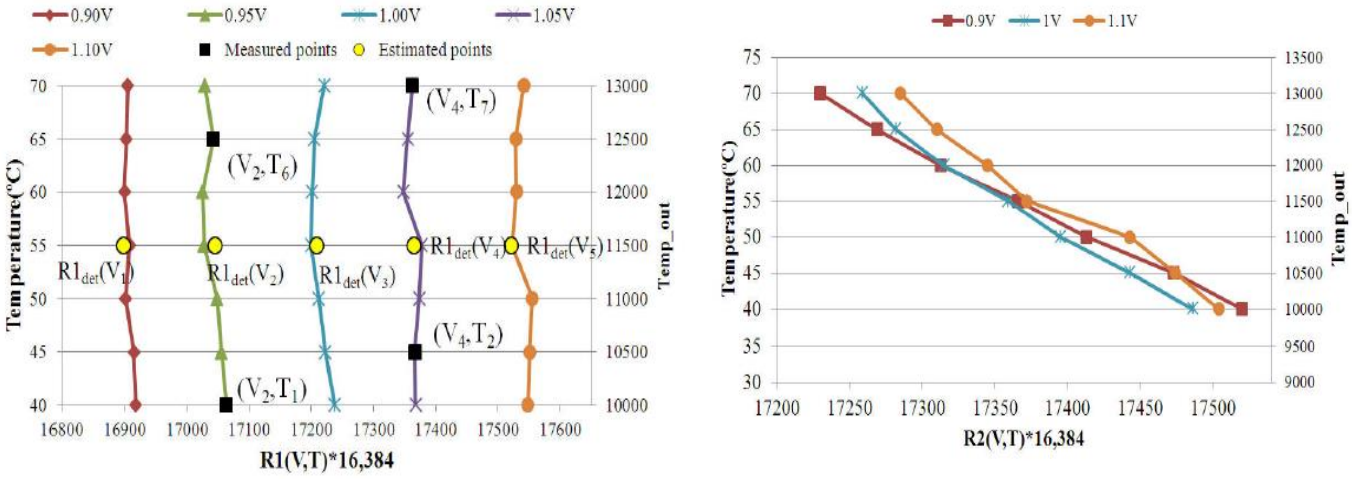


Fig. 2.3 Simulation result of R1 and R2 under different voltages and temperatures [24]

In [24], the cell combination of the RDC and the CDC1 have similar temperature coefficients but different voltage coefficients. Subsequently, the RDC and the CDC2 have similar voltage coefficients but different temperature coefficients which is searched from the cell library. The DRE circuit in Fig 2.2 can eliminate the influence of voltage or temperature coefficient by the characteristics of divison.

As shown in Fig. 2.3, the R1 value is got from the ratio of the two counters which is triggered by the CRO and RRO1, respectively. The R1 value will be affected by voltage variations but have a low-temperature dependency since the CRO and the RRO1 have similar temperature coefficient but different voltage coefficient. Therefore, R1 can be used to detect the current supply voltage under different temperature.

In other hands, the R2 value is got from the ratio of the two counters which is triggered by the CRO and RRO2, respectively. The R2 value will be affected by temperature variation but have a low-voltage dependency compared to the common delay-lined base PTAT since the CRO and the RRO2 have similar voltage coefficients but different temperature coefficients. Therefore, R2 can be used to detect the temperature and use the voltage information from R1 to eliminate the voltage variation of R2.

2.3 Challenge of Design the Delay Ratio Estimator

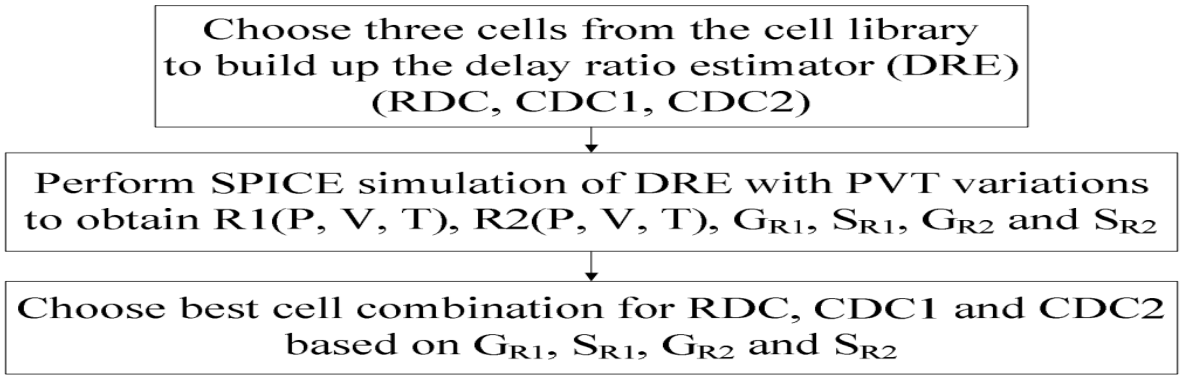


Fig. 2.4 Design flow of delay ratio estimator [24]

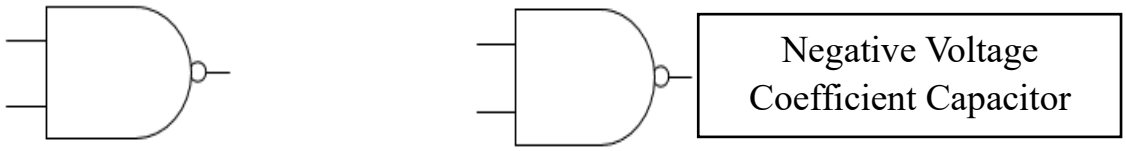
Fig. 2.4 shows the design flow of delay ratio estimator, three logic cells in standard cell library are chosen to build up the delay ratio estimator and perform SPICE simulation under different PVT variations to obtain the delay ratio characteristic. After SPICE simulation, the best cell combination will be chosen to build up the delay ratio estimator. However, there is no theoretical reason for the flow of searching the best cell combination and it takes a lot of time to perform SPICE simulation.

In order to get a ratio to detect supply voltage under different temperature value, the cell combination which has similar temperature coefficients but has different voltage coefficients should be found. However, the characteristic of two delay cells to meet the above conditions can't be easily found, the cell combination for the DRE can only be found after a large number of simulation.

In order to replace the flow of finding the best cell combination to build up the delay ratio estimator, the temperature and voltage coefficients of the common delay cell like NOT, NAND gate should be found by simulation and design other circuits to tune the temperature and voltage coefficients of the common delay cell.

2.4 Cell Combination of Relative Reference Modeling

In section 2.1, an all-digital method which uses three standard cell, compared delay cell 1(CDC1), reference delay cell (RDC), compared delay cell 2 (CDC2) to build up the delay ratio estimator to cancel out the temperature or voltage variation had been introduced. However, the voltage coefficient and temperature coefficient of each standard cells are unknown, and can only be known from SPICE simulations. Therefore, the design flow of DRE needs to try many cell combinations in cell library to find out which two delay cells will have similar voltage coefficients or temperature coefficients. However, the searching flow of DRE takes too much simulation time and the lack of theoretical basis which is been criticized.

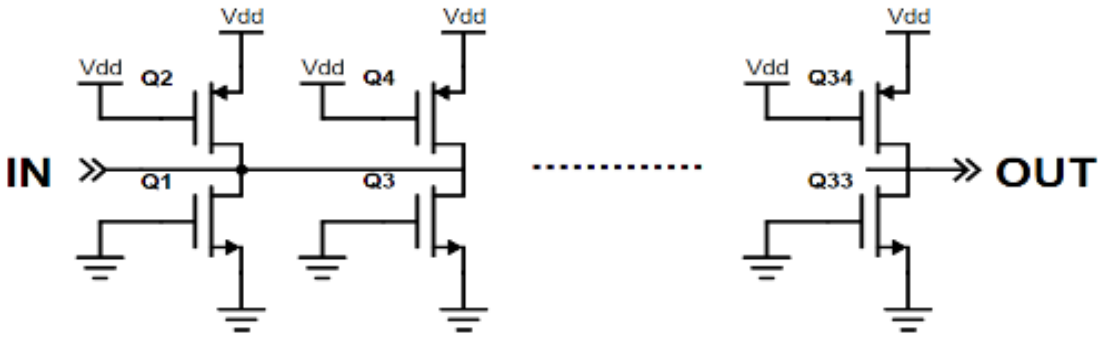


(a)RDC (b)CDC1

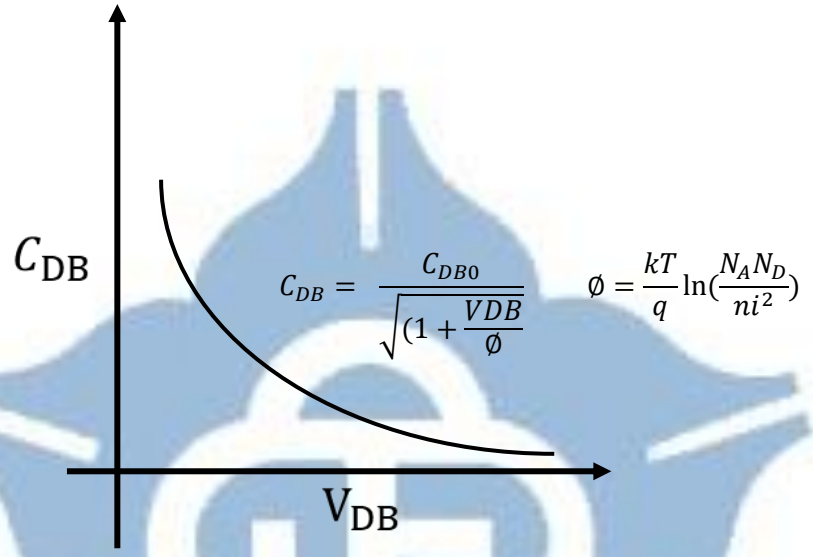
Fig. 2.5 RDC and CDC1 in the proposed design

In this thesis, the proposed method to design the DRE don't need to spend a lot of time to try all cell combinations in the cell library but directly adjust the temperature or voltage coefficient of the ring oscillator. In proposed design, RDC is a 2-input NAND gate, and CDC1 is the proposed high voltage sensitivity 2-input NAND gate, as shown in Fig 2.5(a) and Fig 2.5(b). In general, the propagation delay of delay cell is inversely proportional to the supply voltage and is proportional to the output loading. If the output loading of delay cell will be decreased when the supply voltage rises and increase when the supply voltage falls, then the propagation delay will be more dramatic changed under supply voltage variation and let the delay cell becomes more sensitive to the supply voltage variation.

Fig. 2.6(a) shows the schematic of the proposed MOS capacitor, the increasing of the reverse bias between the N-P junction will cause the depletion width decrease, and the depletion capacitance will be proportional to the depletion width. As a result, the bias between drain and body of the transistor will influence the value of the MOS junction capacitor, as shown in Fig 2.6(b).



(a) Negative voltage coefficient capacitor



(b)Voltage characteristic of negative voltage coefficient capacitor

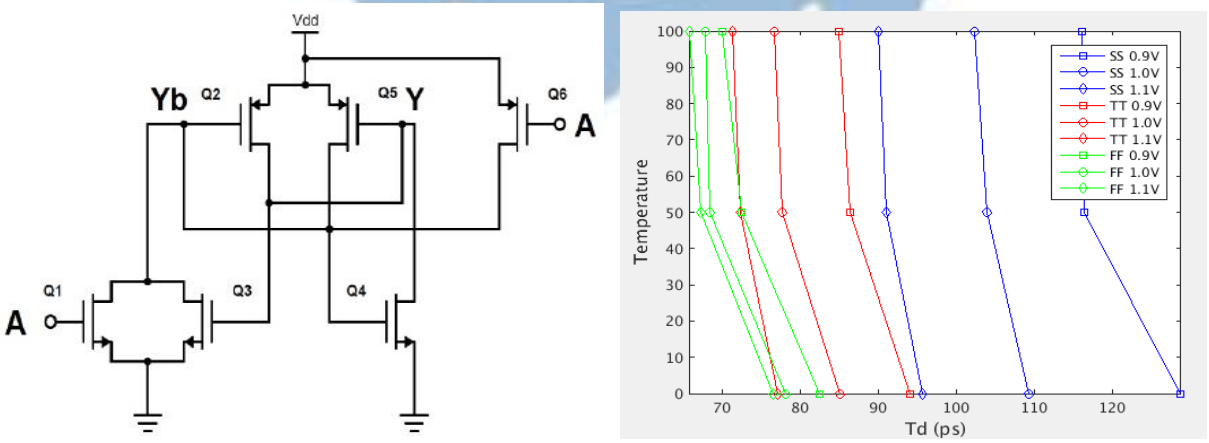
Fig. 2.6 MOS capacitor architecture and its characteristic

RDC is a 2-input standard NAND gate in the cell library, CDC1 is the 2-input standard NAND gate with the MOS capacitor to enhance the voltage sensitivity. Table. 2.1 shows the voltage and temperature sensitivity among four different delay cells. Although the MOS capacitor can enhance the voltage sensitivity of the NAND gate, it also increases the temperature sensitivity. To eliminate the influence of temperature variation, CDC1 and RDC should have similar temperature sensitivity. In the proposed design, negative temperature coefficient delay cells, thyristor [32] will be used to adjust the temperature coefficients of CDC1 so that the two different ring oscillator composed of CDC1 and RDC can have similar temperature coefficients.

Table. 2.1 SPICE simulation of voltage and temperature sensitivity among four different delay cells

	Voltage Sensitivity (at TT 50˚C)	Temperature Sensitivity (at TT 1.0V)
Standard NAND	-5.175ps / 100mV	0.0361ps / ˚C
Standard NAND with 32 MOS Capacitor	-9.9275ps / 100mV	0.14978ps / ˚C
Standard NAND with 64 MOS Capacitor	-18.965ps /100mV	0.2709ps / ˚C
Standard NAND with 128 MOS Capacitor	-35.095ps /100mV	0.5405ps / ˚C

Fig. 2.7(a) shows the schematic of the negative temperature coefficients delay cell, thyristor. The drain current of Q1 is the positive temperature coefficient and inversely proportional to the propagation delay of thyristors [32]. If the temperature increases, the drain current will increase and the propagation delay of thyristor will decrease. Table. 2.2 shows the voltage and temperature sensitivity of the thyristor.



(a) Schematic of thyristor [32]

(b) Propagation delay of thyristor versus temperature and voltage

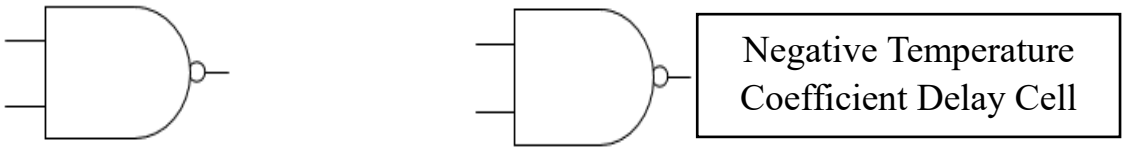
Fig. 2.7 Negative temperature coefficient delay cells architecture and characteristic

Table. 2.2 Voltage and temperature sensitivity of the thyristor

	Voltage Sensitivity (at TT 50˚C)	Temperature Sensitivity (at TT 1.0V)
Thyristor	-7.9388ps / 100mV	-0.08392ps / ˚C

In order to resist the voltage variation, the proposed temperature sensor uses the voltage classifier to detect the current supply voltage and compensate for the output according to the current supply voltage. However, there may have errors when detecting the current supply voltage, to lower the influence of voltage classifier, the proportional to the absolute temperature(PTAT) circuit should have low-voltage dependency.

Fig. 2.8(b) shows the CDC2 in proposed delay ratio estimator, in order to eliminate the influence of voltage variation on PTAT circuit by using the characteristic of division, CDC2 and RDC need to have similar voltage coefficients. Although the characteristic of division can eliminate the influence of voltage variation, it also cause the problem of temperature sensitivity to be offset. To allow the PTAT to have sufficient temperature sensitivity, the temperature sensitivity of CDC2 and RDC requires large difference. In general, most of the standard cells have a positive temperature coefficient, increasing or decreasing the temperature coefficient can obtain large temperature coefficient difference between CDC2 and RDC. In proposed PTAT circuit, the CDC2 uses the 2-input NAND gate which is the same as the RDC to let the voltage coefficient of the CDC2 and RDC can be close. Subsequently, the temperature coefficient of 2-input NAND gate has been lower by using the negative temperature coefficient delay cell, thyristor, to get large temperature coefficient difference between CDC2 and RDC.



(a)RDC (b)CDC2

Fig. 2.8 RDC and CDC2 in proposed design

2.5 Low Temperature Dependency Voltage Classifier

Fig. 2.9 shows the architecture of the compared ring oscillator (CRO) which is composed of 2-input standard NAND gate (RDC) shown in Fig 2.5(a). Fig. 2.10 shows the architecture of the reference ring oscillator 1 (RRO1) which is composed of 2-input standard NAND gate with the MOS capacitors (CDC1) shown in Fig 2.5(b). In RRO1 shown in Fig 2.10, the path selector can be used to choose how many thyristors need to be enabled under different process corner and lets the CRO and RRO1 have similar temperature coefficients.

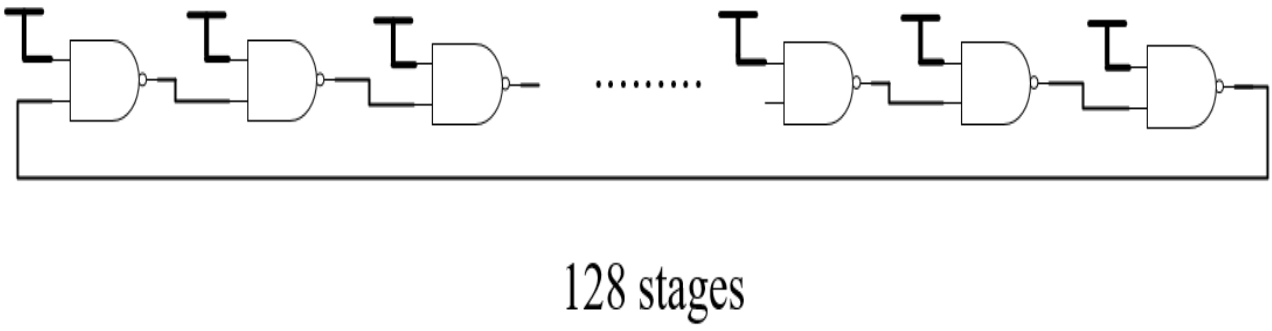


Fig. 2.9 Proposed architecture of compared ring oscillator (CRO)

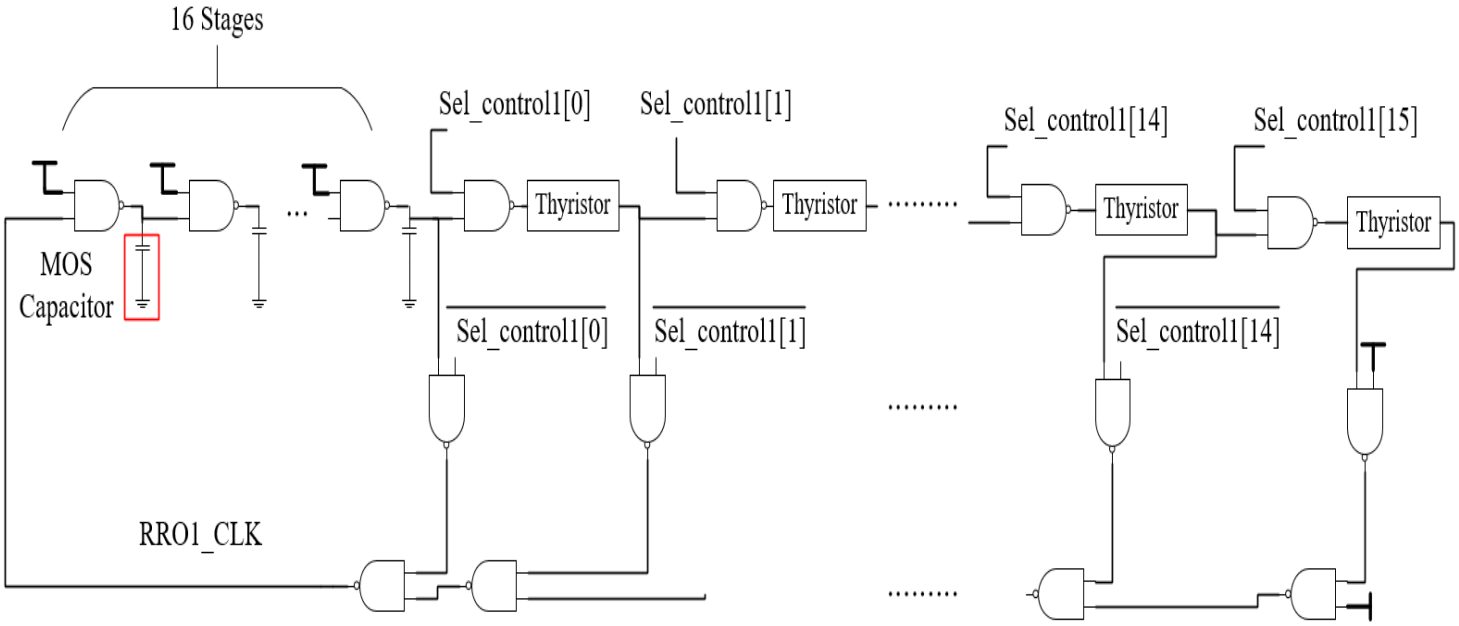


Fig. 2.10 Proposed architecture of reference ring oscillator 1 (RRO1)

Fig. 2.11 shows the proposed difference calculator, which composed of two ring oscillators, RRO1 and CRO. The output of the two ring oscillators will be divided into a low-speed clock and an external high-speed clock, Ref_CLK (100MHz) is used to quantify the periods of RRO1_div and CRO_div. Subsequently, the subtractor will subtract the two results (C1 and C2) and get the R1 value. In Eq. (2.8), the division method will eliminate the most of the voltage and temperature sensitivity and cause the problem of low-voltage sensitivity on the voltage classifier in [24]. In order to let the voltage classifier have a sufficient resolution, proposed voltage classifier use the subtraction method instead of division.

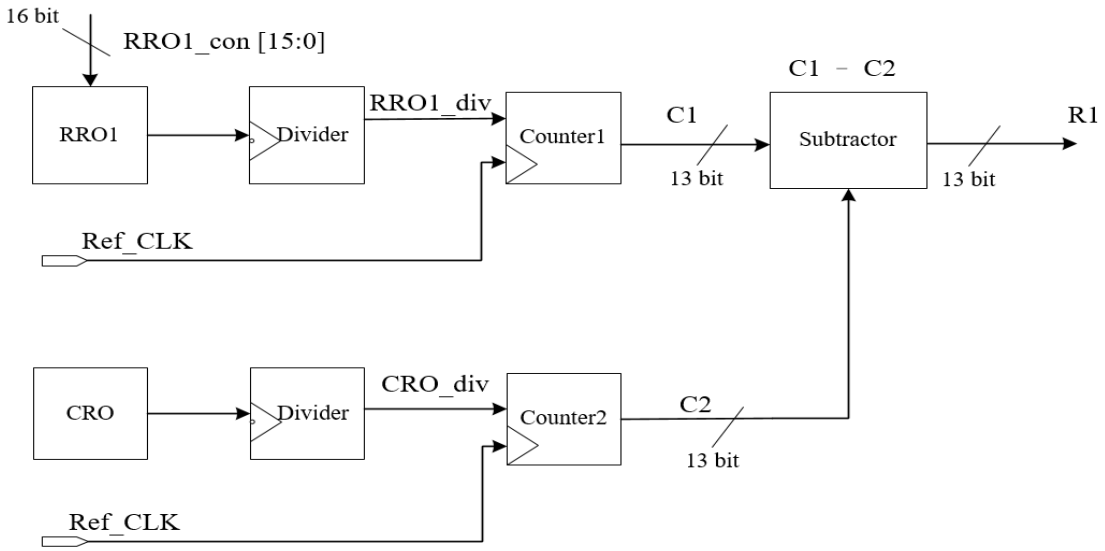


Fig. 2.11 Proposed difference calculator

The difference calculator output value, R1 can be expressed in (2.9), where the P_{RRO1} is the period of the ring oscillator 1 (RRO1), P_{CRO} is the period of the compared ring oscillator (CRO), Div_coef1 and Div_coef2 are the coefficients of the divider, P_{Ref_CLK} is the period of the reference clock.

$$\mathrm{R1} = \frac{(\ (P_{RRO1} * \ Div\_coef1) - (P_{CRO} * \ Div\_coef2)\ )}{P_{Ref\_CLK}} \tag{2.9}$$

The P_{RRO1} can be expressed in (2.10), where the N_1 is the stages number of compared delay cells 1(CDC1), D_{CDC0} is the propagation delay of CDC1 at (1.0V, 50℃). V_{b1} is the voltage sensitivity of CDC1 and T_{r1} is the temperature sensitivity of CDC1, and $T_{current}$ is the current temperature value, $V_{current}$ is the current supply voltage.

$$P_{RRO1} = N_1 * \{D_{CDC0} + [(V_{current} - 1.0\mathrm{V}) * V_{b1}] + [(T_{current} - 50℃) * T_{r1}]\} \tag{2.10}$$

The P_{CRO} can be expressed in (2.11), where the N_2 is the stages number of reference delay cells (RDC), D_{RDC0} is the propagation delay of RDC at (1.0V,50℃).

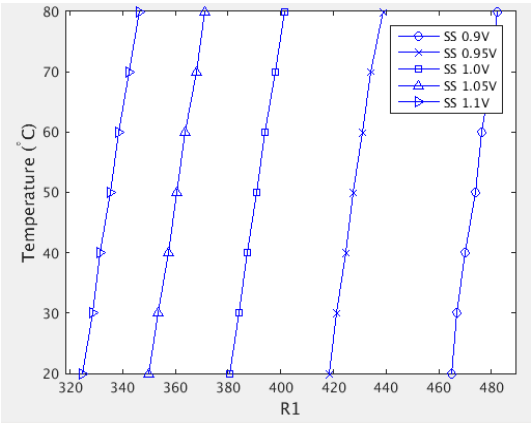
V_{b2} is the voltage sensitivity of RDC and T_{r2} is the temperature sensitivity of RDC, and $T_{current}$ is current temperature value, $V_{current}$ is the current supply voltage.

$$P_{CRO} = N_2 * \{D_{RDC0} + [(V_{current} - 1.0\text{V}) * V_{b2}] + [(T_{current} - 50℃) * T_{r2}]\} \quad (2.11)$$

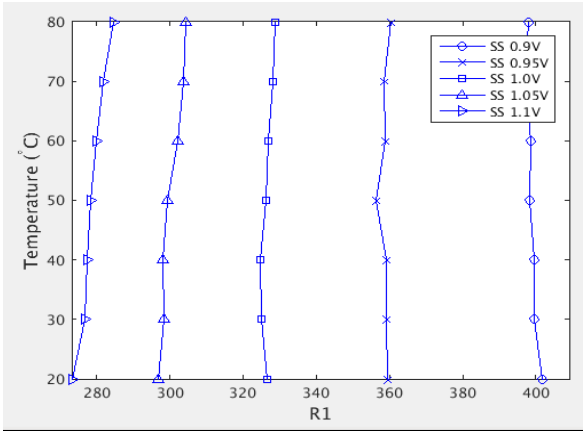
Assuming $N_1 = N_2$, $Div_{coef1} = Div_{coef2}$, and the CRO and RRO1 have similar temperature sensitivity $T_{r1} \approx T_{r2}$. The R1 in (2.9) can be derived into (2.12) which can be used to detect the voltage and will not have the temperature dependency.

$$\text{R1} = \frac{Div_{coef1} * N_1 * \{(D_{CDC0} - D_{RDC0)} + [(V_{current} - 1.0\text{V}) * (V_{b1} - V_{b2})]\}}{P_{Ref\_CLK}} \quad (2.12)$$

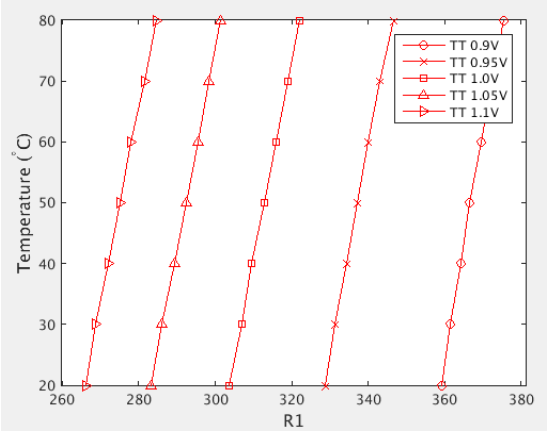
Fig. 2.12 shows the pre-layout simulation of R1 value, the N_1 is 16, the N_2 is 64, the Div_{coef1} is 1500, Div_{coef2} is 400, R1 value is suffered from temperature variation before temperature coefficient compensation. Fig. 2.12(b)(d)(f) shows the R1 value under different process corner after temperature coefficient compensation by using the path selector to choose the number of the thyristors used for compensation. The temperature coefficient of R1 becomes close to zero after temperature coefficient compensation. Subsequently, R1 is sensitive to voltage variations but not sensitive to temperature variations. As a result, R1 can be used to sense the current voltage under different temperature value.



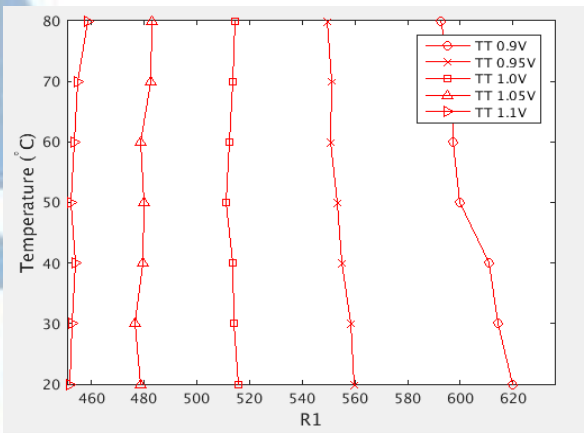
(a) R1 before temperature cofficient compensation under SS case (open 0 stage thyristor)



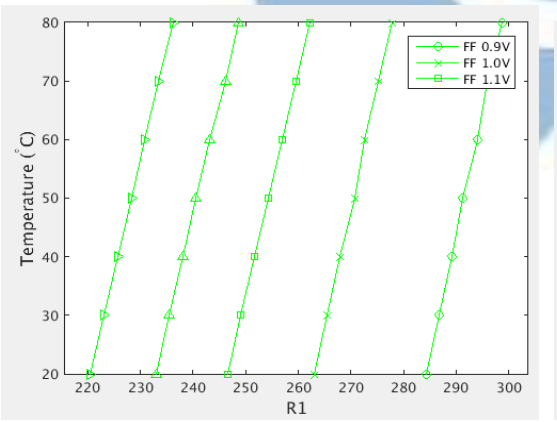
(b) R1 after temperature cofficient compensation under SS case (open 1 stage thyristor)



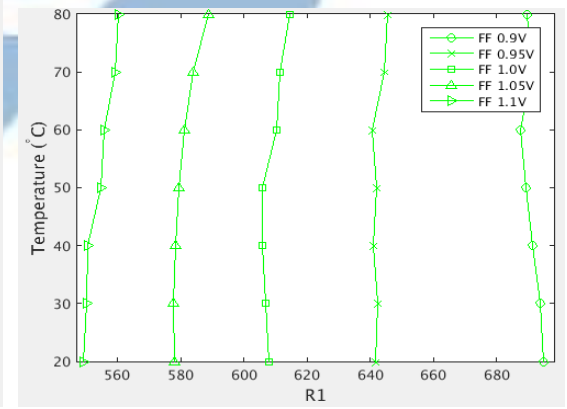
(c) R1 before temperature cofficient compensation under TT case (open 0 stage thyristor)



(d) R1 after temperature cofficient compensation under TT case (open 4 stages thyristor)



(e) R1 before temperature cofficient compensation under FF case (open 0 stage thyristor)



(f) R1 after temperature cofficient compensation under FF case (open 6 stages thyristor)

Fig. 2.12 R1 pre-layout simulation before and after temperature coefficient compensation under different PVT variations

2.6 Low Voltage Sensitivity PTAT Circuit Design

Fig. 2.13 shows the architecture of the reference ring oscillator 2 (RRO2) which is composed of 2-input standard NAND gates with the negative temperature coefficient delay cells (CDC2 shown in Fig. 2.8(b)). In RRO2, the 16-stages of 2-input NAND with thyristors let the RRO2 and CRO can have a similar voltage coefficient after digital calibration. In order to keep the temperature sensitivity of the PTAT circuit, negative temperature coefficient delay cells are added to the RRO2 and lets the delay ratio R2 becomes sensitive to temperature variations but not sensitive to voltage variations. As shown in Fig. 2.14, proposed PTAT uses the delay ratio estimator which use the clock of CRO to quantize the period of the RRO2.

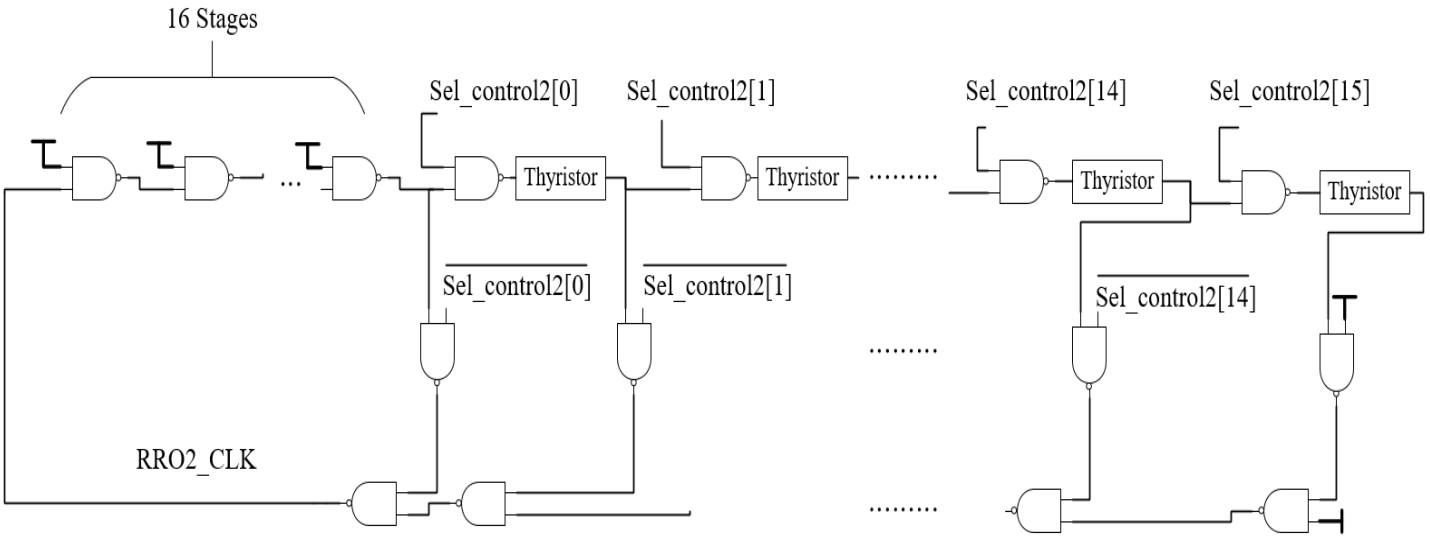


Fig. 2.13 Proposed reference ring oscillator 2 (RRO2)

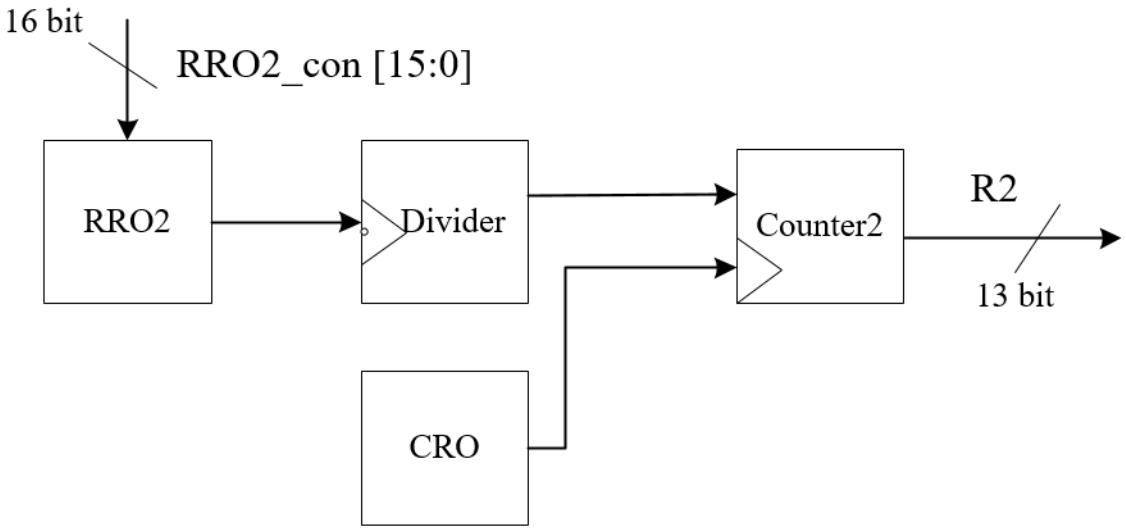


Fig. 2.14 Proposed PTAT based on delay ratio estimator

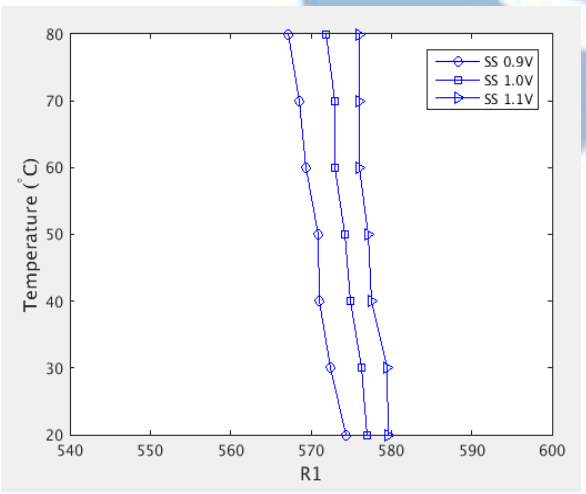
The PTAT output R2, can be expressed in (2.13) where $Period_{RRO2}$ is the period of RRO2, $P^{\alpha 2}$ is the process coefficient of RRO2, $V^{\beta 2}$ is the voltage coefficient of RRO2, $T^{\gamma 2}$ is the temperature coefficient, $Divider\_coef$ is the divisor of divider, and $Period_{CRO}$ is the period of CRO, $P^{\alpha 1}$, $V^{\beta 1}$, $T^{\gamma 1}$ represent process, temperature, voltage coefficient of the CRO, respectively.

$$\mathrm{R2} = \frac{Period_{RRO2} * (P^{\alpha 2} * V^{\beta 2} * T^{\gamma 2}) * Divider\_coef}{Period_{CRO} * (P^{\alpha 1} * V^{\beta 1} * T^{\gamma 1})} \tag{2.13}$$

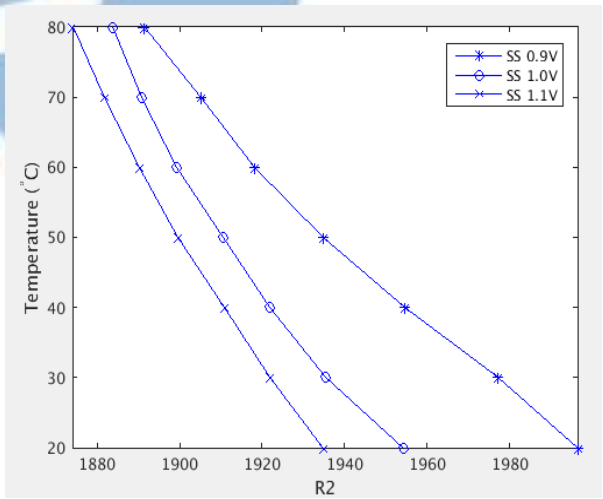
The process variation of R2 can be eliminated by the calibration flow, therefore, the $P^{\alpha 1}$ and $P^{\alpha 2}$ can be ignored. Subsequently, if the two ring oscillators CRO and RRO2 have similar voltage coefficients $V^{\beta 1} \approx V^{\beta 2}$, the (2.13) can be derived into (2.14). In (2.14), R2 can be used to detect the temperature value under voltage variations.

$$R2 = \frac{Period_{RRO2} * Divider\_coef}{Period_{CRO}} * \left(\frac{T^{r2}}{T^{r1}}\right) \quad (2.14)$$

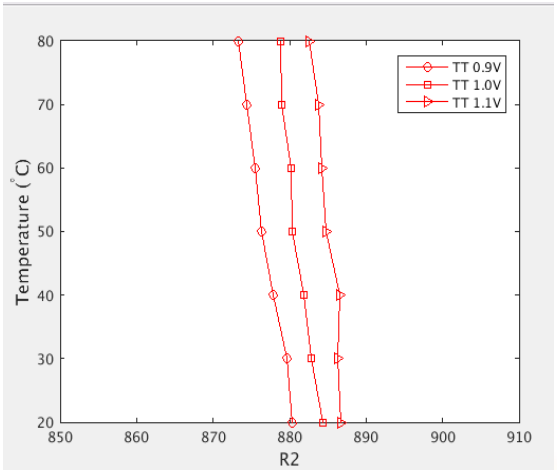
Fig. 2.15 shows the pre-layout simulation of R2 value. As shown in Fig. 2.15(a)(c)(e), the CRO and RRO2 have similar temperature coefficient before negative temperature coefficient compensation, $\frac{T^{r3}}{T^{r2}} \approx 1$(constant). Fig. 2.15(b)(d)(f) shows the R2 value under different process corner after negative temperature coefficient compensation by using the path selector to choose the number of the thyristors of the RRO2. The temperature coefficient of RRO2 becomes more negative after temperature coefficient compensation, $T^{r1} \neq T^{r2}$, the R2 value will have strong temperature dependency for PTAT circuit design. However, the voltage coefficient of RRO2 is not same as CRO, $V^{\beta 1} \neq V^{\beta 2}$, the influence of voltage variations can't be eliminated. In order to lower the temperature error caused by voltage variations, the proposed temperature sensor uses the voltage classifier in section 2.5 to detect the current supply voltage and then the voltage dependency of the PTAT circuit can be further reduced.



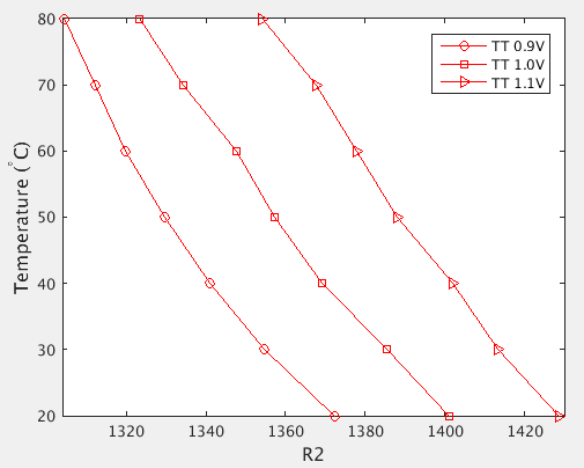
(a) R2 before temperature cofficient compensation under SS case



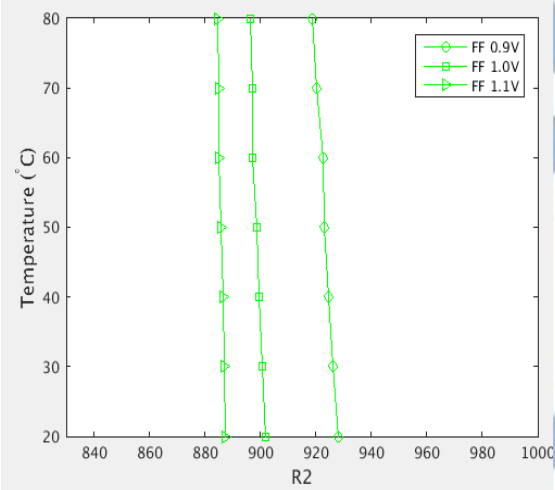
(b) R2 after temperature cofficient compensation under SS case



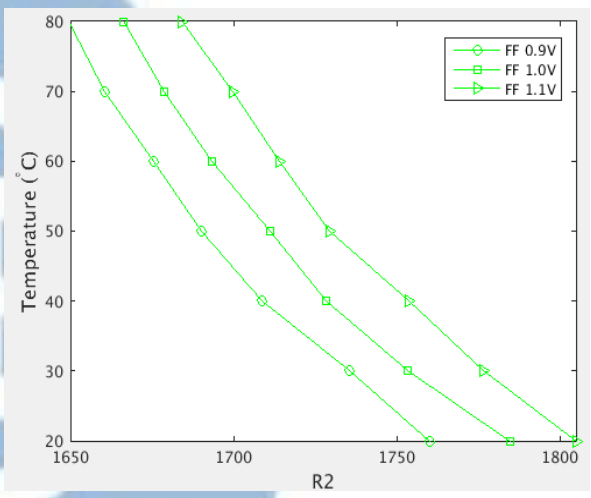
(c) R2 before temperature cofficient compensation under TT case



(d) R2 after temperature cofficient compensation under TT case



(e) R2 before temperature cofficient compensation under FF case



(f) R2 after temperature cofficient compensation under FF case

Fig. 2.15 R2 pre-layout simulation before and after temperature coefficient compensation under different PVT variations

Fig. 2.16 shows the proposed delay ratio estimator which use the high voltage sensitivity 2-input NAND gates with MOS capacitors to compose the RRO1 and let the RRO1 and CRO having large voltage sensitivity difference, and the negative temperature coefficient delay cells are used to keep the temperature sensitivity between

RRO1 and CRO. In the simulation results, the R1 which defined in Eq. (2.9) has a low-temperature dependency but has high voltage dependency. The output R2 which is defined in Eq. (2.13) uses the negative temperature coefficient delay cells to let the CRO and RRO2 have different temperature coefficient and use the characteristics of the division to eliminate the influence of voltage variations.

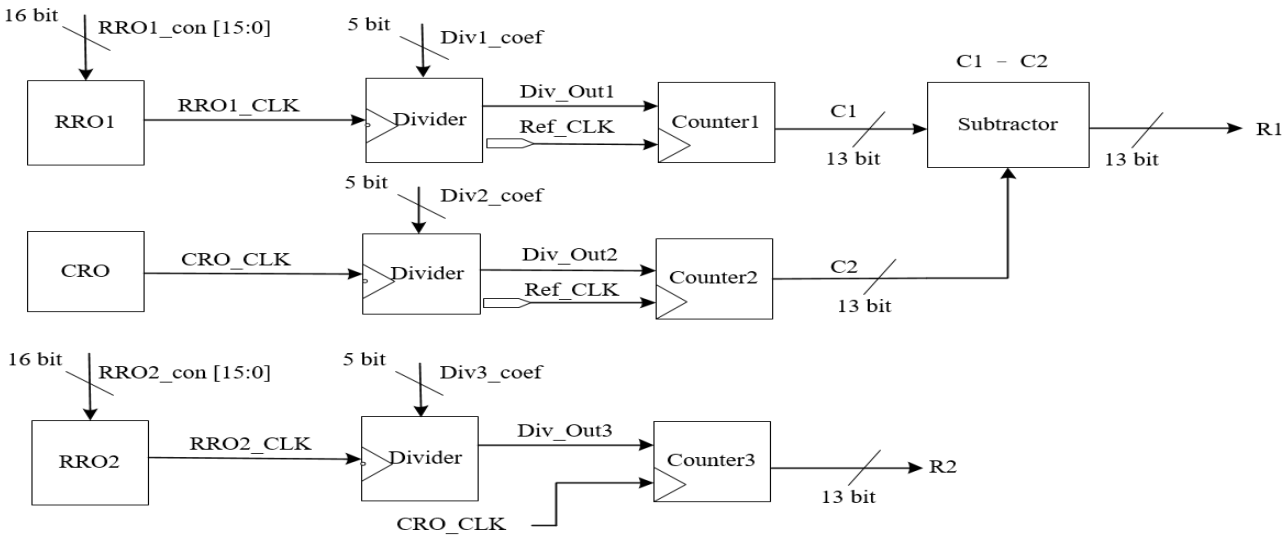


Fig. 2.16 Proposed delay ratio estimator

In Fig. 2.16 Ref_CLK is generated by an on-chip oscillator shown in Fig. 2.17. In order to get a stable 100MHz Ref_CLK, the path selector is used to tune the Ref_CLK to 100MHz under different PVT conditions. Table. 2.3 shows the pre-layout simulation and post-layout simulation of the on-chip oscillator which can provide 100MHz under different PVT corners.

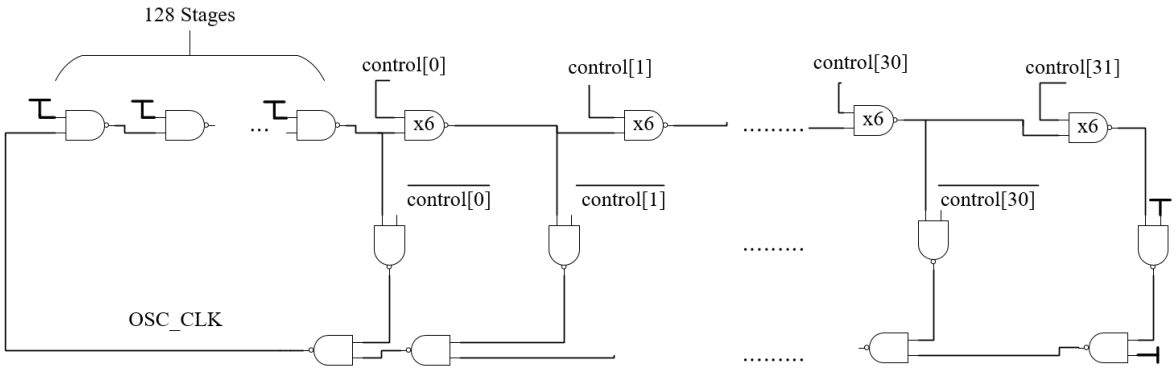


Fig. 2.17 Schematic of on-chip oscillator

Table 2.3 On-chip oscillator frequency range under different PVT corners

	Pre-layout simulation	Post-layout simulation
SS@0.9~1.1V@0~100℃	38~136MHz	27~117MHz
TT@0.9~1.1V@0~100℃	54~197MHz	41~184MHz
FF@0.9~1.1V@0~100℃	85~260MHz	66~242MHz

2.7 Design Flow of the Proposed Delay Ratio Estimator

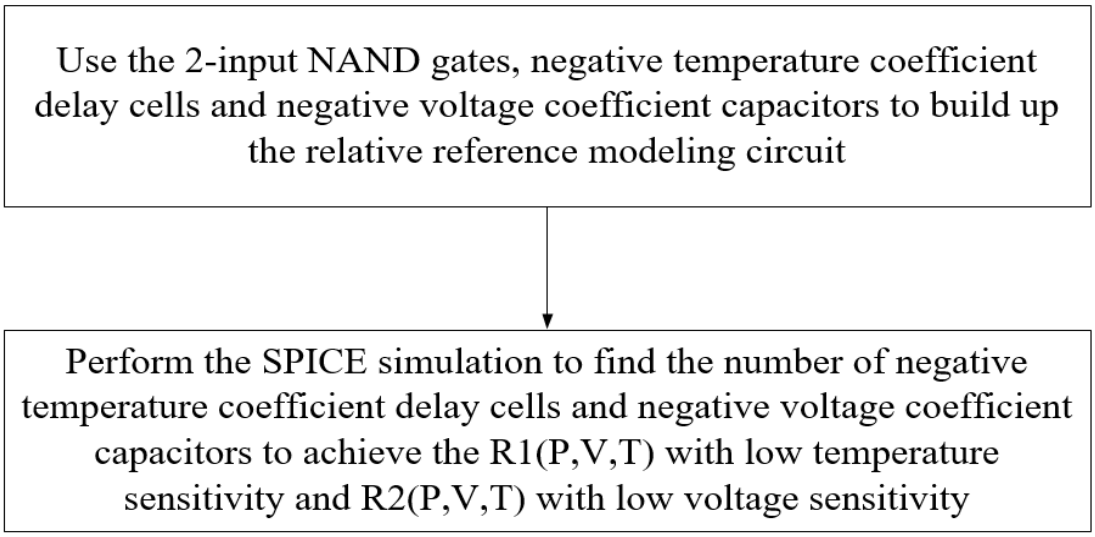


Fig. 2.18 Design flow of proposed delay ratio estimator

Fig. 2.18 shows the design flow of the proposed delay ratio estimator which uses the negative temperature coefficient delay cells and negative voltage coefficient

capacitors to build up the relative reference modeling circuit. Compared to the design flow in [24], as shown in Fig 2.4, the proposed delay ratio removes the requirement of finding the best cell combination which needs to try many the delay cells in the cell library to build up the relative reference modeling circuit and perform many times of SPICE simulation. The best cell combination in [24] is by the simulation-based method without theoretical reason oppositely. The proposed delay ratio estimator can tune the voltage and temperature coefficient of the delay cells, and does not need to try the cell combinations.

2.8 Architecture of Proposed Temperature Sensor

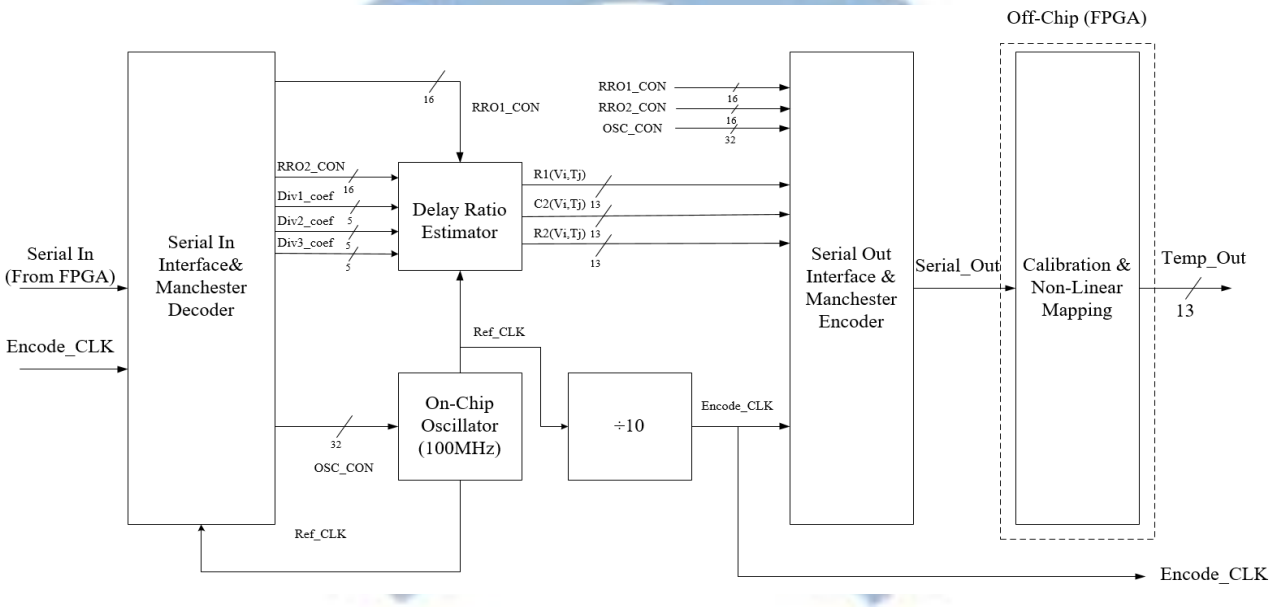


Fig. 2.19 Test chip architecture of proposed temperature sensor

Fig. 2.19 shows the test chip architecture of proposed temperature sensor. The input setting of delay ratio estimator and the on-chip oscillator will use the FPGA test board and data are encoded in Manchester codes. After input setting configurations, the delay ratio estimator will calculate the R1 and R2 value. Subsequently, the Manchester encoder will encode the R1 and R2 value into data sequence of Manchester codes and

outputs, Serial_Out. Before the normal operation of the temperature sensor, the process variations of R1 and R2 should be eliminated by calibrating.

Fig 2.20 shows the calibration and non-linear mapping circuit. After getting the data sequence output from the proposed test chip, the data sequence should be decoded to get the R1 and R2 value by using the FPGA test broad. At first, R1 should be measured under three voltages (0.9V1.0V,1.1V) and get the threshold values of R1(0.9V), R1(1.0V) and R1(1.1V) to eliminate the process variation. Subsequently, the voltage detector will use R1(0.9V), R1(1.0V) and R1(1.1V) to interpolate and gets the threshold values for R1(0.925V), R1(0.95V), R1(0.975V), R1(1.025V), R1(1.050V), R1(1.075V). After the calibration of R1 is completed in the normal operation, the value R1(Vi,Tj) at the unknown voltage Vi and unknown temperature Tj will be calculated, then the voltage detector will detect the current supply voltage. As illustrated in Fig 2.21, if the R1(0.9V) is 675, R1(0.925V) is 650 and the current R1(Vi,Tj) is 662. The R1(Vi,Tj) is more close to the threshold R1(0.925V) than the threshold R1(0.9V), the voltage detector will determine the current supply voltage is 0.925V (Current_Volt = 4'd1).

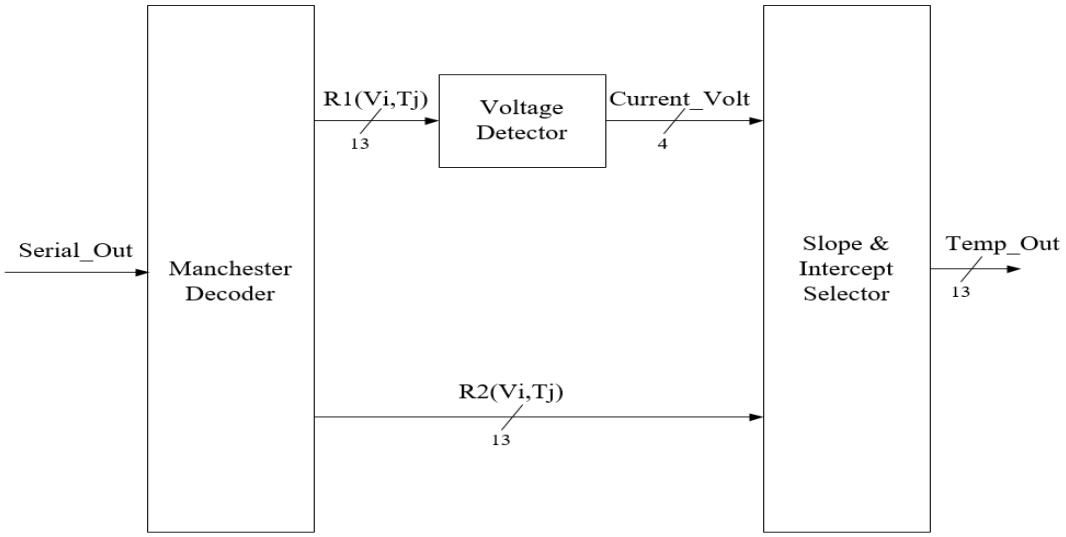


Fig 2.20 Architecture of calibration and non-linear mapping

Table 2.4 Output of voltage detector and the corresponding supply voltage

Current_Volt	Current Supply Voltage
4'd0	0.9V
4'd1	0.925V
4'd2	0.95V
4'd3	0.975V
4'd4	1.0V
4'd5	1.025V
4'd6	1.05V
4'd7	1.075V
4'd8	1.1V

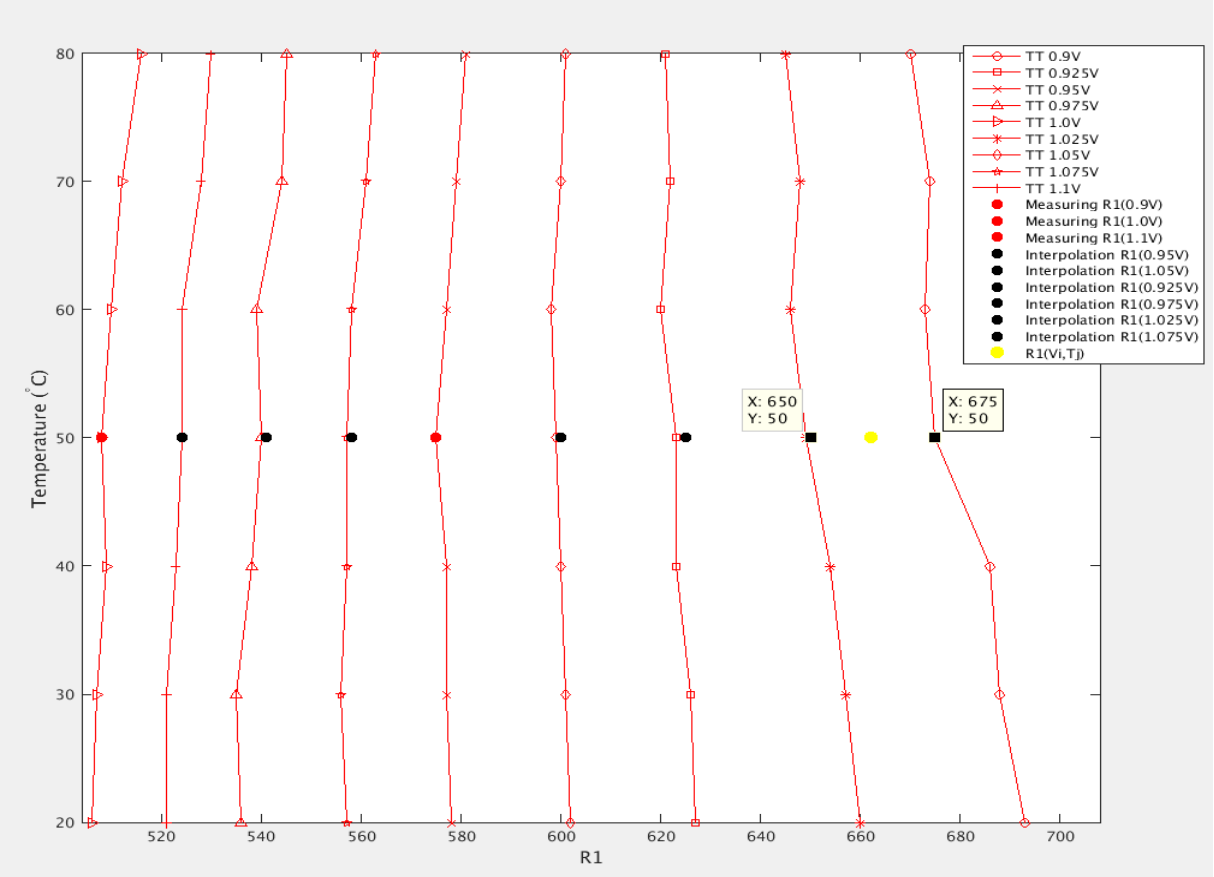


Fig 2.21 R1 value after calibration at TT corner

As shown in Fig 2.15, the PTAT R2(Vi,Tj) needs to establish the relationship with the absoulte temperature before it can be used as a temperature sensor. The relationship between the absoulte temperature and the R2(Vi,Tj) can be fitting as a second order

equation to represent as expressed in (2.15). The second order equation needs to do the 3-point calibration under different voltage and then $a(Vi), b(Vi), c(Vi)$ coefficients can be calculated. As shown in Fig 2.15, R2 will have different $a(Vi), b(Vi), c(Vi)$ under voltage variations. After getting the $a(Vi), b(Vi), c(Vi)$ value, the slope and intercept selector in Fig 2.20 will select the appropriate $a(Vi), b(Vi), c(Vi)$ based on the current supply voltage information (Current_Volt) and let the R2 can tolerates voltage variations.

$$\text{Temp\_Out} = a(Vi) * \left(R2(Vi, Tj)\right)^2 + b(Vi) * R2(Vi, Tj) + c(Vi) \qquad (2.15)$$

2.9 Summary

In chapter 2.4, we proposed the method to build up the relative reference modeling circuit which directly tuned the temperature and voltage coefficient of the delay cells. Subsequently, the low-temperature dependency voltage classifier had been proposed in section 2.5, which use 2-input NAND gates and high voltage sensitivity 2-input NAND gates to build up the relative reference modeling circuit and implemented the difference calculator to detect the current supply voltage under temperature variations. In section 2.6, the low voltage dependency PTAT circuit had been introduced which use the 2-input NAND gates and negative temperature coefficient delay cells to implement the delay ratio estimator.

In section 2.7, we analyzed the problem in the design flow of delay ratio estimator in [24]. Compared to [24], the proposed delay ratio estimator removes the searching process of best cell combination which needs to spend a lot of time to perform the SPICE simulation. In section 2.8, the test chip implementation of proposed temperature sensor had been introduced which contains the circuitry required for the subsequent wafer test interface and calibration.

Chapter 3 Experimental Results

3.1 Test Chip Implementation

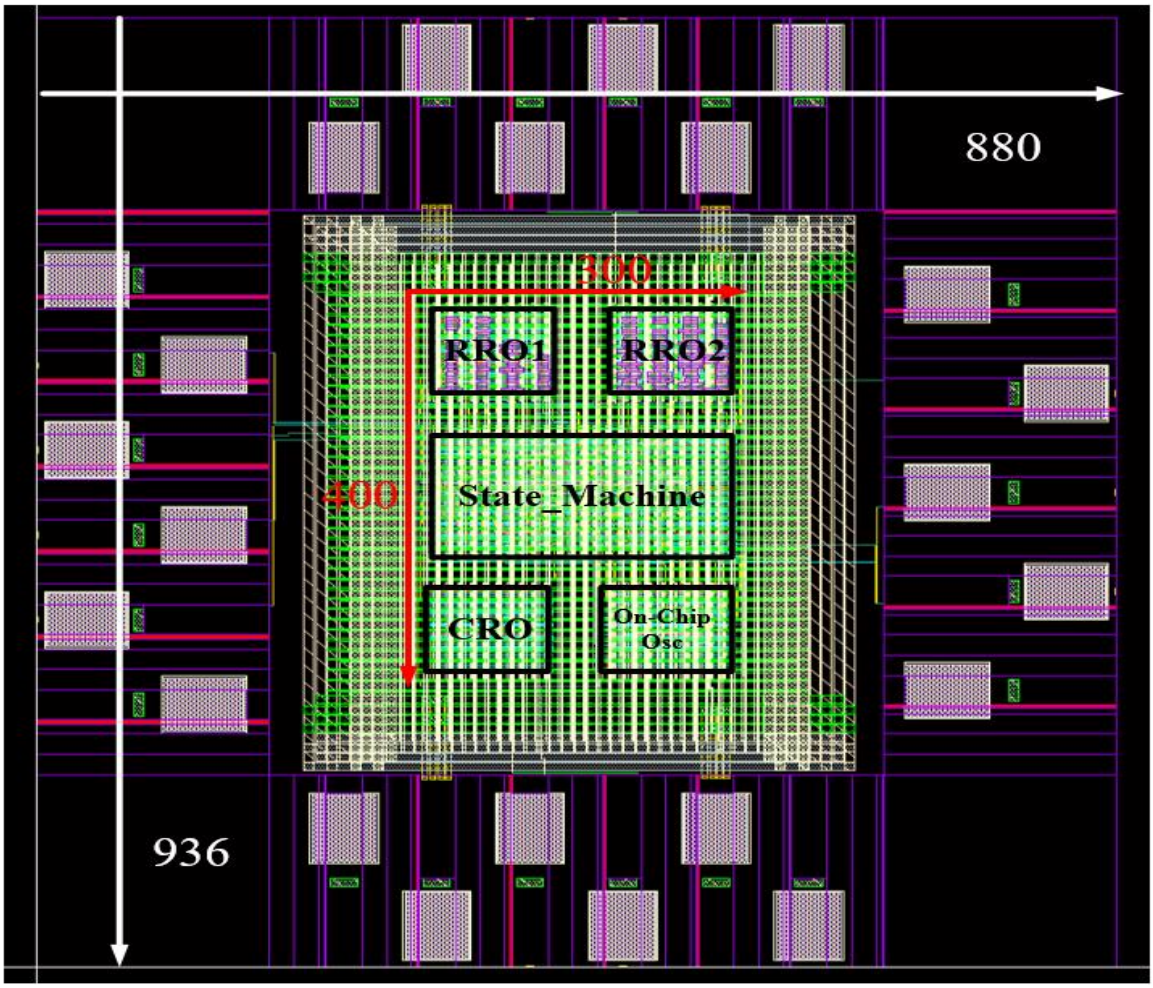


Fig. 3.1 Layout of the test chip

The layout of the test chip is shown in Fig. 3.1. The architecture of the test chip is shown in Fig. 2.19. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The core size of the chip is $300\mu m * 400\mu m$. The chip size including I/O PADs is $880\mu m * 936\mu m$.

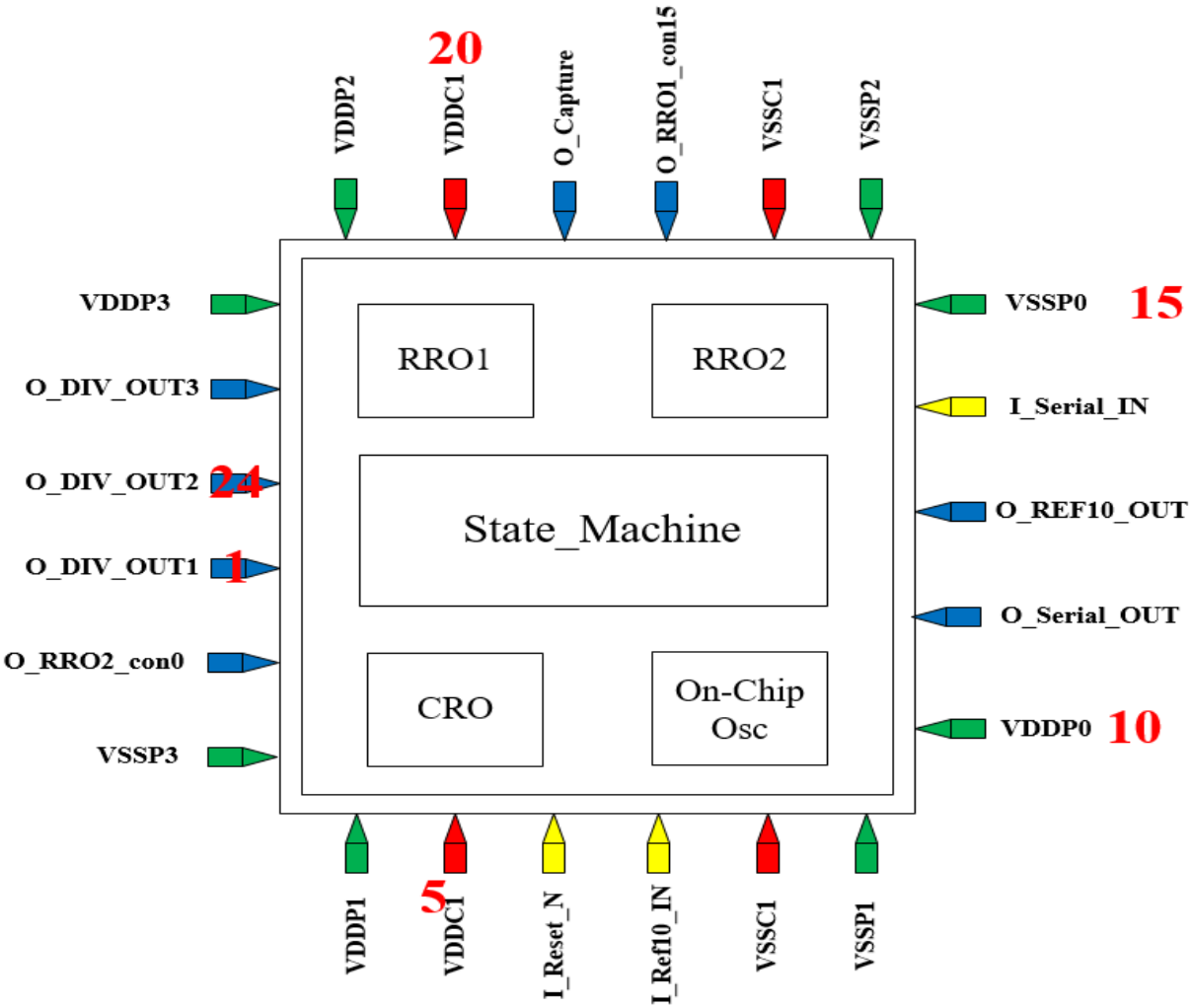


Fig. 3.2 Chip floorplan and I/O plan

Fig. 3.2 shows the test chip I/O planning and the floor planning of the proposed temperature sensor. There are 3 input pins, 8 output pins, and 12 power pins. The test chip consists of an RRO1 circuit, an RRO2 circuit, an CRO circuit, an On-Chip Oscillator circuit, and the State_Machine circuit. The detail I/O description is shown in Table. 3.1.

Table. 3.1 I/O pad Description

Pin Number	Pin Name	Input/Output	information
1	O_DIV_OUT1	Output	RRO1 divided Signal
2	O_RRO2_con0	Output	Serial in interface and Manchester decoder debug pin

3	VSSP3	Input	Pad Power
4	VDDP1	Input	Pad Power
5	VDDC1	Input	Core Power
6	I_Reset_N	Input	System asynchronous reset
7	I_Ref10_IN	Input	Serial in interface and Manchester decoder debug pin
8	VSSC1	Input	Core Power
9	VSSP1	Input	Pad Power
10	VDDP0	Input	Pad power
11	O_Serial_OUT	Output	Sequence data of R1, R2 and debug signal
12	O_Ref10_OUT	Output	On-chip oscillator debug pin
13	I_Serial_In	Input	Sequence data of Manchester code(from FPGA test board) for test chip input setting
14			
15	VSSP0	Input	Pad Power
16	VSSP2	Input	Pad Power
17	VSSC1	Input	Core Power
18	O_RRO2_con15	Output	Serial in interface and Manchester decoder debug pin
19	O_Capture	Output	Serial in interface and Manchester decoder debug pin
20	VDDC1	Input	Pad Power
21	VDDP2	Input	Pad Power
22	VDDP3	Input	Pad Power
23	O_DIV_OUT3	Output	RRO2 divided Signal
24	O_DIV_OUT2	Output	CRO divided Signal

3.2 Test Plan

In order to save the numbers of I/O pad, proposed test chip uses the FPGA board to send the data sequence for the test chip input setting. The FPGA test board will encode the test pin value into the Manchester code as shown in Fig. 3.3. The Manchester code uses the two bits signal to represent the one bit signal of data. Subsequently, the

FPGA test board will use a low-speed clock to send the packet formatted as shown in Fig. 3.4 into the test chip and the serial interface & Manchester decoder circuit shown in Fig. 2.20 will use a high speed-clock to sample the input packet. After getting the packet from the FPGA test board, the test chip will decode the packet into original data and sets up the test chip. The output R1, R2 and debug pins will be also encoded into the sequence of Manchester codes and uses a low-speed clock to send the packet as shown in Fig. 3.5 into the FPGA test board. Subsequently, the FPGA will use a high-speed clock to sample the output packet and decode the packet to get the R1, R2 and debug pin values.

Before using the temperature sensor, the Ref_CLK should be tuned to 100MHz under different PVT conditions by using the control code OSC_CON in Fig. 3.5. The FPGA will sent different packet to tune the Ref_CLK to 100MHz under PVT conditions.

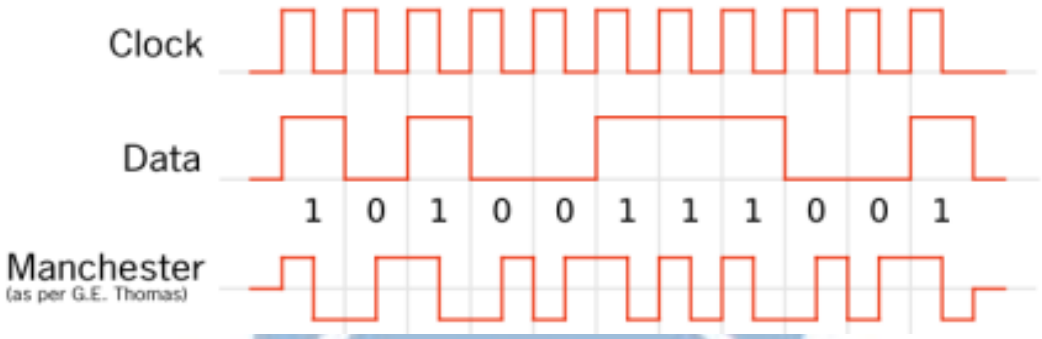


Fig. 3.3 Waveform of the Manchester encoder

(https://en.wikipedia.org/wiki/Manchester_code)

Header (8bits)	RRO1_CON (8bits)	RRO2_CON (8bits)	OSC_CON (10bits)	Div1_coef (10bits)	Div2_coef (10bits)	Div3_coef (10bits)

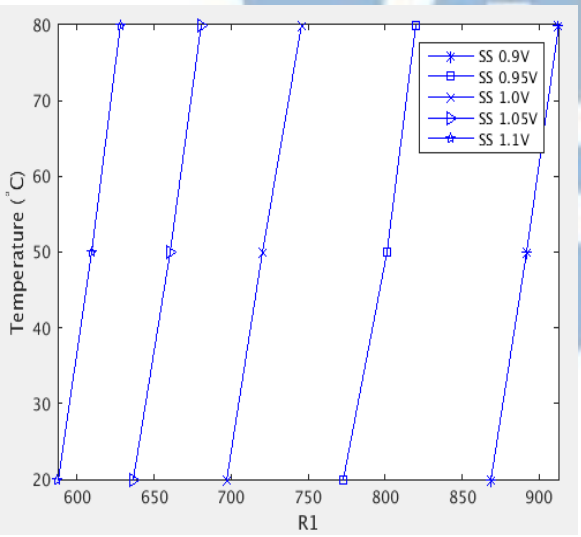
Fig. 3.4 Serial input packet for test chip input setting

R1_Header (16bits)	R1 (26 bits)	R2_Header (8bits)	R2 (26bits)	C2_Header (8bits)	C2 (26bits)	Input Pattern Header (8bits)	RRO1_CON (8bits)	RRO2_CON (8bits)	OSC_CON (10bits)

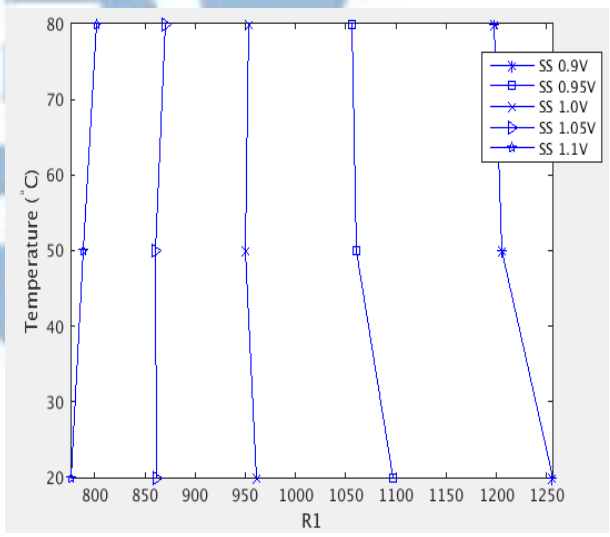
Fig. 3.5 Serial output packet for test chip measurement and debug

3.3 Post-Layout Simulation of the Voltage Classifier

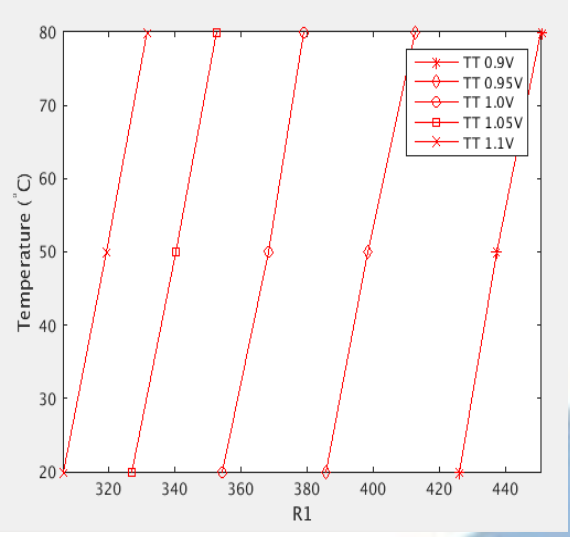
Fig. 3.6(a)(c)(e) shows the post-layout simulation of R1 value. R1 value suffers from temperature variations before temperature coefficient compensation delay cells have been enabled. Fig 3.6(b)(d)(f) shows the R1 value under different process corner after temperature coefficient compensation by using the path selector to choose the number of the thyristors. The temperature coefficient of R1 becomes close to zero after temperature coefficient compensation. Subsequently, R1 is sensitive to voltage variations but is not sensitive to temperature variations which can be used to sense the supply voltage under temperature variation.



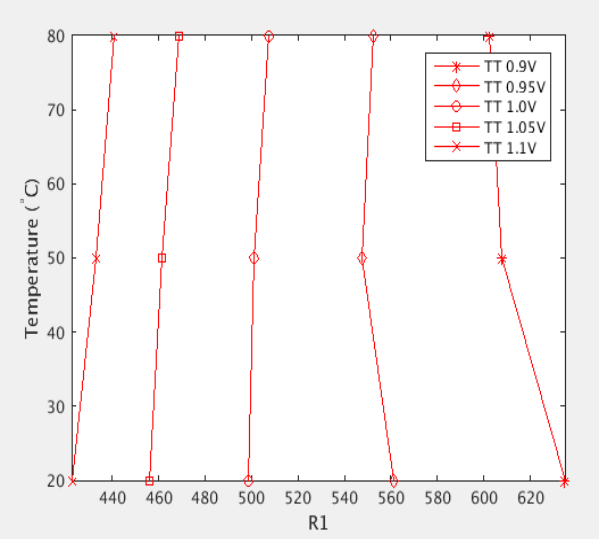
(b) R1 before temperature cofficient compensation under SS case (open 0 stage thyristor)



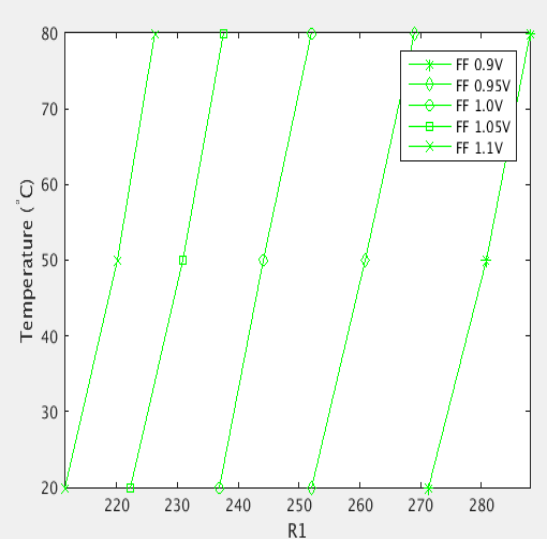
(b) R1 after temperature cofficient compensation under SS case (open 1 stage thyristor)



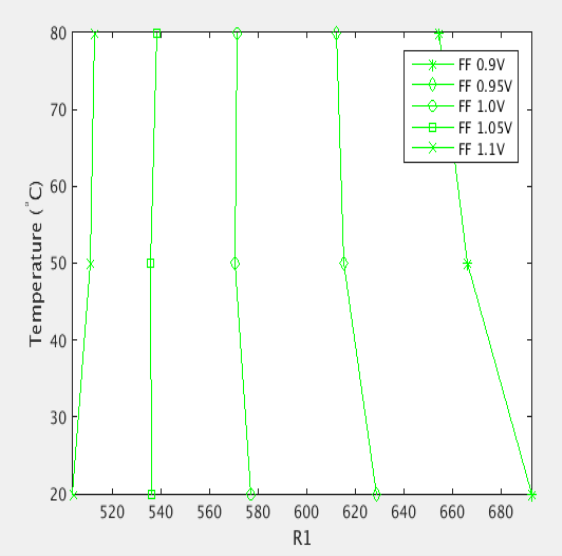
(c) R1 before temperature cofficient compensation under TT case (open 0 stage thyristor)



(d) R1 after temperature cofficient compensation under TT case (open 2 stages thyristor)



(e) R1 before temperature cofficient compensation under FF case (open 0 stage thyristor)

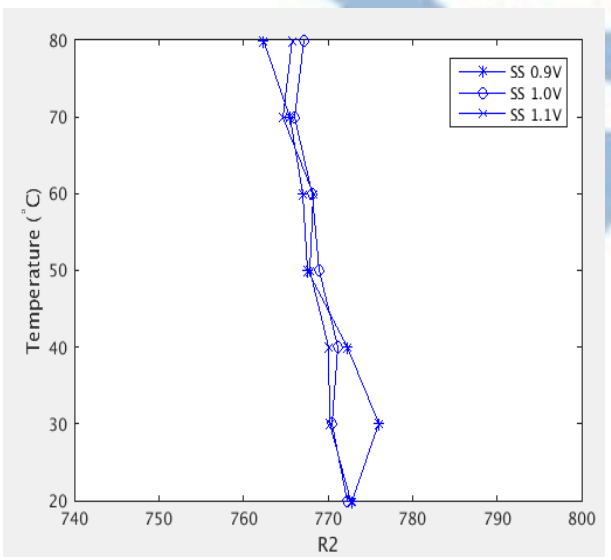


(f) R1 after temperature cofficient compensation under FF case (open 5 stages thyristor)

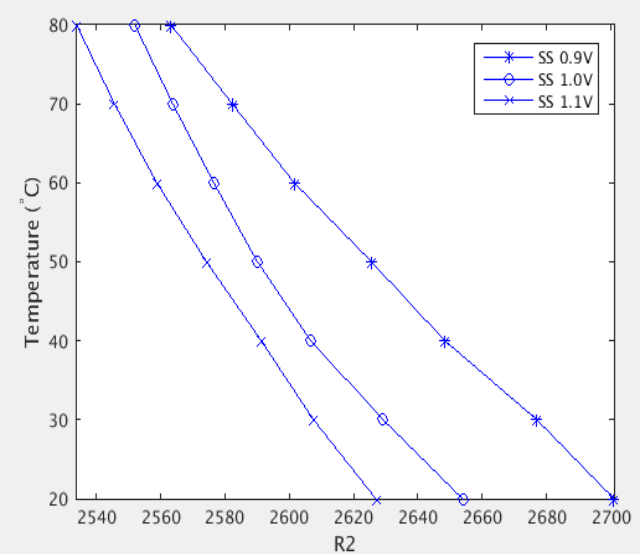
Fig. 3.6 R1 post-layout simulation before and after temperature coefficient compensation under different PVT variations

3.4 Post-Layout Simulation of the PTAT Circuit

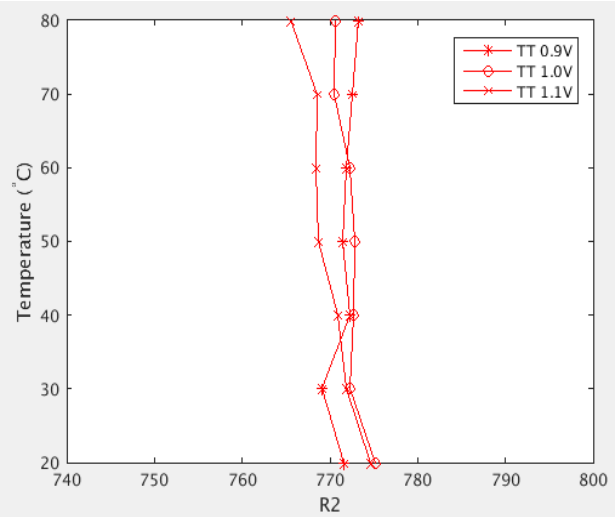
Fig. 3.7 shows the post-layout simulation of R2 value. As shown in Fig. 3.7 (a)(c)(e), the CRO and RRO2 have similar temperature coefficient before temperature coefficient compensation and then the R2 value will not have temperature dependency. Fig. 3.7 (b)(d)(f) shows the R2 value under different process corner after temperature coefficient compensation by using the path selector shown in Fig. 2.13 to choose the number of the thyristors used for compensation. The temperature coefficient of RRO2 becomes more negative after temperature coefficient compensation. The R2 value will have strong temperature dependency for serving as a PTAT circuit. However, the voltage coefficient of the RRO2 is not same as the CRO. There existing the influence of voltage variations. In order to lower the error of the temperature sensor caused by voltage variations, the proposed temperature sensor uses the voltage classifier to detect the current supply voltage and then the output of the proposed PTAT can have low voltage dependency.



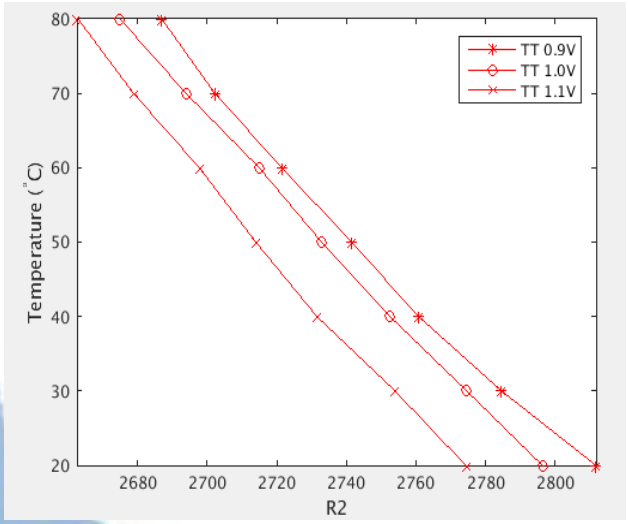
(a) R2 before temperature cofficient compensation under SS case (open 0 stage thyristor)



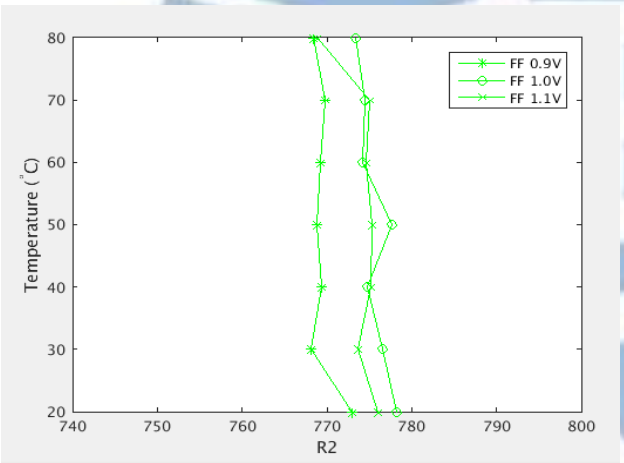
(b) R2 after temperature cofficient compensation under SS case (open 6 stage thyristor)



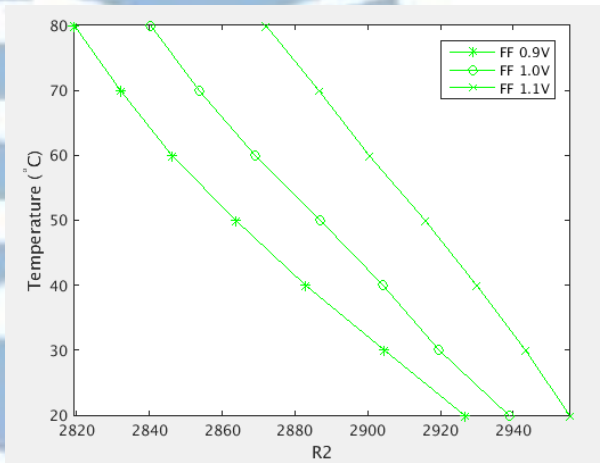
(c) R2 before temperature cofficient compensation under TT case (open 0 stage thyristor)



(d) R2 after temperature cofficient compensation under TT case (open 7 stages thyristor)



(e) R2 before temperature cofficient compensation under FF case (open 0 stage thyristor)



(f) R2 after temperature cofficient compensation under FF case (open 8 stages thyristor)

Fig. 3.7 R2 post-layout simulation before and after temperature coefficient compensation under different PVT variations

3.5 Calibration of the Voltage Classifier

The resolution of the proposed voltage classifier is 25mV and three calibration points are R1(0.9V,50℃), R1(1.0V,50℃) and R1(1.1V,50℃). In calibration flow, the R1 value will be measured at (0.9V,50℃), (1.0V,50℃) and (1.1V,50℃) to get the R1(0.9V), R1(1.0V) and R1(1.1V). The other threshold values R1(0.925V), R1(0.950V), R1(0.975V), R1(1.025V), R1(1.05V) and R1(1.075V) will be calculated by using the three calibration points to interpolate as shown in Fig. 3.8 and Eq. (3.1) to Eq. (3.6). After calibration, the R1(Vi,Tj) which is at a unknown voltage Vi and unknown Tj will use the 9 different threshold value R1(0.9V), R1(0.925V), R1(0.950V), R1(0.975V), R1(1.0V), R1(1.025V), R1(1.05V), R1(1.075V) and R1(1.1V) to determine which threshold is more close to the R1(Vi,Tj) and detect the current supply voltage.

$$R1(0.95V) = \frac{R1(0.9V) + R1(1.0V)}{2} \tag{3.1}$$

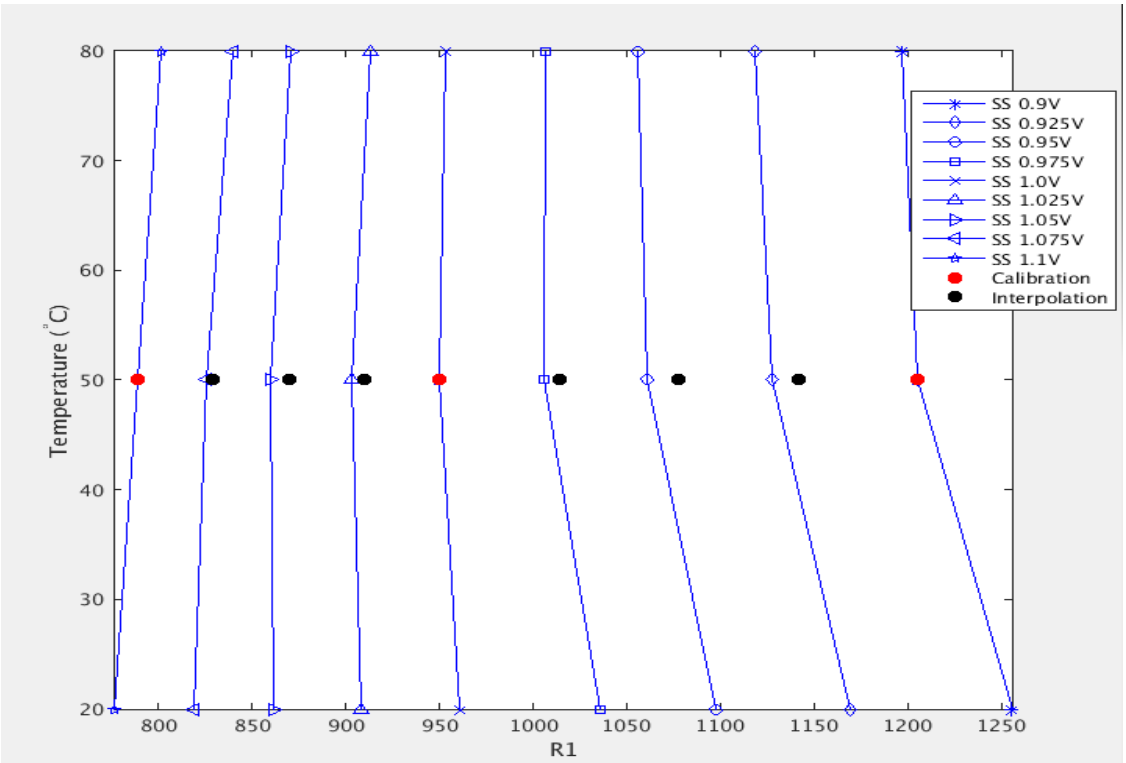
$$R1(1.05V) = \frac{R1(1.1V) + R1(1.0V)}{2} \tag{3.2}$$

$$R1(0.925V) = \frac{R1(0.9V) + R1(0.95V)}{2} \tag{3.3}$$

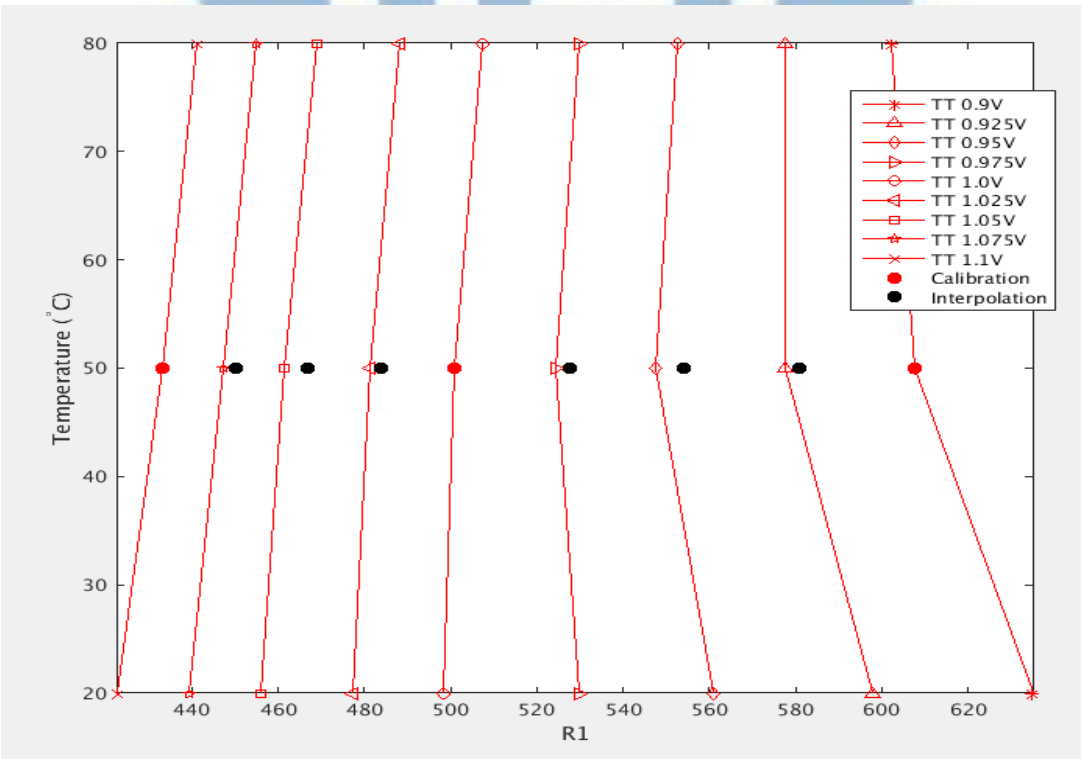
$$R1(0.975V) = \frac{R1(1.0V) + R1(0.95V)}{2} \tag{3.4}$$

$$R1(1.025V) = \frac{R1(1.0V) + R1(1.05V)}{2} \tag{3.5}$$

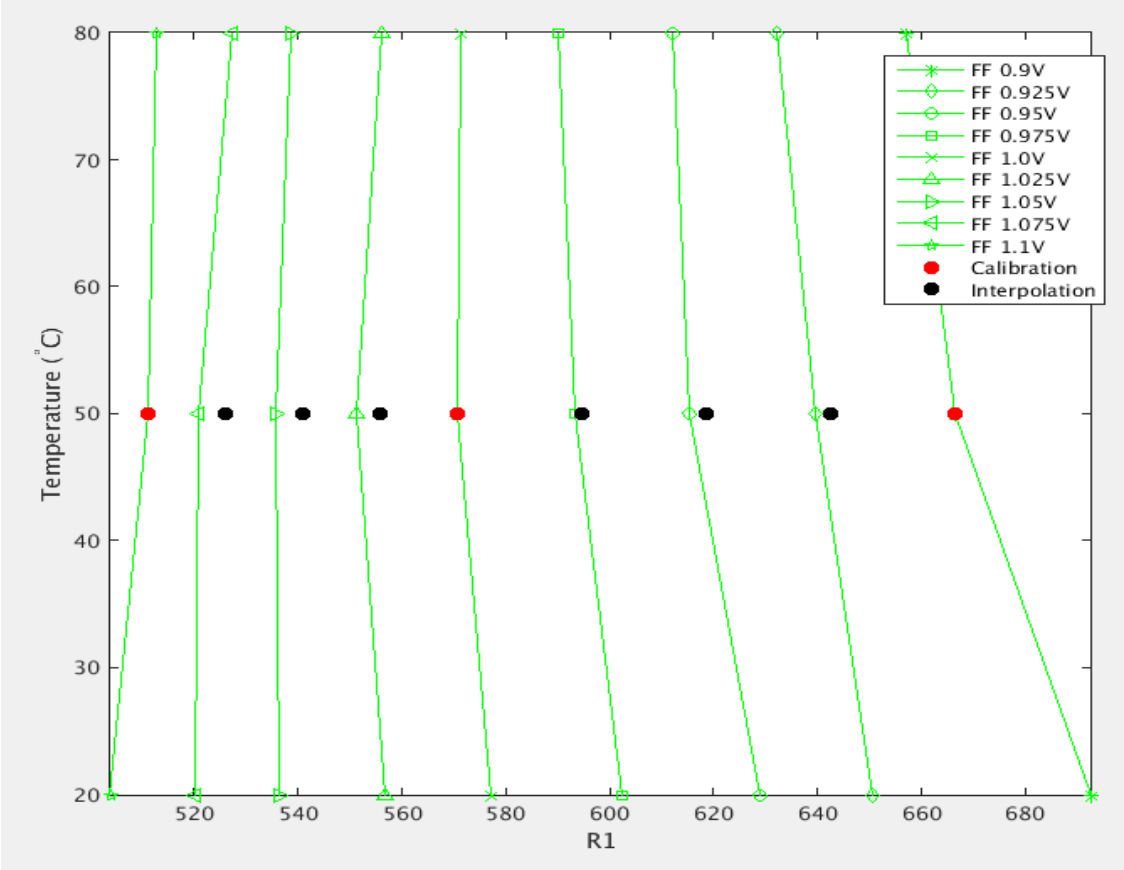
$$R1(1.075V) = \frac{R1(1.1V) + R1(1.05V)}{2} \tag{3.6}$$



(a) Calibration and interpolation threshold value of R1 at SS corner



(b) Calibration and interpolation threshold value of R1 at TT corner



(c) Calibration and interpolation threshold value of R1 at FF corner

Fig. 3.8 Calibration and interpolation threshold value of R1 under different corner

Fig. 3.9 shows the classified error of proposed voltage classifier at TT corner, the threshold R1(1.075) is 450 and the threshold R1(1.1V) is 433, the R1(1.075V,20℃) is 439 which is more close to the threshold R1(1.1V) and the voltage classifier will determine the current supply voltage is 1.1V. However, the actual supply voltage at R1(1.075V,20℃) is 1.075V and cause the error of 25mV. Due to the proposed voltage classifier will still have temperature dependency at TT corner after temperature compensation which will cause the classifier error. Subsequently, proposed voltage classifier can detect the supply voltage accurately at SS and FF corners under 25mV resolution.

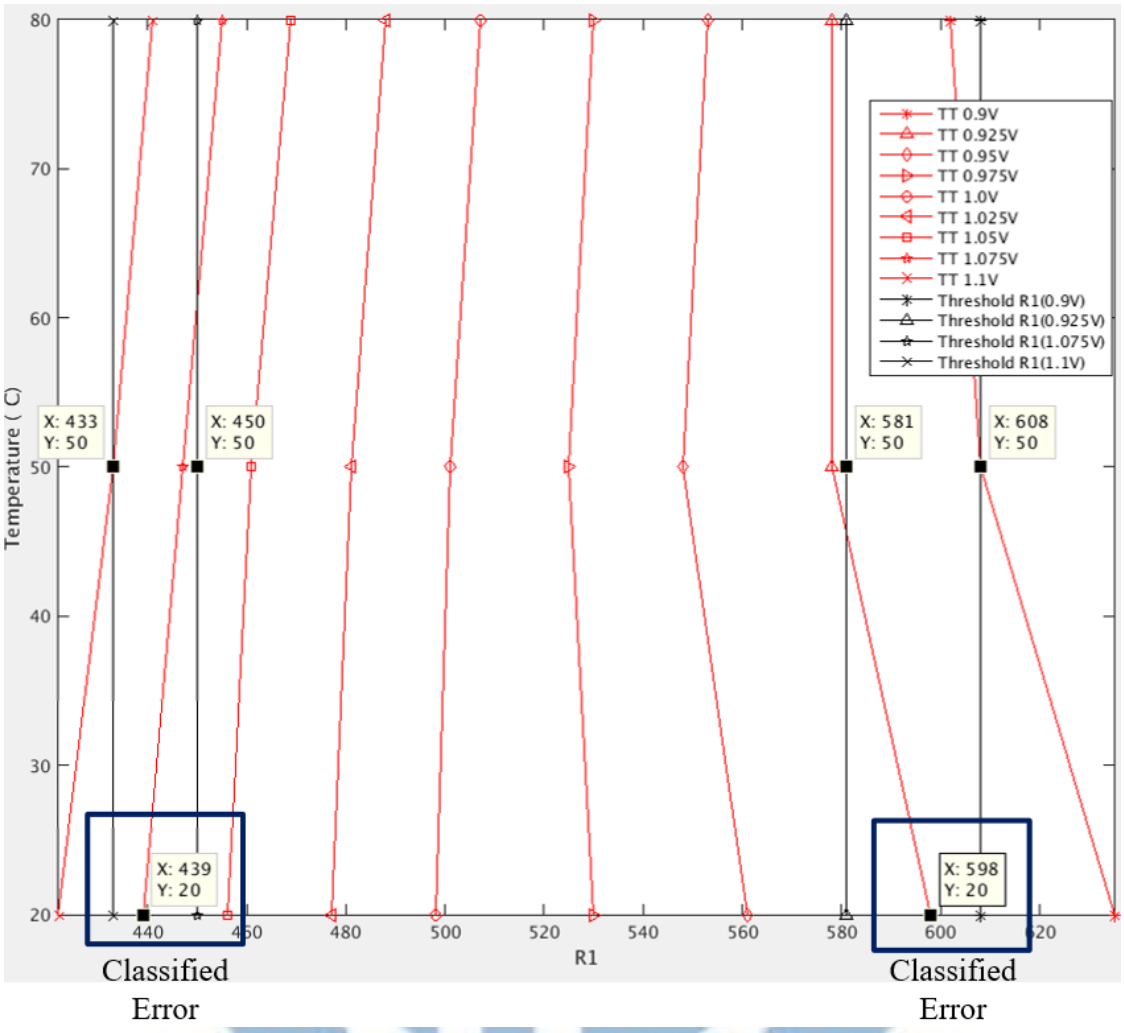


Fig. 3.9 Classified error according to the threshold value at TT corner

If there will not have classified error as shown in Fig. 3.9 to consider the worst case error of proposed voltage classifier. The maximum error will occur when the current supply voltage falls into the center of two adjacent thresholds as shown in Fig. 3.10. If the resolution of voltage classifier is 25mV and the current supply voltage is 1.0875V, the voltage classifier will classify current supply voltage into 1.075V or 1.1V, so the maximum error will be the half of voltage resolution (i.e.12.5mV). Table. 3.2 shows the maximum error of proposed voltage classifier which is inferred from Fig. 3.9 and Fig. 3.10.

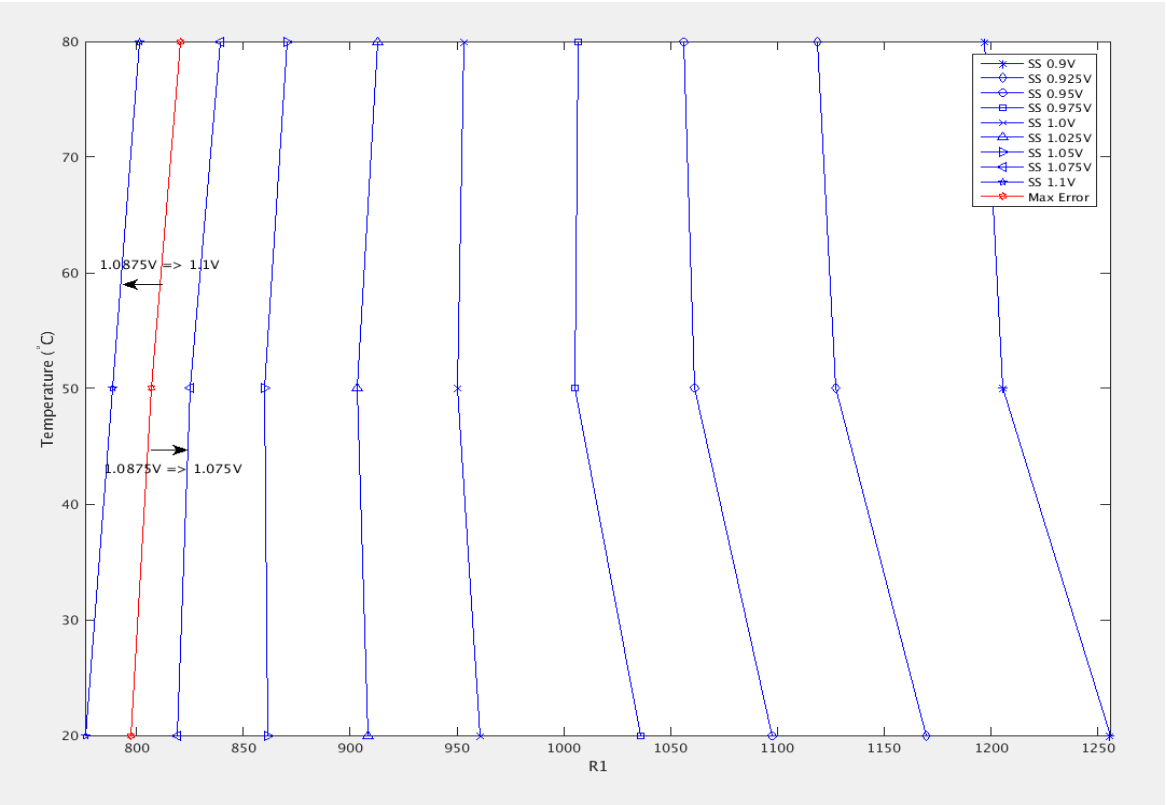


Fig. 3.10 Worst case of proposed voltage classifier

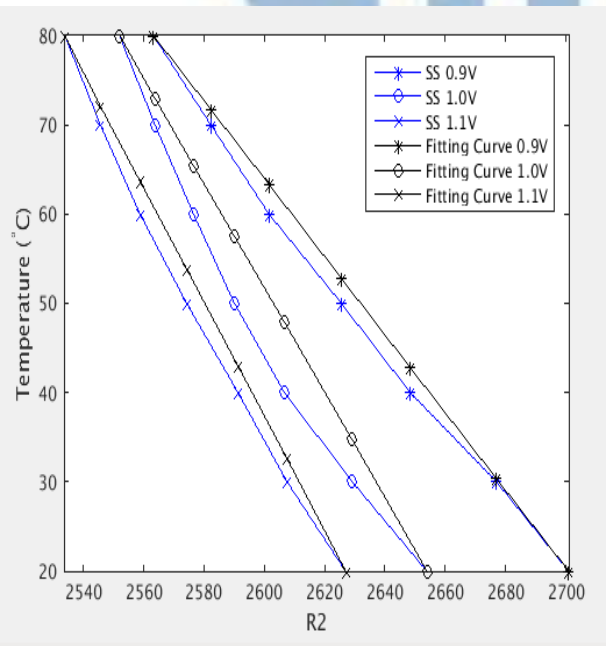
Table 3.2 Maximum error of proposed voltage classifier after calibration

	SS	TT	FF
Maximum Error	12.5mV	25mV	12.5mV

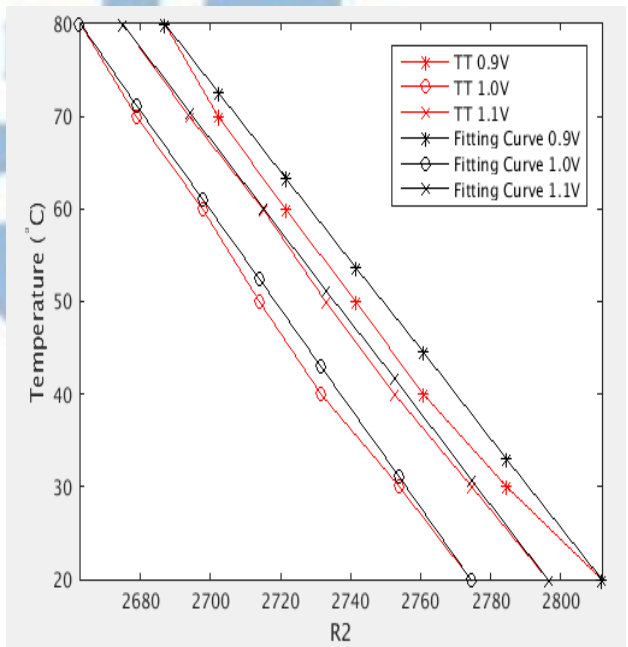
3.6 Calibration of the Proposed PTAT

The proposed PTAT circuit, R2 needs to be calibrated at known temperatures after the test chip tape-out to eliminate the process variations and to solve the equations (3.1) or (3.2) coefficients to build up the relationship between R2 and the absolute temperature. Fig. 3.11 shows the first-order fitting curve which uses (3.1) at different PVT. There will have large fitting error between the first-order curve and the actual R2 curve which will increase the error of the temperature sensor. Fig. 3.12 shows the error of proposed temperature sensor after first-order fitting (two-point calibration) which has a large error of $-1.6℃\sim7.8℃$.

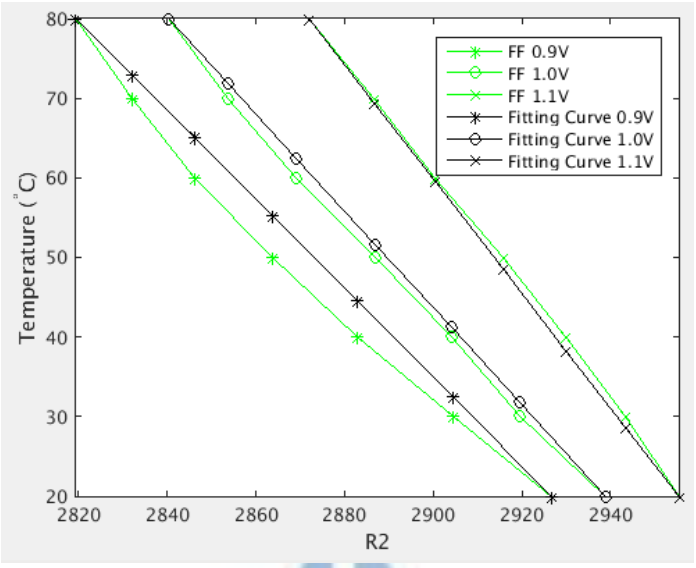
$$1_{st}\ \text{Fitting Curve} = \text{a(Vi)} * R2(Vi, Tj) + b(Vi) \qquad (3.1)$$



(a) R2 and the fitting curve verus voltage and temperature at SS corner



(b) R2 and the fitting curve verus voltage and temperature at TT corner



(c) R2 and the fitting curve verus voltage

and temperature FF corner

Fig. 3.11 R2 and the first-order fitting curve at different PVT conditions

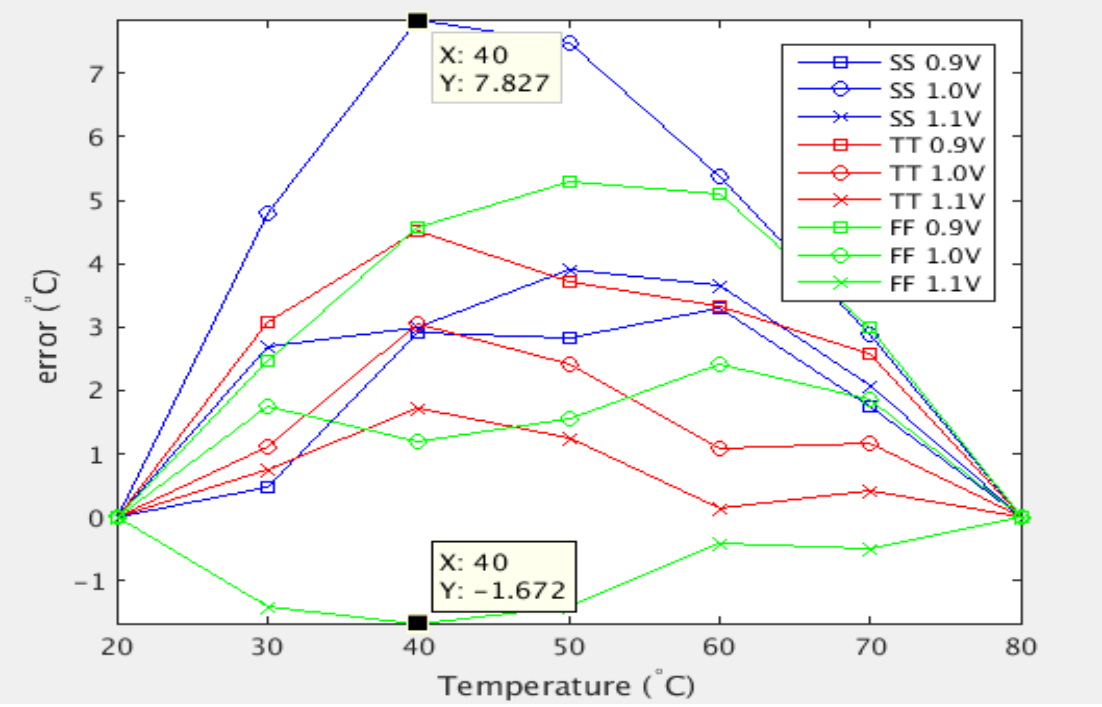
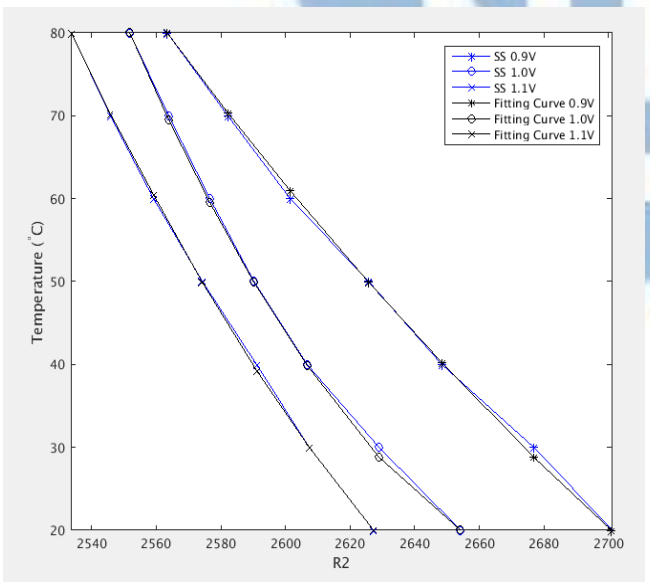


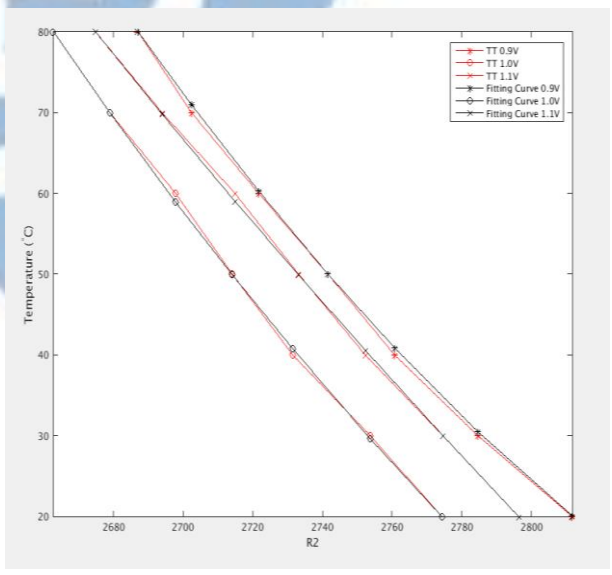
Fig. 3.12 The error of proposed temperature sensor after first-order curve fitting

Fig. 3.13 shows the second-order fitting curve which can be expressed by (3.2). The second-order curve can be fitting closely to the actual R2 curve. However, the second-order curve requires three calibration points to solve the equation coefficients in (3.2) which increases the testing cost of the proposed temperature sensor. Fig. 3.14 shows the error of proposed temperature sensor which error is reduced to $-1.2℃\sim1.1℃$. In order to lower the error of proposed temperature sensor, the second-order curve fitting method should be adopted. The first-order curve fitting method is not acceptable, if the influence of the voltage classifier error is included. The proposed temperature sensor with the first-order curve fitting method will have large temperature error which may exceed 10 degrees.

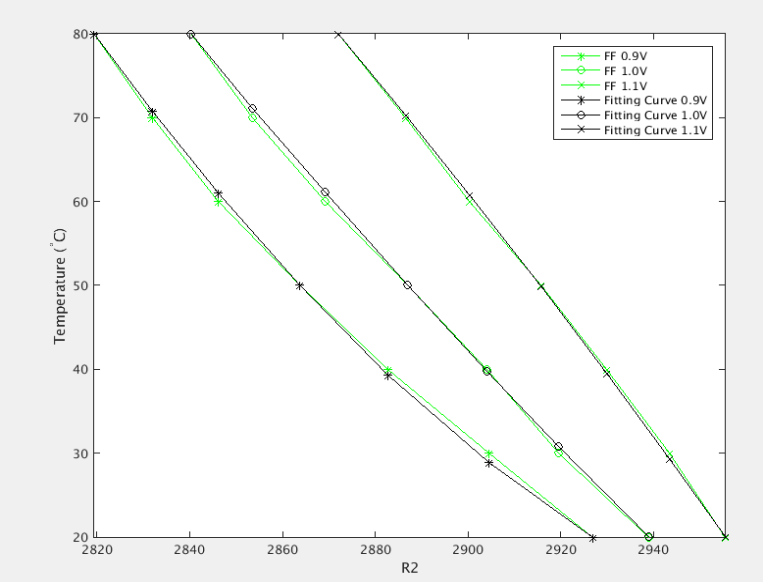
$$2_{nd}\ \text{Fitting Curve} = \text{a(Vi)} * R2(Vi,Tj)^2 + b(Vi) * R1(Vi,Tj) + c(Vi) \qquad (3.2)$$



(b) R2 and the fitting curve verus voltage and temperature at SS corner



(b) R2 and the fitting curve verus voltage and temperature at TT corner



(c) R2 and the fitting curve verus voltage

and temperature FF corner

Fig. 3.13 R2 and the second-order fitting curve at different PVT

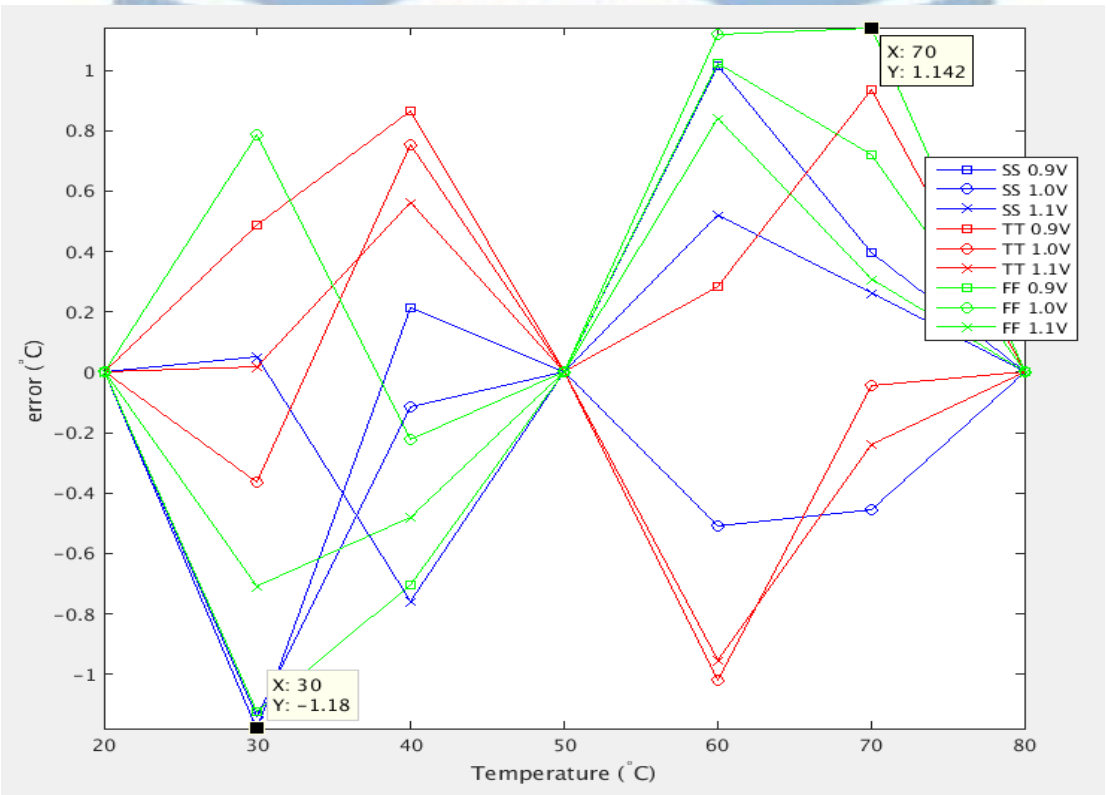


Fig. 3.14 The error of proposed temperature sensor after second-order curve fitting

3.7 Worst Case Error of the Proposed Temperature Sensor

The error of temperature sensor shown in Fig. 3.12 and Fig. 3.14 is not considering that the voltage classifier may introduce voltage classification error. In this section, the influence of the voltage classifier on the proposed temperature sensor will be discussed. In section 3.5, the maximum error of proposed voltage classifier had been discussed. Although proposed voltage classifier can detect the supply voltage accurately at SS and FF corners under 25mV resolution, there still have a 12.5mV maximum error since the resolution is not fine. The proposed temperature sensor will compensate for the PTAT output according to the voltage information from the voltage classifier.

At TT process corner, the proposed voltage classifier may have 25mV error as shown in Fig. 3.9. Fig. 3.15 shows the error of the proposed temperature sensor which considers the 25mV voltage classifier error, and the worst case error is increased to $-4.3℃\sim4.3℃$ after three point calibration.

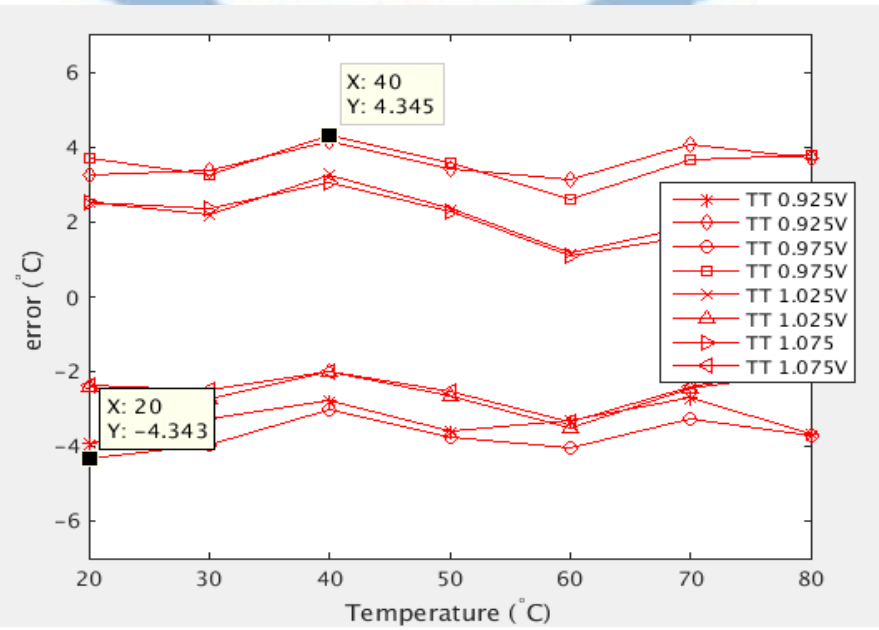
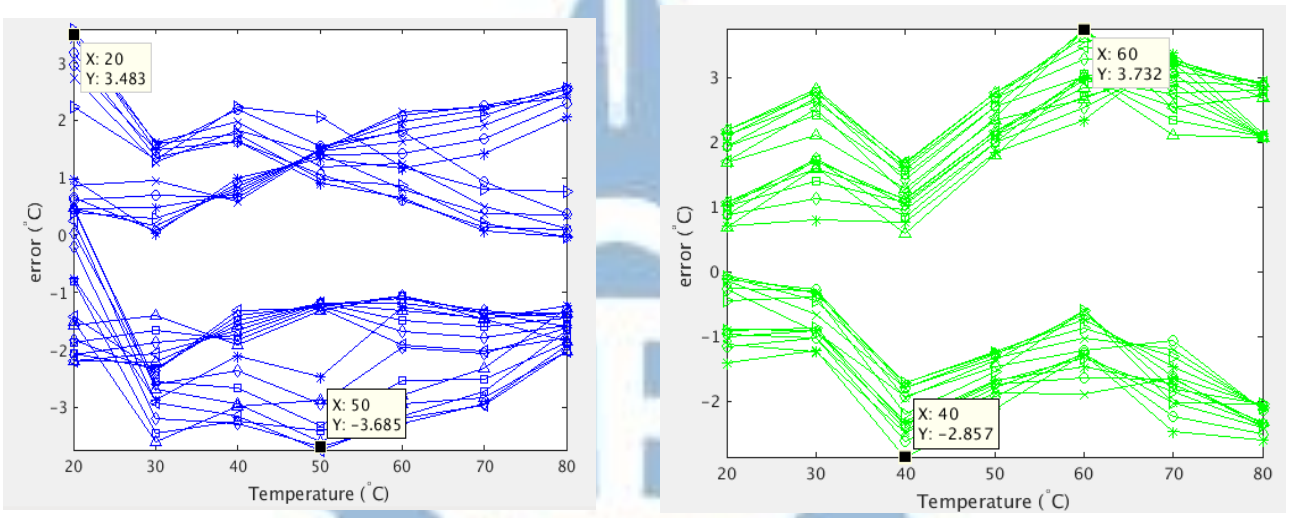


Fig. 3.15 Proposed temperature sensor error under 25mV voltage maximum error at TT corner

At SS and FF process corners, the proposed voltage classifier may have 12.5mV maximum error due to the insufficient of the voltage classifier resolution. Fig. 3.16(a) shows the error of the temperature sensor at SS process corner which considers the 12.5mV voltage classifier error and the worst case error is $-3.7\sim3.5℃$ after three point calibration. Fig. 3.16(b) shows the error of the temperature sensor at FF process corner which considers the 12.5mV voltage classifier error and the worst case error is $-2.9\sim3.7℃$ after three point calibration.



(a) SS corner (b) FF corner

Fig. 3.16 Influence of the 12.5mV voltage maximum error on proposed temperature sensor at SS and FF process corners

3.8 Comparison Table

Table. 3.3 shows the comparison table of the proposed temperature sensor and other smart temperature sensors. The temperature sensors in [33] and [35] cannot resist the voltage variations and have large error under voltage variations. The temperature sensor in [36] which needs voltage supply regulator at advanced CMOS process and have the high power consumption. The temperature sensor in [34] which use the voltage difference to resist the voltage variation but the error is still too large under variation. The other temperature sensor in [31] is full-custom design and needs extra read circuit

like high resolution off-chip ADC and needs to find the appropriate CTAT and PTAT which is matched. Subsequently, [12] is full-custom design which is more complex and is not portable to different process, also need a high-order curve fitting method.

Table 3.3 Performance comparisons of temperature sensor (tape-out version)

	[33] ASP-DAC'16	[35] TVLSI'12	[31] JSSC'15	[12] JSSC'16	[34] TBioCAS'17	[36] ISSCC'12	Proposed Work
Method	Digital	Digital	Analog	Analog	Analog	Analog	Digital
Technology(nm)	28	130	65	65	65	32	90
Voltage Insensitivity	No	No	Yes	Yes	Yes	Yes	Yes
Supply Regulator	No	No	No	No	No	Yes	No
Temp. Range(℃)	0~100	0~100	0~100	0~100	30~70	20~100	20~80
VDD Range(V)	Fixed 0.9V	Fixed 1.2V	0.6~1	0.85~1.05	0.2~0.4	1.4~1.8	0.9~1.1
Resolution(℃)	0.44	0.78	N/A	0.3	N/A	0.2	0.6
Conversion Rate (k sample/S)	5	5	20	45.5	N/A	2	24.2
Error (℃)	-4.3~4.3 (at 0.9V)	-4~4 (at 1.2V) -90~90 (1.08V~1.32V)	-2.4~1.5	-5~2.2	-5~8.1	-1.5~1.5	-4.3~4.3
Power (mW)	0.45	1.2	0.36	0.15	0.25	3.8	4.4
Area(mm^2)	0.003738	0.12	0.648	0.0042	N/A	0.02	0.12
Energy for one conversion (μJ)	0.009	0.24	0.0018	0.0033	N/A	1.9	0.18
Supply Sensitivity(℃/mV)	N/A	N/A	0.0098	0.034	0.069	0.0075	0.043
Master Curve	1_{st}	3_{rd}	1_{st}	2_{nd}	1_{st}	1_{st}	2_{nd}
Temp. Calibration Point	2pt	1pt	2pt	2pt	2pt	2pt	3pt

Chapter 4 Cost-Down Version of Proposed Temperature Sensor

4.1 Introduction

The number of thyristors in the cost-down version will be reduced to 8 which need more time to achieve enough resolution of the proposed temperature sensor. Therefore, the conversion rate will be reduced to 2k sample/sec. Although the conversion rate will be lower, it still quite enough for most IoT applications.

In the tape-out version, the conversion rate of R1 is 200k sample/sec and the conversion rate of R2 is 24.2k sample/sec. Due to the conversion rate of R2 in the cost-down version is 2k sample/sec, the conversion rate of R1 is lowered to 2k sample/sec. Therefore, the reference clock (Ref_CLK) which used to get the R1 value can be lowered to 10MHz in the cost-down version.

The power consumption of each thyristor is 16uW, for the considerations of measurement and conversion rate, the total number of thyristors used is 192 which occupies most of the power consumption and area of the tape-out version temperature sensor.

As shown in Table 4.1, the proposed temperature sensor removes the trimming flow and reduces the number of thyristors in the cost-down version. The clock speed of the reference clock is reduce to one-tenth of the reference clock used in the tape-out version. However, the conversion rate of the cost-down version will be reduced to 2k sample/sec.

Table 4.1 Resource comparisons of two versions temperature sensors

	Tape-out version	Cost-down version
Ref_CLK	100MHz	10MHz
Conversion rate(k/S)	24.2k	2k
Number of thyristor	192	8
Trimming	Yes	No

4.2 Architecture of Cost-Down Version Temperature Sensor

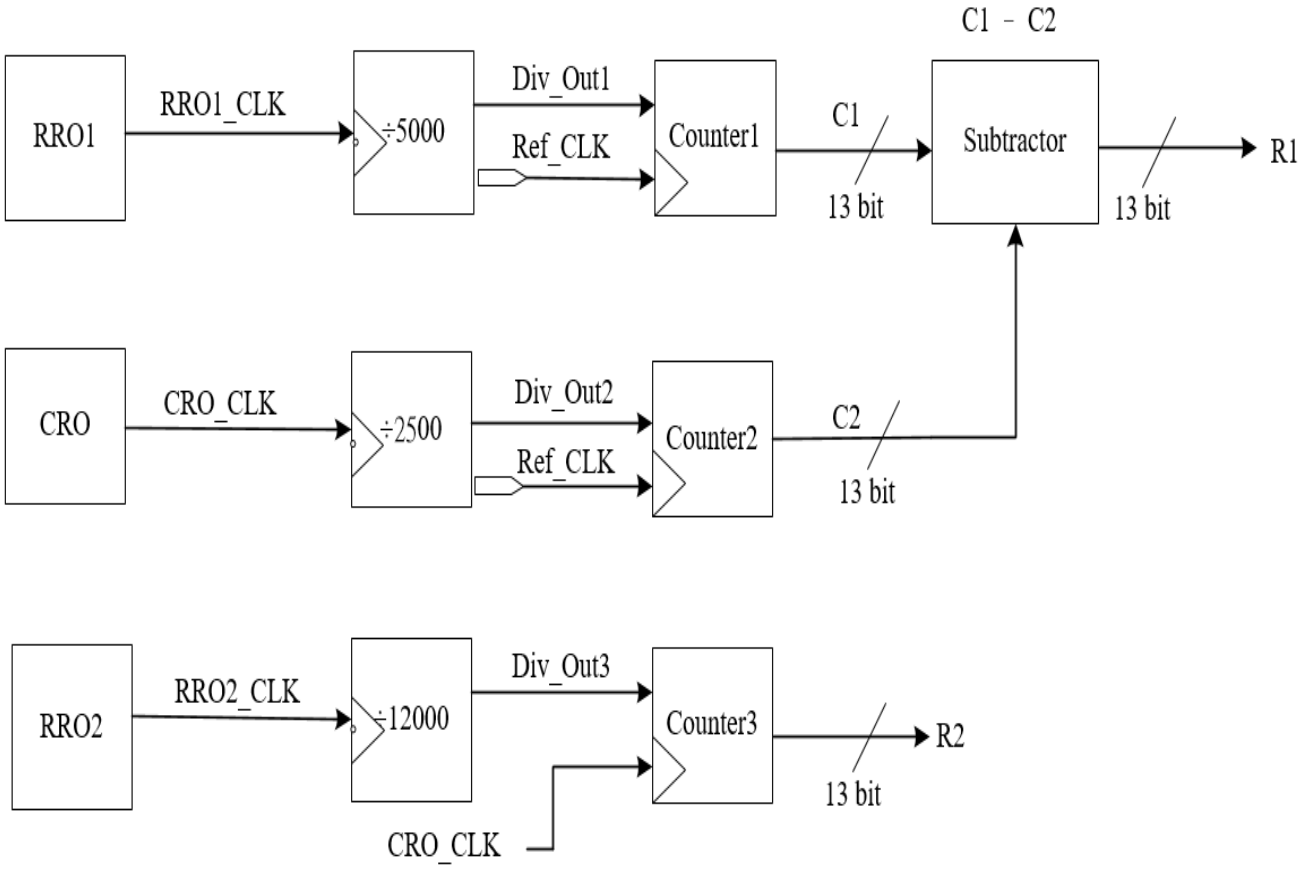


Fig. 4.1 Cost-down version of proposed delay ratio estimator (DRE)

Fig. 4.1 shows the cost-down version of the proposed delay ratio estimator which

use the high voltage sensitivity 2-input NAND gates with MOS capacitors to compose the RRO1 and let the RRO1 and CRO having large voltage sensitivity difference. In the simulation results, the output R2 uses the negative temperature coefficient delay cells to let the CRO and RRO2 have different temperature coefficient and use the characteristics of the division to eliminate the influence of voltage variations. Addition, the Ref_CLK in the cost-down version is 10MHz.

The delay ratio estimator output value, R1 can be expressed in (4.1), where the P_{RRO1} is the period of the ring oscillator 1 (RRO1), P_{CRO} is the period of the compared ring oscillator (CRO), P_{Ref_CLK} is the period of the reference clock.

$$\mathrm{R1} = \frac{(\ (P_{RRO1} * \ 5000) - (P_{CRO} * \ 2500)\ )}{P_{Ref\_CLK}} \tag{4.1}$$

The P_{RRO1} can be expressed in (4.2), where the N_1 is the stages number of high voltage sensitivity 2-input NAND gates with MOS capacitors (N_1 = 17 in this design), D_{CDC0} is the propagation delay of a high voltage sensitivity 2-input NAND gate with a MOS capacitors at (1.0V, 50℃). V_{b1} is the voltage sensitivity of a 2-input NAND gate with a MOS capacitors and T_{r1} is the temperature sensitivity of a high voltage sensitivity 2-input NAND gate with a MOS capacitors, and $T_{current}$ is the current temperature value, $V_{current}$ is the current supply voltage.

$$P_{RRO1} = N_1 * \{D_{CDC0} + [(V_{current} - 1.0\mathrm{V}) * V_{b1}] + [(T_{current} - 50℃) * T_{r1}]\} \tag{4.2}$$

The P_{CRO} can be expressed in (4.3), where the N_2 is the stage number of 2-input NAND gates (N_2= 129 in this design), D_{RDC0} is the propagation delay of a 2-input NAND gate at (1.0V,50℃). V_{b2} is the voltage sensitivity of a 2-input NAND gate and T_{r2} is the temperature sensitivity of a 2-input NAND gate, and $T_{current}$ is current

temperature value, $V_{current}$ is the current supply voltage.

$$P_{CRO} = N_2 * \{D_{RDC0} + [(V_{current} - 1.0\text{V}) * V_{b2}] + [(T_{current} - 50\text{°C}) * T_{r2}]\} \quad (4.3)$$

Where $N_1 = 17$ and $N_2 = 129$ and the Eq. (4.1) can be derived as (4.4) by using Eq. (4.2) and Eq. (4.3).

$$\text{R1} = \frac{\{(85000D_{CDC0} - 322500D_{RDC0}) + V_a + T_b\}}{P_{Ref\_CLK}} \quad (4.4)$$

Where V_a is $(V_{current} - 1.0\text{V}) * (85000V_{b1} - 322500V_{b2})$, T_b is $(T_{current} - 50\text{°C}) * (85000T_{r1} - 322500T_{r2})$.

Where $V_{b1} \approx 2V_{b2}$, $T_{r1} \approx 4T_{r2}$ which is derived from Table 2.1.

Observed from the Eq. (4.4), the temperature coefficients T_b of R1 can become smaller. The R1 value will have low-temperature sensitivity but will be sensitive to the voltage variations which can use to detect supply voltage under temperature variations.

The delay ratio estimator output R2, can be expressed in (4.5) where $Period_{RRO2}$ is the period of RRO2, $P^{\alpha 2}$ is the process coefficient of RRO2, $V^{\beta 2}$ is the voltage coefficient of RRO2, $T^{\gamma 2}$ is the temperature coefficient, and $Period_{CRO}$ is the period of CRO, $P^{\alpha 1}$, $V^{\beta 1}$, $T^{\gamma 1}$ represent process, temperature, voltage coefficient of the CRO, respectively.

$$\text{R2} = \frac{Period_{RRO2} * (P^{\alpha 2} * V^{\beta 2} * T^{\gamma 2}) * 12000}{Period_{CRO} * (P^{\alpha 1} * V^{\beta 1} * T^{\gamma 1})} \quad (4.5)$$

The process variation of R2 can be eliminated by the calibration flow, therefore, the $P^{\alpha 1}$ and $P^{\alpha 2}$ can be ignored. the (4.5) can be derived into (4.6).

$$\text{R2} = \frac{Period_{RRO2} * 12000}{Period_{CRO}} * \left(\frac{T^{r2}}{T^{r1}}\right) * \left(\frac{V^{\beta 2}}{V^{\beta 1}}\right) \quad (4.6)$$

In Eq. (4.6), the $V^{\beta 2} \approx 1.001V^{\beta 1}$ (at TT 20℃), $V^{\beta 2} \approx 1.005V^{\beta 1}$ (at TT 80℃) and $T^{r2} \approx 0.971T^{r1}$ (at TT 0.9V), $T^{r2} \approx 0.986T^{r1}$ (at TT 1.1V) which is observed from simulation result, the voltage coefficient of R2, $\left(\frac{V^{\beta 2}}{V^{\beta 1}}\right)$ is close to 1 (constant). The R2 will have the low-voltage sensitivity due to the characteristics of division will offset the voltage sensitivity of two ring oscillator.

Fig. 4.2 shows the architectures of the three ring oscillator (CRO, RRO1, RRO2), compared to the tape-out version, the cost down version doesn't need to trim the stage of thyristors used for compensation. In the tape-out version, the RRO1 have 16 stage of thyristors and each stage have 4 of thyristors which are used to trim and let the voltage sensor (R1) will not be suffered from temperature variations. In the cost-down version, the proposed voltage sensor will not adopt the method of trimming, instead, compensate for voltage sensor through the temperature information calculated by R2 and let the voltage sensor will not be suffered from the temperature variations.

In the tape-out version, the RRO2 have 16 stages of thyristors, each stage has 8 of thyristors. Due to the consideration of high conversion rate, more thyristors must be used which can let the R2 change drastically with temperature variation in a short period measurement. Subsequently, the RRO2 need to trim the appropriate numbers of thyristors under different process corner to let the R2 have sufficient resolution and high conversion rate.

In the cost-down version, due to the conversion rate is lower and there has more time to achieve the sufficient resolution of the proposed temperature sensor. Therefore, the number of thyristors can be reduced, too. In the cost-down version of RRO2, the numbers of thyristors are 8 and the RRO2 doesn't need to be trimmed under different process corners.

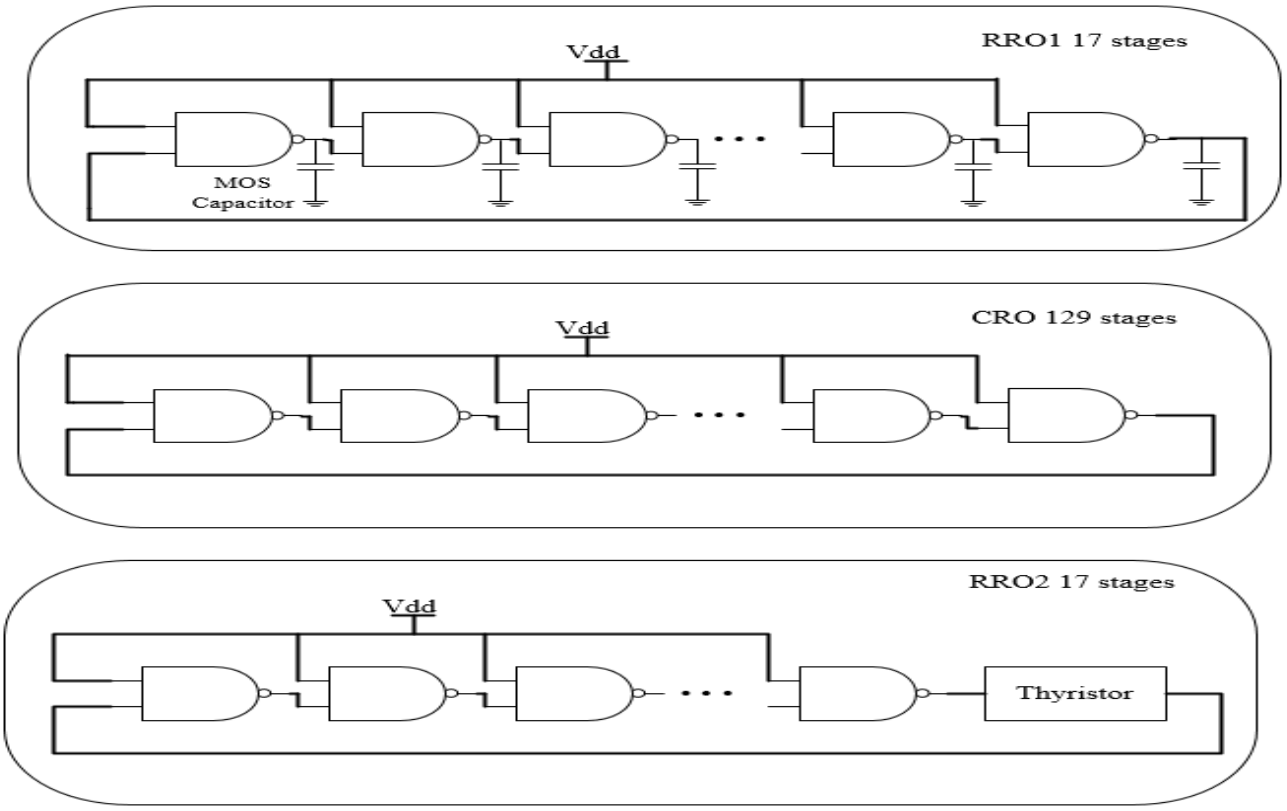


Fig. 4.2 Cost-down version of three ring oscillators

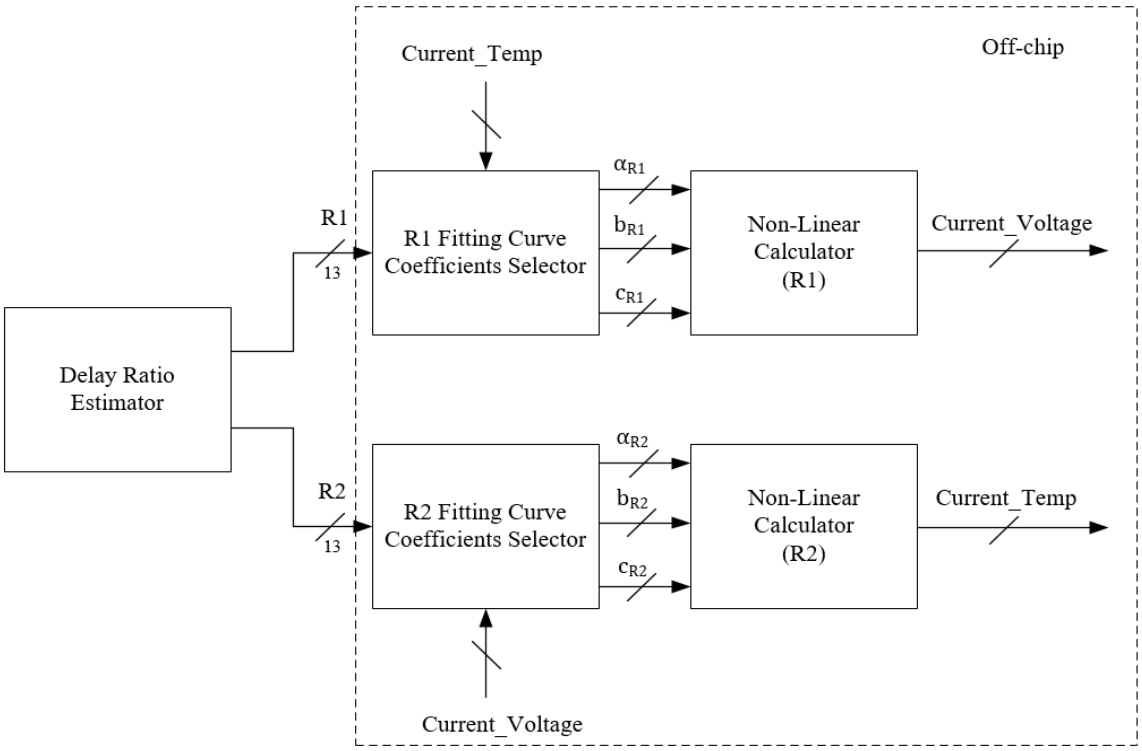


Fig. 4.3 Cost-down version of proposed voltage and temperature sensor

Fig. 4.3 shows the architecture of cost down version voltage and temperature sensor, the delay ratio estimator will calculate the R1 which is used to sense the current voltage and R2 is used to sense the current voltage.

At the calibration mode, the proposed voltage and temperature sensor need to measure R1 and R2 at (20℃,0.9V), (50℃,0.9V), (80℃,0.9V), (20℃,1.0V), (50℃,1.0V), (80 ℃ ,1.0V), (20 ℃ ,1.1V), (50 ℃ ,1.1V) and (80 ℃ ,1.1V). After calibration, the coefficients of fitting curves which is used to calculate the current voltage and temperature will be determined.

In the cost-down version after calibration, the R1 will be used with the fitting curve method to calculate the current supply voltage, as shown in Eq. (4.7). Then the R2 will use the fitting curve method to calculate the current temperature Eq. (4.8). Subsequently, the temperature information will feedback to the voltage sensor and the R1 will choose the appropriate coefficients of the fitting curve according to the current temperature. Therefore, the voltage sensor can calculate the current supply voltage under temperature variations. The voltage information will feedback to the temperature sensor and the R2 will choose the appropriate coefficients of the fitting curve according to the current voltage. Therefore, the temperature sensor can calculate current temperature under voltage variations.

$$\text{Current\_Voltage} = a_{R1}(Tj) * R1(Vi,Tj)^2 + b_{R1}(Tj) * R1(Vi,Tj) + c_{R1}(Tj) \quad (4.7)$$

$$\text{Current\_Temp} = a_{R2}(Vi) * R2(Vi,Tj)^2 + b_{R2}(Vi) * R2(Vi,Tj) + c_{R2}(Vi) \quad (4.8)$$

4.3 Algorithm of Calculating the Coefficients of Fitting Curves

As shown in Fig. 4.4 in the off-chip process, the proposed temperature sensor will interpolate 198 fitting curves from 0.9V to 1.1V and the temperature sensor will choose the fitting curve according to the current supply voltage and calculate the current temperature.

After calibration, the proposed temperature sensor only determines the coefficients of fitting curves at (0.9V, 1.0V, 1.1V). However, the proposed temperature sensor will not get each coefficient of fitting curves by measuring at the different voltage which will spend lots of time on calibration. Therefore, the proposed temperature sensor will use known coefficients of the fitting curve at (0.9V, 1.0V, 1.1V) to interpolate and get the coefficients of the fitting curve at different voltages.

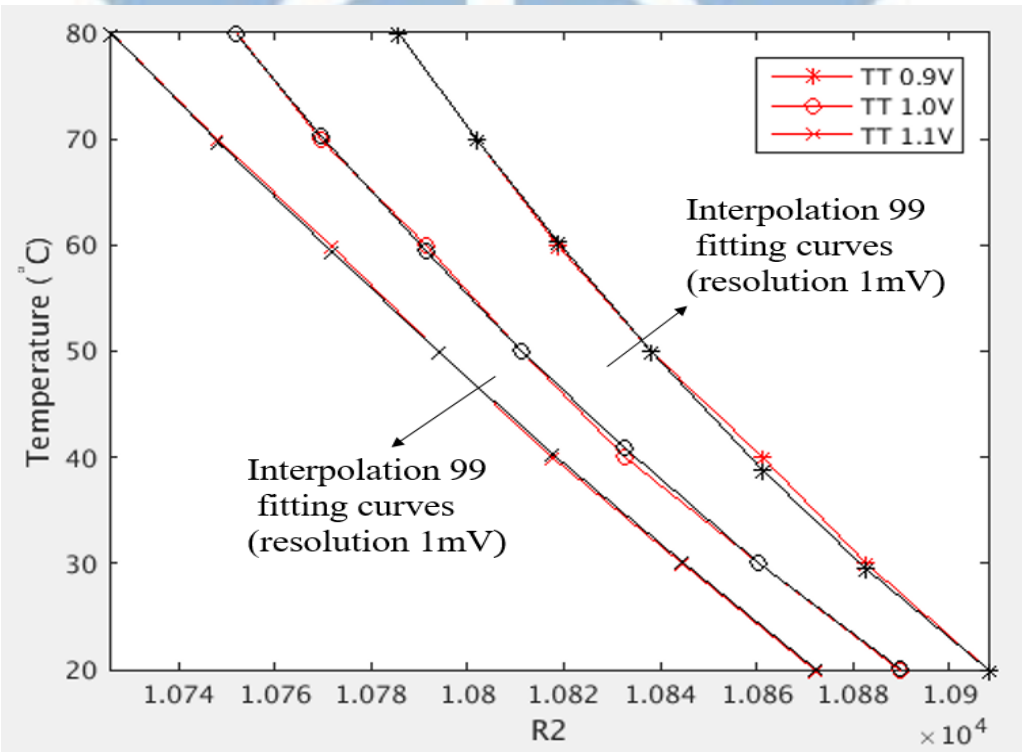


Fig. 4.4 Fitting curve interpolation of R2

$$d_{a1\_R2} = \{a_{R2}(1.0V) - a_{R2}(0.9V)\}/99 \quad (4.9)$$

$$d_{b1\_R2} = \{b_{R2}(1.0V) - b_{R2}(0.9V)\}/99 \quad (4.10)$$

$$d_{c1\_R2} = \{c_{R2}(1.0V) - c_{R2}(0.9V)\}/99 \quad (4.11)$$

$$d_{a2\_R2} = \{a_{R2}(1.1V) - a_{R2}(1.0V)\}/99 \quad (4.12)$$

$$d_{b2\_R2} = \{b_{R2}(1.1V) - b_{R2}(1.0V)\}/99 \quad (4.13)$$

$$d_{c2\_R2} = \{c_{R2}(1.1V) - c_{R2}(1.0V)\}/99 \quad (4.14)$$

If Current_Voltage is 0.9V~1.0V

$$a_{R2}(Vi) = a_{R2}(0.9V) + (i * d_{a1\_R2}) \quad (4.15)$$

$$b_{R2}(Vi) = c_{R2}(0.9V) + (i * d_{b1\_R2}) \quad (4.16)$$

$$c_{R2}(Vi) = c_{R2}(0.9V) + (i * d_{c1\_R2}) \quad (4.17)$$

Where i = 1~99, and V1 = 0.901V, V2 = 0.902V….. V99 = 0.999V

If Current_Voltage is 1.0V~1.1V

$$a_{R2}(Vi) = a_{R2}(1.0V) + (i * d_{a2\_R2}) \quad (4.18)$$

$$b_{R2}(Vi) = c_{R2}(1.0V) + (i * d_{b2\_R2}) \quad (4.19)$$

$$c_{R2}(Vi) = c_{R2}(1.0V) + (i * d_{c2\_R2}) \quad (4.20)$$

Where i = 1~99, and V1 = 1.001V, V2 = 1.002V….. V99 = 1.099V

Where $a_{R2}(0.9V)$, $b_{R2}(0.9V)$ and $c_{R2}(0.9V)$ are the coefficients of the second order R2 fitting curve at 0.9V, $a_{R2}(1.0V)$, $b_{R2}(1.0V)$ and $c_{R2}(1.0V)$ are the coefficients of the second order R2 fitting curve at 1.0V, $a_{R2}(1.1V)$, $b_{R2}(1.1V)$ and $c_{R2}(1.1V)$ are the coefficients of the second order R2 fitting curve at 1.1V.

Where $a_{R2}(Vi)$, $b_{R2}(Vi)$ and $c_{R2}(Vi)$ are the coefficients of the second order R2 fitting curve at voltage Vi,.

Observed from the simulation results, the coefficients of fitting curves at (0.9V, 1.0V, 1.1V) is decremented as the voltage rises. Therefore, the proposed temperature sensor will use the arithmetic progression to approximate the coefficients at others voltage according to the known coefficients at (0.9V, 1.0V, 1.1V). As shown in Eq. (4.9) to Eq. (4.14), the proposed temperature sensor will calculate the difference of the arithmetic according to the known coefficients at (0.9V, 1.0V, 1.1V) which is calculated at calibration flow. Subsequently, the proposed slope and intercept selector will calculate the coefficients of fitting curves at different voltage as shown in Eq. (4.15) to Eq. (4.20) and choose the appropriate coefficients of fitting curves according to the current supply voltage.

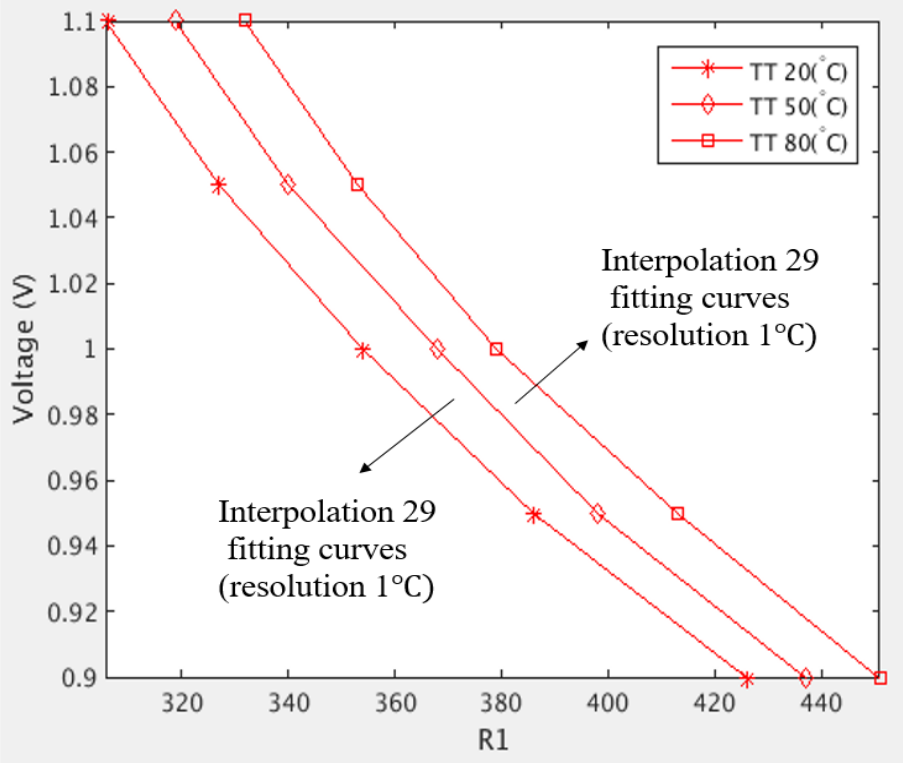


Fig. 4.5 Fitting curve interpolation of R1

As shown in Fig. 4.5, proposed voltage sensor will interpolate 58 curve fitting curves from 20 ℃ to 80 ℃ and the voltage sensor will choose the fitting curve according to the current temperature and calculate the current voltage.

After calibration, the proposed voltage sensor only determines the coefficients of the fitting curves at (20℃, 50℃, 80℃). However, the proposed voltage sensor can't get each coefficient of fitting curves by measuring at the different temperature which will spend lots time on calibration. Therefore, the proposed voltage sensor will use known coefficients of the fitting curve at (20℃, 50℃, 80℃) to interpolate and get the coefficients of the fitting curve at the different temperature.

$$d_{a1\_R1} = \{a_{R1}(50℃) - a_{R1}(20℃)\}/29 \quad (4.21)$$

$$d_{b1\_R1} = \{b_{R1}(50℃) - b_{R1}(20℃)\}/29 \quad (4.22)$$

$$d_{c1\_R1} = \{c_{R1}(50℃) - c_{R1}(20℃)\}/29 \quad (4.23)$$

$$d_{a2\_R1} = \{a_{R1}(80℃) - a_{R1}(50℃)\}/29 \quad (4.24)$$

$$d_{b2\_R1} = \{b_{R1}(80℃) - b_{R1}(50℃)\}/29 \quad (4.25)$$

$$d_{c2\_R1} = \{c_{R1}(80℃) - c_{R1}(50℃)\}/29 \quad (4.26)$$

If Current_Temp is 20℃~50℃

$$a_{R1}(Tj) = a_{R1}(20℃) + (j * d_{a1\_R1}) \quad (4.27)$$

$$b_{R1}(Tj) = c_{R1}(20℃) + (j * d_{b1\_R1}) \quad (4.28)$$

$$c_{R1}(Tj) = c_{R1}(20℃) + (j * d_{c1\_R1}) \quad (4.29)$$

Where j = 1~29, and T1 = 21℃, V2 = 22℃….. V29 = 49℃

If Current_Temp is 50℃~80℃

$$a_{R1}(Tj) = a_{R1}(50℃) + (j * d_{a2\_R1}) \quad (4.30)$$

$$b_{R1}(Tj) = c_{R1}(50℃) + (j * d_{b2\_R1}) \quad (4.31)$$

$$c_{R1}(Tj) = c_{R1}(50℃) + (j * d_{c2\_R1}) \quad (4.32)$$

Where j = 1~29, and T1 = 51℃, V2 = 52℃….. V29 = 79℃

Where $a_{R1}(20℃)$, $b_{R1}(20℃)$ and $c_{R1}(20℃)$ are the coefficients of the second order R1 fitting curve at 20℃, $a_{R1}(50℃)$, $b_{R1}(50℃)$ and $c_{R1}(50℃)$ are the coefficients of the second order R1 fitting curve at 50℃, $a_{R1}(80℃)$, $b_{R1}(80℃)$ and $c_{R1}(80℃)$ are

the coefficients of the second order R1 fitting curve at 80℃.

Where $a_{R1}(Tj)$,$b_{R1}(Tj)$ and $c_{R1}(Tj)$ are the coefficients of the second order R1 fitting curve at temperature Tj.

Observed from the simulation results, the coefficients of fitting curves at (20℃, 50℃, 80℃) is decremented as the temperature rises. Therefore, the proposed voltage sensor will use the arithmetic progression to approximate the coefficients at others temperature according to the known coefficients at (20℃, 50℃, 80℃). As shown in Eq. (4.21) to Eq. (4.26), the proposed voltage sensor will calculate the difference of the arithmetic progression according to the known coefficients at (20℃, 50℃, 80℃) which is calculated at calibration flow. Subsequently, the proposed slope and intercept selector will calculate the coefficients of fitting curves at different temperature as shown in Eq. (4.27) to Eq. (4.32) and choose the appropriate coefficients of fitting curves according to the current temperature.

4.4 Operating Flow of the Proposed Temperature Sensor

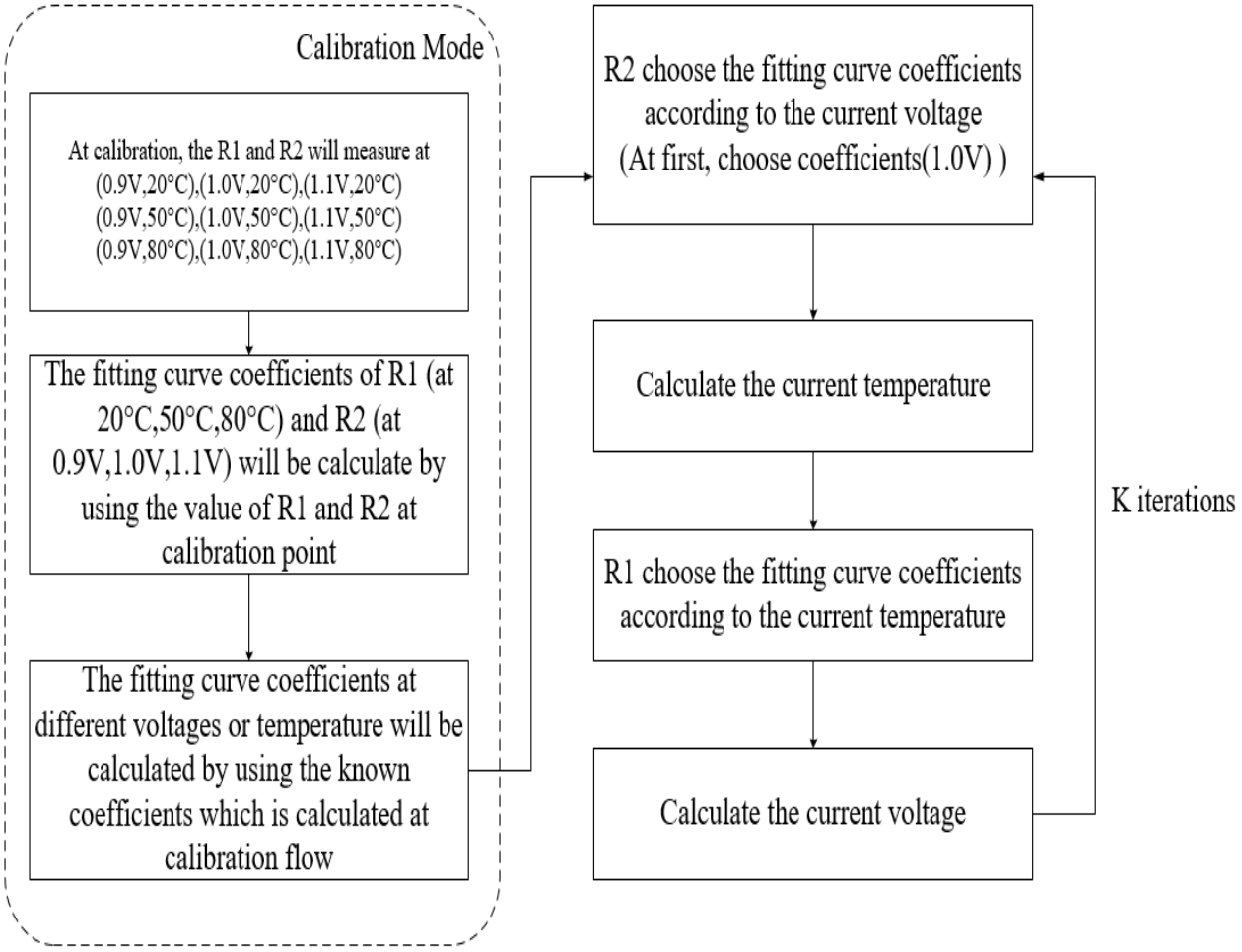


Fig. 4.6 Operating Flow of the proposed temperature sensor

(Cost-down version)

As shown in Fig. 4.6, the proposed temperature and voltage sensor need to be calibrated and get the values of R1 and R2 at calibration points. After calibration, the proposed temperature sensor will calculate the coefficients of the fitting curve at (0.9V, 1.0V, 1.1V) and the difference of the arithmetic progression according to the known coefficients by using the known coefficients at (0.9V, 1.0V, 1.1V). The proposed voltage sensor will calculate the coefficients of the fitting curve at (20℃, 50℃, 80℃) and

difference of the arithmetic progression according to the known coefficients by using the known coefficients at (20℃, 50℃, 80℃).

After calibration and coefficients calculation, the proposed temperature sensor will choose the coefficients of the fitting curve at 1.0V and calculate the current temperature in the normal mode. Although at this stage, the proposed temperature doesn't know the value of current supply voltage. However, due to the low-voltage sensitivity of the proposed temperature sensor, the 10% voltage variations will not make the error of the temperature sensor exceed 20℃. Subsequently, the temperature information will pass to the voltage sensor.

Due to the low-temperature sensitivity of the proposed voltage sensor, 20℃ temperature error does not cause the voltage error of the voltage sensor to exceed 15mV. Therefore, the propose voltage sensor can calculate the current supply voltage according to the temperature information. Subsequently, the voltage information will pass to the temperature sensor.

After getting the voltage information, the proposed temperature sensor will choose the appropriate coefficients of the fitting curve and calculate the current temperature again. After k iteration (k = 2 in this design), the error of voltage and temperature will converge and the proposed temperature sensor can work under voltage variation, the proposed voltage sensor can works under temperature variations.

4.5 Experimental Results

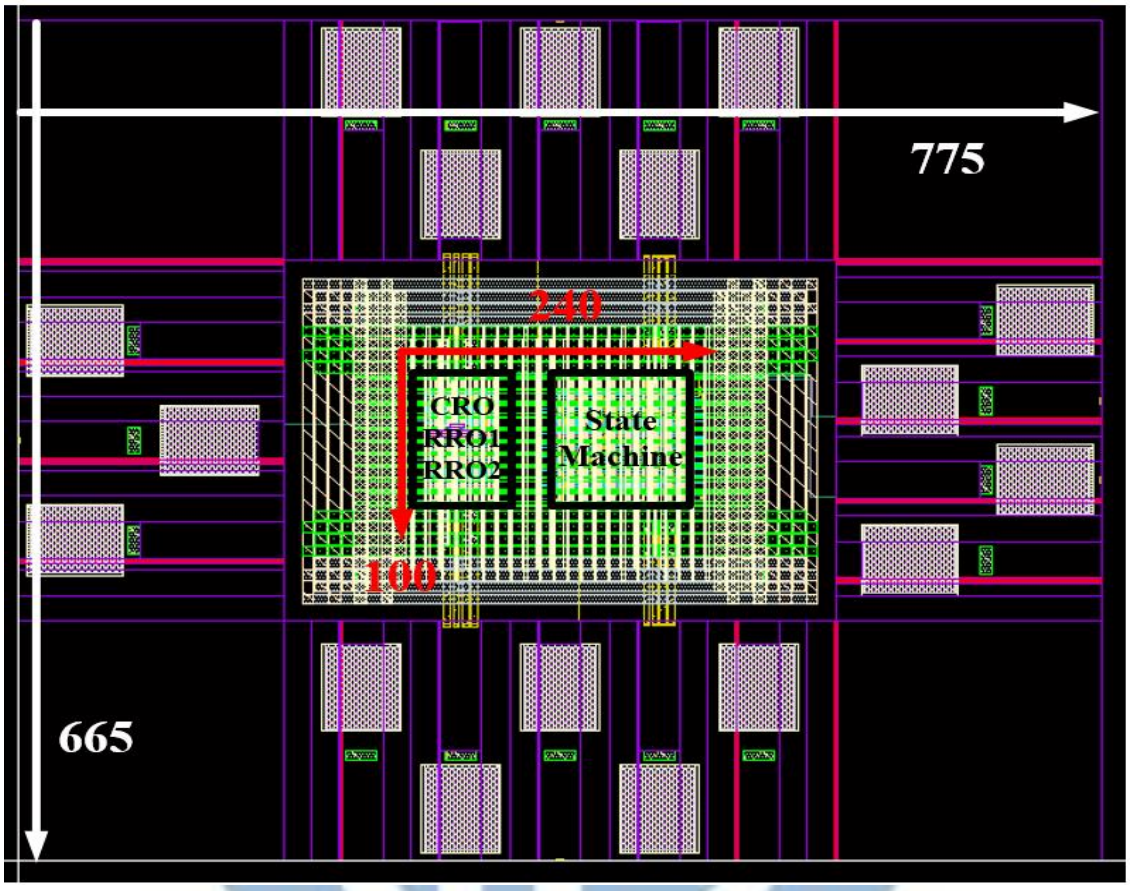
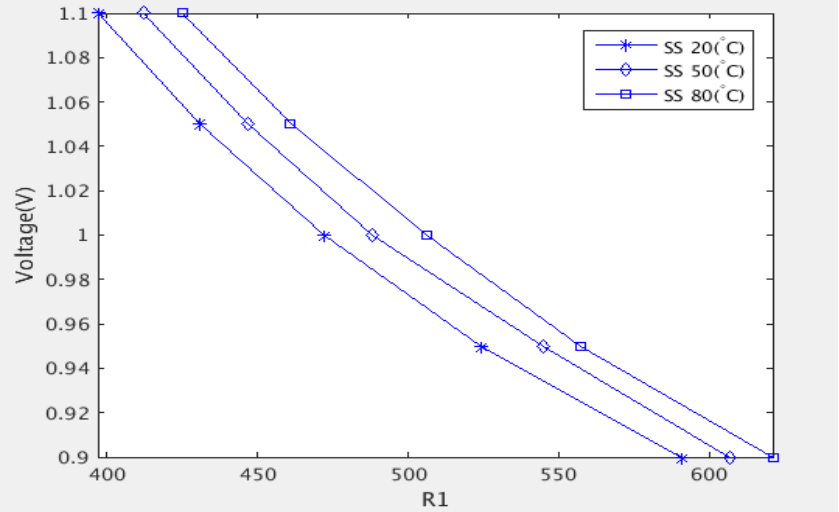
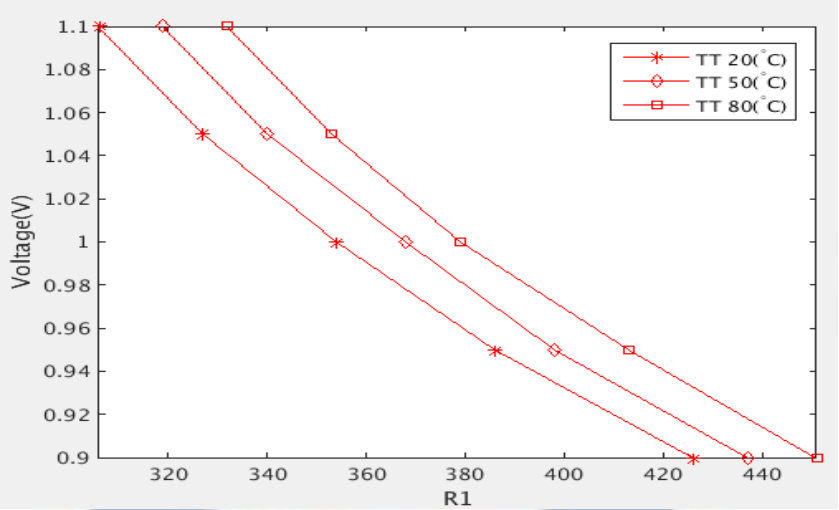


Fig. 4.7 Layout of the proposed temperature (cost-down version)

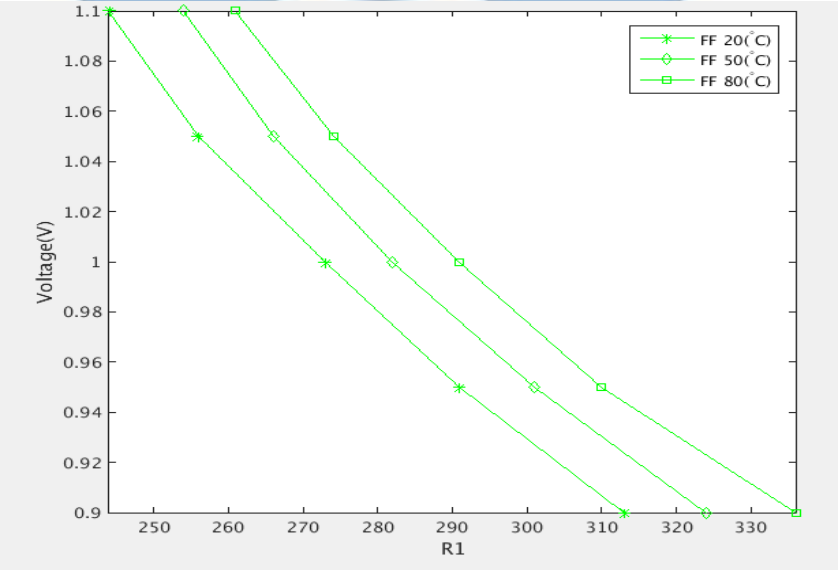
The layout of the proposed temperature is shown in Fig. 4.7. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The core size of the chip is $240\mu m * 100\mu m$. The chip size including I/O PADs is $775\mu m * 665\mu m$.



(a) R1 post-layout simulation at SS corner

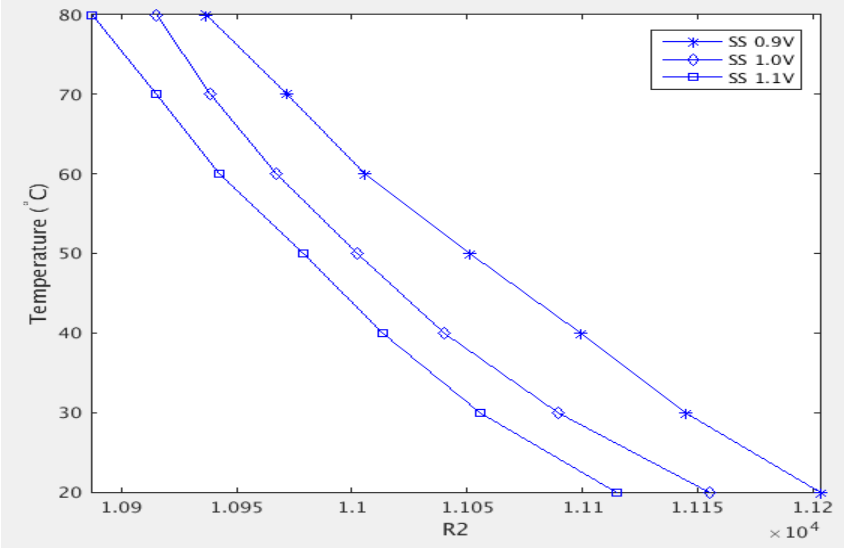


(b) R1 post-layout simulation at TT corner

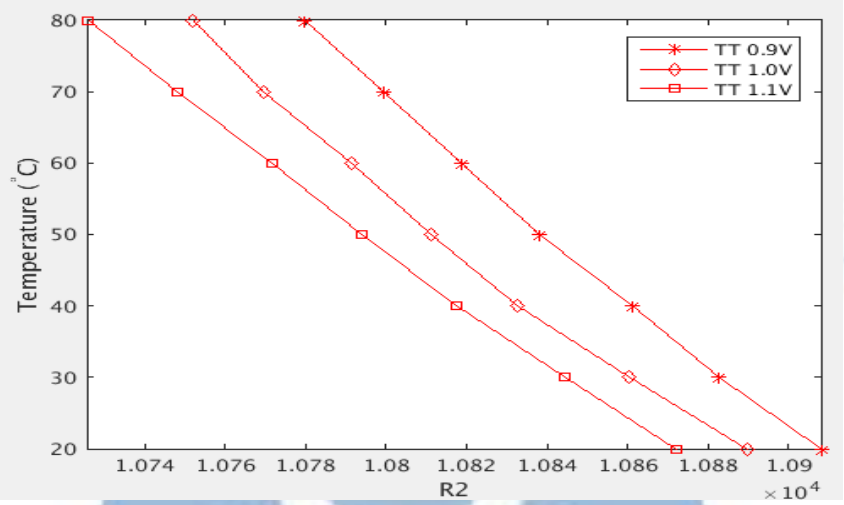


(c) R1 post-layout simulation at FF corner

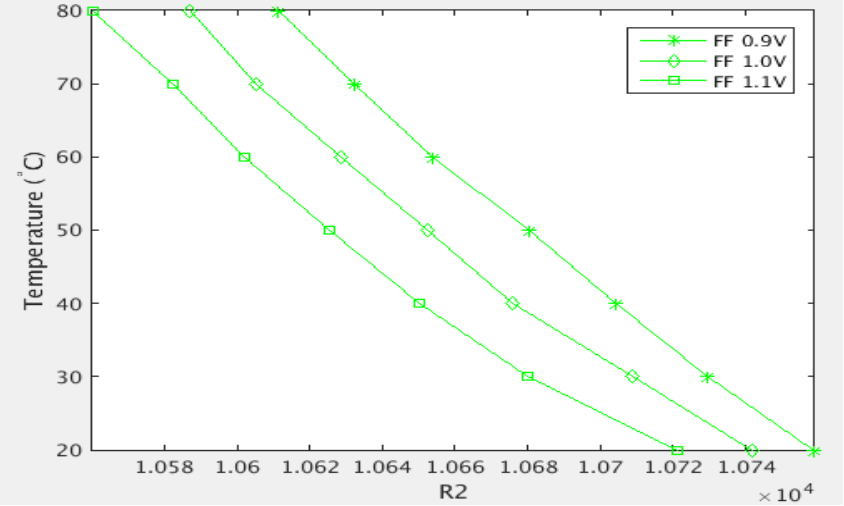
Fig. 4.8 R1 post-layout simulation under different PVT variations



(a) R2 post-layout simulation at SS corner



(b) R2 post-layout simulation at TT corner



(c) R2 post-layout simulation at FF corner

Fig. 4.9 R2 post-layout simulation under different PVT variations

Fig. 4.8 shows the post-layout simulation of R1 value under different PVT conditions. The RRO1 use the high voltage sensitivity 2-input NAND gates with MOS capacitors to let the RRO1 and CRO having large voltage sensitivity difference. Also, the characteristics of the subtraction will offset some of the temperature sensitivity of R1. As a result, the R1 value is sensitivity to the voltage variations and have low-temperature sensitivity. Subsequently, the R1 will use the fitting curve method to calculate the current supply voltage as shown in Eq. (4.1) and choose the appropriate coefficients of the fitting curve according to the temperature information which is calculated by R2 value. Due to the low-temperature sensitivity of R1, the voltage information calculated by R1 can tolerate a range of temperature errors which is calculated by R2.

Fig. 4.9 shows the post-layout simulation of R2 value under different PVT conditions, Due to the RRO2 use the high negative temperature coefficient delay cells to let the RRO2 and CRO having large temperature sensitivity difference and the characteristics of the division will offset some of the voltage sensitivity of R2. As a result, the R2 value is sensitivity to the temperature variations but have low-voltage sensitivity. Subsequently, the R2 will use the fitting curve method to calculate the current temperature as shown in Eq. (4.2) and choose the appropriate coefficients of the fitting curve according to the voltage information which is calculated by R1 value. Due to the low-voltage sensitivity of R2, the temperature information calculated by R2 can tolerate a range of voltage errors which is calculated by R1.

As shown in Fig. 4.6, the PTAT (R2) will not have any voltage information at 1st iteration. Fig. 4.10 shows the error of PTAT (R2) under 10% voltage variations and different corner, the maximum error of PTAT at 1st iteration is 15.2℃ ~ -14.9℃. Due to the low-temperature sensitivity of R1, the temperature error from the PTAT at 1st iteration is tolerable. Subsequently, the voltage sensor will choose the coefficients of

the fitting curve according to the temperature information which is calculated by R2, even the temperature error at 1st may exceed 15 degrees, it will not cause serious impact on the proposed voltage sensor.

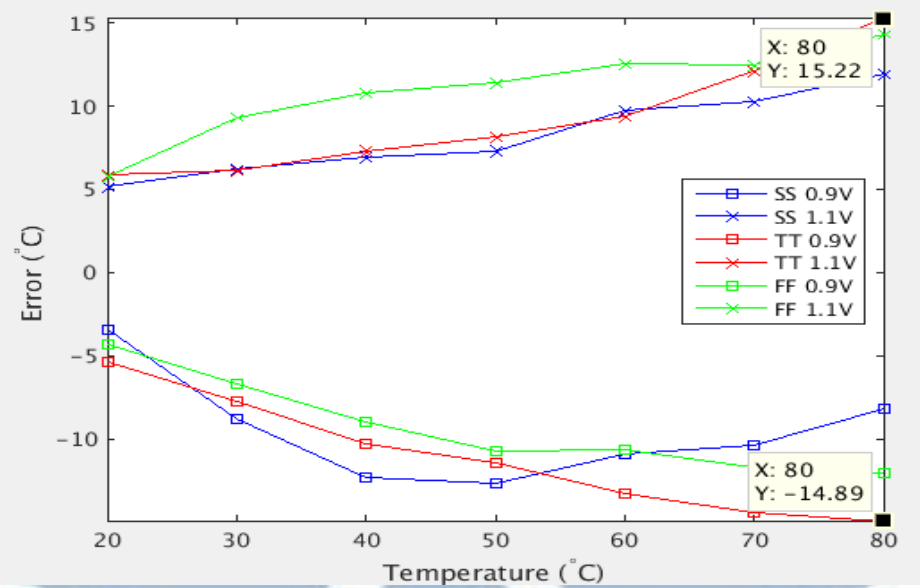
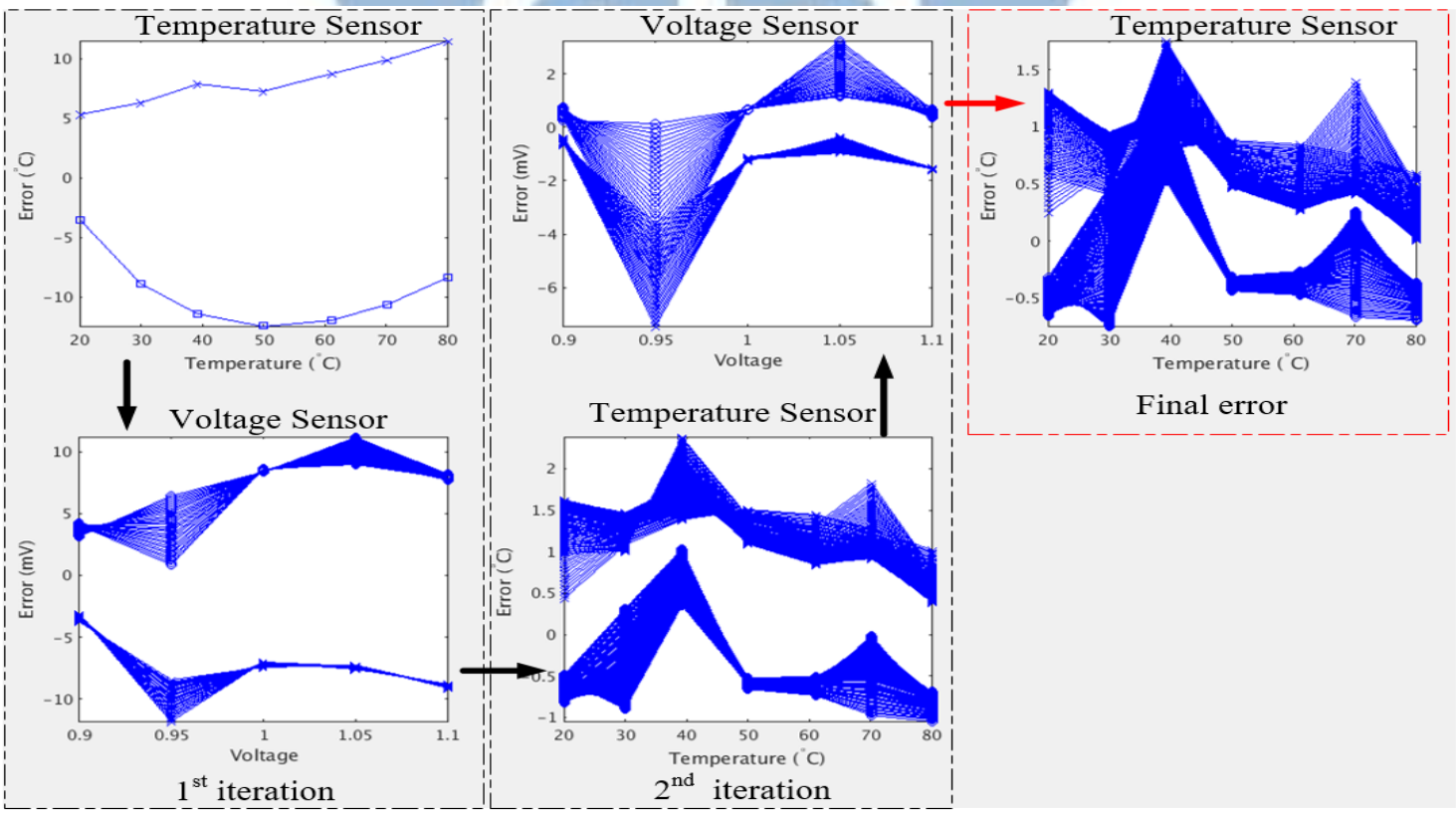
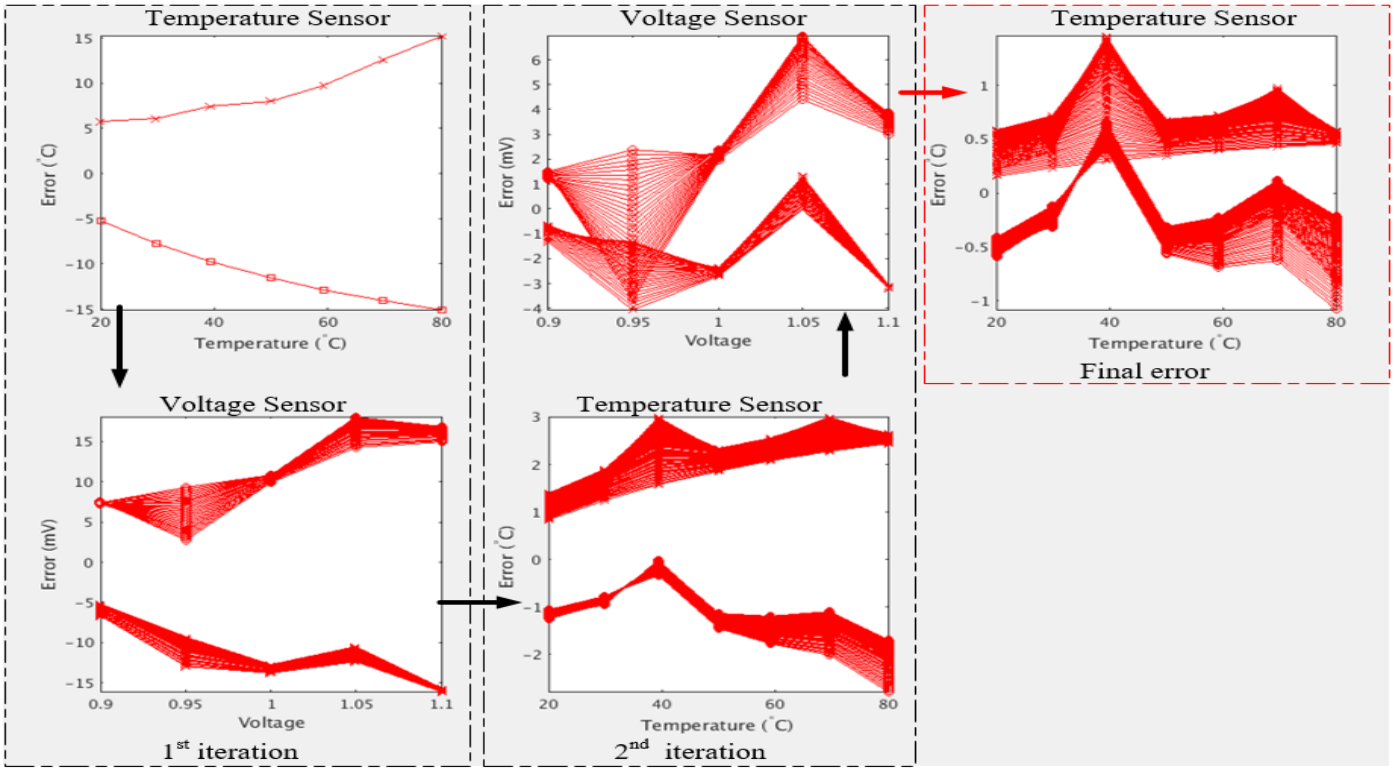


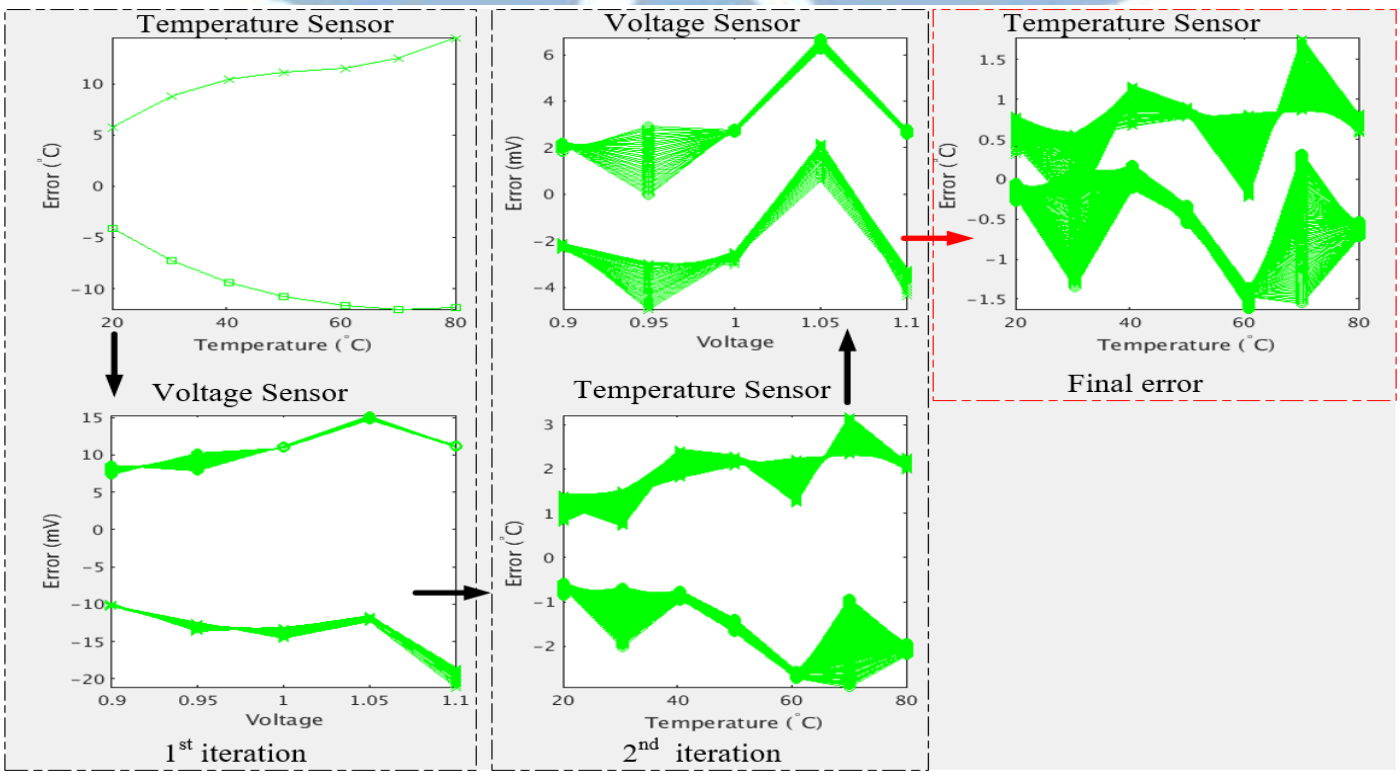
Fig. 4.10 Proposed temperature sensor maximum error under 10% voltage variations (without voltage sensor)



(a) Error of the proposed voltage and temperature sensor at different iteration (SS)



(b) Error of the proposed voltage and temperature sensor at different iteration (TT)



(c) Error of the proposed voltage and temperature sensor at different iteration (FF)

Fig. 4.11 Error of the proposed voltage and temperature sensor at different iteration and process corner

Fig. 4.11 shows the error of the proposed voltage and temperature sensor at different iteration and process corner. At the 1st iteration, the proposed temperature sensor will choose the coefficients of the fitting curve at 1.0V. Even if the proposed temperature sensor will not have correct supply voltage information at 1st iteration, the maximum error of temperature sensor will not exceed 20 degrees under 10% voltage variation. At 1st iteration, the proposed voltage sensor will get the temperature information from the temperature sensor and calculate the current supply voltage. Even if the proposed temperature sensor will have 15 degrees error, the error of voltage sensor at 1st iteration will not exceed 20mV, which can provide a voltage information to the proposed temperature sensor at 2nd iteration.

At the 2nd iteration, the proposed temperature sensor will get a voltage information and calculate the current temperature under voltage variation. As shown in Fig. 4.11 the maximum error of the proposed temperature sensor will not exceed 4 degrees. Subsequently, the voltage sensor will get the temperature information and calculate the current supply voltage under temperature information. As shown in Fig. 4.11 the maximum error of the proposed voltage sensor will not exceed 8mV which can provide an accurate voltage information to the temperature sensor.

As shown in Fig. 4.11 the maximum error of temperature sensor after two iteration will convergence to within ±2℃. The final error of proposed the temperature sensor is 1.75℃~ -0.71℃ at SS corner, 1.42℃ ~ -1.08℃ at TT corner, 1.72 ~ -1.57 at FF corner.

The maximum error of proposed voltage sensor is 3.2mV ~ -7.3mV at SS corner, 6.8mV ~ -4.1mV at TT corner, 6.6mV ~ -4.8mV at FF corner.

Table 4.2 Performance comparisons of temperature sensor (cost-down version)

	[33] ASP-DAC'16	[35] TVLSI'12	[31] JSSC'15	[12] JSSC'16	[34] TBioCAS'17	[36] ISSCC'12	Proposed Work
Method	Digital	Digital	Analog	Analog	Analog	Analog	Digital
Technology(nm)	28	130	65	65	65	32	90
Voltage Insensitivity	No	No	Yes	Yes	Yes	Yes	Yes
Supply Regulator	No	No	No	No	No	Yes	No
Temp. Range(℃)	0~100	0~100	0~100	0~100	30~70	20~100	20~80
VDD Range(V)	Fixed 0.9V	Fixed 1.2V	0.6~1	0.85~1.05	0.2~0.4	1.4~1.8	0.9~1.1
Resolution(℃)	0.44	0.78	N/A	0.3	N/A	0.2	0.39
Conversion Rate (k sample/S)	5	5	20	45.5	N/A	2	2
Error (℃)	-4.3~4.3 (at 0.9V)	-4~4 (at 1.2V) -90~90 (1.08V~1.32V)	-2.4~1.5	-5~2.2	-5~8.1	-1.5~1.5	-1.58 ~ 1.75 (PVT)
Power (mW)	0.45	1.2	0.36	0.15	0.25	3.8	0.68 @(TT,1.0V,20℃)
Area(mm^2)	0.003738	0.12	0.648	0.0042	N/A	0.02	0.024
Energy for one conversion (μJ)	0.009	0.24	0.0018	0.0033	N/A	1.9	0.34
Supply Sensitivity(℃/mV)	N/A	N/A	0.0098	0.034	0.069	0.0075	0.0167
Master Curve	1_{st}	3_{rd}	1_{st}	2_{nd}	1_{st}	1_{st}	2_{nd}
Temp. Calibration Point	2pt	1pt	2pt	2pt	2pt	2pt	3pt

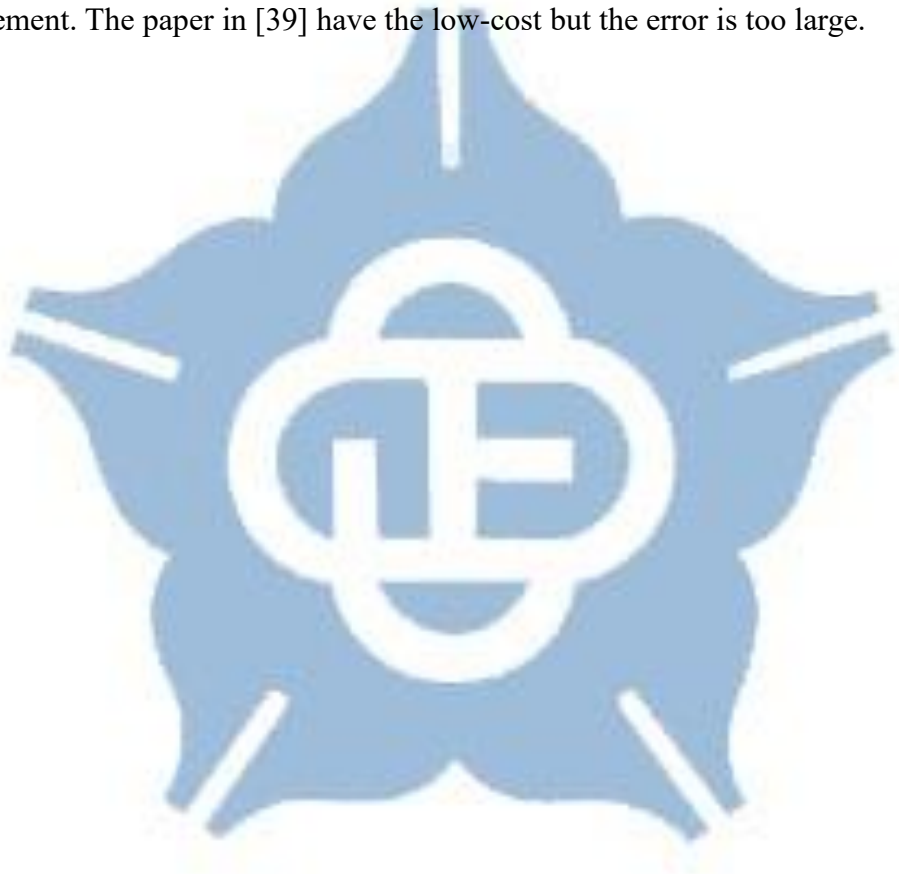
Table 4.3 Performance comparisons of voltage sensor

	[39] ECDSD'13	[37] VLSI-DAT'13	[27] SAS'16	[38] ITC'07	[40] TCAS-I'11	Proposed Work
Type	Voltage Sensor	IR-drop Monitor	Voltage Sensor	IR-drop Monitor	TDC	Voltage Sensor
Technology(nm)	65	90	90	90	45	90
Temp. Insensitivity	No	No	Yes	Yes	Yes	Yes
Temp. Range(℃)	N/A	N/A	0~75	-40~90	30-90	20~80
VDD Range(V)	0.9~1.2	0.8~1.0	0.9~1.1	0.9~1.1	0.9~1.1	0.9~1.1
Resolution(mV)	100	3.74	0.027	N/A	27.5	2.5
Error (mV)	85	4.81	57.2	N/A	N/A	7.3
Power(mW)	0.05	1.94@0.8V	1.00@1.0V	N/A	N/A	0.68@1.0V
Area(mm^2)	0.0027	0.184	0.063	0.027	N/A	0.024
Voltage Calibration Point	N/A	3pt	1pt	5pt	3pt	3pt

Table. 4.2 shows the performance comparisons of the recent temperature sensors. The temperature sensors in [33] and [35] cannot resist the voltage variations and have a large error under voltage variations. The temperature sensor in [36] which needs a voltage supply regulator at advanced CMOS process and have the high power consumption. The temperature sensor in [34] which uses the voltage difference to resist the voltage variation but the error is still too large under voltage variations. The other temperature sensor in [31] is full-custom design and needs extra read circuit like high-resolution off-chip ADC and needs to find the appropriate CTAT and PTAT which is matched. Subsequently, [12] is a full-custom design which is more complex and is not

portable to the different process, also need a high-order curve fitting method. In addition, most of these recent works cannot against the PVT variations which lowers the accuracy of the performance.

Table. 4.3 shows the performance comparisons of the recent IR-drop and supply voltage sensor. Although [37] shows the better error, however, it can't resist the temperature variations and can't operate at different environment. The paper in [38] needs 5 point voltage calibration which needs to spend lots time on the chip measurement. The paper in [39] have the low-cost but the error is too large.



Chapter 5 Conclusion and Future Works

5.1 Conclusion

In this thesis, the cell combination to build up the delay ratio estimator has been proposed which improved the shortcoming of the previous works [24]-[27]. The proposed work uses the high voltage sensitivity 2-input NAND gates and the 2-input NAND gates to build up the difference calculator which can detect the current supply voltage under temperature variations. Subsequently, the proposed temperature sensor uses the 2-input NAND gate with negative temperature coefficient delay cells and 2-input NAND gates to build up the delay ratio estimator which the output can be used as the proportional to absolute temperature (PTAT) circuit and have lower supply sensitivity than the common delay-line based PTAT circuits.

The proposed all-digital temperature sensor can tolerate process and voltage variations after three-point calibration without the requirement of a supply regulator and is suitable for battery operated system or IoT applications. The test chip of the temperature sensor was implemented in 90nm CMOS technology and occupies a die area of 0.82 mm^2. Subsequently, the worst case temperature error under PVT variations is $-4.3℃\sim4.3℃$ and the supply sensitivity can be achieved as $0.043℃/mV$.

5.2 Future Works

The resolution of the proposed voltage classifier will dominate the temperature error of the proposed temperature sensor which had been discussed in section 3.7. In order to lower the influence of voltage variations to the temperature sensor, the resolution of voltage classifier needs to be improved and reduces the classified error under temperature variations. The high voltage sensitivity can be achieved by adding

more MOS capacitors. However, as shown in Table 2.1, the temperature sensitivity will be also increased when more MOS capacitors are added. As a result, it needs to add more negative temperature coefficient delay cells to compensate the temperature coefficient and let the difference calculator will not be suffered from the temperature variations. However, the negative temperature coefficient delay cells in the proposed work consumes large power consumption and thus, it is not possible to add to many capacitors for compensation issue.

In order to lower the influence of voltage variations, the proposed temperature sensor uses low-voltage dependency PTAT which the linearity is worse but the supply sensitivity is better as compared to the common delay-line based PTAT circuits. The non-linearity of the proposed PTAT is caused by the division method and the negative temperature coefficient delay cells. Subsequently, the non-linearity results in high calibration cost in proposed temperature sensor.

As mentioned above, if the power consumption of the negative temperature coefficient delay cell can be decreased, the resolution of voltage classifier can be finer by adding more MOS capacitors and the influence of voltage variations to the proposed temperature sensor could be reduced. The calibration cost of the proposed temperature sensor is too high, if the linearity of the proposed PTAT can be improved, the calibration cost can be lower.

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