

國立中正大學

資訊工程研究所碩士論文

使用卷積碼並建構於可程式邏輯板之人
體通道傳輸收發器之設計與實現

**Design and Implementation of a Human
Body Channel Communication Transceiver
on FPGA Using Convolutional Codes.**

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Design and Implementation of a Human Body Channel Communication Transceiver on FPGA Using Convolutional Codes. (使用卷積碼並建構於可程式邏輯板之人體通道傳輸收發器之設計與實現)
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摘要

現今，隨著技術的進步，穿戴式個人娛樂裝置與個人醫療照護裝置愈來愈普及。對於醫療照護裝置，傳統上，病人必須到醫院或者是在家接著線材監測生理狀況，對於長時間觀察上十分不方便，因此有許多無線的隨身監控的醫療裝置被應用，一般來說，無線的穿戴式裝置以藍芽、wifi 來傳遞訊號，但是無線信號接收器有著高功耗、易受到干擾的問題。因此，由人體來當作信號傳輸媒介的技術被提出，因為信號在人體通道內具有較低的信號衰減且不容易受到周遭環境干擾的特性，人體通道傳輸能克服大部分使用無線射頻技術遇到的困難，另外，因為信號在離開人體耗能量會急速衰減，因此，相對於使用無線射頻技術，人體通道傳輸較不會有個人隱私會被竊聽盜取的問題。

本論文提出了一個寬帶式訊號使用卷積加密方法的人體通道傳輸器，並將其實作在可程式化邏輯版(FPGA)上，目的是為了快速驗證所提出架構的可行性。在傳收端，資料會由卷積加密器加密並且經過位元填充器和 NRZI 編碼後，藉由 SMA 線傳輸到人體上。在接收器端，一個過取樣的相位偵測器用來回復資料與時脈，由於透過卷積碼增加了資料的可靠性，在 140 公分的傳遞距離下使用 3.125 Mbps (6.25Mcps) 的資料傳輸速度收送資料，bit error rate (BER)表現可以達到傳輸接收 10^8 個位元資料沒有任何錯誤，因此，所提出的人體通道接收器適用於醫療穿戴性裝置與娛樂性裝置上。

關鍵字:人體通道傳輸、可程式邏輯板、超取樣資料回復、卷積碼

Abstract

Nowadays, portable entertainment and healthcare devices has developed rapidly because of the advance semiconductor fabrication process. For the chronic patients, the wireless healthcare devices brings a lot of convenience. In general, the wireless radio frequency (RF) communication has drawbacks of high power consumption and sensitive to interferences. Body channel communication (BCC) uses the human body as a transmission medium which is more stable and has less power consumption. However, the body antenna effects causes interferences in human body.

In this thesis, a wideband signal BCC transceiver using the convolutional encoding method is implemented on a field programmable gate array (FPGA) in order to verify the feasibility of the proposed design. In the transmitter side, the data will be encoded by convolutional encoding method and then modulated by a bit-stuffer and a NRZI modulator. The modulated data are transmitted directly to a human body through a SMA cable and an electrode. In the receiver side, the oversampling phase detection CDR will recover the clock and data. By means of using convolutional encoding method to increase the data reliability, there are no error bits occurred over 10^8 bits received at data rate 3.125 Mbps(6.25Mcps) in transmission distance under 140 cm. According to the experimental results, the proposed BCC transceiver is suitable for healthcare and entertainment devices.

Keywords: Body channel communication, FPGA, Oversampling CDR, Convolutional encoding method

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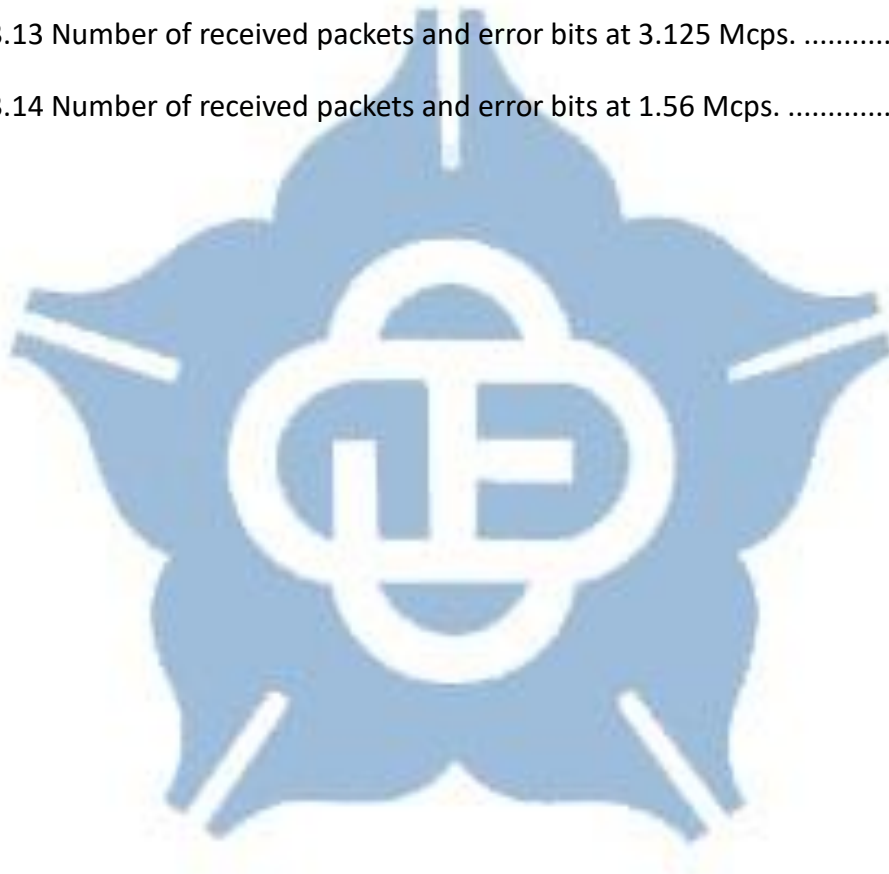
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Chapter 1 Introduction

1.1 Introduction of Body Channel Communication

As the wearable device are widely applied in healthcare and entertainment area, there are many researches focus on design of the body area network (BAN). The Wireless Body Area Network (WBAN) is a network composed of sensor nodes, in which the body sensor nodes connect a central hub and as well as with each other. For the healthcare area, the people who suffer from chronic diseases such as asthma, diabetes and heart attacks should carefully control their body state. The WBAN applications can alert the hospital, even before the patients have a heart attack. Furthermore, the on-body syringe can automatically inject insulin for the diabetes patients.

In the standard of WBANs, IEEE standard 802.15.6, it has three physical layers : Ultra-Wideband (UWB), Narrow-band (NB), and Body channel communication (BCC). Table 1.1 shows the summary of the operating frequency for the physical layers.

Table 1.1 frequency band and bandwidth of different physical layers specified in IEEE

802.15.6. [1]

Human-Body Communication	
Frequency	Bandwidth
16 MHz	4 MHz
27 MHz	4 MHz
Narrowband Communication	
Frequency	Bandwidth
402-405 MHz	300 kHz
420-450 MHz	300 kHz
863-870 MHz	400 kHz
902-928 MHz	500 kHz
956-956 MHz	400kHz
2360-2400 MHz	1 MHz
2400-2438.5 MHz	1 MHz
UWB Communication	
Frequency	Bandwidth
3.2-4.7 GHz	499 MHz
6.2- 10.3 GHz	499 MHz

One of the major concerned issue of WBAN is the operating time of the sensor devices which powered by batteries. The RF communication method such Zigbee, Bluetooth, have bad energy efficiency. Although some researches claim that Zigbee has operating time of three years [2], they have at a low data rate under 250 kb/s. Second, the high frequency bands of UWB and NB, suffer from huge signal attenuation through the human body channel due to the body shadowing effects [14]-[19]. The third main issue to be taken into consideration is that the other RF wireless products may operating in the same frequency band and result in interruption.

Body channel communication (BCC) utilize the human body as a communication medium to let the set of on-body sensor nodes communicate with a coordinator. As shown in Figure 1.1, the coordinator such a NIKE smart watch collects all the information through the human body instead of radio frequency propagating method. Subsequently, the collected information attained by the body sensors can be delivered to the user smart phone or a remote server for further processing.

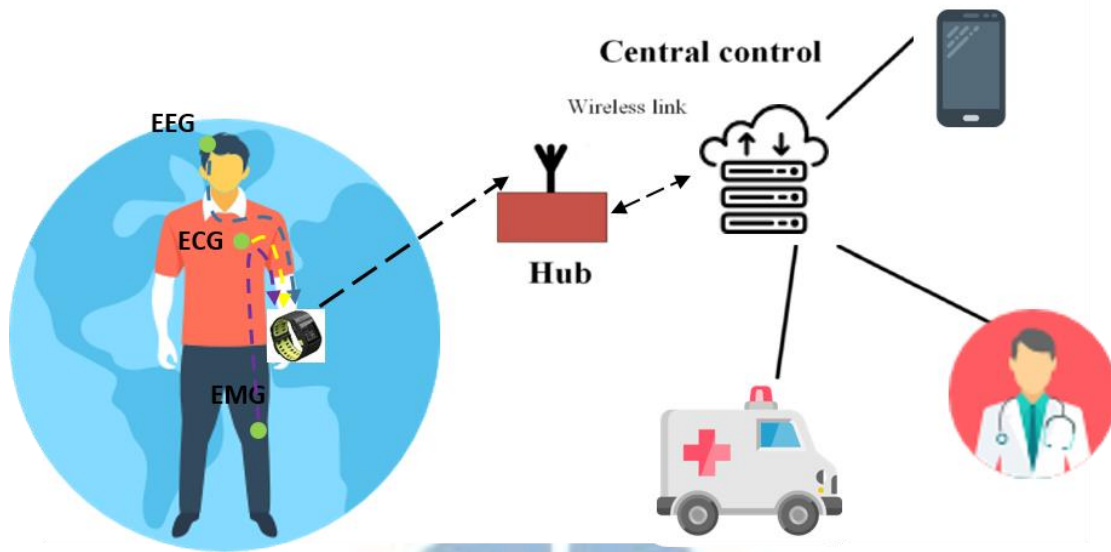


Figure 1.1 A simple demonstration of the body channel communication

There are some advantages for using the BCC. First, because of operating a frequency range below 100MHz, the BCC technique has relatively high data rate with minimum energy efficiency (energy per bit) as compared to Zigbee, Bluetooth, and the Ultra-Wideband. Second, the path loss of the signal for BCC is less than using RF propagation method. Moreover, the BCC is almost insensitive to the motion of the human body [3].

Along with development of RF communication, there are several low-power RF technique has been proposed, likes low power Bluetooth 、 Near-Field Communication(NFC). Table 1.2 shows BCC compares other wireless communication protocols. NFC is developed to use in short-term communication. Its power consumption is similar to low energy Bluetooth and it has shorter times to set-up than general Bluetooth. The low energy Bluetooth has low power consumption than general Bluetooth. However, there are several security issues on Bluetooth and NFC. The security issues suffered on BCC is less due to the signal is largely attenuated when it emits from the human body [42]. Moreover, the security on BCC can be more prompted by using human physiological measurement to establish customized secret key among

network nodes [41]. Last, as a portable devices on body, the energy efficient of BCC is higher than Bluetooth and NFC.

Table 1.2 Comparison for various wireless communication protocols.

Aspect	NFC	Bluetooth	Bluetooth low energy	BCC [25]
Frequency	13.56 MHz	2.4-2.5 GHz	2.4-2.5 GHz	1 MHz-150 MHz
Bit rate	424 kbps	2.1 Mbps	1 Mbps	60 Mbps
Range	< 20cm	100 m	50 m	1.8m (body max length)
Set-up time	< 0.1 s	< 6 s	< 0.006 s	N/A
Power consumption	< 15 mW	< 30 mW (Varies with class)	< 15 mW	1.85 mW
Energy/bit	35.3 nJ/b	2 nJ/b	1 nJ/b	31 pJ/b

Table 1.3 shows the requirements for the data rate of the biomedical signal processing and multimedia signals. For healthcare application, according to the standard of IEEE 802.15.4, the data rate of Electrocardiography (ECG) is 0.012 Mbps. In the other application [2], the data rate of the Electromyography (EMG) is 1.536 Mbps. Table 1.3 shows that the data rate below 10 Mbps are sufficient for the multimedia applications. Table 1.4 shows the existing BCC products on the market. The BodyCom is a development platform which offers develop boards and software to let customers can develop their own BCC applications. The DisneyResearch team builds several interactive games and the demonstrated videos can be found on the youtube. They use BCC to transfer digital

data which are provided with BCC wearable devices on the game participants. Panasonic develops an one touch ID authentication for the workers use. The workers can enable the devices by using transfer digital authentication through human body with a wearable wristband. The one touch ID authentication is developed for helping factories improve work safety and production efficiency.

Table 1.3 Requirements for data rate of the medical signals and multi-media signals

	ECG	EMG	Audio streaming	Video streaming
Data Rate (Mbps)	0.012 [9]	1.536 [2]	1 [2]	< 10 [2]

Table 1.4 Commercial BCC products on the market.

	BodyCom [37], [38]	DisneyResearch [39]	Panasonic one touch ID authentication [40]
Purpose	Development board	Interactive game	ID authentication

1.2 Characteristics of Human Body

Channel

Before designing a body channel communication transceiver, the first thing is to understand the body channel characteristics. According to the survey for several studies, the following works introduce some important characteristics of the body channel. In brief, a variety of factors such as signal frequency, signal transmission distance [10], the various surrounding environment [3], the different human body and the motion [3] and would add interferences into the BCC.

In general, BCC can be classified into galvanic (waveguide propagation) coupling and capacitive (electrostatic) coupling. The difference between two coupling method is that in capacity coupling, the transmitter and the receiver ground electrodes are floating. In galvanic coupling, electrodes are all connected to the body. The concept of two coupling methods is shown in Figure 1.2.

In capacitive coupling, the forward path of the signal goes through the human body, and the return signal path is closed by the air capacitive coupling with the external ground to be a signal loop. The capacitive coupling method is adopted in the proposed design, because it can achieves relatively high data rate and less affected by the transmission distance as compared with the galvanic coupling method [4].

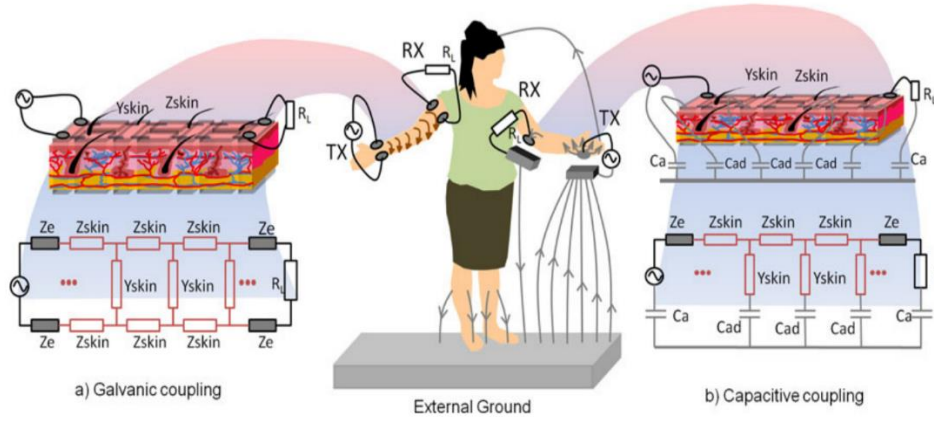


Figure 1.2 Coupling methods. (a) Galvanic (left) (b) Capacitive (right) [4]

To optimize the performance and power of BCC transceiver, theoretical and experimental model of the signal transmission on the body has been studied in [10]-[13]. A disturbed RC circuit model is shown in Figure 1.3 [10]. Figure 1.4 shows the measured result and the corresponded simulation results. When the signal frequency is below 4 MHz, the path loss of the signal has no difference in different transmission distances. This is because the signal attenuation is dominated by the capacitive return path. Beyond the threshold (4MHz), the longer transmission distance has the higher impedance in the body path. In this region, the body channel acts as a band pass filter. Therefore, if the BCC want to be universal for everyone, the inconvenience of adjustment parameter on BCC receiver should be concerned. However, in [23], [36], some self-adaptive path loss compensation methods have been proposed. With above that, the robustness of BCC may even be promoted.

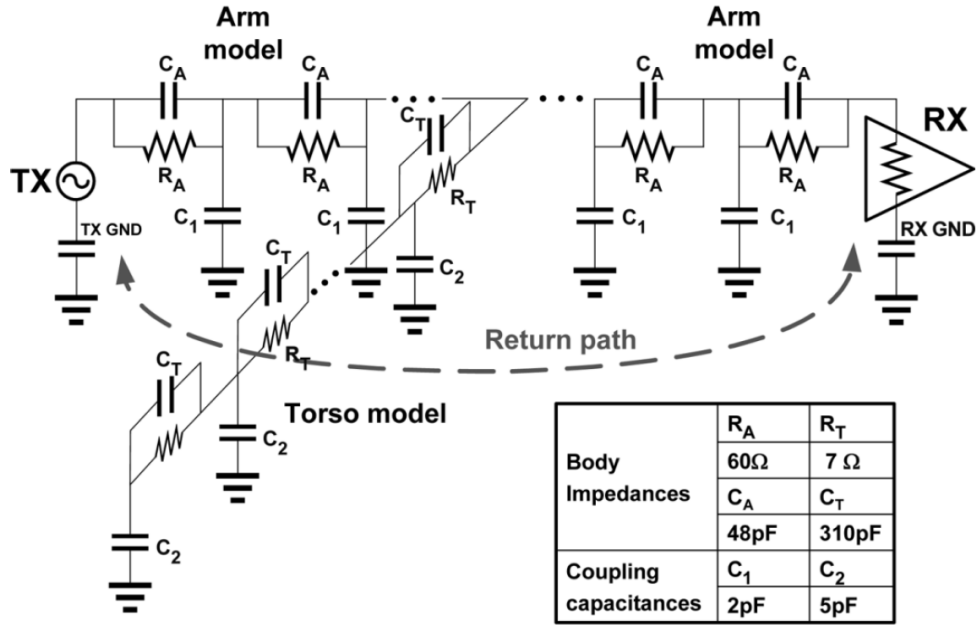


Figure 1.3 RC circuit model for body channel. [10]

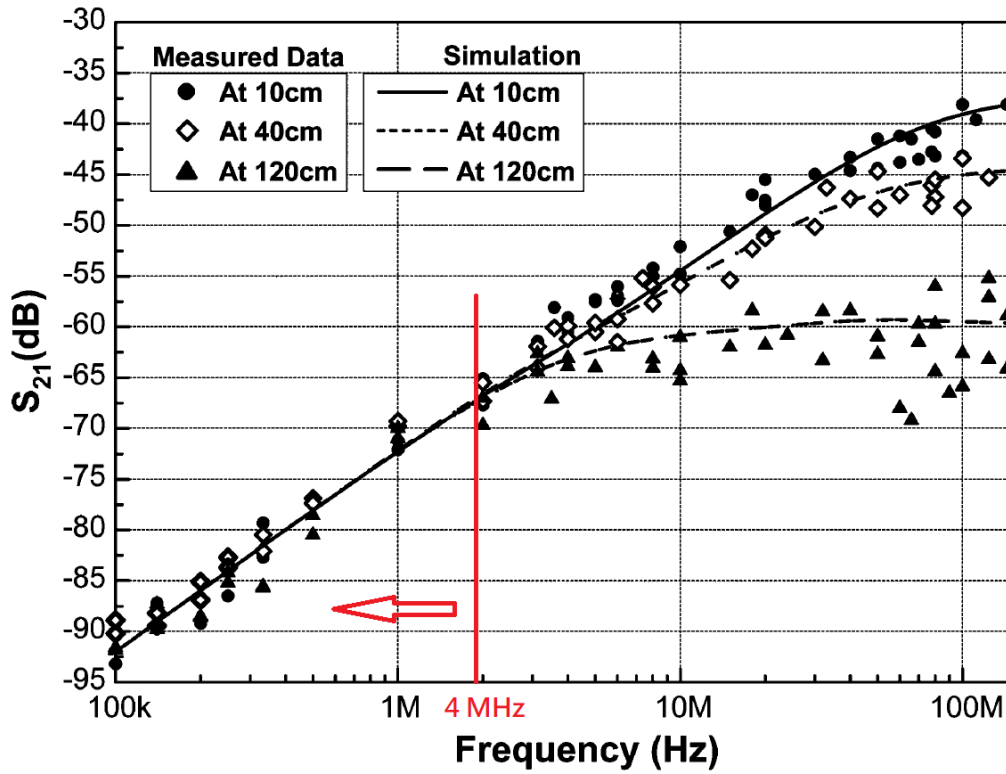


Figure 1.4 Measured S_{21} -parameter of the body channel. [10]

In [20], the body antenna effects, that is the human body receives and couples electromagnetic interferences and wireless signal by the adjacent devices. For the sake

of designing a BCC transceiver to overcome the impacts of random jitter which is caused by body antenna effects, the time-domain characteristics of the human body channel also needs to be measured. As shown in Figure 1.5, if the transmitter transmits square waves to the receiver through a human body with the air coupling in return path. The signal will be attenuated to shark shape waves. The amplitude of the shark shape is largely attenuated against the original amplitude from the transmitter. As decreasing the signal frequency, the shark shaped pulse width become narrow.

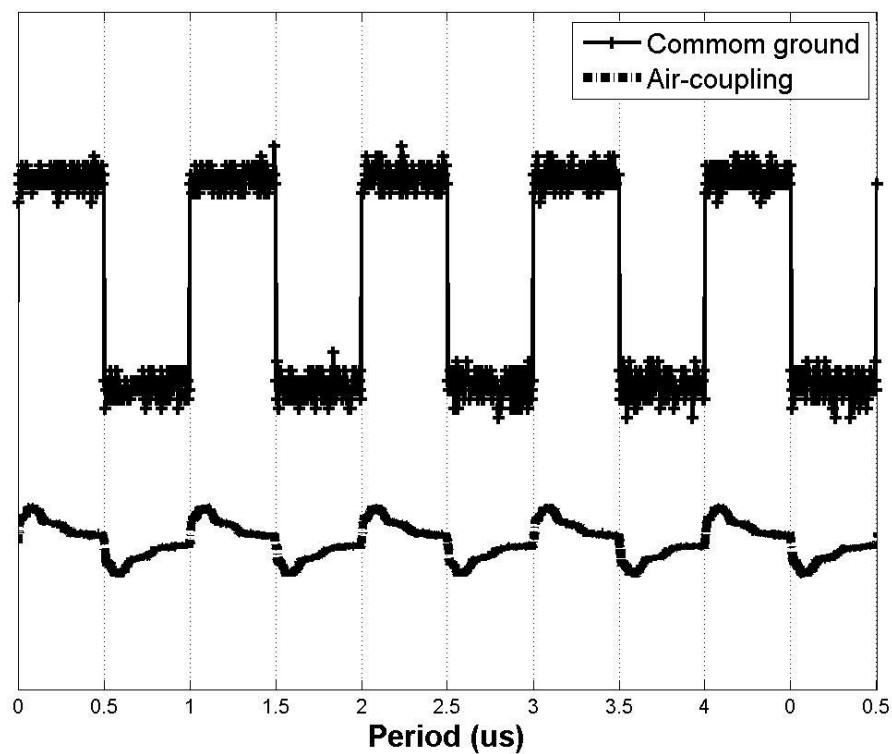


Figure 1.5 Measured waveform with and without the return path. [5]

After understanding the signal attenuated situation, measurement is set up for recovering the attenuated signal. The experiment based on an analog front-end (AFE) board. The received signal ① will be amplified by an variable gain amplifier (VGA) ② and the amplified signal ③ will go through a Schmitt trigger ④. In the end, the logic wave ⑤ is recovered, as shown in Figure 1.6. The gain value of the VGA and

the DC offset of the Schmitt trigger can be adjusted to satisfy different signal frequency and transmission distance as shown in Figure 1.7.

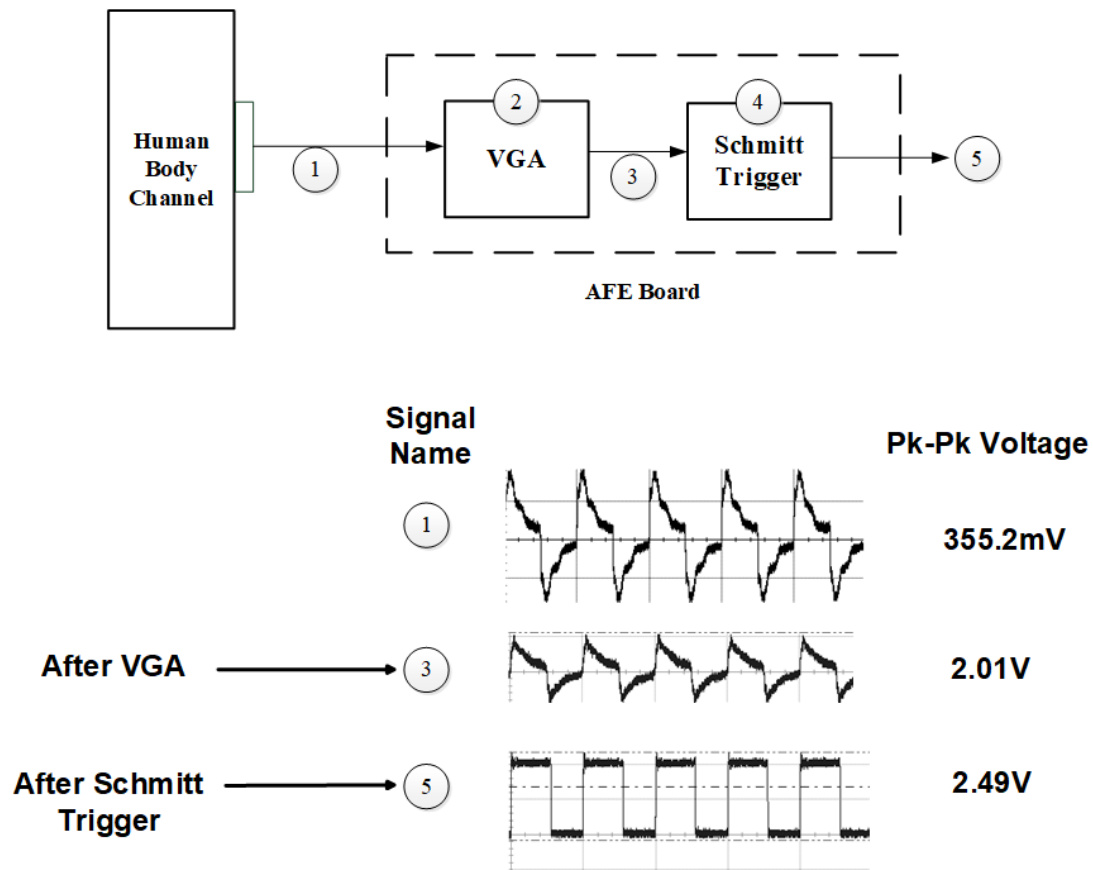


Figure 1.6 The block diagram and the recovery operation of the AFE circuit. [5]

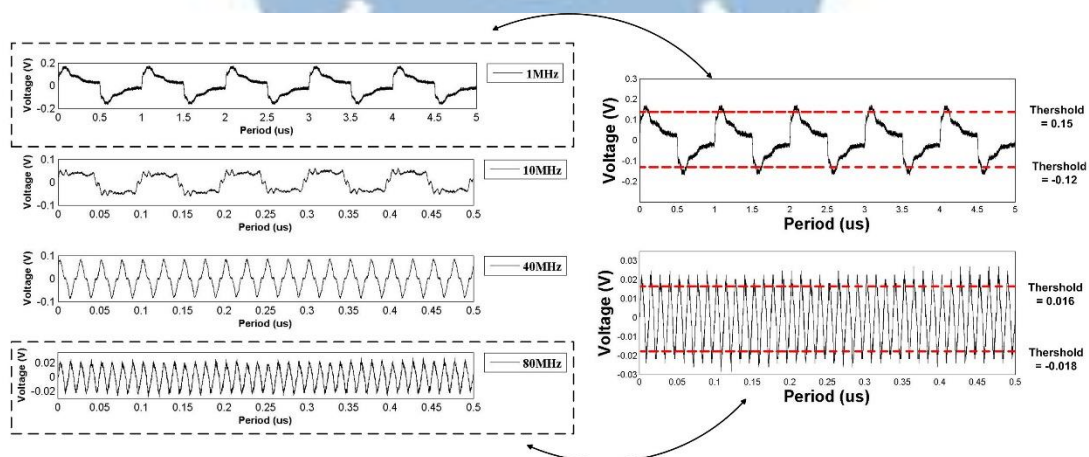


Figure 1.7 The time-domain characteristics with different frequencies at 10 cm. [5]

With a time-domain measurement for body channel, a regular pattern signal can

be transmitted to a human body and recovered by an AFE board. Based on the aforementioned information, Table 1.5 can be built which containing different jitter measurement situations of 1 MHz to 40 MHz and the transmission distances of 10 cm to 140 cm. Moreover, these jitter information can be used to model a realistic situation and be used as the jitter budget for design a BCC transceiver.

Table 1.5 different jitter measurement situation of body channel. [5]

Distance	Frequency	Input Voltage	Period	Period Jitter Peak-to-Peak	Period Jitter RMS	Cycle-to-Cycle Jitter RMS
10 cm	1 MHz	1.0 Vpp	999.99 ns	3.9 ns (3.9% UI)	471.7 ps (0.05% UI)	849.92 ps (0.08% UI)
	10 MHz		99.99 ns	3.65 ns (3.65% UI)	271.3 ps (0.27% UI)	465.09 ps (0.47% UI)
	20 MHz		49.99 ns	3.05 ns (6.01% UI)	314.4 ps (0.63% UI)	485.63 ps (0.97% UI)
	30 MHz		33.33 ns	1.5 ns (4.50% UI)	160.1 ps (0.48% UI)	295.92 ps (0.89% UI)
	40 MHz		25.01 ns	2.6 ns (10.39% UI)	155.6 ps (0.62% UI)	845.55 ps (3.38% UI)
140 cm	1 MHz		999.88 ns	43.5 ns (4.35% UI)	3.5 ns (0.35% UI)	5.63 ns (0.56% UI)
	10 MHz		99.96 ns	10 ns (10% UI)	1.1 ns (1.1% UI)	1.78 ns (1.78% UI)
	20 MHz		49.99 ns	3.4 ns (6.8% UI)	253.6 ps (0.5% UI)	467.95 ps (0.94% UI)
	30 MHz		33.35 ns	1.72 ns (5.15% UI)	219 ps (0.66% UI)	2.13 ns (6.39% UI)
	40 MHz		25.42 ns	7.1 ns (27.93% UI)	643 ps (2.53% UI)	4.33 ns (17% UI)

1.3 Design Regulation

In order to obtain high energy efficiency and signal-to-noise ratio (SNR), the data rate should as high as possible. However, rapid change of electric field will let body scatter electromagnetic waves to interfere the operating electronic devices near body. This phenomenon is called electromagnetic interference (EMI). Figure 1.8 shows an EMI measurement for a person carries a BCC transmitter. In this measurement, the distance from the measured location to the signal transmitter is 3m. It indicates the higher frequency on BCC transmitter, the larger power of e-field around the measured person.

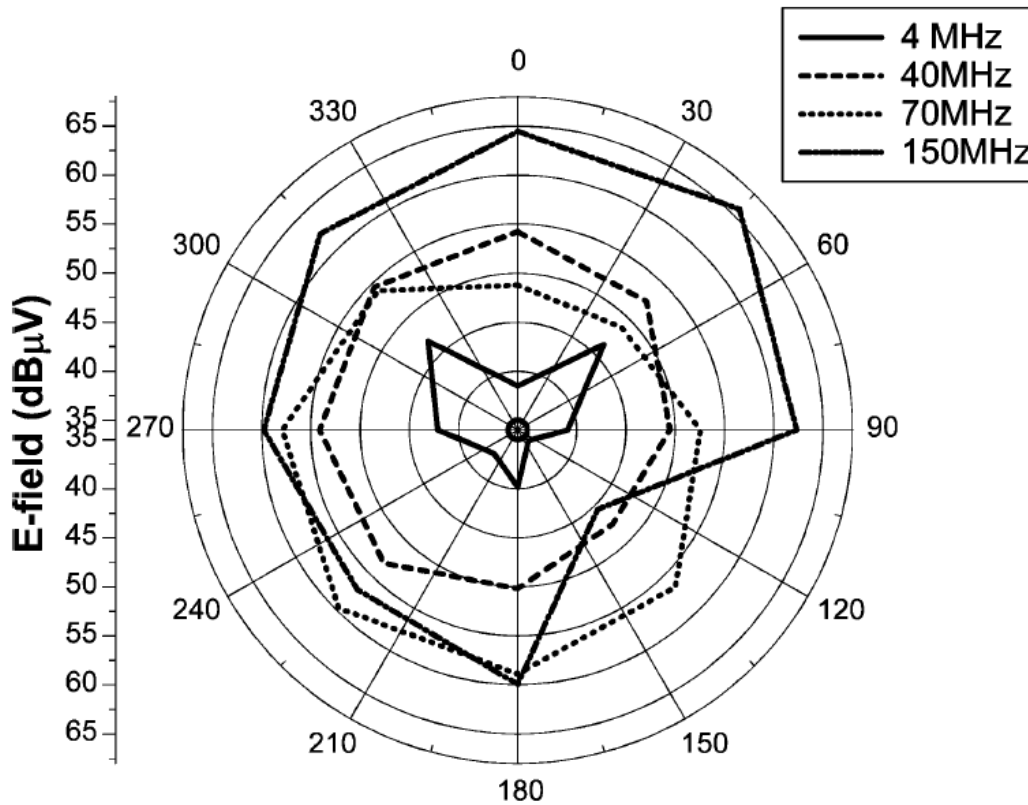


Figure 1.8 E-field around a person with a BCC transmitter [10].

Figure 1.9 shows the maximum power spectral density of the transmitted signal that in FCC regulations (Federal Communication Commission Regulation Limit). The

maxTXPSD in Figure 1.9 implies that the transmitted power can be increased without violating FCC regulations when the frequency decreases.

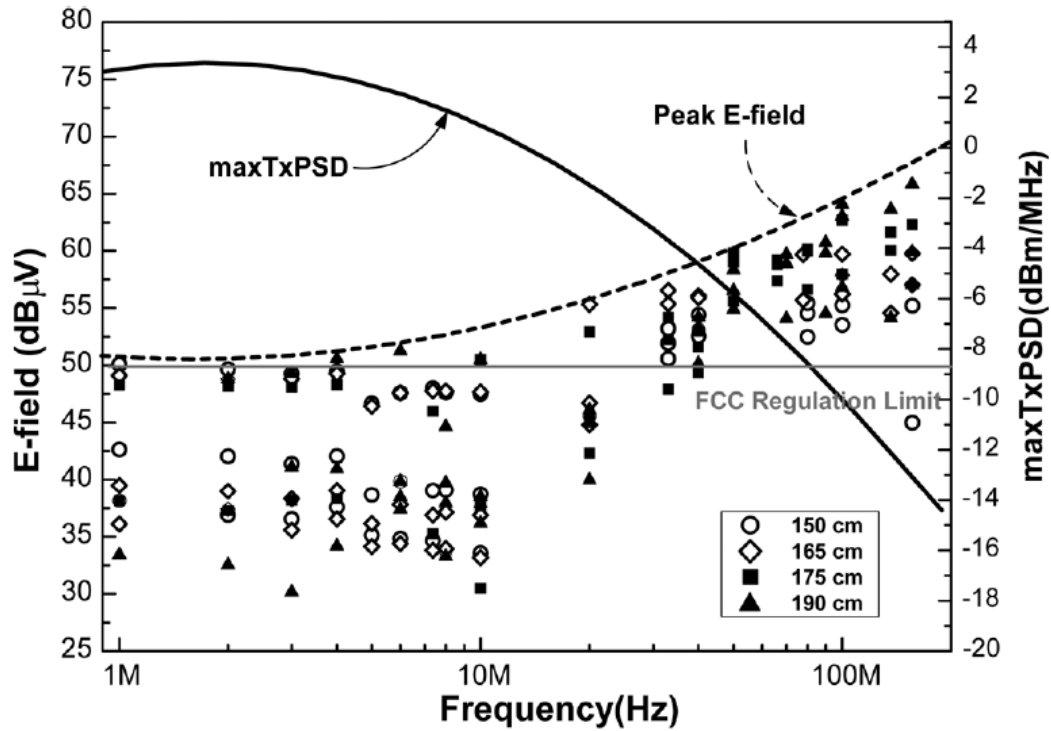


Figure 1.9 Measured E-field data from multiple individuals.

The safety standard of the design for BCC transceiver which is also introduced by the International Commission on Non-Ionizing Radiation Protection (ICNIRP) and IEEE international Committee on Electromagnetic Safety [43], [44]. The standards limit human exposure to electric magnetic and electromagnetic field in RF regime based on tissue-heating effect. The restriction imposed for BCC frequency band-of-interest (<150 MHz) is stated in a localized specific absorption rate (SAR) of $4 \text{ W} \cdot \text{kg}^{-1}$ for general public exposure [43]. The body surface area (BSA) is necessary to get before calculating a SAR limitation. The equation of BSA is shown in Equation 1.1, where the weight is in kilograms and the height is in centimeters.

$$\text{BSA} = (W^{0.425} * H^{0.725}) * 0.007184 \quad (1.1)$$

Estimating that the human limb takes 5% total body weight (and surface area), for

a person weighting 60 kg and having 175 cm in height. The value of BSA is 1.73 m^2 , a total power less than 12 W should be incident on a limb in this case; With an electrode having a sensor area of 3.5 cm^2 , a power less than 2.4 mW should be localized onto the attached area of the limb.



1.4 Prior Body Channel Communication

Transceivers

1.4.1 Basic Architecture of a BCC Transceiver

Figure 1.10 shows the block diagram of the BCC transmitter. The transmitter consists a pseudo-random binary sequence (PRBS) generator, an encoder, a modulator, and a driving buffer. The generated random data will be modulated by the modulator, and with a driver, the modulated data will be transmitted to the human body through an electrode.

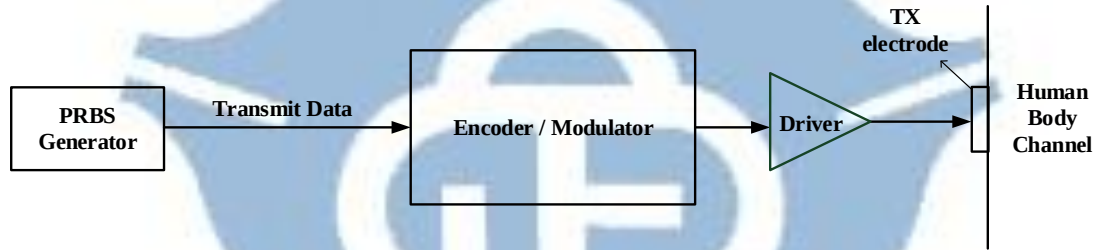


Figure 1.10 Block diagram of BCC transmitter.

Figure 1.11 shows the block diagram of the BCC receiver. The receiver consists a variable gain amplifier (VGA) and a Schmitt trigger on an analog front end circuit. After the VGA amplifies the attenuated signal from the human body, the Schmitt trigger recovers logic waves by distinguishing the amplitude over voltage thresholds or not. Subsequently, the clock and data recovery circuit (CDR) will recover the clock and the data. According to the recovered data and the recovered clock, the RX_Data is demodulated by the demodulator.

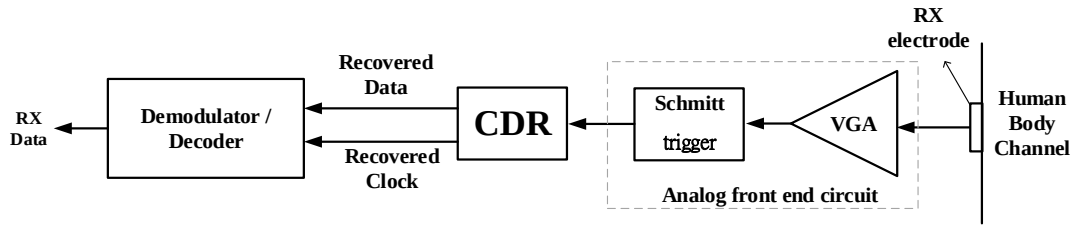


Figure 1.11 Block diagram of the BCC receiver.

1.4.2 Modulation Scheme: Frequency/Amplitude

Shift Keying (FSK/ASK)

The frequency shift keying (FSK) or the amplitude shift keying modulation scheme are often used in radio frequency modulation. It also has been applied in body channel communication [20]-[22].

FSK modulation utilizes two different frequencies to be a binary symbol individually. In [20], an adaptive frequency hopping (AFH) technique is proposed. It divided 30-120 MHz frequency band into 4 channels. Each channel has 25 MHz bandwidth and can support a maximum data rate up to 10 Mb/s. With AFH, every channel status is uninterruptedly monitored and the clean channel will be chosen for the adaptive frequency hopping. The operation of AFH has shown in Figure 1.12. There are more than 10 dB improvement for interference resistance which is achieved by the 4 channel AFH approach.

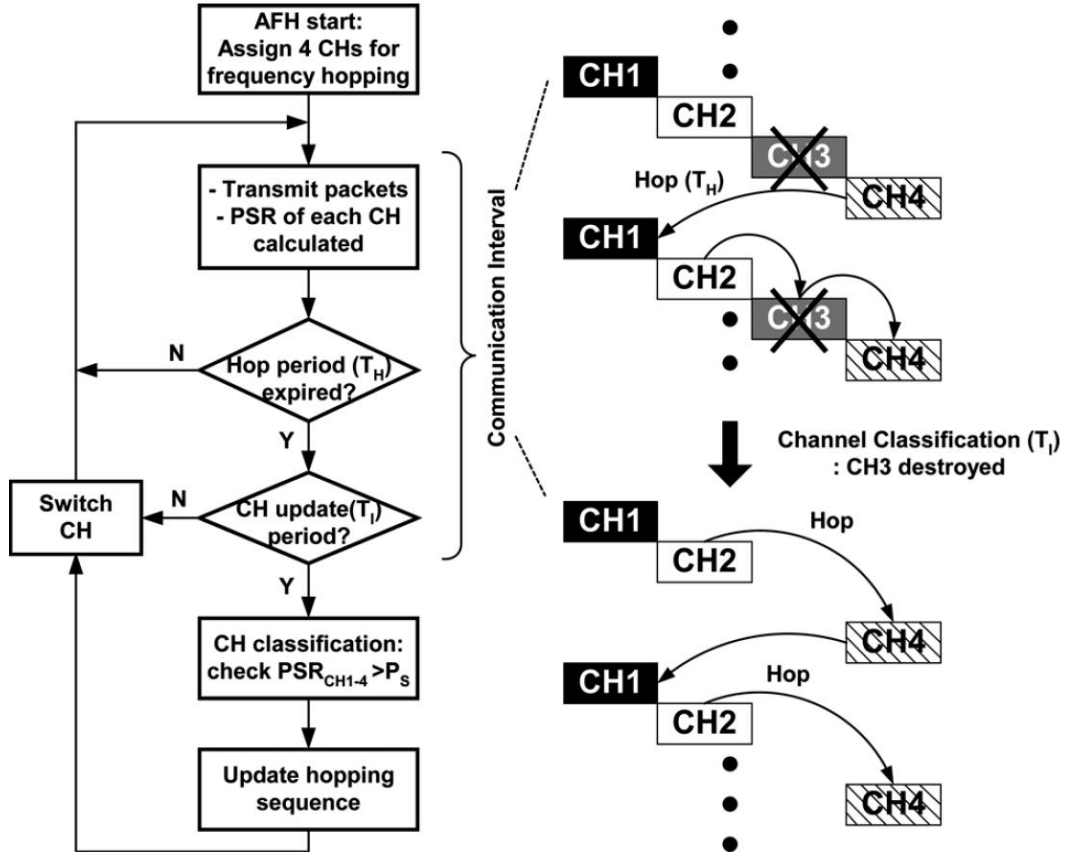


Figure 1.12 The concept of the adaptive frequency hopping (AFH) [20].

Figure 1.13 shows the overall architecture of the adaptive frequency hopping BCC transceiver. With dual frequency synthesizers, a direct-switching modulator can achieve the worst case for the blank time of the frequency band switching in $4.2\mu s$. Subsequently, a DLL-based demodulator demodulates the 10 Mb/s FSK signal in the baseband. Moreover the proposed demodulator reduces the transition jitter by half.

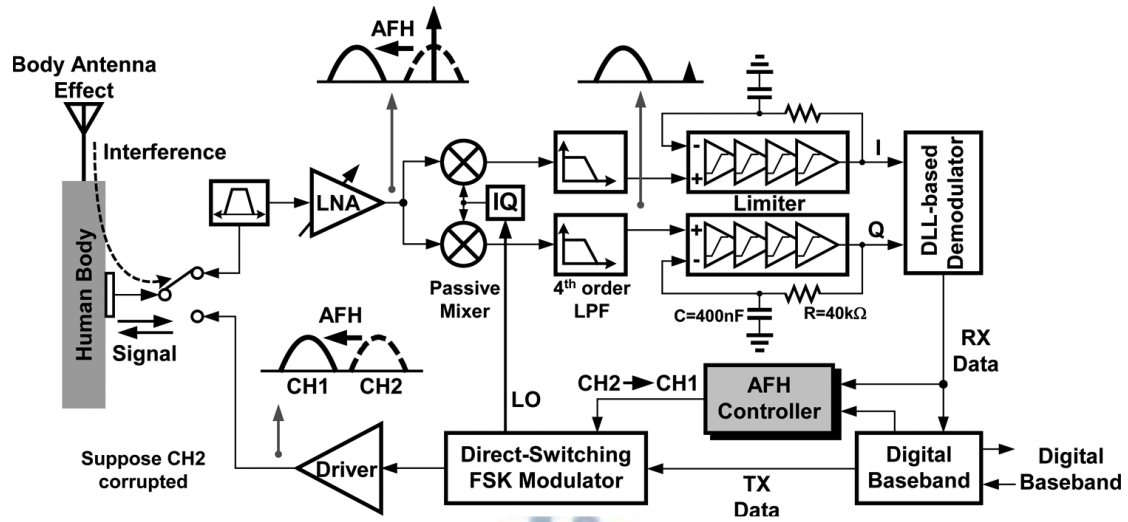


Figure 1.13 the architecture of the AFH BCC transceiver [20].

Figure 1.14 shows the other architecture of the BCC transceiver with FSK modulation. A crystal oscillator on base station (BS) is used to synchronize the on-chip oscillator on each sensor node wirelessly. This step helps the frequency calibration between BS and the sensor nodes and reduces the frequency drift problem of the on-chip oscillator. In the transmitter side, the frequency synthesizer as aforementioned calibrates the injection locked digitally controlled oscillator (DCO) output frequency. The data will be modulated with a sub-band double FSK modulator. Then it is transformed to high modulation wideband signal with the wideband FSK modulator as shown in Figure 1.15. In the receiver, the received signal is amplified with a LNA and is demodulated by the fixed-time-delay wideband FSK demodulator and the sub-band FSK demodulator. This study use injection-locked approach to achieve a low power consumption. Thereafter, the signal with wide-band FSK modulation largely reduces the interferences in the specific frequency band.

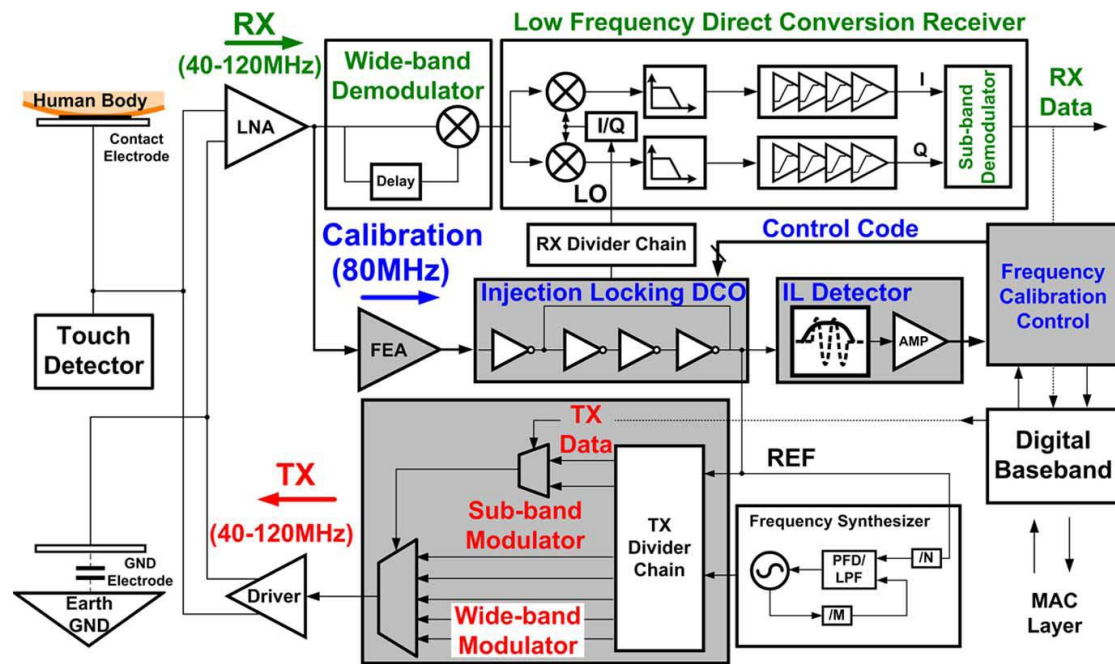


Figure 1.14 Overall low-energy double FSK transceiver for BCC [21].

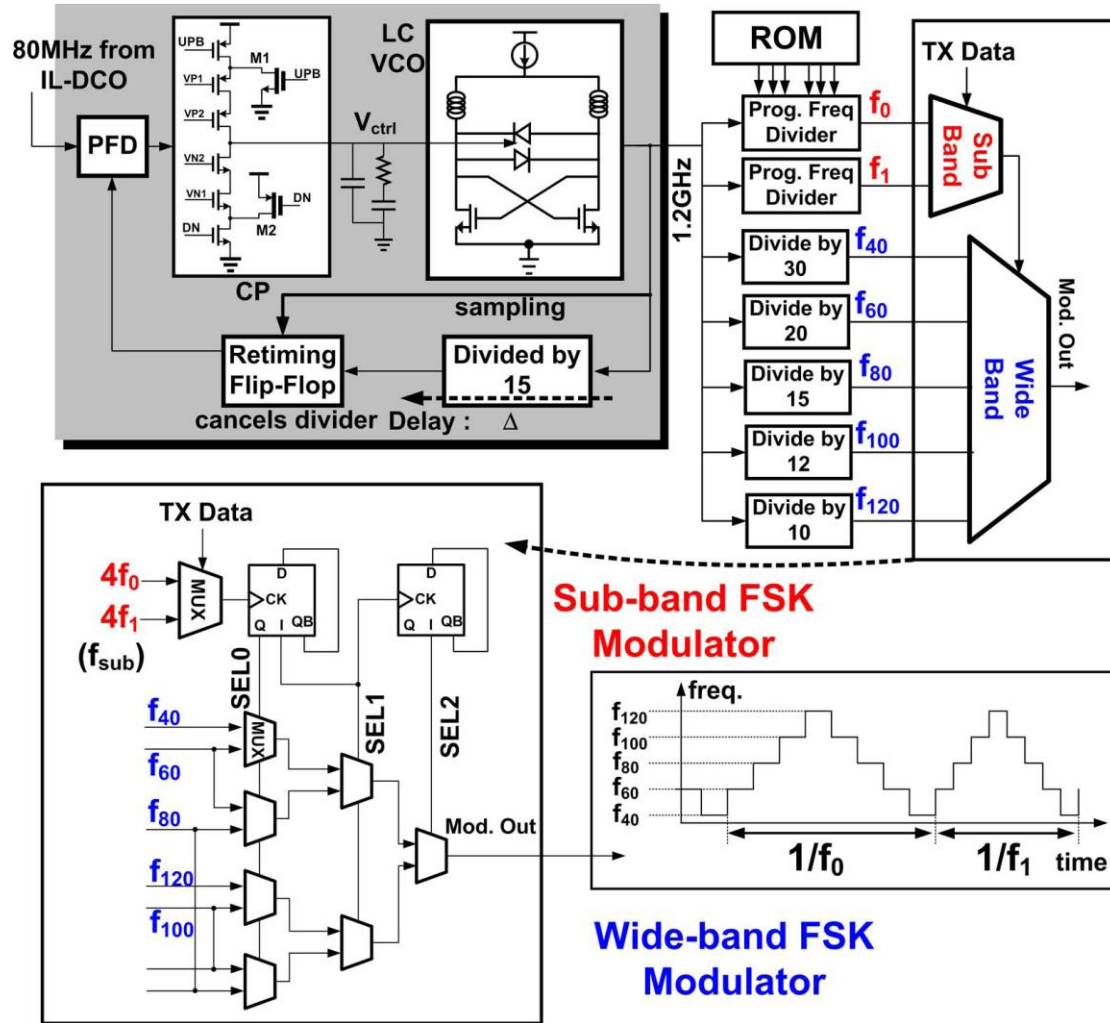


Figure 1.15 The sub-band and the wide-band FSK modulator [21].

The amplitude shift keying (ASK) modulation utilize the produced signal with or without a signal to be a digital symbol. In [22], an On-off keying (OOK) modulation which is one form of the ASK modulation is shown in Figure 1.16. This study utilizes two bands to design a full-duplex transceiver which can achieve 80 Mb/s data rate. The transmitter and the receiver utilize different frequency band. For instance, if transmitter use the L-band, the receiver use H-band, and vice versa.

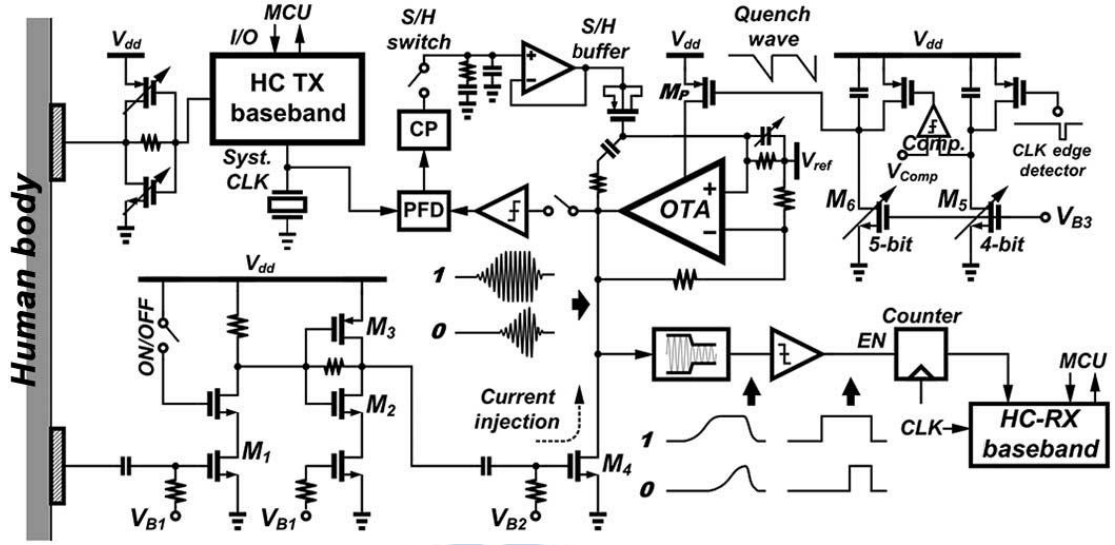


Figure 1.16 The schematic of the full-duplex OOK BCC transceiver [22].

1.4.3 Modulation Scheme: Orthogonal frequency-division multiplexing (OFDM)

The orthogonal frequency division multiplexing modulation (OFDM) modulates data on the multiple sub-carrier frequency band and is proposed in [8], [24]. Because of the orthogonal characteristic of the sub-carriers, the OFDM can mitigate the frequency selectivity and avoid inter-symbol interference (ISI) which is caused by multipath fading effect. As shown in Figure 1.17, a 16-quadrature amplitude modulation (QAM) gathering with 64 subcarriers pseudo-OFDM modulation is proposed [8]. In the transmitter side, the data are used by a 16-QAM mapping block to generate 13-bit point for each subcarrier input of the 64-point IFFT. The cyclic prefix and pilots are used to help synchronization and channel estimation. Then, the parallel data are converted into input serial data of a direct switch FSK modulator. In the receiver side, a miniaturized FSK demodulator without a PLL/DLL and double branch in synchronization is used, which reducing the area over by > 50 % as compared to the

conventional design. Then, the data will be demodulated with Fast Fourier Transformation (FFT) and 16-QAM de-mapping. Last, the bit error rate performance of P-OFDM is better than the FSK TRX at an input level of -74 dBm.

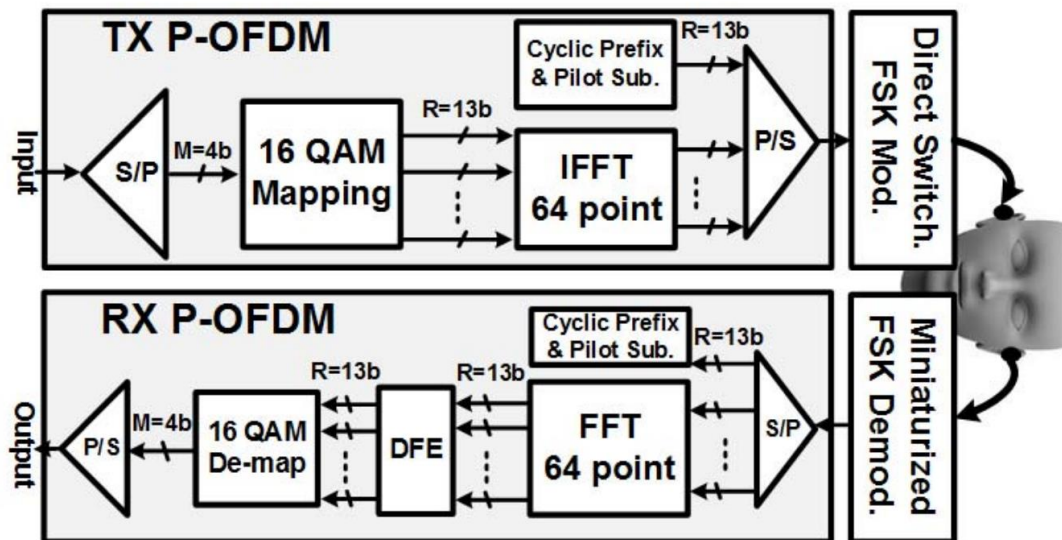


Figure 1.17 The P-OFDM transceiver diagram [8].

1.4.4 Modulation Scheme: Frequency Selective Digital Transmission Transceiver (FSDT)

The frequency selective digital transmission (FSDT) modulation is a method which modulates the data with a coding gain and is presented in [25], [26]. The code length of the encode data is larger than the original data to provide good data reliability. Subsequently, the digital form modulated data are directly transmitted to the human body. The architecture of FSDT modulation using Walsh codes is shown in Figure 1.18. The Walsh code has orthogonal characteristics. Each received Walsh code can be correctly recovered if the corrupted data length is less than the half of the code word.

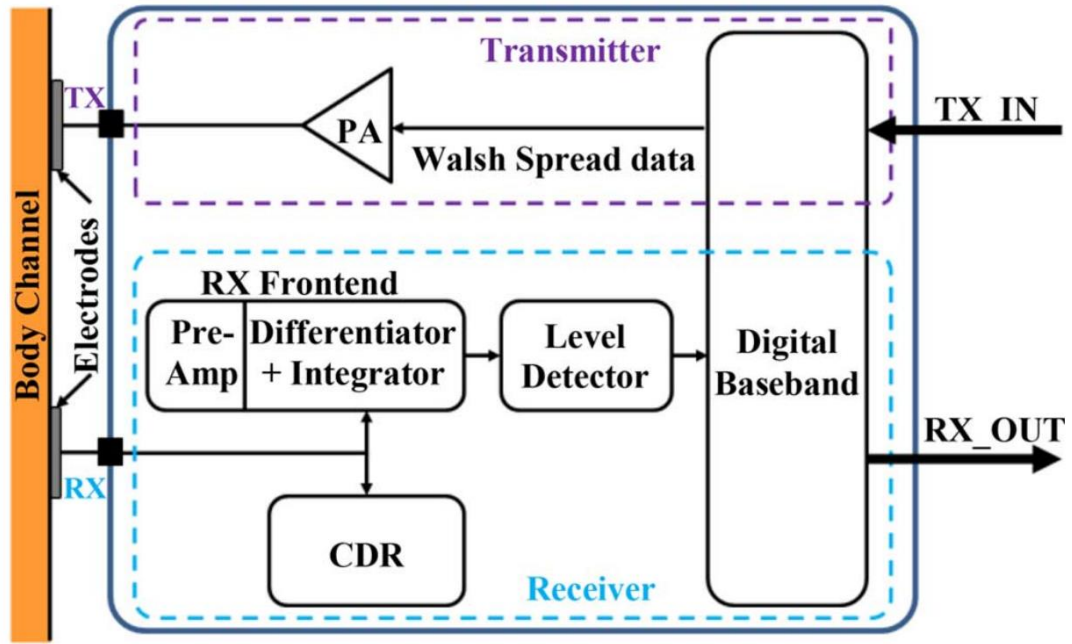


Figure 1.18 The block diagram for Walsh code FSDT baseband transceiver. [25]

The fixed number of transitions and the repetitive of the Walsh code generate several frequency band which has shown in Figure 1.19. With this feature, the frequency band of output Walsh code data can provide a strong interference resistance [25].

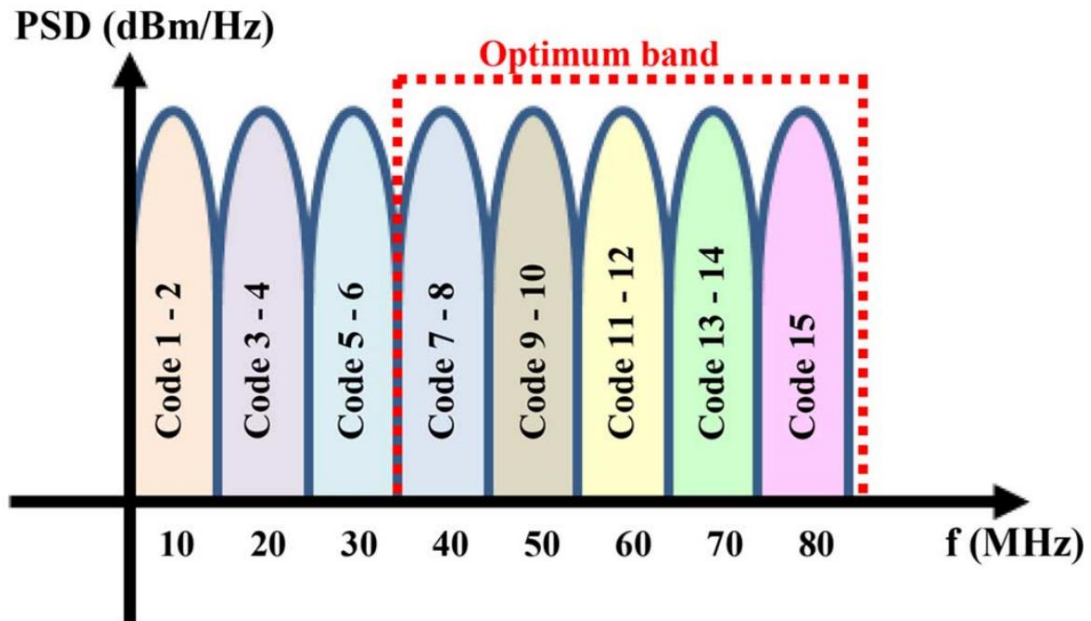


Figure 1.19 Fundamental frequencies of 16-bit Walsh code clocked at 160 MHz [25].

1.4.5 Modulation: Wide-band Signaling (WBS)

A wideband signal BCC transceiver which have features such low complexity and high data rate capability is proposed in [27], [28], [35]. As shown in Figure 1.20, in the transmitter side, the spread spectrum clock circuit generates a clock with spread spectrum. In the meantime, the linear feedback shift register generates a sequence of pseudo random numbers. The data are converted into non-return-to-zero inverted (NRZI) data and directly transmit to the human body. The CDR recovers the received data which are amplified and recovered to digital waveform with an analog front-end circuit. WBS has great resistance ability of the specific interference due to the spread spectrum characteristic. Moreover, the power consumption is low because without complicated modulation. In [27], this BCC transceiver can support a maximum data rate up to 40 Mb/s, and the energy efficiency is 0.0485 nJ/b.

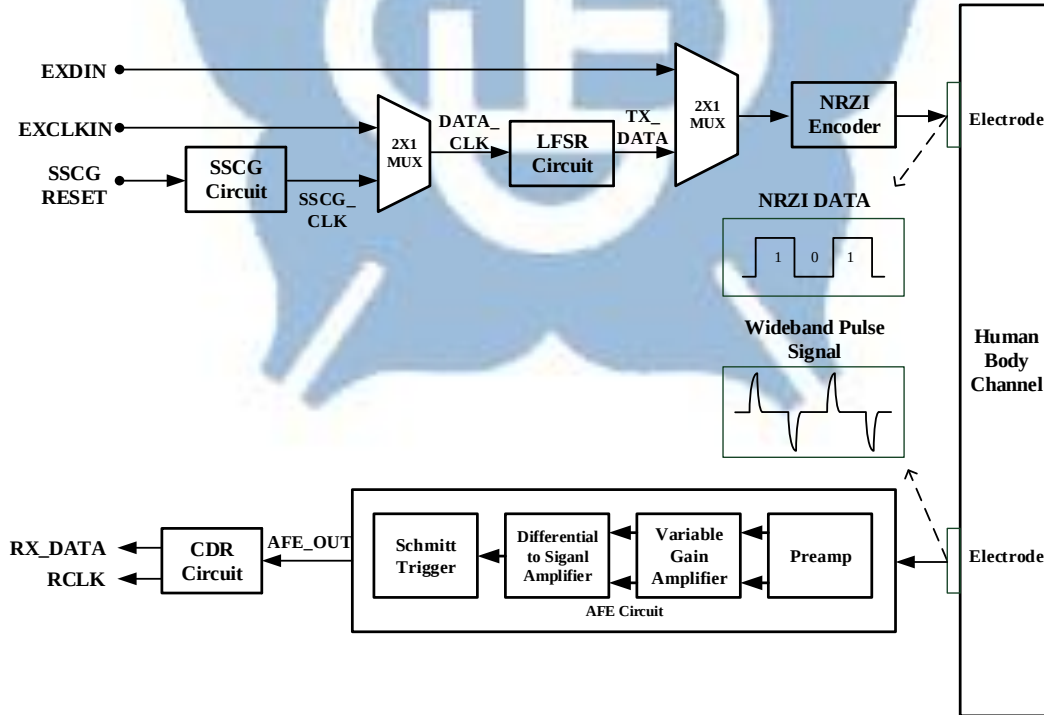


Figure 1.20 The architecture of WBS BCC transceiver [27].

1.5 Motivation

According to the above survey, body channel communication is a way different from RF wireless transmission and can achieve relatively high data rate and suffers from less interferences. The characteristics of BCC show that the frequency of the application range should be under 150 MHz and it has low power consumption and can be applied for healthcare and entertainment portable devices.

The FSK modulation is a simple concept to use two different frequencies be a digital symbol. Nonetheless, the peaks in the power spectrum density indicate the signal will often strongly contaminated by specific interferences. In [20], an AFH method is proposed to perform frequency hopping to reduce interference effects. However, the blank time for frequency hopping is a drawback for the stable healthcare device. For the wideband FSK [21], there still needs a high quality oscillator to divide 5 frequency band in order to support the wideband modulation. Simultaneously, each BCC node should be calibrated with a stable oscillator such as a crystal oscillator. The power consumption of an external oscillator should be concerned. Last, the data rate of FSK architecture is limited because that the oversampling requirement in the receiver design.

The amplitude shift keying (OOK) modulation [22] is often strongly contaminated by noise interferences owing to the fact that noise affects the amplitude. The OFDM modulation can achieve a high data rate with a narrow frequency band [8], [24]. However, the complicated design largely increases the power consumption and chip area. The FSDT based architecture [25] can achieve 60 Mb/s data rate and have great data reliability. Nonetheless, the code rate is low with respect to using redundant bits to protect the original data. The WBS BCC transceiver is proposed in [27], it directly transmits binary signals into human body. It has low power consumption and can

achieve high data rate. Nevertheless, it has low tolerance for large frequency drift as compared with other modulations. It means the decoding ability is deteriorated owing to the different frequency between the transmitter and the receiver.

From above discussion, the ideal body channel communication transceiver should concern about (1) solving the impacts of interferences from nearby electronic devices or other wireless signal propagating in air, (2) amplifying the attenuated signals in different transmission distance, (3) fitting BAN safety requirements, (4) designing a transceiver with low energy per bit and being suitable for multimedia or healthcare application. Therefore, aiming to design a low energy consuming and miniaturized portable BCC device, the WBS based architecture is adopted owing to it has low design complexity and has advantages in power consumption and chip area. In addition, FPGA can provide stable oscillating source to avoid frequency drift in WBS architecture. Moreover, in this thesis, a convolutional encode method is adopted to enhance the data reliability to overcome the impacts of random jitter and has higher code rate than prior design in [29]. In prior study [45], Manchester modulation method is used. However, it will cost half of signal transmission bandwidth. With NRZI modulation, more design elasticity can be achieved. Hence, a wide-band signal body channel communication transceiver with convolutional encoding method is proposed.

1.6 Outline of Thesis

Chapter 1 briefly introduces the body area network, characteristics of human body channel, prior BCC transceivers and the motivation of the proposed BCC transceiver.

The rest of the thesis is organized as follows: Chapter 2 shows the architecture of the proposed BCC transceiver, which includes the transmitter side and the receiver side.

Chapter 3 shows the experimental results. Chapter 4 concludes this thesis.



Chapter 2 The Proposed BCC Transceiver Based on FPGA Boards

2.1 An architecture overview for the proposed BCC transceiver

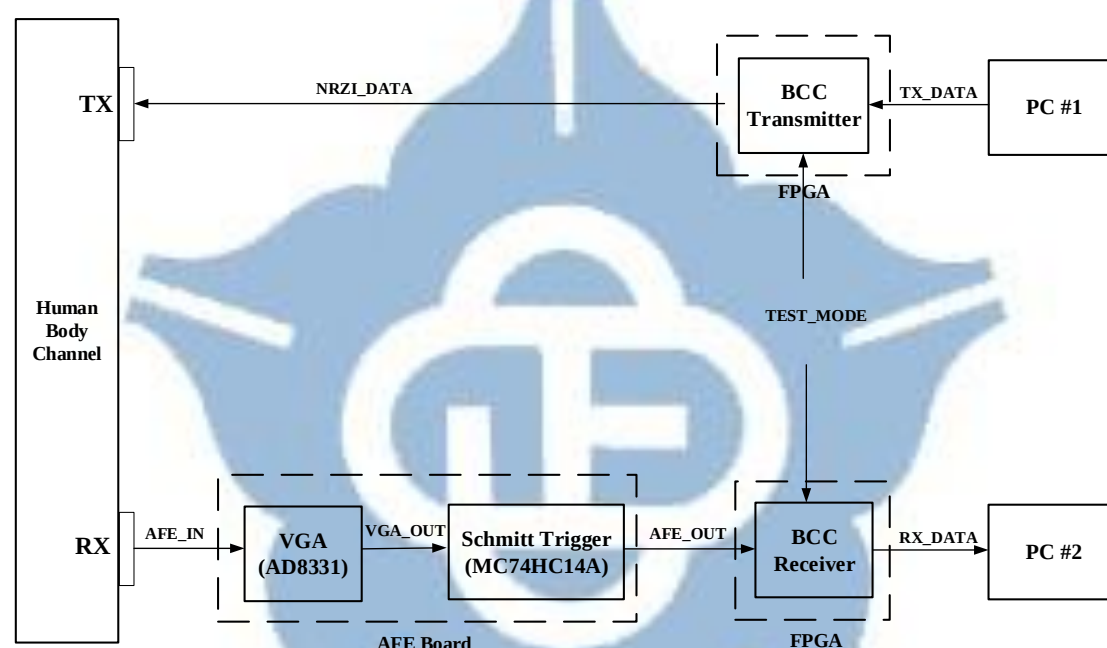


Figure 2.1 The overall architecture of the proposed BCC transceiver.

The overall measurement setup of the BCC transceiver is shown in Figure 2.1. In the first, PC #1 transmits data to the FPGA-based BCC transmitter. The transmitter encodes and modulates the input data before sending it to the human body. Because the signal is attenuated when going through human body, an AFE board is used to pre-process the received signal. After the attenuated signal is restored to digital waveform, the data are sent to the FPGA-based BCC receiver for clock and data recovery. The recovery data are demodulated and decoded by the receiver. Finally, the decoded data

are sent to the PC #2.



2.2 Wideband Signaling BCC Transmitter

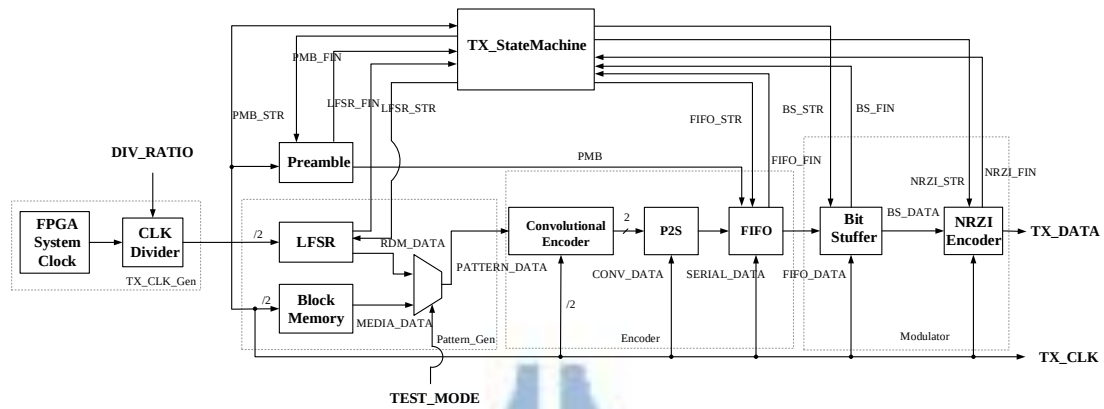


Figure 2.2 The block diagram of the proposed BCC transmitter.

Figure 2.2 shows the block diagram of the proposed BCC transmitter. The clock divider divides the system clock (100 MHz) of the FPGA board and triggers all blocks. The user can choose to send the multimedia images stored in the FPGA memory block or sends the random data generated from the linear feedback shift register (LFSR) pattern generator. The convolutional encoder used encoded format (2,1,7) to encode data in order to increase data reliability. The first and second parameter in the encoding format means the encoder outputs two bits when one bit data inputs. The last parameter in the encoding format means 6 register store the input values and the newest input data does XOR according the polynomial generated matrix. The FIFO puts packet header and then encodes data in order. The modulator consists of a bit stuffer to limit the maximum length of the consecutive identical digits (CID), and then, the NRZI output waveform will have more data transition.

2.2.1 Pattern Generator

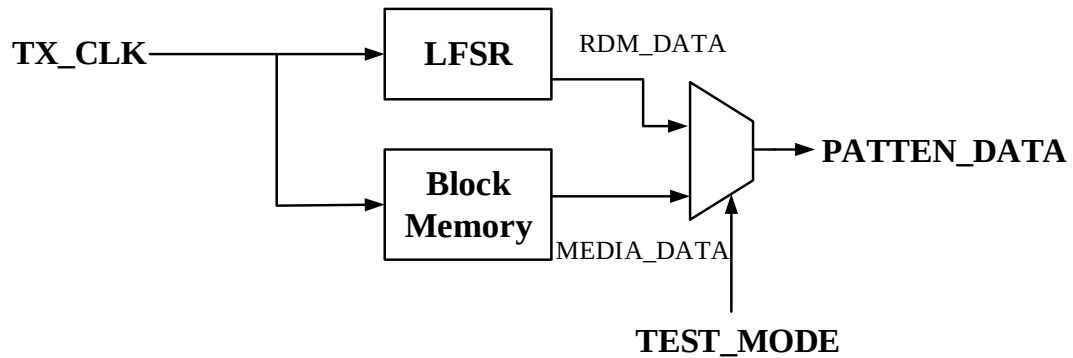


Figure 2.3 The block diagram pattern generator.

The user can use the TEST_MODE signal to choose which data to transmit. The linear feedback shift register (LFSR) block generates $2^{20} - 1$ bits repetition by twenty register and a XOR gate which is shown in Figure 2.4. The corresponding feedback polynomial equation of the LFSR is shown in Equation 2.1. The random data included longest 19 consecutive identical data. The block memory stores the multimedia image data which are converted into binary format by Matlab.

$$1 + x^{19} + x^{20} \quad (2.1)$$

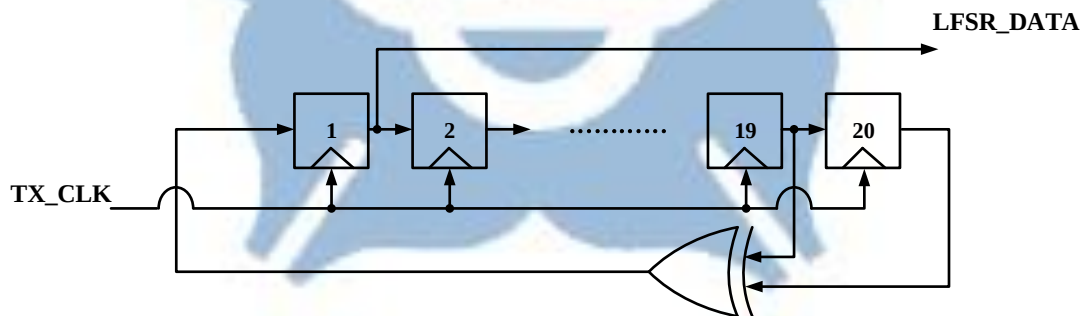


Figure 2.4 The architecture of linear feedback shift register circuit.

Both LFSR random data and multimedia image data will be encoded by the convolutional method. Eventually, the encoded data will be formatted as a packet with the purpose of being recognized by the receiver. The packet format is shown in Figure 2.5. The preamble block generates the regular sequence and the start frame delimiter (SFD) to be the packet header. The guard bits are inserted to let the Viterbi decoder of

the receiver decoding the data correctly. The number of guard bits are determined by the number of constraint length of convolutional encoding method used in our design.

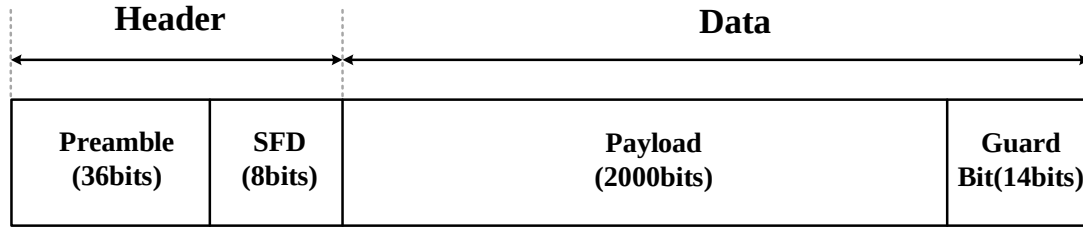


Figure 2.5 The TX packet format.

2.2.2 Convolutional Encoder

With the aim of increasing the data reliability, a convolutional encoding method which belong to channel code is adopted. As compared to Walsh codes modulation in [29], the code rate ($1/2$) of the adopted convolutional encoding is 1.6 times higher than the code rate of the Walsh code ($5/16$). As shown in Figure 2.6, the convolutional encoder uses six registers to save the input data. The output data are generated by exclusive-or the values in the registers and the current input data. The convolutional encoded format (2, 1, 7) stands for two output data bit is produced by one input data bit exclusive-or six registers which is used in IEEE standard 802.11a/g [34]. The output is alternately generated according to two generator polynomials:

$$g^{(0)} = (1011011) \text{ or } (91)_{10} \quad (2.2)$$

$$g^{(1)} = (1111001) \text{ or } (121)_{10} \quad (2.3)$$

The digit '1' in polynomials in binary format means that the value of register is involved in XOR calculation, and vice versa.

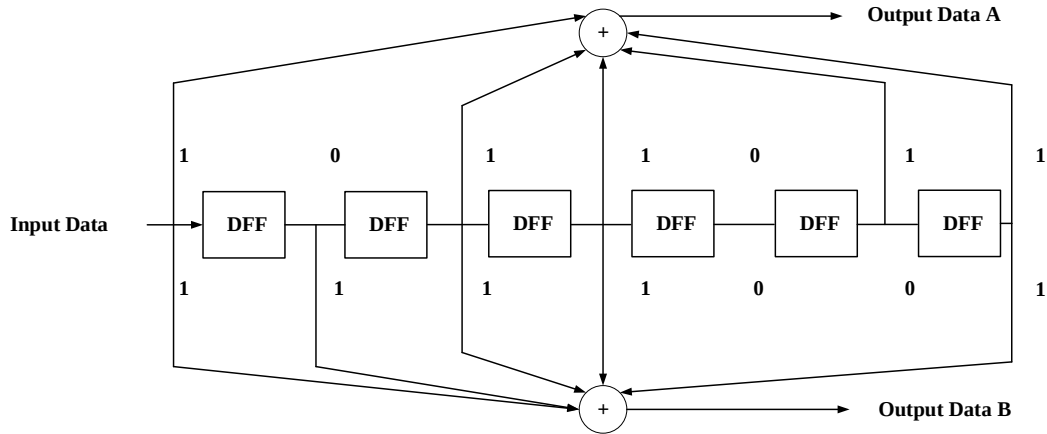


Figure 2.6 Convolutional encoder (2 , 1 , 7).

2.2.3 Modulator

The FIFO combines preamble data and encodes data into a sequence data and send them to the bit-stuffing block. Because the wideband signal using NRZI modulation will have no data transition when there have continuous identical digits (CID). The CID will affect the accuracy of the wide-band clock and data recovery (CDR) circuit. The None-Return-to-Zero Inverted (NRZI) block mechanism is shown in Figure 2.7. When the input bit is 0, NRZI block inverts the output. When the input is 1, NRZI block keeps the state. In order to increase the transition in transmitted data, the input data to NRZI should have more bit 0. The bit-stuffing method can constraint the max length of CID by inserting an extra data bit. Therefore, the bit-stuffing method is used to insert data bit “0” when the input data bits are continuous “1”s. As a result, the CID length of NRZI block output data will be limited to 2. Finally, the NRZI data will be directly transmitted to human body.

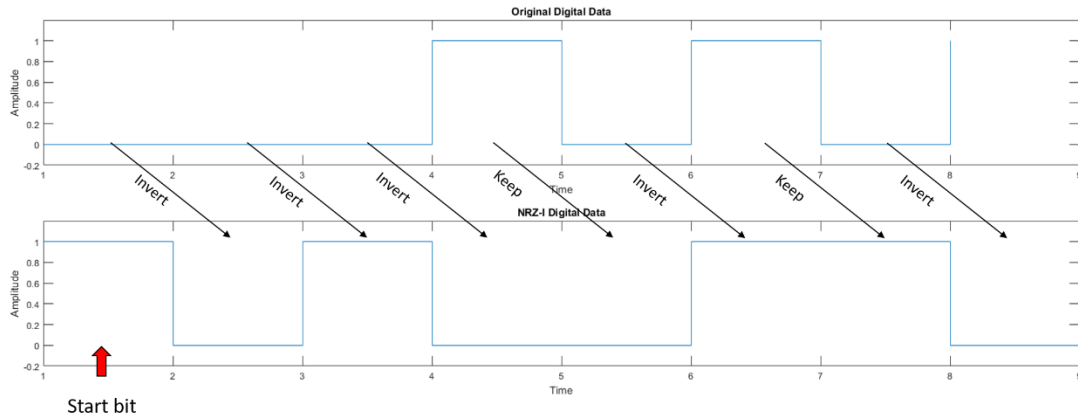


Figure 2.7 The mechanism of NRZI.

2.2.4 TX operating flow chart

Figure 2.8 shows the operating flow chart of the proposed BCC transceiver. In the beginning, the TX_INNER_RESET signal will reset the transmitter. Then, the preamble will be generated to the FIFO. The convolutional encoder encodes the LFSR random data or binary data in FPGA block memory depend on the TEST_MODE signal. After the data are encoded, the preamble and encoded data are transmitted in NRZI format. Because the latency of the decoded time of Viterbi decoder needs about 246 cycles, the transmitter waits for 250 cycles and then transmits the next packet.

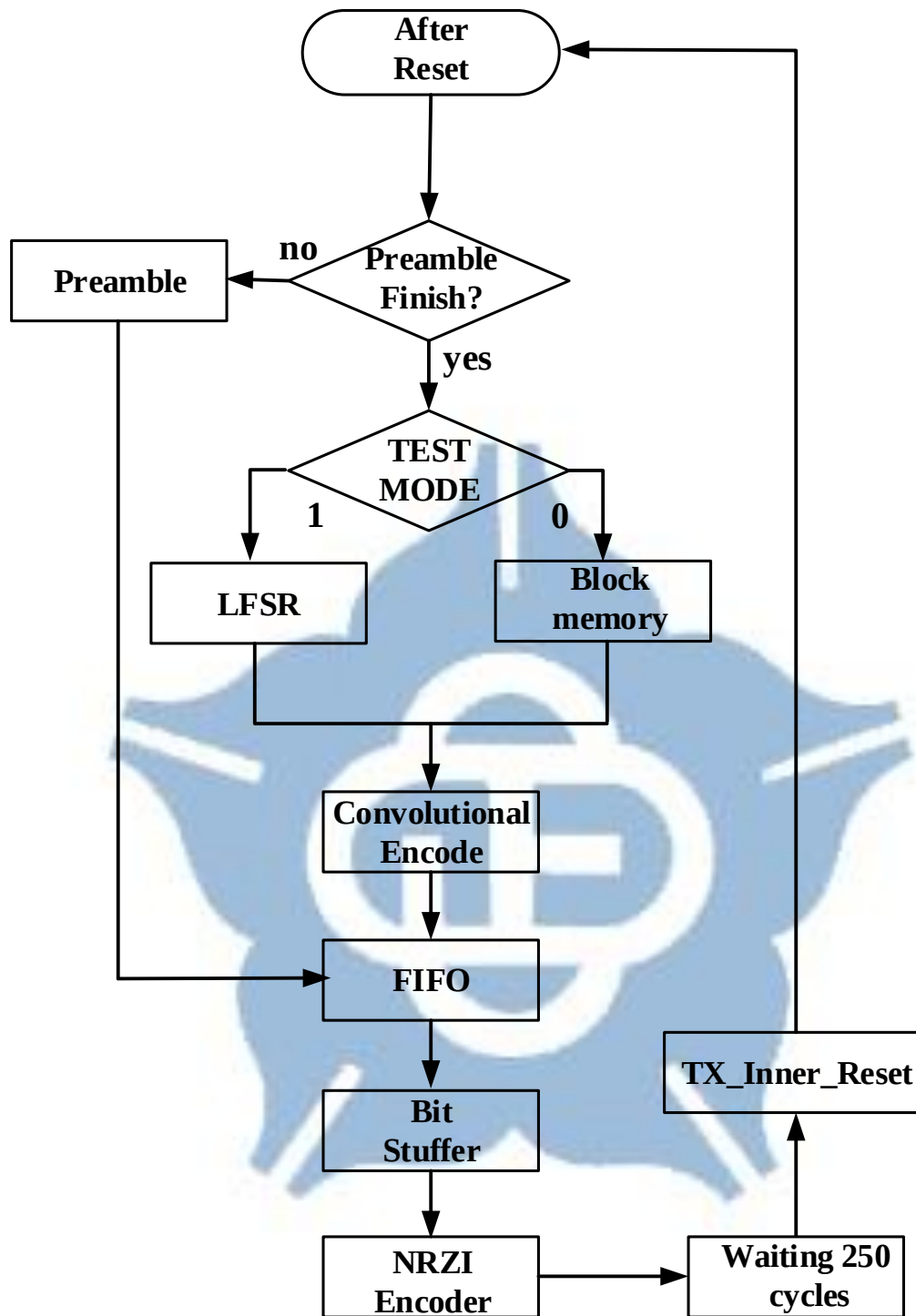


Figure 2.8 The operating flow chart of the proposed transmitter.

2.3 Wideband Signal BCC Receiver

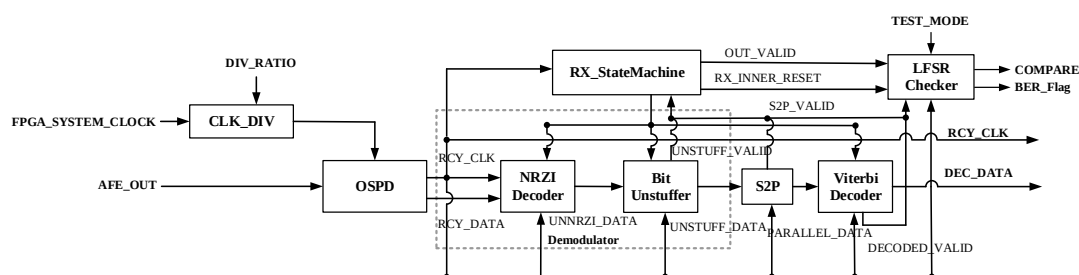


Figure 2.9 The block diagram of the proposed BCC receiver.

The block diagram of the proposed BCC receiver is shown in Figure 2.9. The AFE_OUT data is pre-amplified and triggered by an AFE board. According to AFE_OUT, the oversampling phase detector (OSPD) produces the recovery clock and the recovery data. NRZI decoder and Bit-Unstuffer are contained in the demodulator which demodulates RCY_DATA based on RCY_CLK to demodulated data. When the demodulated data is ready, the RX_StateMachine lets Viterbi decoder to decode the demodulated data to the decoded data. Last, if the TEST_MODE is high, the LFSR_Checker will compare the decoded data with the local random data patterns which is the same as the transmitter side. Any unmatched data will trigger the BER_Flag signal.

2.3.1 Oversampling Phase Detector

The block diagram of oversampling phase detector is shown in Figure 2.10. The FPGA system clock is divided by frequency divider. A sixteen phases clock generator uses the divided clock to generate sixteen phases. Based on sixteen phases, a RCY_CLK and RCY_DATA can be generated.

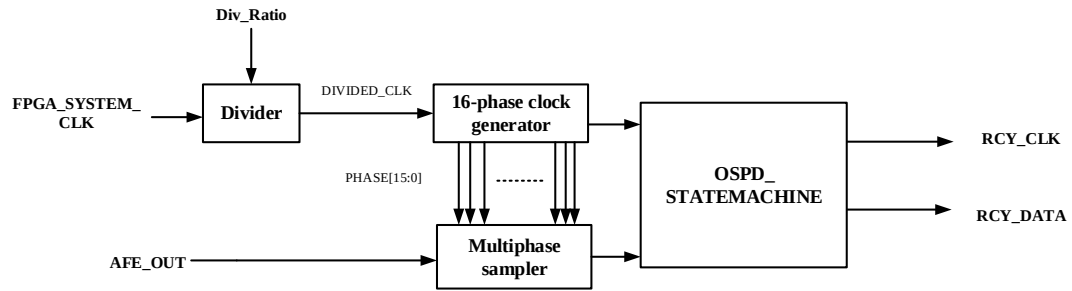


Figure 2.10 The block diagram of oversampling phase detection.

Figure 2.11 shows the timing diagram of the oversampling phase detection without phase error. The divided clock oversamples sixteen times at one input data symbol. In the meantime, sixteen phases is aligned to the sampling value. When the phase counter situation is equal to N, the OSPD state machine will compare the sampled value of phase (N-1) and the value of AFE_OUT. If the compared result is different, a data transition edge is detected. As the same time, the value of EDGE registers are refreshed to (N-1). The value in EDGE register retains the same when there are no phase error which is impacted by jitter noise.

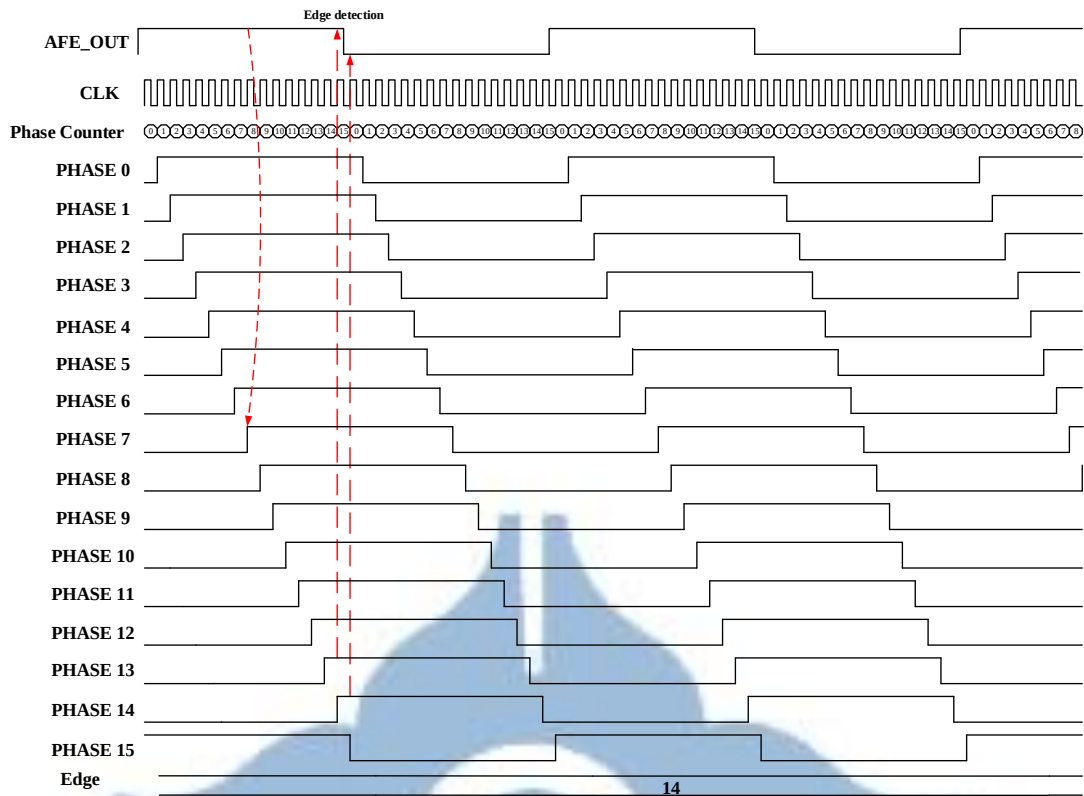


Figure 2.11 Timing diagram of the oversampling phase detector in no phase error case.

Figure 2.12 shows the timing diagram of the oversampling phase detector with phase error and have more than one consecutive identical digits situation. As aforementioned, a TRANSITION_EDGE signal is pulled high when a rising edge or a falling edge occurred. Then, the TRANSITION_EDGE_FLAG is pulled high for waiting a RCY_CLK is pulled high. The RCY_CLK will be pulled high when the difference between phase counter and EDGE is equal to eight while the TRANSITION_EDGE_FLAG is high. This step ensures any edge alternated to lead a RCY_CLK to be pulled high.

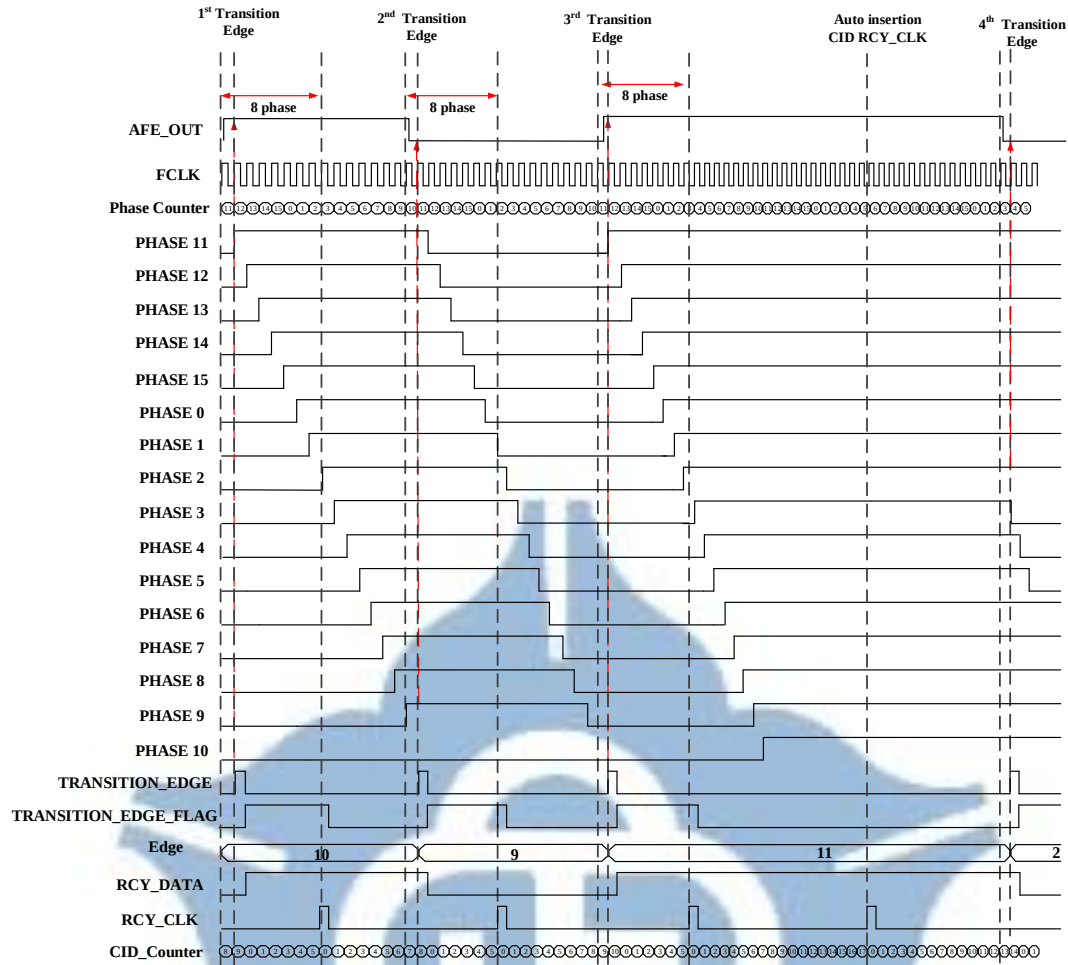


Figure 2.12 Timing diagram of OSPD generating RCY_CLK and RCY_DATA with phase error and CID situation.

The flow of the state machine is shown in Figure 2.13. For the 1st transition edge, the value of phase counter is 11. The exclusive-or of the AFE_OUT sampled by FCLK and the value sampled by the positive edge of the PHASE 10 is 1. Therefore, a data transition is detected. The value of EDGE is set to 10 ($N = 10$), and the TRANSITION_EDGE is pulled high. CID_COUNTER is set to 0 when the TRANSITION_EDGE is pulled high. Because the edge transition is occurred, the RCY_DATA will change the value to the sample value of phase 11($N+1$). An edge transition will lead the TRANSITION_EDGE_FLAG to be pulled high for waiting the absolute value of phase counter minus the value of EDGE is eight. For example, when

the Phase Counter equals to 2, the EDGE value (10) subtracts Phase Counter (2) is 8, and then, RCY_CLK is pulled high for one FCLK cycle and the CID_COUNTER is set to 0. When the RCY_CLK is high, the TRANSITION_EDGE_FLAG is pulled down. Otherwise, with the value of an internal CID counter being equal to seventeen, the RCY_CLK also be pulled high for one FCLK cycle when there are no data transition is occurred. When RCY_CLK is pulled high, the CID counter will be reinitialized as zero.

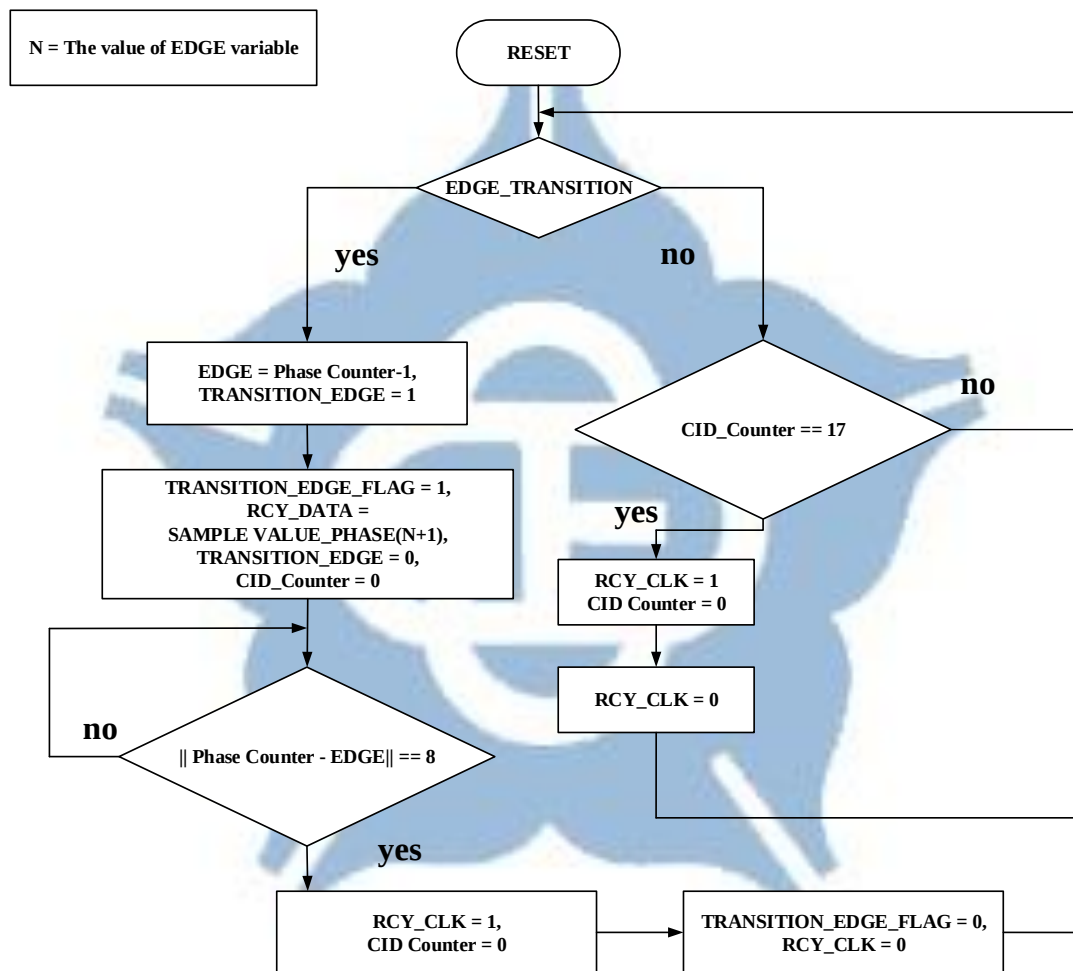


Figure 2.13 The operating flow chart of OSPD.

2.3.2 Demodulator

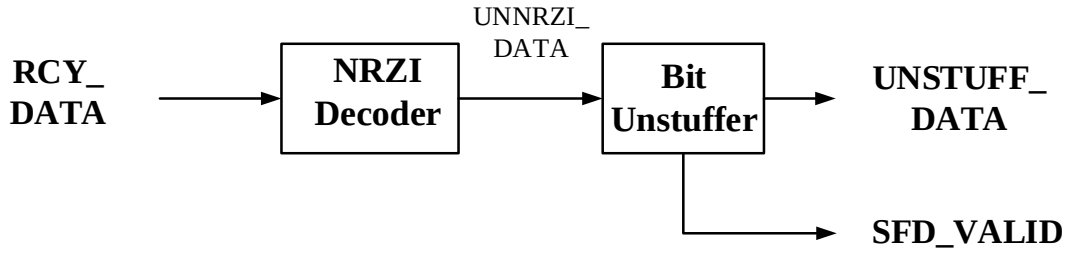


Figure 2.14 The block diagram of demodulator.

The block diagram of demodulator is shown in Figure 2.14. The demodulator contains a NRZI decoder which continuously decodes the RCY_DATA. If the bit-unstuffer detects the SFD sequence, the bit-stuffer will begin to remove the inserted data bits. When the redundant data bits are removed by the bit-unstuffer, the data bits are arranged to S2P block waiting for the Viterbi decoder to decode then.

2.3.3 Viterbi Decoder

The Viterbi decoder is generated by an auto Viterbi Decoder code generator from [30]. Figure 2.15 shows the GUI interface of Viterbi code generator. The parameter “Polys” means the decimal notation of convolution code generator polynomials. As mentation before, the binary notation of convolutional code in the proposed BCC transceiver is 1011011 and 1111001. Consequently, the parameter should be fulfilled 91 and 121. Other parameters can be adjusted to achieve higher performance of Viterbi decoder while the circuit area will increase.

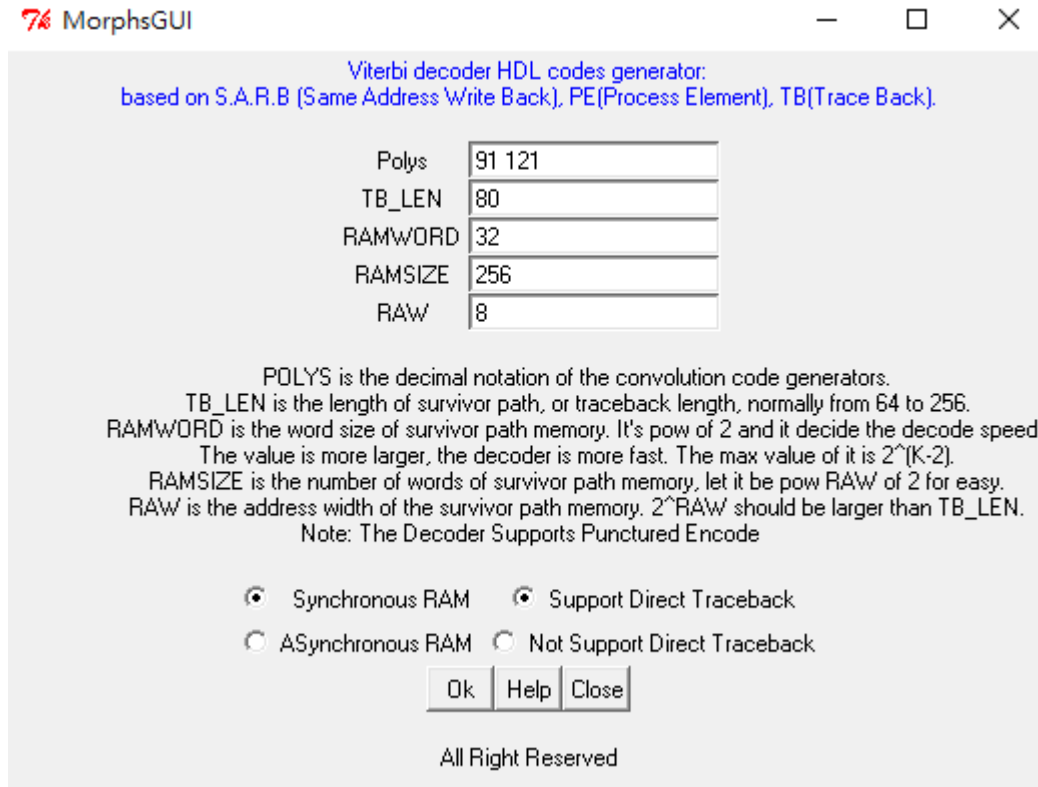


Figure 2.15 The GUI interface of Viterbi code generator.

Viterbi algorithm is used to find out a maximum likelihood sequence on the received data. The found out path in the trellis diagram is the most likely path in the trellis of the convolutional encoder. Moreover, the corrupted data can be correct by tracing back the path. An example of how the Viterbi decoder decodes the received data is shown in Figure 2.16. The example is based on the parameters (2, 1, 3) of convolutional codes. Then, the processes of decoding can be introduced more clearly with the block diagram of a basic Viterbi decoder.

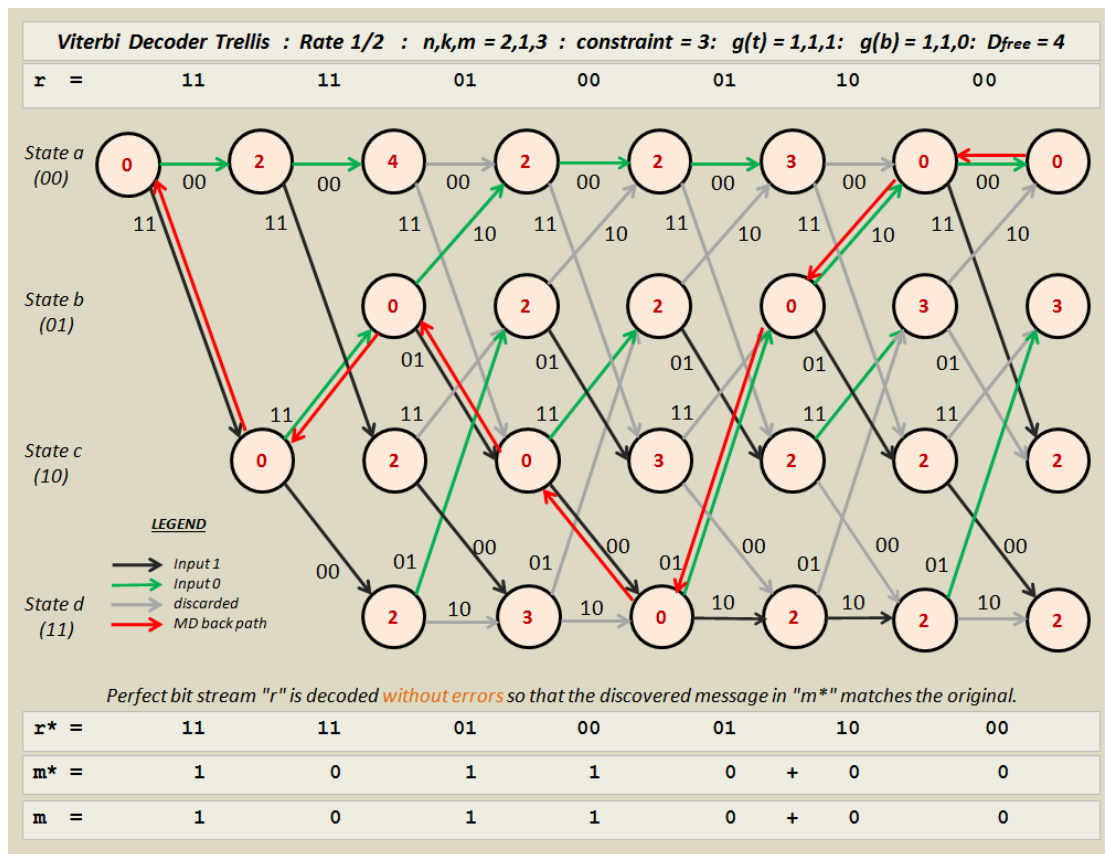


Figure 2.16 A trellis for Viterbi decoder with no error instance. [30]

First of all, the number of states is $4(2^2)$ owing to the number of registers is two. Hence, there are only two situations on each state, input data equals to 1 or input data equals to 0. At each state, the branch metric unit (BMU) is used to calculate the hamming distance of the received data and each possible path value that is restored in the path metrics unit (PMU). The value of accumulated error metric is recursively computed by an add-compare select unit (ACS) and the output decision is restored in the survivor metric unit (SMU). After tracing the final survivor path in SMU, the most likely path can be found and the correct data can be retrieved. The overall block diagram is shown in Figure 2.17.

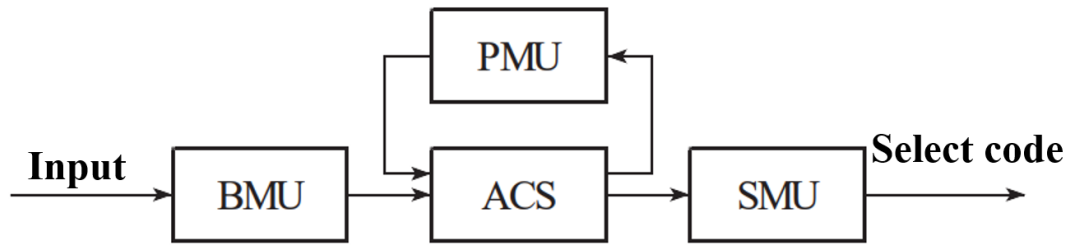


Figure 2.17 The block diagram of a basic Viterbi decoder.

2.3.4 RX operating flow chart

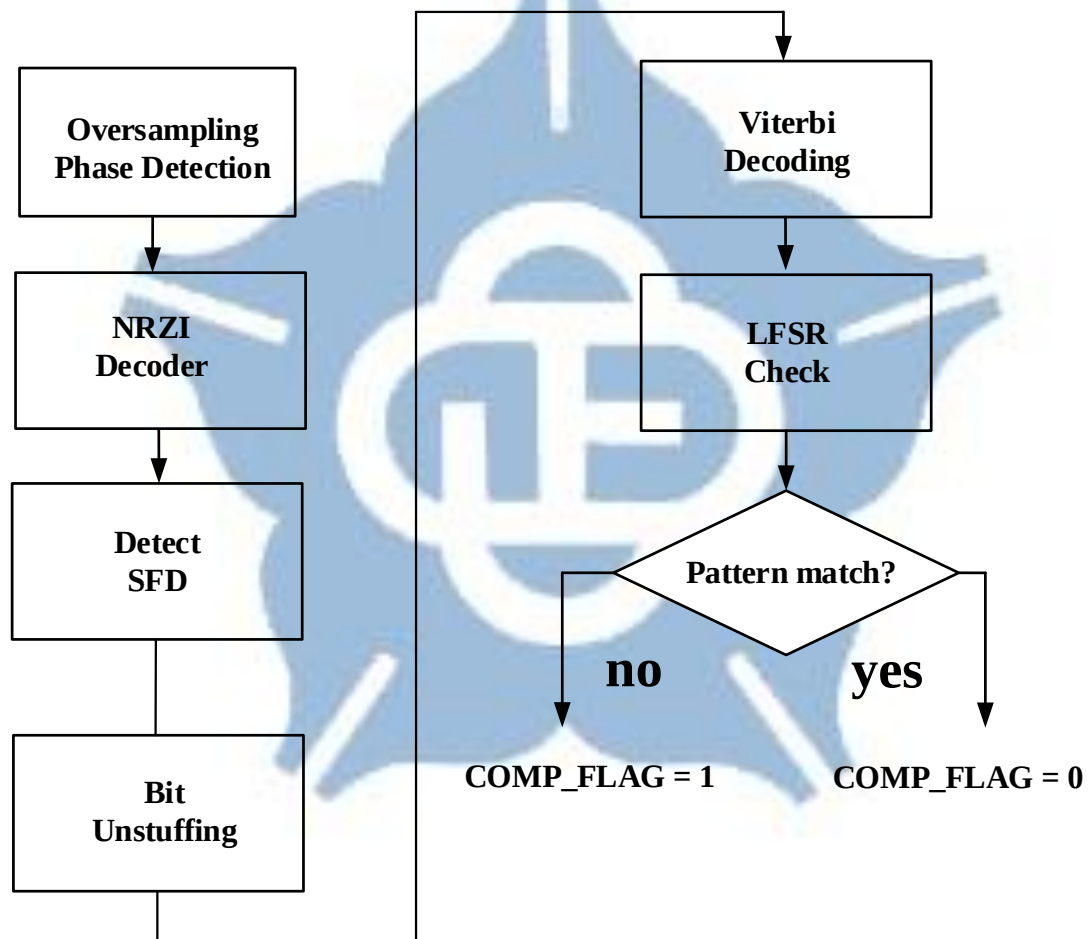


Figure 2.18 The operating flow chart of the proposed BCC receiver.

Figure 2.18 shows the flow chart of the proposed BCC receiver. In the first, the oversampling phase detector recovers data and clock. The NRZI decoder continuously demodulates the RCY_DATA. After detecting the SFD sequence, the un-bitstuffer

begins to remove the redundant data bits until the number of un-bitstuffing data bits are equal to 2000. Based on the un-bitstuffing data, the Viterbi decoder decodes data and sends the decoded data to LFSR checker for pattern matching. The RX_INNER_RESET is pulled high for soft resetting the Viterbi decoder when the number of compared data bits equals to 1000. If there are any mismatch data, the COMP_FLAG will be pulled high correspondingly.



Chapter 3 Experimental Results of Proposed BCC Transceiver

3.1 Jitter Model and Simulation Results

In order to verify the performance of the proposed transceiver, A jitter model which is similar to additive white Gaussian noise (AWGN) channel noise is built. The AWGN noise is a random noise in the nature and the time domain is almost likely in Figure 3.1. The values of jitter is generate by Matlab function is shown in Figure 3.2. At the transmitter side, the value of jitter/normalization is added on the transmitter clock in order to simulate a data jitter. In addition, the parameter for normalization can be controlled so as to generate different peak to peak data jitter.



Figure 3.1 the time domain of AWGN.

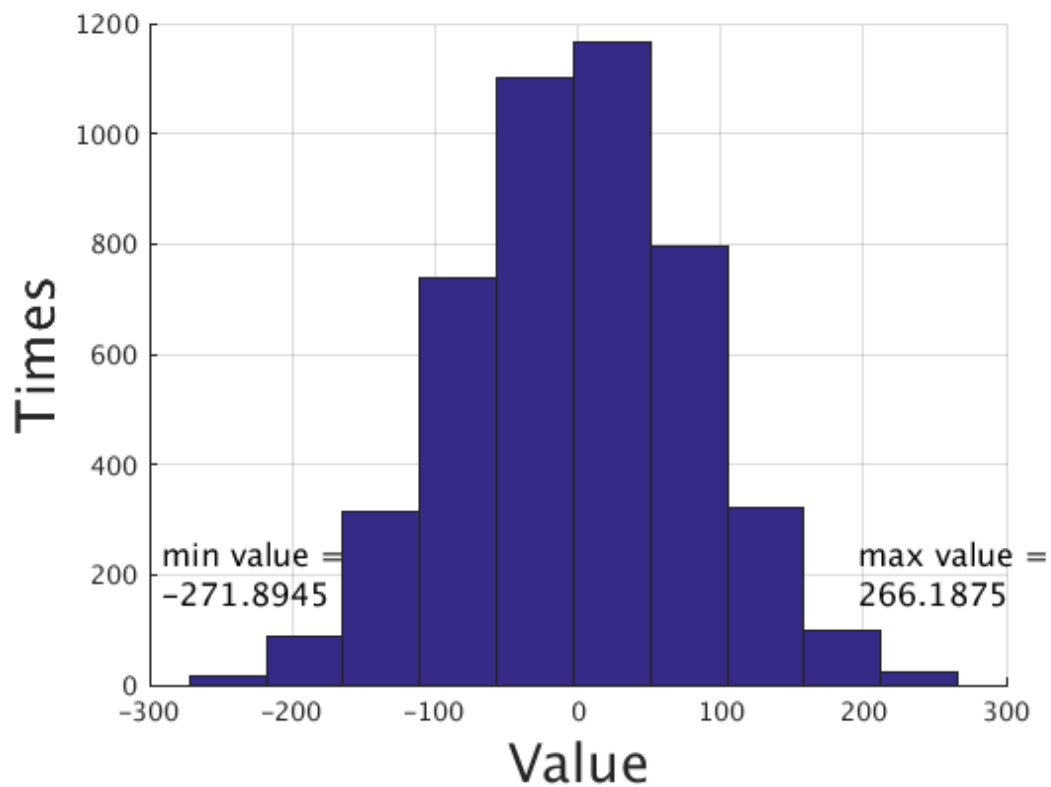


Figure 3.2 the normal distribution histogram of jitter model.

Figure 3.3 shows if the different constraint length of convolutional encoding method is applied to the proposed design which has CID equals two. The longer constraint length, the more data reliability the proposed design can achieve. The X axis means the amount of peak to peak data jitter added in simulation. The Y axis means that there are a first compared error occurred at the number of the received bits

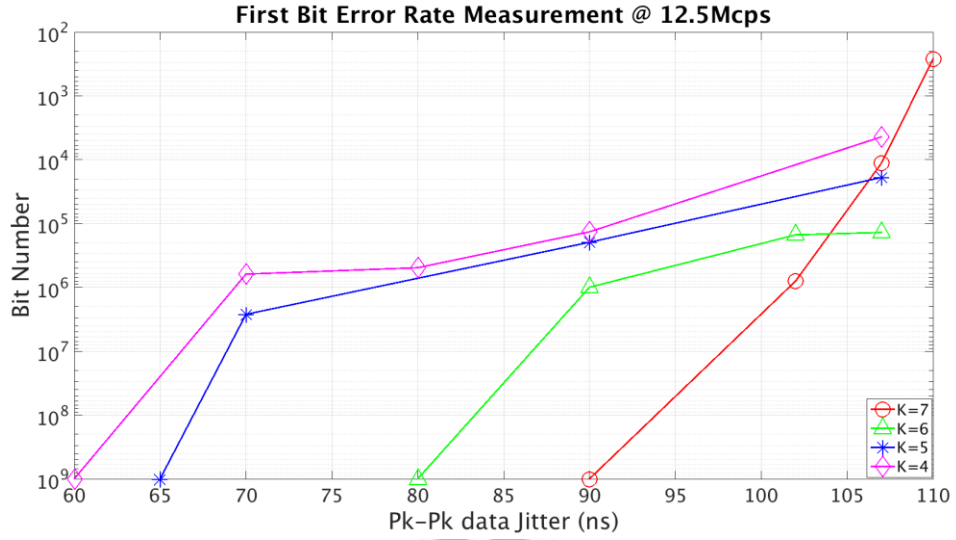


Figure 3.3 The proposed design with different constraint length with CID 2.

Figure 3.4 shows the performance of the proposed transceiver with oversampling phase detector but without using convolutional encoding method. The bigger number of CID means less data transition of transmitted data. If the consecutive identical digits are reduced, the OSPD CDR has better BER performance at the same Pk-Pk jitter.

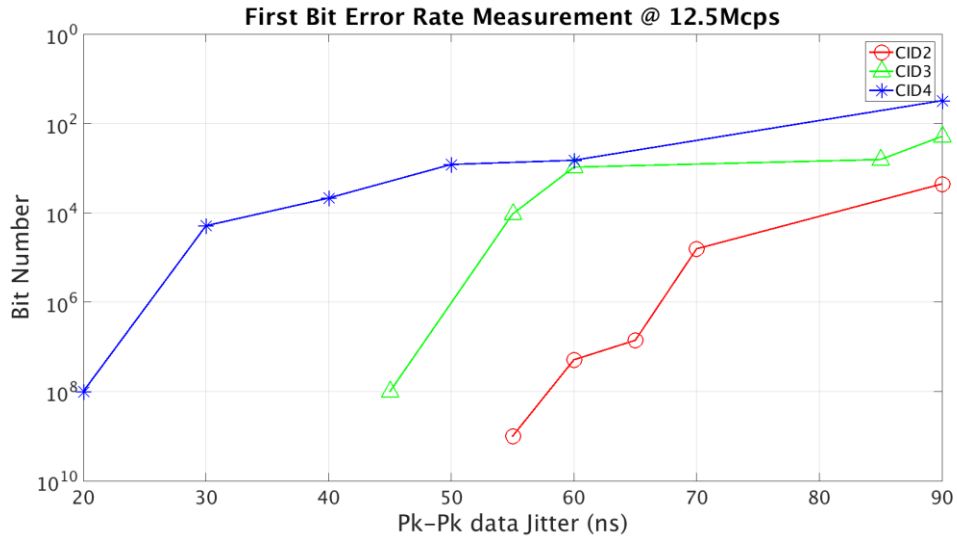


Figure 3.4 Performance of the proposed transceiver using OSPD without using convolutional encode method.

Figure 3.5 shows the first bit error rate (BER) simulation in different architectures.

The pink line means the simulation result in the architecture using Walsh codes method(code rate = 1/8) [29]. The CDR in [29] uses a sampler and a vote integrator to recovery clock and data. The red line used the CDR [29], and the vote integrator with some modifications and adding the convolutional encoding method. It can achieve better BER performance than the original design in [29]. The green line uses the proposed OSPD CDR without convolutional code and the blue line uses the proposed OSPD with the convolutional encoding method. The bottleneck of the BER performance can be observed in the figure. The BCC BER performance can be improved by means of adding convolutional encoding method. There are no error bits occurred with the peak to peak data jitter smaller than 90ns in blue line at 12.5 Mcps.

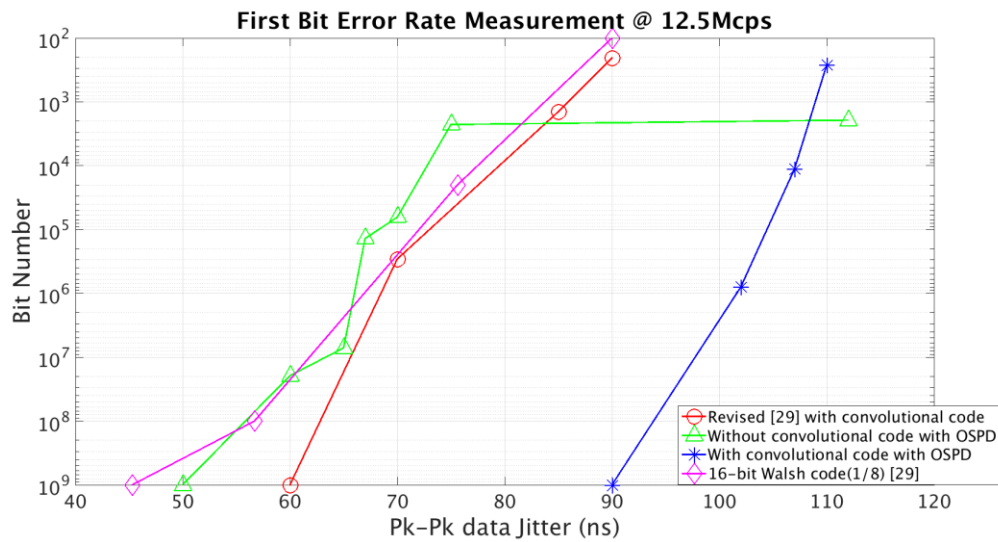


Figure 3.5 First BER simulation in different architectures.

Figure 3.6 and Figure 3.7 shows the power spectrum density (PSD) of the proposed transmitter output with regular and random data patterns at 6.25 Mbps. In consequence of using NRZI format to transmit data, there are various frequency scattered in PSD. Thus, the transmitted data are robust to against the specific interferences.

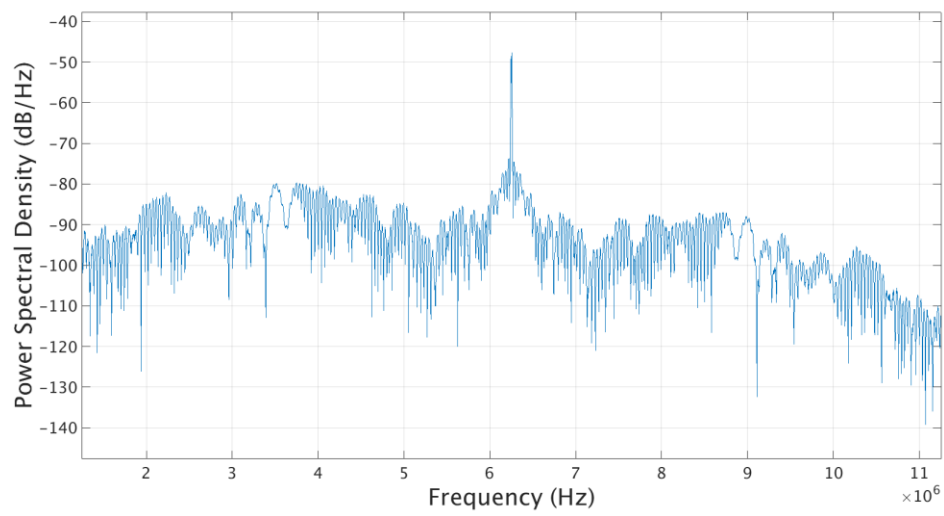


Figure 3.6 Power spectral density (PSD) with regular data patterns.

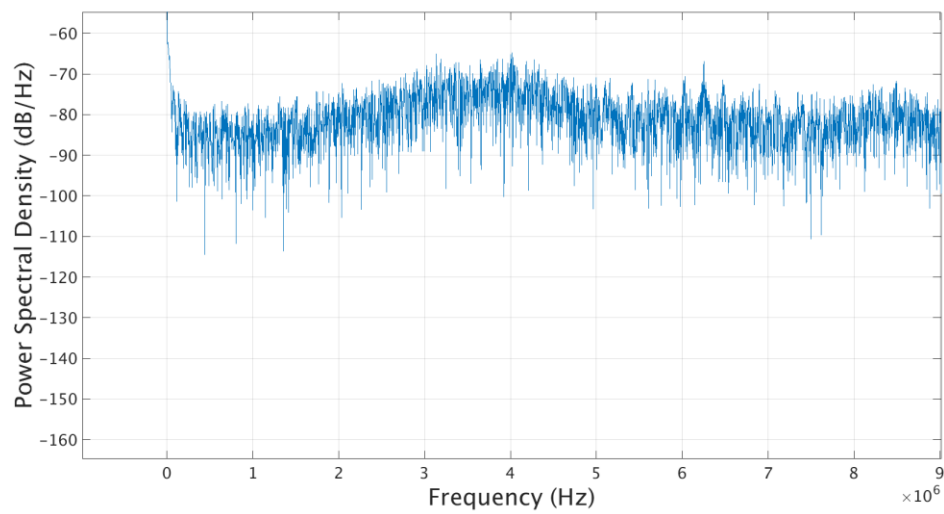


Figure 3.7 Power spectral density (PSD) with random data patterns.

3.2 Information of Artix-7 Evaluation

Board

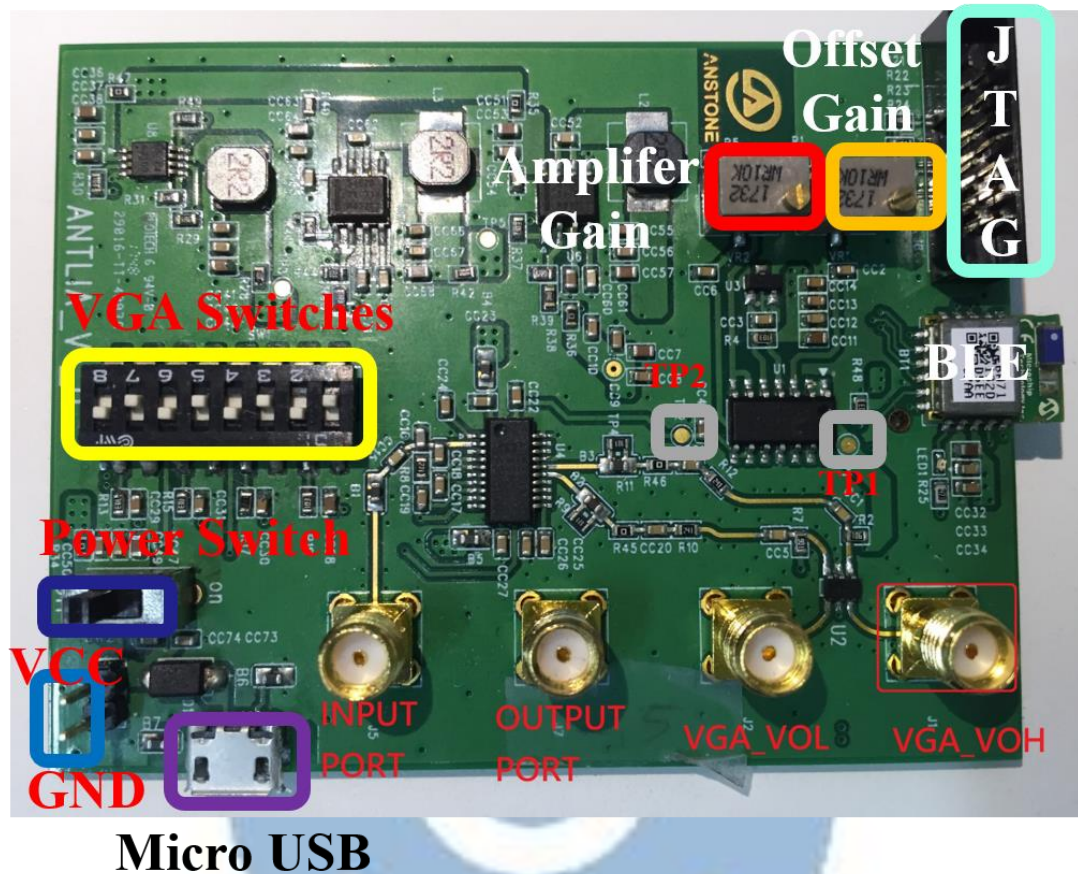


Figure 3.8 Overview of the FPGA Artix-7 board.

The overview of the FPGA board is shown in Figure 3.8. The power of the FPGA can be supplied by a 9V battery or a micro USB cable. The control voltage for amplifier gain control can be measured from TP2 and the DC level of the Schmitt trigger can be measured from TP1 with a multimeter. The VGA switches are used to control the function of the VGA and listed in Table 3.1. The option of the switches of 1 to 8 is set to “01010101”. The FPGA pin assignment table is shown in Table 3.2. Figure 3.9 shows the SMA cables and electrodes used in the BCC measurement.

Table 3.1 Function switch of VGA.

[1,2]	Function
00	Floating
01	Function VGA opened
10	Function VGA closed
11	Function VGA closed
[3,4]	Function
00	Floating
01	Function LNA opened
10	Function LNA closed
11	Function LNA closed
[5,6]	Function
00	Floating
01	LNA high gain mode
10	LNA low gain mode
11	LNA low gain mode
[7,8]	Function
00	Floating
01	Gain slope opened
10	Gain slope closed
11	Gain slope closed

Table 3.2 FPGA pin assignment table.

Net name	FPGA pin	Description
VGA_VOL_FPGA	V13	VGA amplifies signal and output positively.
VGA_VOH_FPGA	V12	VGA amplifies signal and output negatively.
FPGA_VGA_OUT	B14	FPGA IO pin
BT_P0_0	V9	Bluetooth pin00
BT_P1_2	U9	Bluetooth pin12
BT_P1_3	U12	Bluetooth pin13
BT_P1_6	T12	Bluetooth pin16
BT_P1_7	V14	Bluetooth pin17
BT_P2_0	U14	Bluetooth pin20
BT_P2_7	V17	Bluetooth pin27
BT_P3_6	V16	Bluetooth pin37
BT_RESET_N	U17	RESET_N for Bluetooth
BT_TX_FPGA_RX	T17	Bluetooth UART transmit pin
BT_TX_FPGA_RXT	U10	Bluetooth UART receive pin
FPGA_CLK_100MHz	P14	FPGA master clock

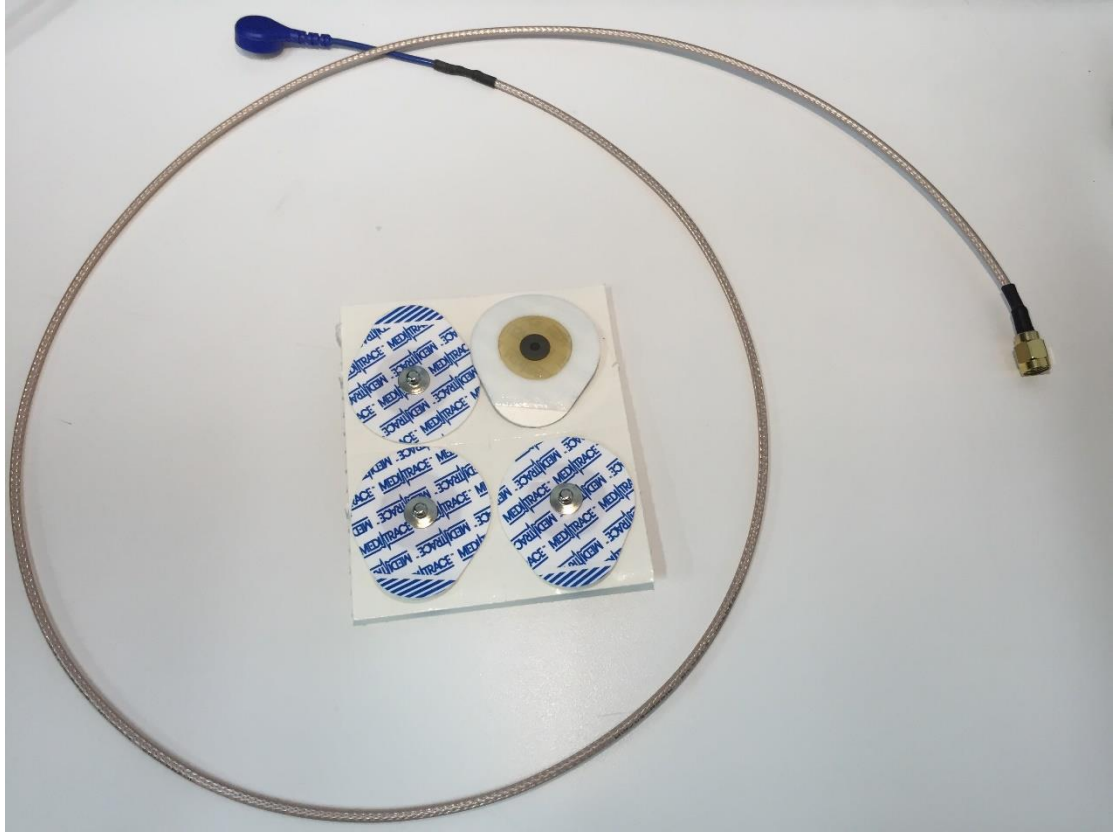


Figure 3.9 SMA cable and electrodes.

3.3 Setup a BCC transceiver verification environment

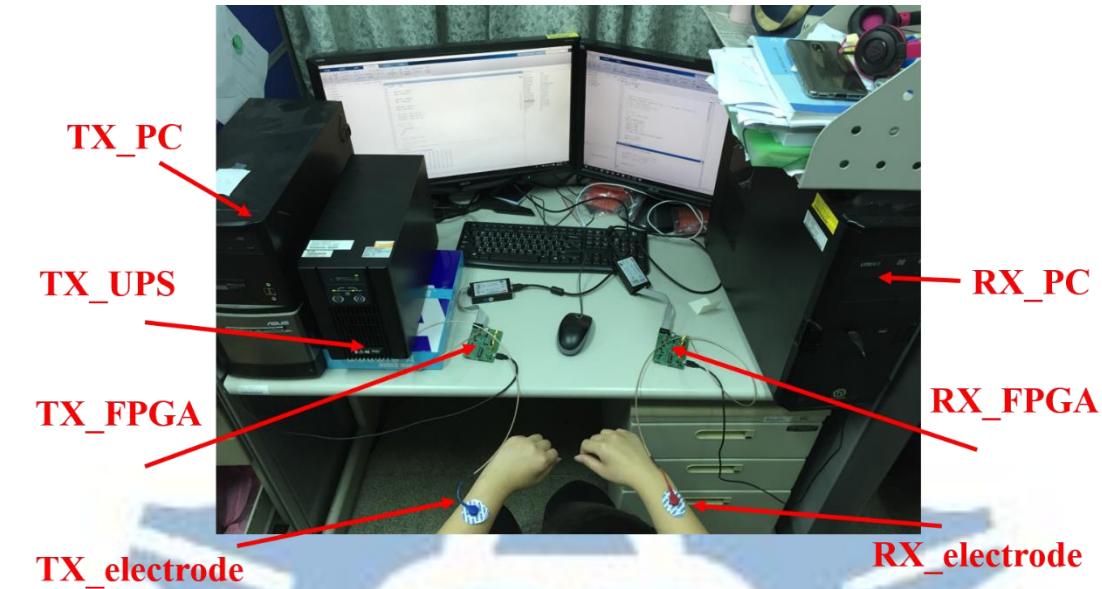


Figure 3.10 The verification environment of the proposed BCC transceiver.

Figure 3.10 shows the verification environment of the proposed BCC transceiver. In the transmitter side, the TX FPGA and TX PC are supplied by an Uninterruptible Power System (UPS). The RX FPGA and RX PC are supplied directly by power outlet. This step makes sure that the grounds of TX and RX are coupled. Because there are not enough control I/O pins on FPGA board, a virtual input / output (VIO) IP is used in FPGA and a JTAG cable connects PC and FPGA. After that, the TX FPGA transmits data through a SMA cable and an electrode to the human body. The discussion for different types of electrodes can be found in [32]. The RX PC can probe RX FPGA signals by using an integrated logic analyzer (ILA) IP integrated on RX FPGA which is illustrated in Figure 3.11.

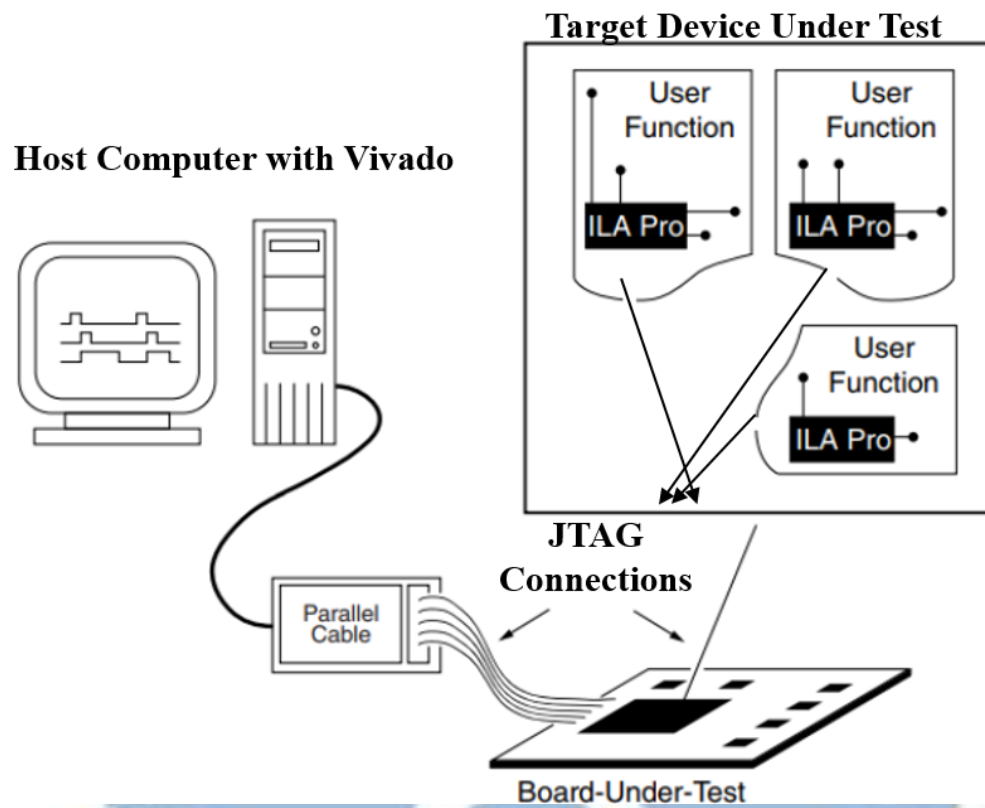


Figure 3.11 Debug IP core of ILA system block diagram [33]

3.4 Experimental Result

Figure 3.12, 3.13, and 3.14 show the number of transmitted packets by the proposed BCC transceiver and there are no error occurred at 6.25 Mcps, 3.125 Mcps, 1.56 Mcps after 10^8 random bits received. Table 3.3 shows the used resources of the proposed BCC transceiver on FPGA.

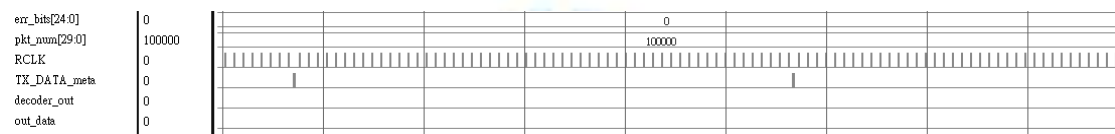


Figure 3.12 Number of received packets and error bits at 6.25 Mcps.

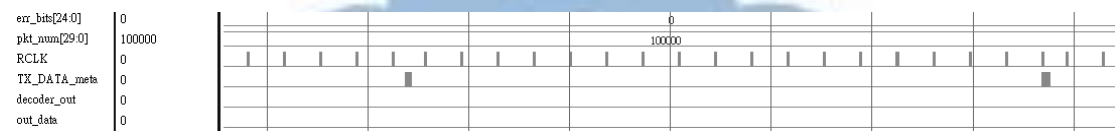


Figure 3.13 Number of received packets and error bits at 3.125 Mcps.

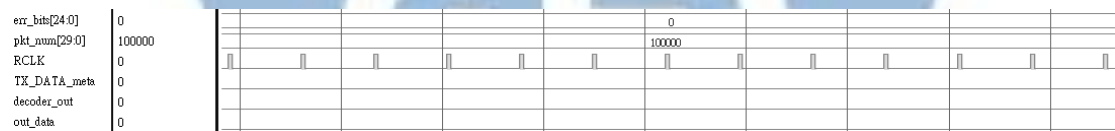


Figure 3.14 Number of received packets and error bits at 1.56 Mcps.

Table 3.3 Utilization of the proposed BCC transceiver.

Slice Logic Utilization	Used	Available	Utilization
BCC Transmitter			
Number of Slice Registers	2934	20800	14.11%
Number of Slice LUTs	1320	10400	12.69%
Number of Occupied Slices	816	8150	10%
Number used as Memory	0	9600	0%
BCC Receiver			

Number of Slice Registers	3715	20800	17.86%
Number of Slice LUTs	3952	10400	38%
Number of Occupied Slices	1182	8150	15h%
Number used as Memory	0	9600	0%



3.5 Summary

Table 3.4 Summary of proposed BCC transceiver.

Data rate	780 Kbps ~ 3.125 Mbps
Chip rate	1.56 Mcps ~ 6.25 Mcps
Transmission Distance	10 ~ 140 cm
Core Voltage	1.0 V (for FPGA)
Power Consumption	77 mW(TX) 81 mW(RX) 0.486W(AFE circuit)
Sensitivity	-18.87 dBm
BER	No bit error @ transmitting 10^8 bits
Energy/bit	50.56 nJ/b(without AFE circuit)

Table 3.4 shows the summary of the proposed BCC transceiver using convolutional encoding method and oversampling phase detection CDR. The range of the data rate is from 780 Kbps to 3.125 Mbps. There are no error bits after receiving and decoding over 10^8 bits. The maximum signal transmission distance is 140 cm. The core voltage of Artix-7 FPGA is 1.0V. The sensitivity of the BCC receiver which is determined by the VGA circuit is -18.87 dBm.

Table 3.5 Comparison table.

	[35] VLSI-DAT'16	[28] JSSC'07	[20] JSSC'09	[25] ISSCC'14	[24] VLSI-DAT'15	[8] JSSC'17	Proposed
Process	90 nm	0.25 μm	0.18 μm	65 nm	90 nm	65 nm	FPGA
Supply	1.0 V	1.0 V	1.0 V	1.1 V	1.1 V	1.1 V	1.0 V
Data Rate	1Mbps ~ 40Mbps	2 Mbps	60 kbps ~ 10 Mbps	60 Mbps	29.1 Mbps	1 Mbps	780 Kbps ~ 3.125 Mbps
Modulation	Wideband Signaling	Wideband Signaling	Adaptive Frequency Hopping FSK	3-level Walsh Code	16-QAM OFDM	64 P- OFDM+ Mini. FSK DEM	Wideband Signaling
Sensitivity	-29 dBm	-36 dBm	-65 dBm	-58 dBm	N/A	-78 dBm	-18.87 dBm
Power Consumption	1.21 mW (w/o AFE circuit)	5 mW	3.7 mW	1.85 mW	9.37 mW	1.4mW	158 mW (w/o AFE circuit)
Area	0.14 mm ²	0.85 mm ²	2.30 mm ²	0.072 mm ²	5.2 mm ²	2.13 mm ²	N/A
BER	$< 10^{-8}$ @ 40Mbps	1.1×10^{-7}	10^{-5} (10 Mbps) $< 10^{-9}$ (60 kbps)	10^{-5} @ 60 Mbps	N/A	$< 10^{-7}$	$< 10^{-8}$ @ 3.125 Mbps
Energy/bit	0.03nJ/b	2.5 nJ/b	0.37 nJ/b	31 pJ/b	0.22 nJ/b	1.4 nJ/b	50.56 nJ/b (without AFE circuit)

Chapter 4 Conclusion and Future Works

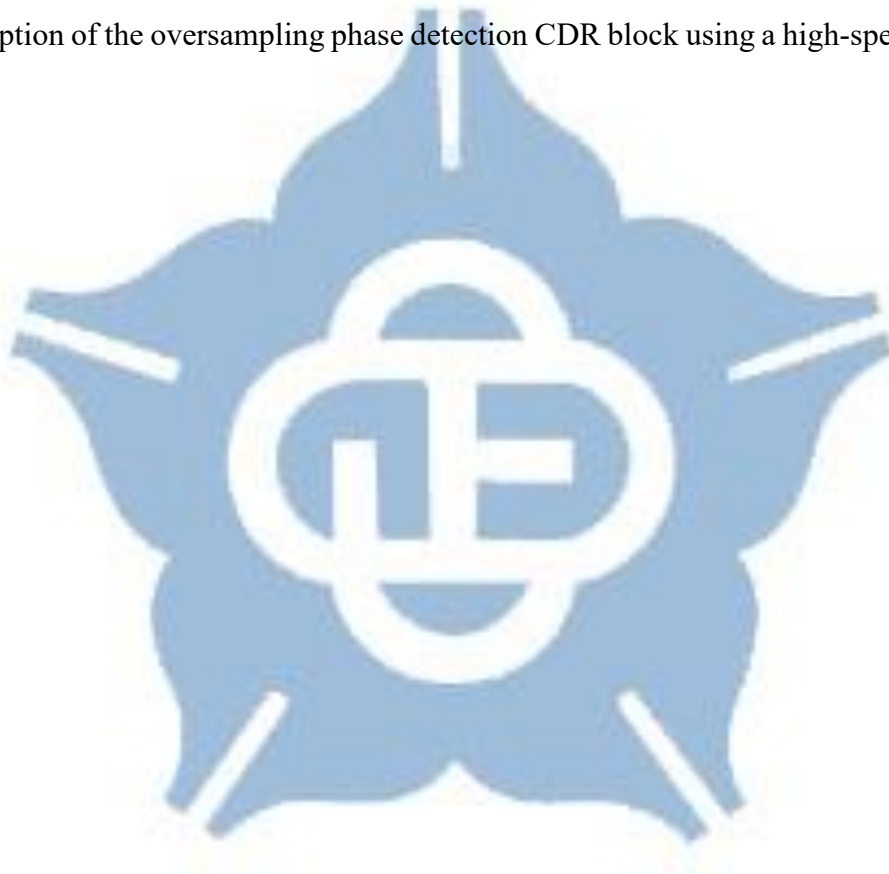
4.1 Conclusion

After understanding the human body channel characteristics, a wideband signal BCC transceiver using convolutional encoding method is proposed and implemented on an Artix-7 evaluation FPGA board. The FPGA board contains an analog front-end (AFE) circuit to amplify the attenuated signal and recovers it to digital waveforms. In the transmitter side, the pattern generator can provide the random pattern or the multimedia image data. With the purpose of enhancing data reliability, the data will be encoded by encoded parameters (2, 1, 7) of convolutional encoding method. It means the encoder output two data bits when there are one input data bit. After that, encoded data are stuffed by the bit stuffer to restrict the CID to 2 and then be modulated to the NRZI format. Furthermore, each transmitted data will be converted into packet format. In the receiver side, the oversampling phase detection CDR recovers data and clock based on the output from AFE board. The Viterbi decoder decodes the demodulated data to the decoded data and then sends to LFSR checker to check bit errors. In the multimedia image mode, the picture will be sent to the RX PC.

The proposed BCC transceiver achieves a data rate ranging from 780 Kbps to 3.125 Mbps that there is no error bits occurred. Therefore, the BER is less than 10^{-8} at 3.125 Mbps (6.25 Mcps).

4.2 Future Works

In this thesis, a stable oscillators is used in FPGA, if the proposed BCC transceiver transfers to ASICs, an on-chip oscillator will be used. Therefore, there needs a frequency tracking ability on the CDR circuit with the preamble sequence to calibrate the frequency error of the on-chip oscillator. Moreover, a DLL-based phase generator can be used to generate multiphase clock to the CDR. It can much decrease the power consumption of the oversampling phase detection CDR block using a high-speed clock.



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