國 立 中 正 大 學

資訊工程研究所碩士論文

使用華氏碼並建構於可程式邏輯板之人體通道傳輸收發器

An FPGA-based Transceiver for Human Body Channel Communication using Walsh Codes

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研究生 張茹華 所提之論文

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經本委員會審查，符合 碩 士學位論文標準。

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摘要

在人口老化及現代科技的發展之下，可攜式醫療電子設備及可隨身佩戴、隨時測量的電子裝置越來越多。這類型的裝置大多是使用無線的方式進行傳輸，像是常見的藍芽傳輸、ZigBee。但是這些技術有很高的耗電量以及因為很多裝置也使用相同頻帶造成嚴重的干擾的問題。因此，以人體通道作為傳輸媒介的技術被提出。人體通道傳輸可以避免干擾的問題、能提供較穩定的傳輸，同時其功率消耗比較低。因為以上的優點，我們提出一個以人體通道傳輸的傳收器。

Virtex-7 VC707 evaluation board (EVB) 板是一張具有穩定且高速工作頻率的 EVB 板，我們把人體通道傳收器建構於其上並且以華氏碼作為調變碼。華氏碼具有正交特性，所以可以容忍低於一半華氏碼長度的錯誤位元資料能被正確解調。除此之外，我們選取長度為 2 的 continuous identical digits (CID)華氏碼避免過長的 CID 出現造成接收端難以回復訊號。在 bit error rate (BER)量測中，以 140 公分傳輸距離傳送 10^8 個位元資料時，在 488 Kbps (3.12 Mcps), 976 Kbps (6.25 Mcps), 以及 1.95 Mbps (12.5 Mcps) 上並沒有任何錯誤資料發生。在 3.9 Mbps (12.5 Mcps) 的傳輸率下，BER 達到 10^{-5}。

在本研究提出的人體通道傳輸收發器，基於傳輸穩定度的提高，我們也提供直接傳輸多媒體資料的模式，在電腦上把圖片分解經由 universal asynchronous receiver/transmitter (UART) 介面送到傳送器，經由最長為 140 公分、1.95 Mbps 的速度傳到人體通道後，能正確地把它接收回，最後可以重建回原來完整的圖片。

關鍵字:人體通道傳輸、人體通道特性、可程式邏輯板、通用非同步收發傳輸器、華氏碼

Abstract

In recent years, the portable healthcare devices are more and more popular. The wireless transmissions are widely used in these devices, such as Bluetooth and ZigBee. However, these techniques have drawbacks of high power consumption and have interferences in the shared frequency band, Therefore, body channel communication (BCC) is proposed because it has relatively low power consumption and has less interferences.

The proposed BCC transceiver which using Walsh codes as modulated codes is implemented on the Vurtex-7 VC707 evaluation board (EVB). The Walsh codes are orthogonal codes and the maximum number of error bits that can be tolerated can be up to half of the code's length. Moreover, the CID of the Walsh codes are limited to 2 to avoid the no data transition situation which makes the receiver difficulty to recover the clock and data. There are no error bits occurred when transmitting 10^8 bits at 140 cm distance and at data rate of 488 Kbps (3.12 Mcps), 976 Kbps (6.25 Mcps), and 1.95 Mbps (12.5 Mcps). Moreover, the BER is 10^{-5} at 3.9 Mbps (12.5 Mcps).

In the proposed BCC transceiver, because of high data reliability, the multi-media transmission is supported. The image can be completely transmitted and received through 140 cm distance and the maximum data rate is 1.95 Mbps.

Keywords : BCC, FPGA, UART, Human Body Channel Characteristics, Walsh codes

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Chapter 1 Introduction

1.1 Introduction of Body Channel Communication

Recently, healthcare devices and consumer electronics are more and more popular. For some reasons, wireless body area network (WBAN) is usually utilized to be implemented above applications. In wireless communication, Bluetooth, ZigBee, and Radio Frequency Identification (RFID) are well-known techniques. In past, Bluetooth is a wireless technology that used in short distance communication. However, the Bluetooth has relatively large power consumption. To overcome power problem, Bluetooth 5.0 supports low energy version, Bluetooth low energy (BLW). ZigBee is a low power wireless personal area network (WPAN). It aims to simpler, less expensive, and more convenient than other WPANs. RFID can identify electromagnetic when attaches objects and has the low frequency (LF), the high frequency (HF), the ultra high frequency (UHF), and the microwave. LF and HF RFID has widely use in everybody's live, such as animal identification, library management, smart card, and so on. However, both operating frequency of LF and HF are low which are 9-135 KHz and 13.56 MHz, respectively. Even though RFID has higher operating frequency than HF, they are difficult to be implemented or have interference. In above depictions, low data rate, large power consumption are problems on wireless communication. Moreover, body shadowing causes that RF transmission has interferences in the environment. [1]. Body channel communication (BCC) utilizes human body as a communication medium to

transmit data. The BCC technology can overcome problems of wireless communication.

In BCC, a human body is used as the communication medium when transmitting data between a transmitter and a receiver. The electrode couples transmitter and human body instead of the antenna. The signal passes through the human body to another electrode that is connected to the receiver. Then, the receiver receives the signal from the electrode. This coupling method of human body has called galvanic coupling. Another, the floating electrodes are coupled to the ground through the air and creating a return path. In the other word, signal electrodes contacting with the skin create the forward path of the signal [2]. The external path is called capacitive coupling. Figure 1.1 shows the diagram of two coupling path. For a galvanic coupling, the transceiver can work on short transmission distance which is shorter than 15 cm and works on a low frequency which is lower than 1 MHz. These two coupling paths make the reason of a higher gain and a higher frequency range from 1 MHz to 100MHz. The characterization is only existing on the BCC transceiver.

In summary, body channel communication transmits data signal through a human body. It has characterizations of a high data rate and lower power consumption. That is why more and more researches use BCC to design transceiver instead of other wireless communications. The following section will introduce modulation method implemented on prior BCC transceivers.

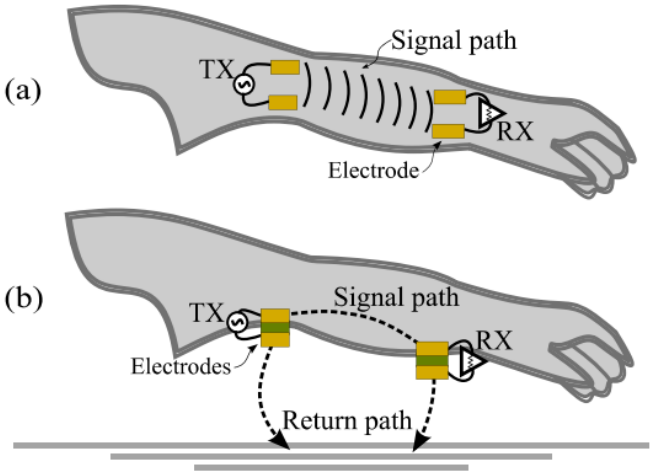


Figure 1.1 HBC coupling methods. (a) Galvanic (b) Capacitive [3]

1.2 Modulation of Body Channel Communication Transceiver

Modulation is a technique for correctly transmitting data and efficient frequency utilization. The following section will introduce some modulations widely used in BCC.

1.2.1 Modulation: Wide-Band Signaling (WBS)

A wideband system means that transferred signal bandwidth exceeds the coherence bandwidth of the channel. A transceiver [3] is shown in Figure 1.2 which consist of a BCC transmitter, a human body channel, an analog front-end (AFE) printed circuit board (PCB), and a BCC receiver. The AFE PCB includes a variable gain amplifier (VGA) and a Schmitt trigger in order to recover the attenuated signal. The transmitter is composed of a spread spectrum clock generator (SSCG) [4], a preamble generator, a non-return-to-zero-inverted (NRZI) encoder with the bit-stuffing control. The SSCG circuit generates the spread spectrum clock signal to trigger the transmitter for electromagnetic interference (EMI) reduction. A preamble generator generates preamble bits and the start frame delimiter (SFD) for synchronization. The output data of the transmitter are encoded by a NRZI encoder and transmitted to the human body channel. Jitter accumulation and duty-cycle distortion happen when the signal transmits through a human body. This situation increases the difficulty in recovering data in the receiver part. The bit stuffer in the transmitter is used to create enough data transitions after NRZI encoding.

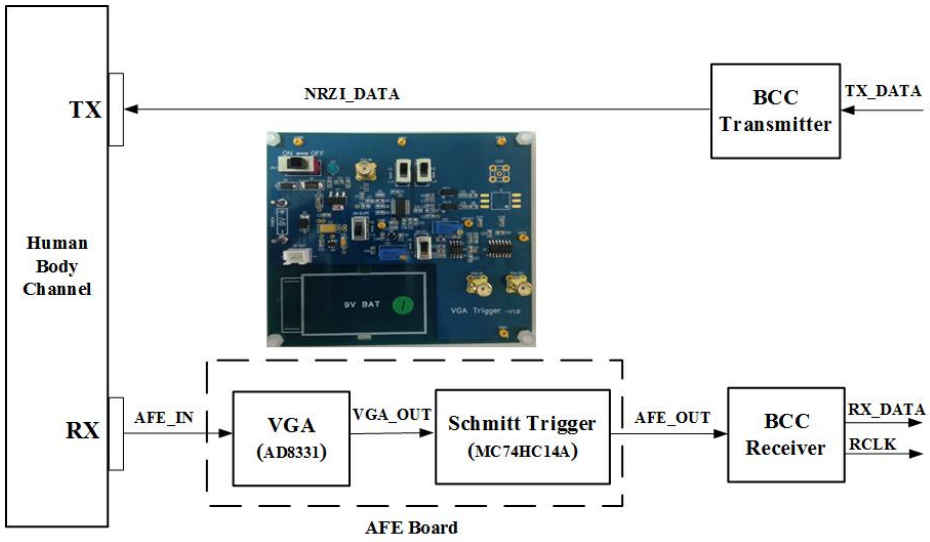


Figure 1.2 BCC transceiver architecture [3]

Figure 1.3 shows the architecture of the receiver [3]. The WBS BCC receiver is composed of an AFE PCB and an all-digital clock and data recovery (CDR) circuit. The AFE PCB recovers received wideband pulse signals from the human body channel back to the digital waveforms. In the receiver, a 7X oversampling sampler and a vote integrator recovers the AFE_OUT to the data (RX_DATA) and the clock signal (RCLK). Subsequently, a bit unstuffer and a NRZI decoder decode the RX_DATA to the original data. The operating frequency is 280 MHz. The data rate of this transmitter ranges from 1 Mbps to 40 Mbps.

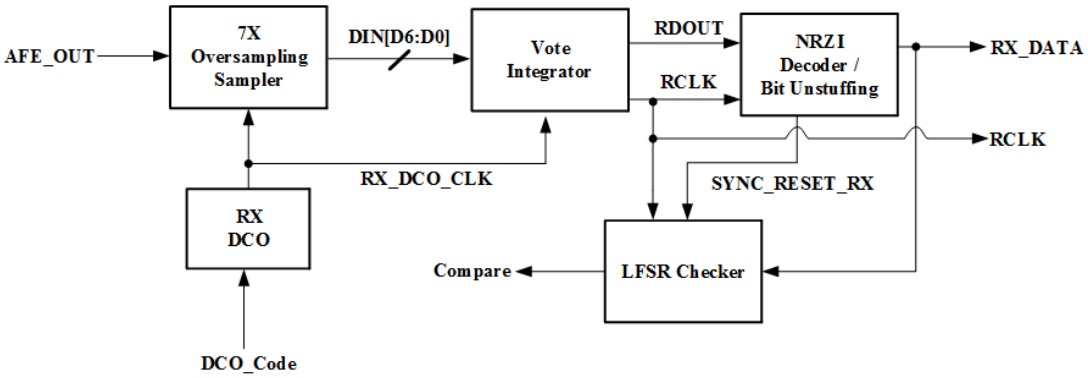


Figure 1.3 WBC BCC receiver architecture [3]

The other WBS BCC architecture is shown in Figure 1.4[5]. Based on the capacitive coupling HBC measurement result [6], an empirical channel model is developed for a practical communication link. The empirical channel model circuit uses an ideal Butterworth bandpass active filter in order to meet the interest bandwidth which is 1 MHz to 100 MHz. The receiver includes a wideband pre-amplifier and a 1-bit digitizer. The wideband pre-amplifier can suppress the common-mode interference and transfer to differential signals with proper V_{CM} at the same time. The 1-bit digitizer includes a bias-generator and a Schmitt trigger. Due to the unpredictable threshold voltage caused by PVT variations, the bias-generator is used to realize the adjustable hysteresis threshold voltage. Subsequently, the Schmitt trigger can utilize this information to recover signal under PVT conditions.

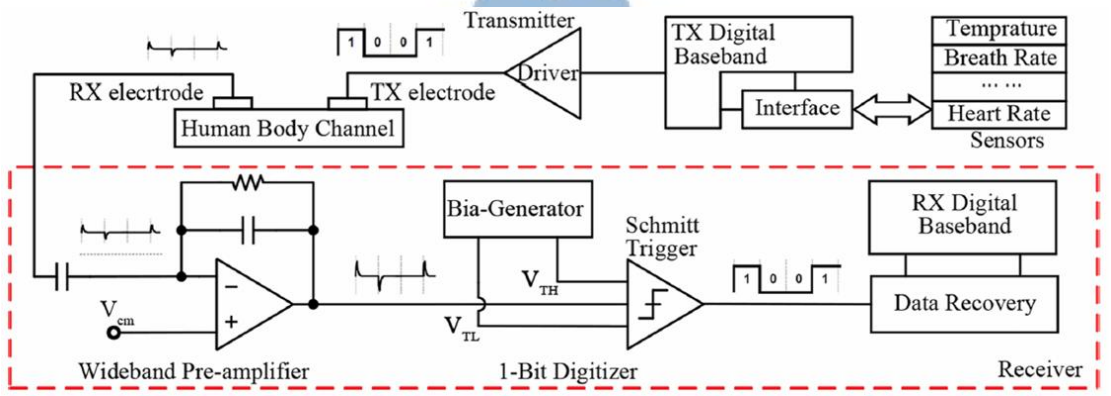


Figure 1.4 The WBS BCC transceiver architecture. Red dash-line-frame is receiver part. [5]

Data recovery diagram is shown in Figure 1.5. The oversampling data recovery circuit uses feedforward 3-phase scheme to choose the best data. The diagram of data recovery algorithm is shown in Figure 1.6. The 3-phase sampling clock samples input data so that we can get 3 sampled data in a symbol period. According to these data, transition information of each phase-slot is known. Accumulating each transition

counts of phase-slot then we can get the most counts of the transition phase-slot. The data of the rest phase sampled are recovery data. The operating frequency of the transmitter is 1 MHz to 100 MHz. The data rate is 5 Mbps.

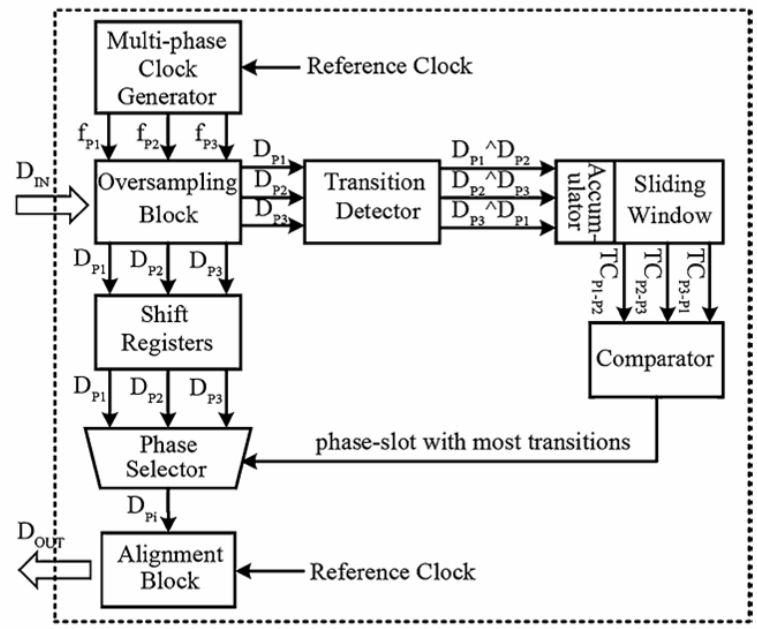


Figure 1.5 Data recovery diagram. [5]

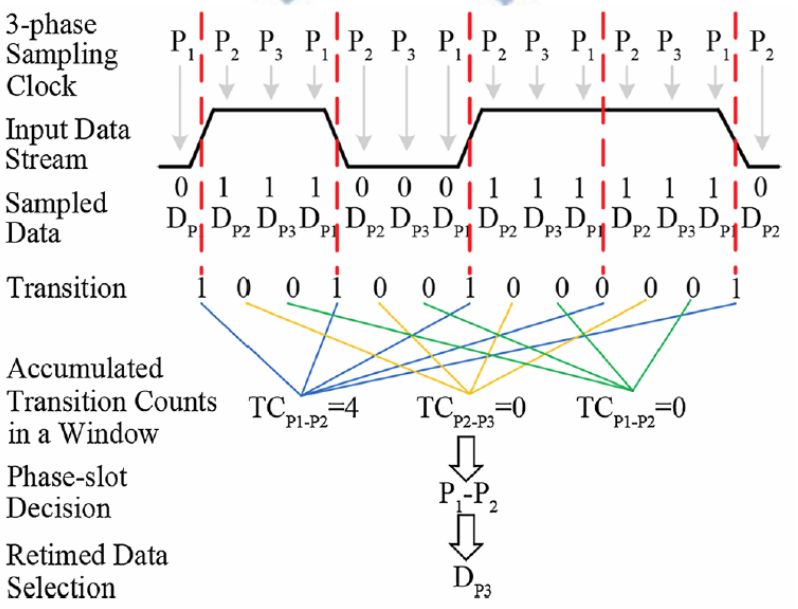


Figure 1.6 Data recovery algorithm diagram. [5]

1.2.2 Modulation: Frequency Shift Keying

Frequency shift keying (FSK) is a frequency modulation scheme to transferring digital information by changing the discrete frequency of a carrier signal. There are many kinds of FSK including binary frequency shift keying (BFSK) and Quadrature frequency shift keying (QFSK).

Body channel characteristic considerably affects by the frequency band of the transceiver [6-8]. That means many issues such as electrode position on the body, transmission distance, human individuals, and so on should be considered when designs a BCC transceiver. To find the optimal frequency band of a transceiver, [9] holds an experiment and collect more than 20 human body transmission data with different weight and height. Figure 1.7 shows the measurement of the attenuation of above experiments. The optimal band which has minimal attenuation for BCC is 30MHz to 50MHz.

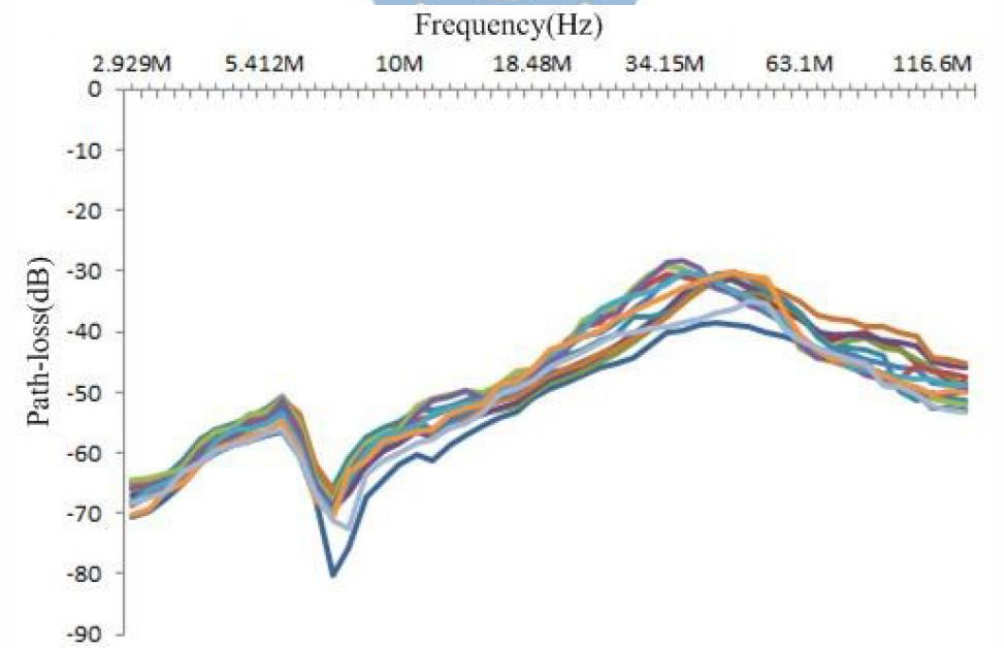


Figure 1.7 Attenuation measurement of BCC [9]

The BCC transceiver [9] supports three modes by using a phase-locked loop (PLL). One is frequency calibration mode. Another is TX modulator mode. The other is RX modulator mode. The block diagram of the transceiver is shown in Figure 1.8. When the transmitter is tracking frequency, B1 signal of the open-loop control (OLC) and close-loop enable (CP_EN) is '0'. A reference frequency signal F_{cal} is sent to the phase frequency detector (PFD). Once the PLL locks, CP_EN turns to "1" and the loop is cut off. At the same time, B1 of OLC turns to "1", input data signal TX_in can be modulated by the VCO. The function of the programmable divider (PN) is a frequency divider. The PN is to cover optimal band of 30-50 MHz. The divided ratio N of two PNs is between 4 and 5 so that the PLL can cover two channels which are 32-39 MHz and 40-47MHz respectively. In the receiver, the received signal RX_in is amplified by the front end amplifier (FEA) and send to the PLL-demodulator through a multiplexer. After frequency calibration, the RX_in is demodulated by the demodulator.

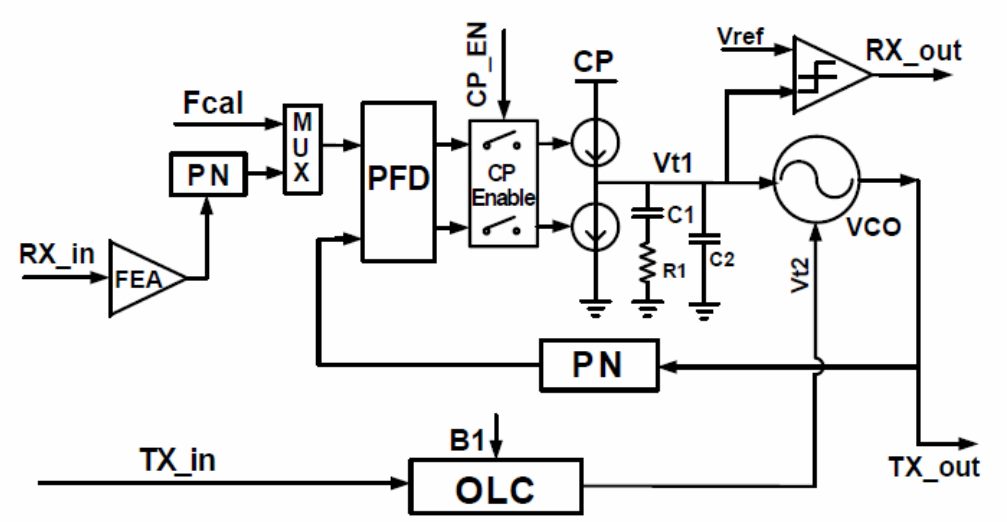


Figure 1.8 The architecture of transceiver [9].

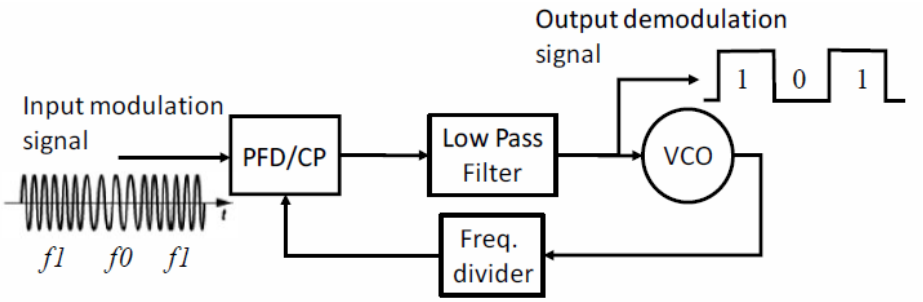


Figure 1.9 Block diagram of PLL-based demodulator [9]

Figure 1.9 shows the block diagram of a PLL-based demodulator [9]. The modulated signal is injected as an input of PFD. When PLL is locked, the input of voltage controlled oscillator (VCO) gets baseband pulse corresponding to two modulation frequencies, thus the FSK signal can be demodulated.

1.2.3 Modulation: Orthogonal frequency-division multiplexing

Orthogonal frequency-division multiplexing (OFDM) is a discrete multitoned modulation. This modulation encodes digital data on multiple carrier frequencies. OFDM uses many closely spaced orthogonal sub-carrier signals to carrier data. Sub-carrier is modulated with a conventional modulation such as the phase-shift keying (PSK) or the quadrature amplitude modulation (QAM) at a low symbol rate. OFDM has benefits of high data rate and high spectrum efficiency, so that [10] designs an OFDM-based BCC transceiver. The transceiver also proposes low power technique to overcome high power consumption drawback of the OFDM. The following paragraph will introduce this OFDM transceiver.

Figure 1.10 shows the block diagram of the OFDM-based transceiver. Before the transmission, data will be encoded by the (2, 1, 6) convolutional encoder which can eliminate the interference from body antenna effect. After that, modem select low-order (QPSK) or high-order (16-QAM) according to the channel condition. Then the signal is transformed from serial to parallel and perform 64-point inverse-Fourier transform (IFFT) operation. Through the parallel to the serial circuit, preamble insertion and cyclic prefix are generated. Preamble insertion allows the receiver to perform synchronization and channel estimation. The cyclic prefix can avoid inner-signal-interference (ISI) and inner-carrier-interference (ICI). Eventually, the required I and Q signal are generated.

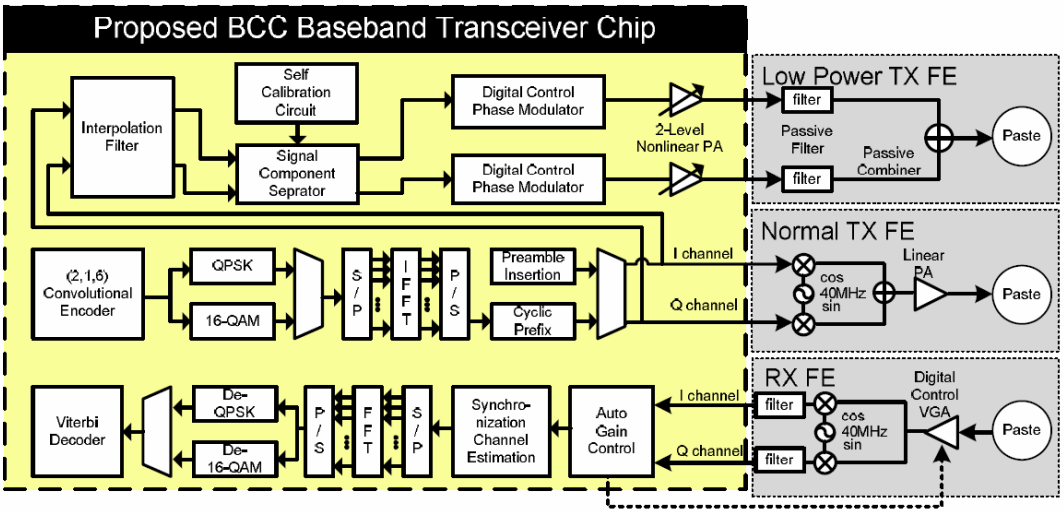


Figure 1.10 block diagram of OFDM-based transceiver [10]

In the receiver part, the auto gain control (AGC) adjusts the recovered signal to a reasonable range so that the latter decision threshold and resolution can be guaranteed. The output of the AGC will send the control signal to an external voltage gain amplifier (VGA). After synchronization, channel estimation estimates correlated angle between the transmitter and the receiver. The carrier frequency offset and sampling clock offset can also be detected, and then Fourier transform (FFT) is performed. QPSK or 16-QAM demodulator will demodulate the bit stream. In the end, a hard-decision 32-quantization length Viterbi decoder decodes bits to original data. Figure 1.11 shows a diagram of the encoder and the Viterbi decoder.

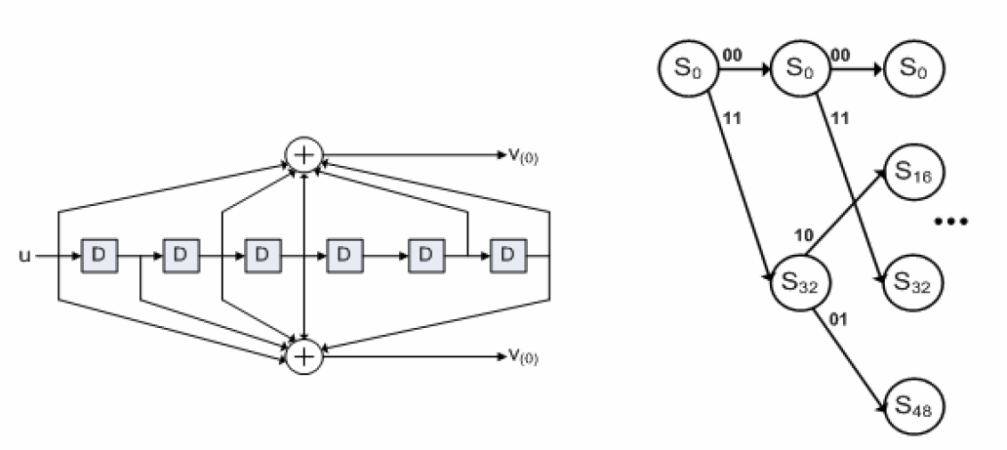


Figure 1.11 Convolution encoder and Viterbi decoder [10]

These two points cause large power consumption. One is high peak to average power ratio (PAPR) lower efficiency of the power amplifier. The other is the amount of flip-flops (F/Fs) in the Viterbi decoder. To overcome large power consumption problem, an uneven multi-level LINC technique is shown in Figure 1.12, voltage scaling and clock-gating technique are applied. Comparing to the architecture of the uneven multi-level LINC in [11], the proposed architecture redesigns delay line to further reduce power as shown in Figure 1.13. After interpolating I and Q signal by 4 times, signal components separator divides the signal into two channel phase modulation signals. The two embedded two-level tunable power amplifiers (PAs) can reduce the power of high-speed front-end circuit and increase the power efficiency of PA.

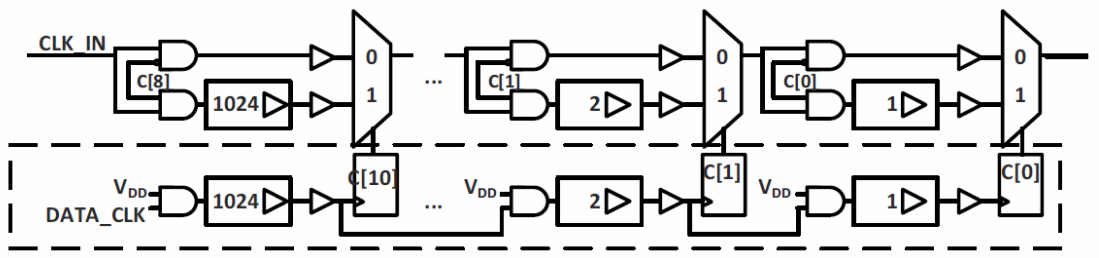


Figure 1.12 Glitch free architecture with duplicated delay line [10]

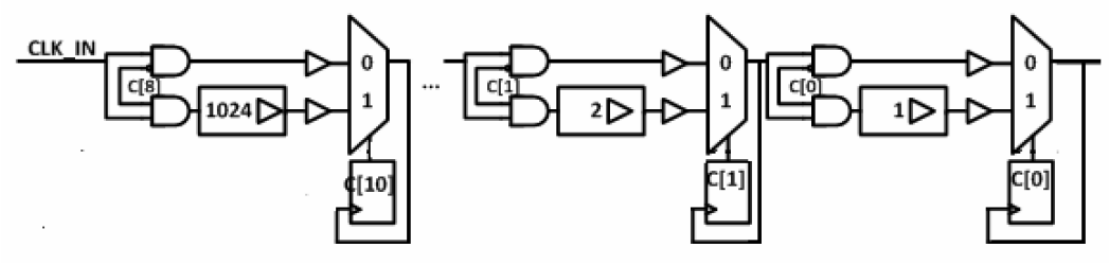


Figure 1.13 Glitch free architecture with Direct-Feedback-Trigger architecture [10]

In Figure 1.12, the delay part of the duplicated delay line will vary by the imbalance layout structure which introduces an unbalanced pulse-width problem and consumes large power. The modified Direct-Feedback-Trigger (DFT) is proposed to overcome these problems, as shown in Figure 1.13. An output of the multiplexer (MUX) connects back directly to the flip-flop as the input clock. Comparing to duplicated delay line, a control signal will be updated at next clock rising edge instead of the code word changes. Therefore, DFT architecture can reduce power consumption.

1.2.4 Modulation: Frequency Selective Digital Transmission Transceiver

The IEEE standard 802.15.6 was approved in 2012. It established the standard for a short-range, low power, and highly reliable wireless communication. According to the standard, physical layer specification of human body communications (HBC) uses the frequency selective digital transmission (FSDT). The data are spread in the frequency domain centered at 21MHz with a 5.25 MHz bandwidth using frequency selective spread codes before transmission. Avoiding interference to other devices, the signal power should be less than -75 dBr (dB relative to the maximum spectral density of the signal) at 400MHz and -80 dBr at 2MHz, respectively [12].

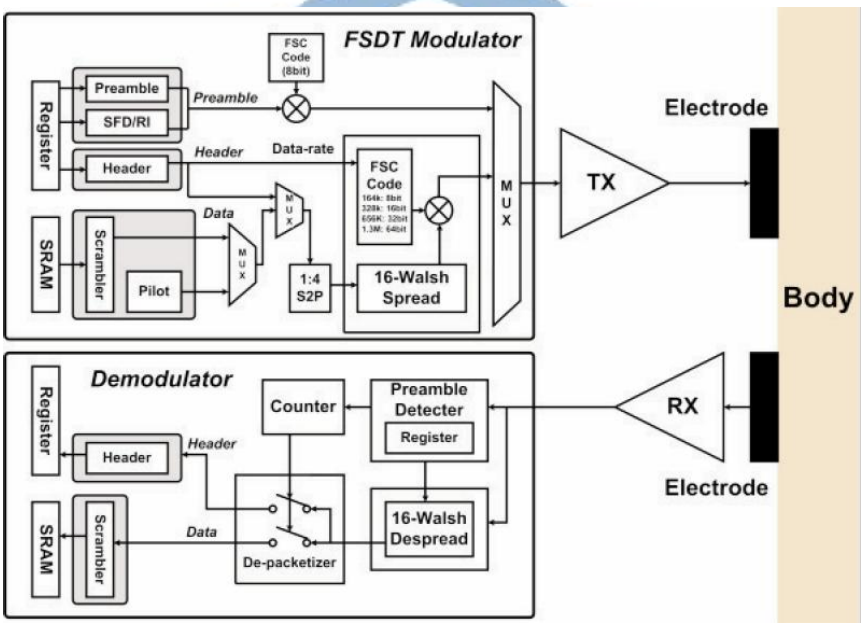


Figure 1.14 Transceiver architecture with the FSDT modem. [13]

In [13], the WBAN HBC transceiver satisfying all specification of the IEEE standard 802.15.6 is presented. The transceiver architecture with the FSDT modem is shown in Figure 1.14. Serial data through the scrambler are transformed to 4 bits

parallel data and spread by FSC and 16 bits Walsh code spreader.

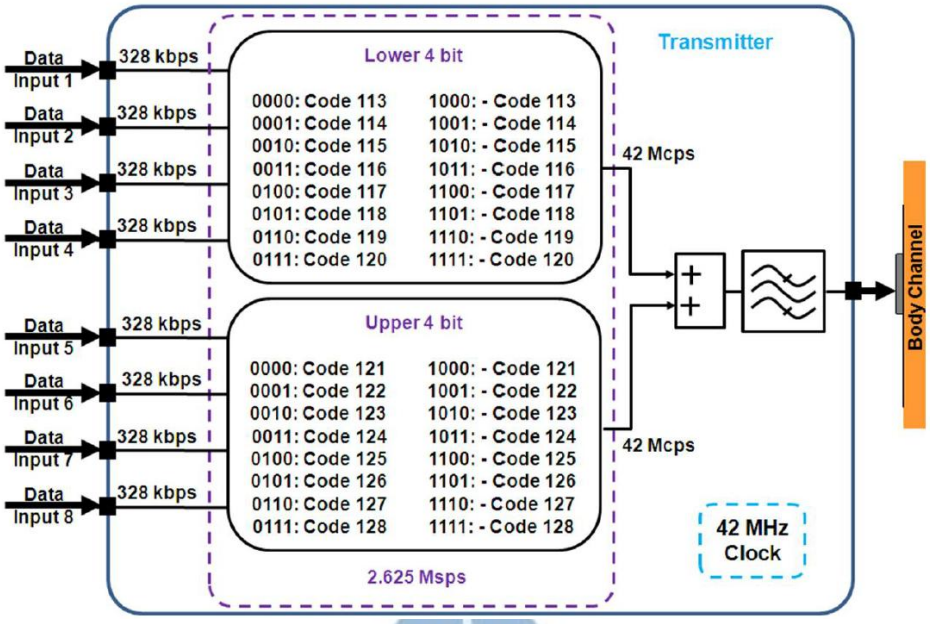


Figure 1.15 block diagram of AM-FSDT. [14]

In [14], another architecture of transceiver with FSDT is proposed. In this architecture, it proposed the amplitude modulated FSDT (AM-FSDT) which is shown in Figure 1.15. The AM-FSDT stacks two of Walsh codes which are assigned to 4 data bits and form a multi-level signal. The stacking of Walsh code is effectively double the bit rate of novel FSDT architecture.

1.2.5 Modulation: Walsh Code

Many BCC transceivers target at biomedical and sensing application so that their data rate is lower than 10Mbps. In [15], they propose a Walsh code transceiver because they aim to transmit multimedia data for emerging wearable smart device and content-rich information for high-end medical devices. This transceiver uses the direct digital data transmission architecture to satisfy features of high data rate and high energy and uses Walsh code modulator to satisfy feature of secure wideband body channel and low path loss. To compensate low data rate by Walsh code, a way of 3-level signaling is made of the transceiver. Apart from 3-level signaling, there's a robust mode by using 2-level Walsh coding with band-stop filter (BSF) to solve strong interference in the environment.

Figure 1.16 shows the structure of the transceiver [15]. Firstly, transferring data need to be transformed from serial bits to parallel bits, then map parallel bits to the corresponding Walsh code by the Walsh code modulator. Two Walsh codes will be stacked into a two-bit output data by the modulator. The 3-level driver transforms the modulator output to 1V/0.5V/0V signal then output to the human body. Figure 1.17 shows the structure of the receiver. The signal through human body will be attenuated, and the carried data may be loss or broken. An analog front-end (AFE) which consisted of a pre-amplifier, an equalizer, and a differentiator is used to recover the signal. Due to an individual of transmitter and receiver, the receiver should recover the clock and data by an integrator and an injection locked oscillator (ILO) based clock recovery circuit. Eventually, a level detector and a Walsh code demodulator demodulate the Walsh code to the original data.

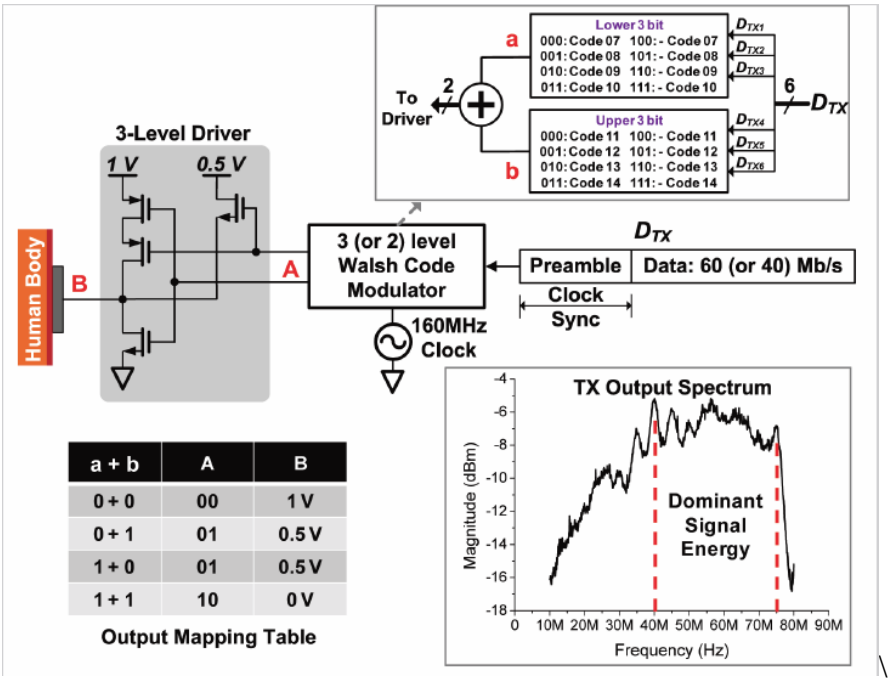


Figure 1.16 Walsh code Transmitter structure [15]

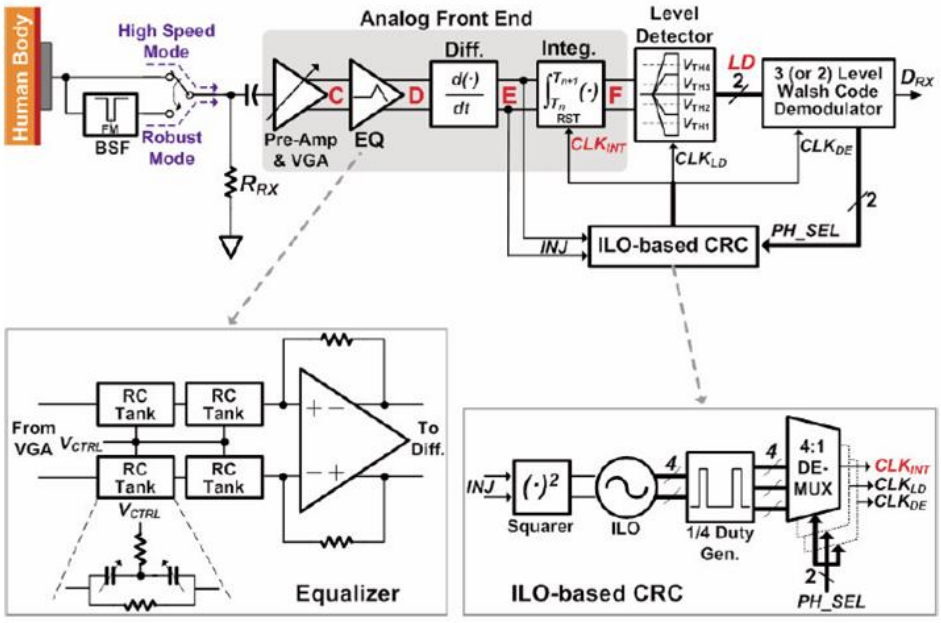


Figure 1.17 Walsh code receiver structure [15]

This Walsh code transceiver uses a 160 MHz clock. There's 3 modes to transfer data, normal mode (Figure 1.18), high data rate mode (Figure 1.19), and low power mode. In the normal mode, there's 3 way to transfer data. First way modulates a 1-bit data as a symbol to a 16-bit Walsh code and can achieve 10 Mbps data rate (Equation 1.1). Second way modulates a 2-bit data to four 16-bit Walsh codes and can achieve 20 Mbps data rate (Equation 1.2). Third way modulates a 3-bit data to eight 16-bit Walsh codes and can achieve 30 Mbps data rate (Equation 1.3). Detail of data rate calculating is as follow:

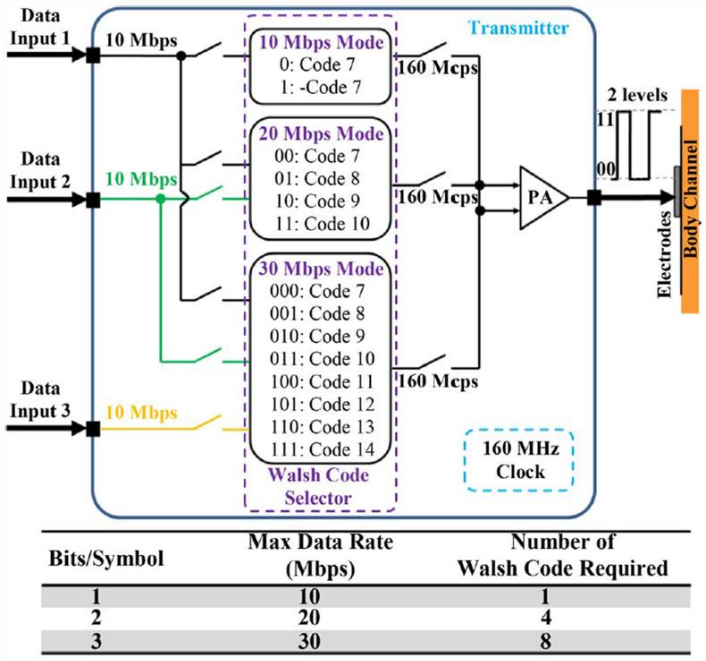
$$160\ (\text{MHz}) \times \frac{1}{16}\left(\frac{length\ of\ data}{length\ of\ Walsh\ code}\right) = 10\ (Mbps) \quad (1.1)$$

$$160\ (\text{MHz}) \times \frac{2}{16}\left(\frac{length\ of\ data}{length\ of\ Walsh\ code}\right) = 20\ (Mbps) \quad (1.2)$$

$$160\ (\text{MHz}) \times \frac{3}{16}\left(\frac{length\ of\ data}{length\ of\ Walsh\ code}\right) = 30\ (Mbps) \quad (1.3)$$

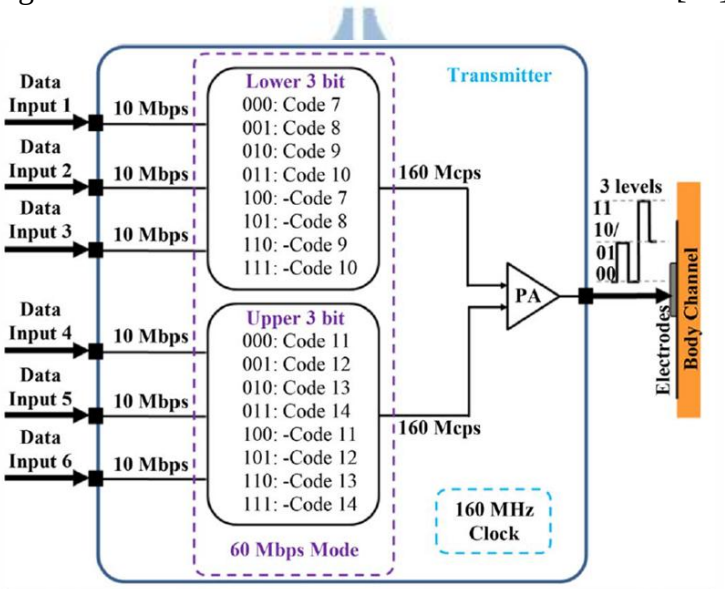
In the high data rate mode, there are two modulators of modulating 3-bit data to 8 Walsh codes. Two outputs of the modulator are stacked and transformed to three-level signal. The Equation 1.4 calculates how data rate achieves 60 Mbps.

$$160\ (\text{MHz}) \times \frac{4}{16}\left(\frac{length\ of\ data}{length\ of\ Walsh\ code}\right) = 60\ (Mbps) \quad (1.4)$$



Bits/Symbol	Max Data Rate (Mbps)	Number of Walsh Code Required
1	10	1
2	20	4
3	30	8

Figure 1.18 Normal mode of Walsh code transceiver. [15]



Bits/ Symbol	Max Data Rate (Mbps)	Amplitude level	Number of Walsh Code Required
3	60	3	8 + 8 inverse

Figure 1.19 High data rate mode of Walsh code transceiver. [15]

In the low power mode, the clock frequency is reduced to 80MHz. The transceiver achieves 5 Mbps of data transfer. Overall of power reduction of achieving 41% power reduction by a simulator.

1.2.6 Summary

In the discussion, the WBS BCC transceiver transmits data directly or using NRZI-encoder so that they use the wide range of operating frequency band. The continuous identical digits (CID) and jitter is an important problem in this architecture. In [3], [5] the bit stuffer is added to avoid the CID and they use the oversampling sampler to sample data to reduce the effort of the jitter. In the FSK modulation, it uses two or more frequencies as the output of 0/1 data. The frequencies of the FSK should be chosen carefully to avoid the popular frequency bands. The interference will occur if there are many applications operating at the same frequency. The OFDM modulation using many sub-frequencies which are orthogonal to each other, this method lowers the interference and have high utilization of the frequency band. However, the phase shifting is a serious problem which should be considered. The FSDT modulation should care about synchronization problem. If the corresponding data is shifted, all data after shifting position will not be demodulated to the original data until the synchronization pattern arrived again. The Walsh code modulation has high data reliability with its orthogonal characteristic, but the drawback is redundant data. The modulation has a tradeoff between data rate and the data reliability.

1.3 FPGA-Based Body Channel Communication Transceiver

Apart from chips, some researches implement their architecture on a Field-Programmable Gate Array (FPGA). The following paragraph will introduce an FPGA-based intrabody communication (IBC) transceiver [16]. The IBC transceiver uses pulse position modulation (PPM) and is built on Xilinx Virtex5 FPGA board (Virtex5-XC5VLX50T), as shown in Figure 1.20. To avoid coupling effects, FPGA board uses a battery as power source. FPGA board generates modulated data signal then transfer through body channel communication by the transmitter and receiver electrodes. Eventually, FPGA board receives a signal from IBC and demodulates back to the original data. The transceiver and receiver electrodes are a pair of commercial self-adhesive Ag/AgCl single electrodes. To check signal through a body, a spectrum analyzer and an oscilloscope is used to analyze the signal. In the experiment, the short transferring distance is 5 cm and the longest transferring distance is 50 cm. Each experiment measures different distance with an increment of 5 cm.

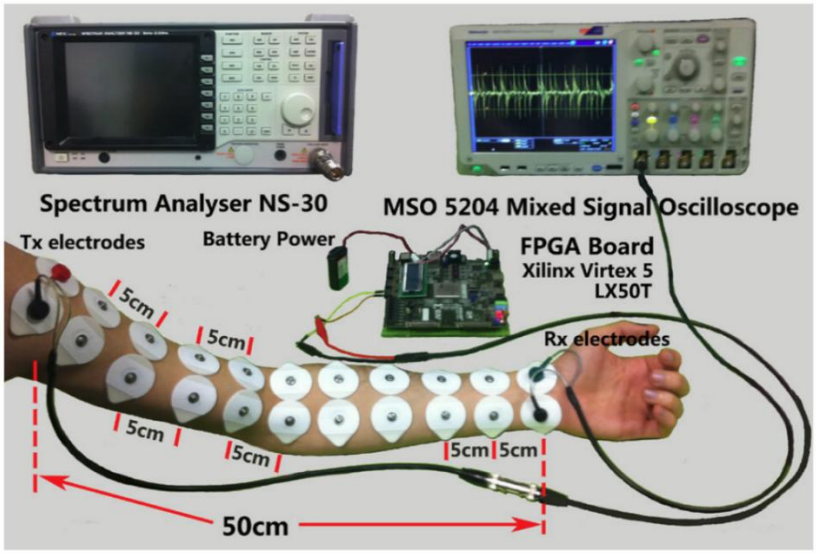


Figure 1.20 Measurement setup and protocol of IBC transceiver by using FPGA board, electrodes, spectrum analyzer, and oscilloscope [16]

Following paragraphs will show the measurement results of the IBC transceiver with 4-PPM and 8-PPM modulation schemes. Comparisons of the transmitter and the receiver pass loss with 4-PPM and 8-PPM are is shown in Figure 1.21 and Figure 1.22, respectively. The transmission distance is 50 cm. There is 41 dB of attenuation with 4-PPM scheme and the power decreases from 6 dBm to 47 dBm. There is 37 dB of attenuation with 8-PPM scheme and the power decreases from 16 dBm to 53 dBm. Next, amplitude and noise are shown in Figure 1.23 and Figure 1.24. The transmission distance is from 5 cm to 50 cm. The noise amplitude is about 4mV. In 4-PPM IBC transceiver, the signal amplitude voltage is from 35 mV to 17.5 mV. In 8-PPM IBC transceiver, the signal amplitude voltage is from 30 mV to 15 mV. Figure 1.25 shows signal noise ratio (SNR) for two subjects. As the transmission distance increasing, the SNR of subject 1 decreases about 6.5 dBm for 2 PPM scheme and SNR of subject 1 decreases about 8.5 dBm for 2 PPM scheme. Figure 1.26 presents simulation result of the bit error rate (BER). The BER of 4-PPM transceiver is between 10^{-5} and 10^{-4}. The

BER of 8-PPM transceiver is between 10^{-13} and 10^{-9}.

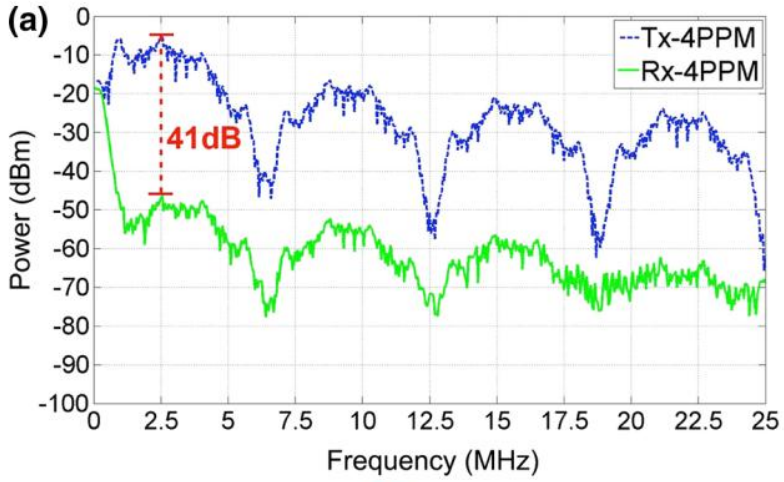


Figure 1.21 Signal spectrum of 4-PPM IBC transceiver. [16]

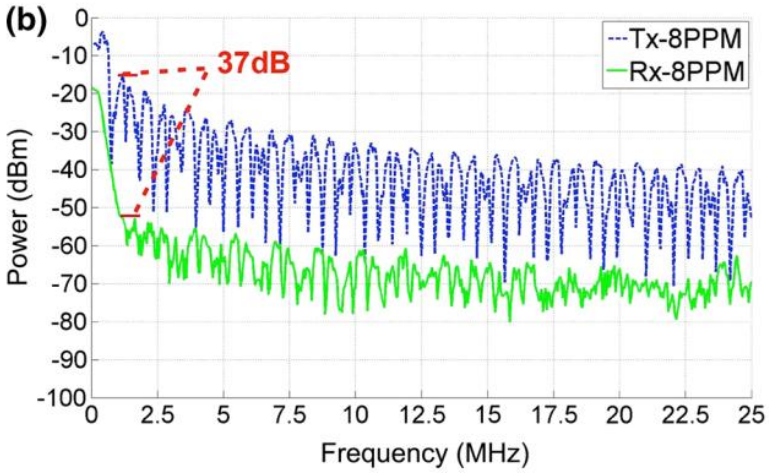


Figure 1.22 Signal spectrum of 8-PPM IBC transceiver. [16]

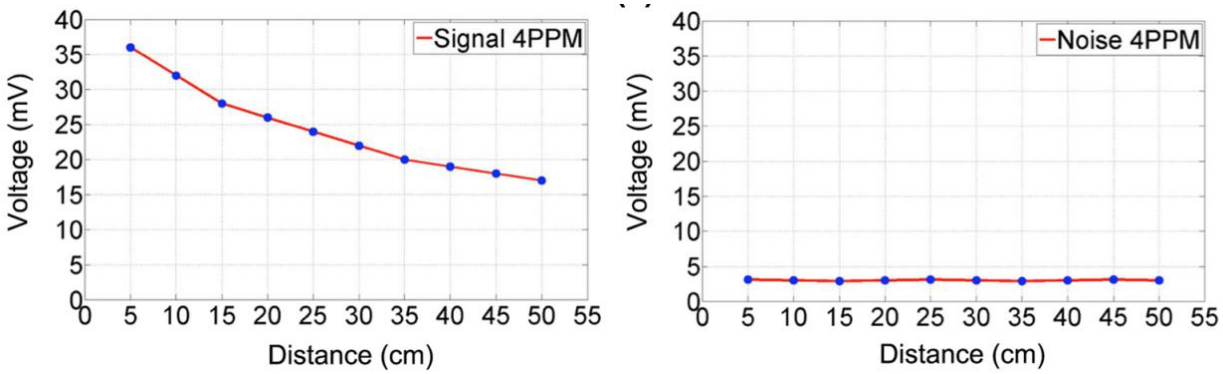


Figure 1.23 Amplitude and noise of 4-PPM IBC transceiver [16]

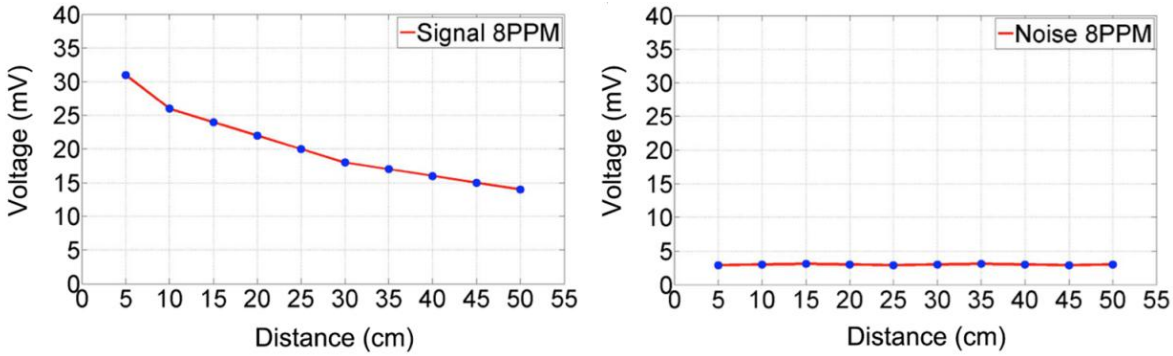


Figure 1.24 Amplitude and noise of 8-PPM IBC transceiver [16]

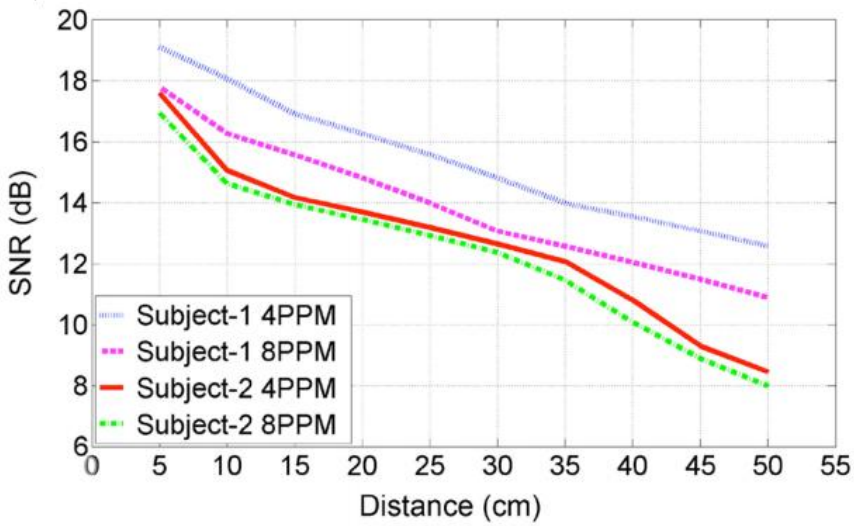


Figure 1.25 SNR versus transmission distance by using 4-PPM and 8-PPM IBC transceiver for 2 subjects [16]

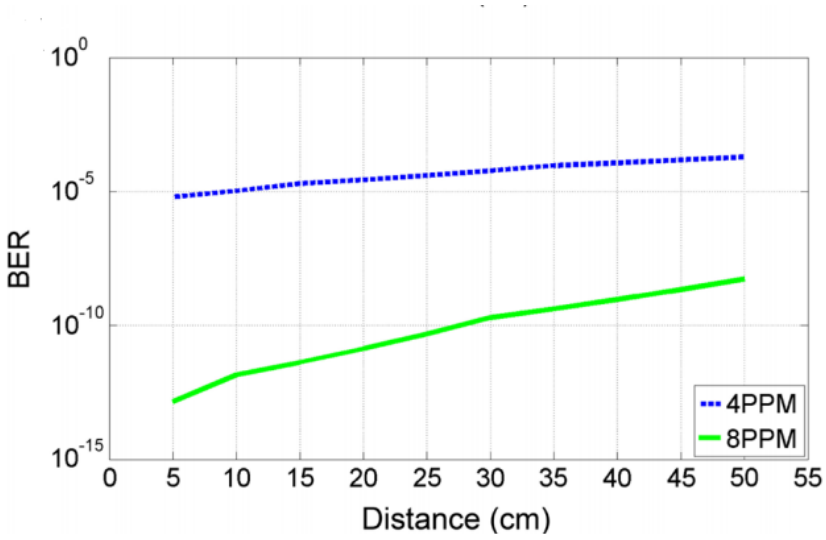


Figure 1.26 Simulation result of BER versus transmission distance by using 4-PPM and 8-PPM transceiver [16]

1.4 Measurement of Body Channel Communication

1.4.1 Measurement Setup

Before measuring the HBC transceiver, the introduction of measurement setup is needed and its illustration is shown in Figure 1.27.

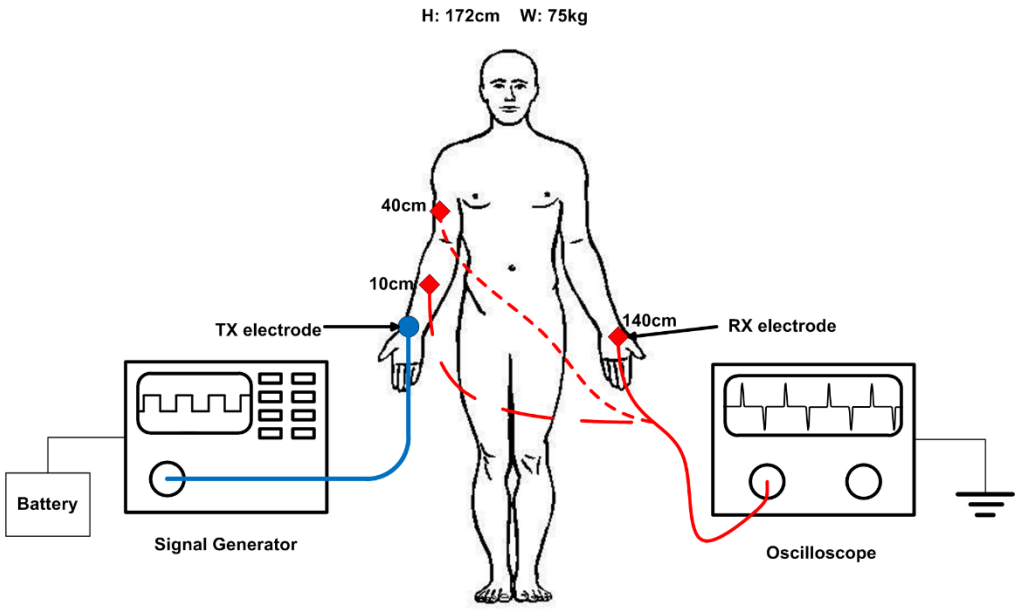


Figure 1.27 Measurement setup for HBC

In Figure 1.27, left part of the figure including a UPS, a signal generator, and a TX electrode serve as a transmitter. The right part of the figure including a RX electrode and an oscilloscope serve as a receiver. The transmitter generates a square signal and transfers to the body channel through a SMA cable (blue line) and a TX electrode. Next, received data signal is transferred from a SMA cable (red line) and a RX electrode to the oscilloscope. The transmission distance between TX and RX is 10, 40, and 140 cm.

The UPS in the transmitter is to form an air-coupling in the return path. Then we can correctly measure the HBC data. According to [17], a length of SMA cable affects power attenuation in HBC. We adopt a 75 cm SMA cable in measurement as shown in Figure 1.28. The electrode is used to connect SMA cable and a human body as shown in Figure 1.29.

Figure 1.28 SMA cable

Figure 1.29 Electrodes

Measurement of the BCC transceiver, illustration is shown in Figure 1.30. Different from above architecture, there is an analog front-end (AFE) board between the RX electrode and the oscilloscope. The AFE board can amplifier attenuated signal through the HBC and recovers signal to digital waveforms.

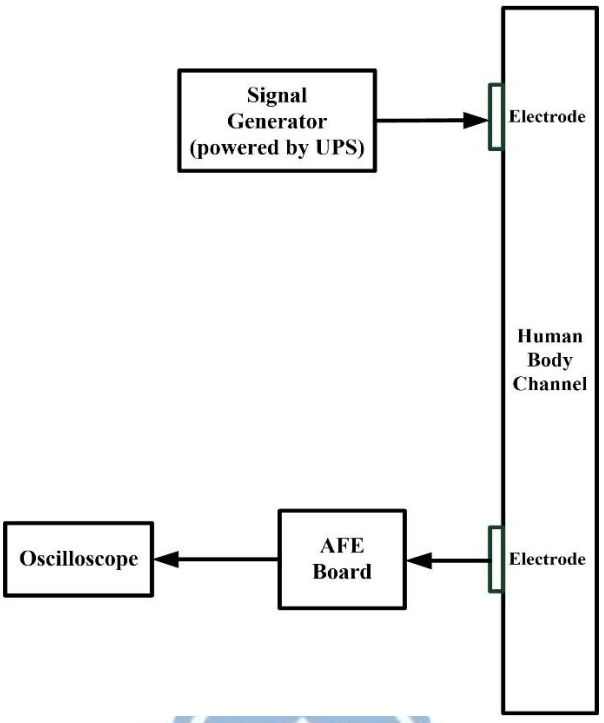


Figure 1.30 Measurement of the BCC transceiver. [24]

1.4.2 Measurement Results of the AFE Board

In this section, a detailed introduction to the AFE board is presented as follows. The AFE board consists of a voltage gain amplifier (VGA) [25], a Schmitt trigger [26], and a 9.0 V rechargeable battery.

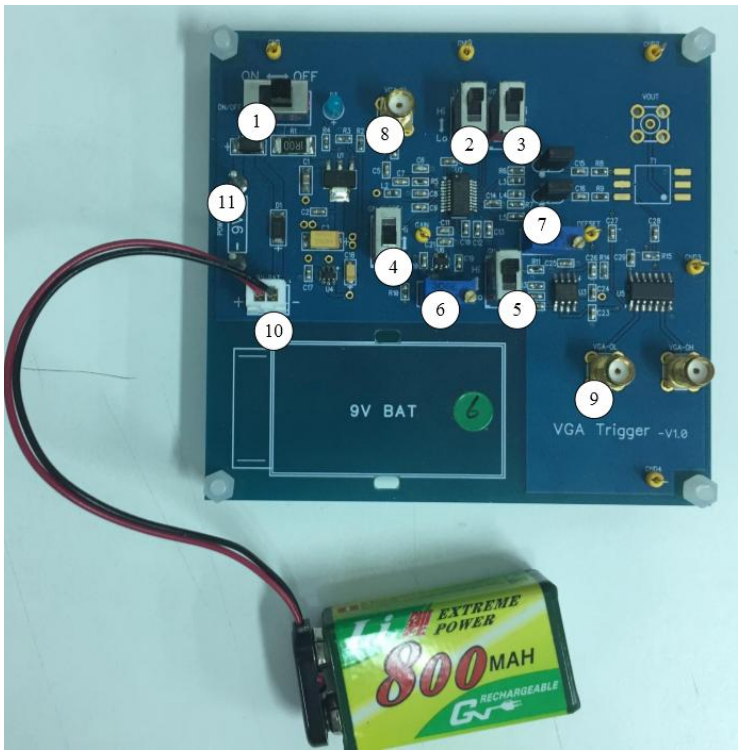


Figure 1.31 AFE board with a rechargeable battery

In Figure 1.31, an AFE board is presented. Number 1 is a power switch of the AFE board. Number 2 and number 3 are the switches of the LNA and the VGA which can be turned on/off. Number 8 is VGA-IN which inputs signal through HBC. Next, attenuated signal will pass through VGA and Schmitt trigger. Number 4 and number 6 determine a value of gain. Number 6 is a variable resistor which can increase or decrease the gain. Increasing or decreasing the gain is controlled by the switch of number 4. In the other word, the gain increases if the switch is turned to Hi, and

decreases if the switch is turned to Lo. The relation of number 5 and number 7 is similar to number 4 and number 6. They control the DC offset voltage of the signal. The range of gain resistor is from 0 to 1.0V. The range of the offset voltage is from 0 to 1.5 V. In addition, the function of the Schmitt trigger is level shifting the amplified signal so as to recover back to the digital signals. After recovering, the signal is outputted to VGA-OUT (number 9). Number 10 is a battery connector which can connect to a 9 V battery. Number 11 is an external power supply input. We can choose number 9 or 10 as a power source of the AFE board. The AFE board component description is shown in Table 1.1.

Table 1.1 AFE board description

Number	**Component**	**Description**
1	ON/OFF	System power switch (5V)
2	LNA-EN	Hi: Enable LNA
3	VGA-EN	Hi: Enable VGA
4	GN-SLOPE	Hi: Gain increase with VR1 Lo: Gain decreases with VR2
5	GN-H/L	Hi: High gain Lo: Low gain
6	VR1	3296W-103-ND Potentiometer (10K)
7	VR2	3296W-103-ND Potentiometer (10K)
8	VGA-IN	SMA connector (input)
9	VGA-OUT	SMA connector (output)
10	9V-BAT	9.0 V battery connector
11	POWER	Power supply pin

The block diagram and the operation of AFE board are shown in Figure 1.32. The attenuated signal pass through HBC has a 272.52 mV peak-to-peak voltage. The signal is a shark-fin-like signal instead of a square signal. The VGA (AD8331) amplifies signal by enlarging its amplitude to 2 V. Upper and lower threshold of the Schmitt trigger (MC74HC14A) is fixed in order to recover amplified signal to square signal. After all, recovery data AFE_OUT outputs.

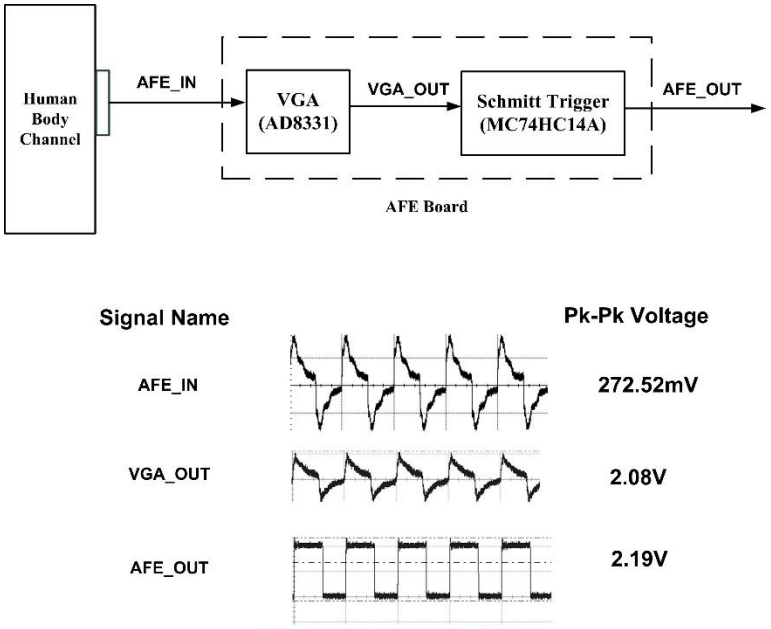


Figure 1.32 Block diagram and operation of AFE board [23]

We measure AFE board and summarizes the results in Table 1.2. Transmission distance and frequency are important issues of the HBC because they can make different signal attenuation. Therefore, we experiment on different transmission distance, 10 and 140 cm, different frequency ranging from 1 MHz to 40 MHz as shown in Table 1.2.

Table 1.2 Summary of BCC measurement [24]

	Frequency	Input Voltage	Gain Value (0 – 1.0 V)	Offset value (0 – 1.5 V)	Recovered Peak-to-Peak Voltage
10 cm	1 MHz	1.0 Vpp	0.65 V (27.5 dB)	0.7 V	2.05 V
	10 MHz				2.06 V
	20 MHz				2.05 V
	30 MHz				2.00 V
	40 MHz				1.83 V
140 cm	1 MHz		1.0 V (43.0 dB)	0.96 V	2.03 V
	10 MHz				2.04 V
	20 MHz				2.08 V
	30 MHz				2.04 V
	40 MHz			1.36 V	1.62 V

After realizing recovery capability of AFE board, we need to know jitter information in different frequency and distance. According to the information, we can decide jitter budget in designing our BCC transceiver when suffering from jitter. Table 1.3 presents measurement results of jitter. We experiment on different transmission distance of 10 cm to 140cm, different frequency of 1 MHz to 40 MHz. This table shows peak-to-peak period jitter, root-mean-square (RMS) period jitter, and RMS cycle-to-cycle jitter. This table, jitter amount also shown in unit interval (UI). A UI represents a symbol time at different data rate. The maximum PK-PK jitter can be up to 28% UI. According to measurement results, the BCC receiver should have large jitter tolerance.

Table 1.3 Summary of the jitter measurement results [24]

Distance	**Frequency**	**Input Voltage**	**Period**	**Period Jitter Peak-to-Peak**	**Period Jitter RMS**	**Cycle-to-Cycle Jitter RMS**
10 cm	1 MHz	1.0 Vpp	999.99 ns	3.9 ns (3.9% UI)	471.7 ps (0.05% UI)	849.92 ps (0.08% UI)
	10 MHz		99.99 ns	3.65 ns (3.65% UI)	271.3 ps (0.27% UI)	465.09 ps (0.47% UI)
	20 MHz		49.99 ns	3.05 ns (6.01% UI)	314.4 ps (0.63% UI)	485.63 ps (0.97% UI)
	30 MHz		33.33 ns	1.5 ns (4.50% UI)	160.1 ps (0.48% UI)	295.92 ps (0.89% UI)
	40 MHz		25.01 ns	2.6 ns (10.39% UI)	155.6 ps (0.62% UI)	845.55 ps (3.38% UI)
140 cm	1 MHz		999.88 ns	43.5 ns (4.35% UI)	3.5 ns (0.35% UI)	5.63 ns (0.56% UI)
	10 MHz		99.96 ns	10 ns (10% UI)	1.1 ns (1.1% UI)	1.78 ns (1.78% UI)
	20 MHz		49.99 ns	3.4 ns (6.8% UI)	253.6 ps (0.5% UI)	467.95 ps (0.94% UI)
	30 MHz		33.35 ns	1.72 ns (5.15% UI)	219 ps (0.66% UI)	2.13 ns (6.39% UI)
	40 MHz		25.42 ns	7.1 ns (27.93% UI)	643 ps (2.53% UI)	4.33 ns (17% UI)

1.4.3 Measurement Results of Human Body Communication

Before measuring, we should know what issues affect transmission of the BCC. Besides the frequency, transmission distance was discussed in [18]. When transmission distance of human body increases, both the resistance of body and coupling capacitance to the external ground increase. In other words, channel length causes a signal loss at the receiver. Body antenna effect cause interfering in BCC [19]-[21], and therefore interference is an issue which we should test. [22] discusses the dynamic human body communication channel. That means it measures effect with moving body. According to the depiction on above, we will measure these issues and present results in the following section.

According to above depiction, we measure several persons with the issues and gathering the result as the reference information to build up our human model. Figure 1.33 presents measured signal power in RX electrode with different distance in the frequency domain [24]. The impedance of the human body is considered as 50 Ω who is in 166 cm tall and 60 kg weight. The amplitude of transmission signal is set to 1.0 Vpp. In Figure 1.33, we can roughly observe two points. First, the longer transmission distance has lower signal power. Second, signal power degrades while frequency increases. The worst case of signal power is at 80MHz in three different distances. When transmission distance is 10 cm, 40cm, and 140 cm, signal power is -19 dBm, -22 dBm, and -26 dBm at 80 MHz, respectively. In addition, in an interval of 10 MHz to 20MHz, the interval has the local worst signal power in three cases. We can examine whether the proposed AFE board is able to recover the attenuated signal by the analysis of the measurement.

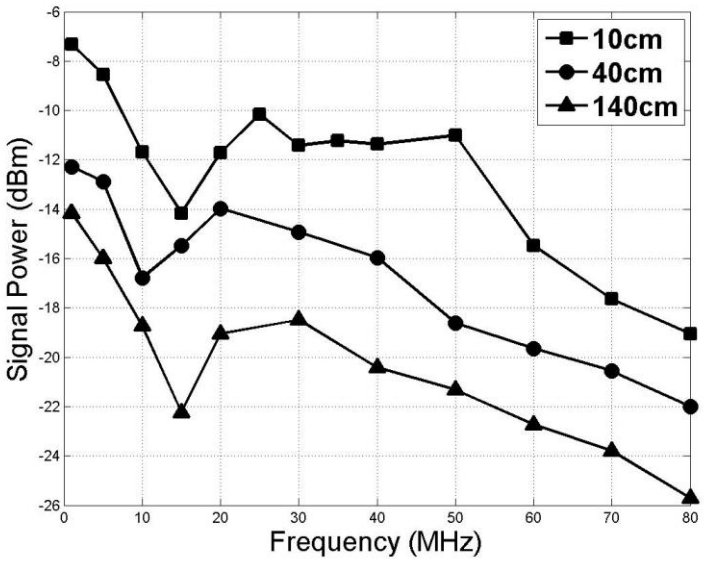


Figure 1.33 Measurement at 10/40/140 cm [24]

In the section, we present measurement results of different human bodies. The experiment has seven persons. Figure 1.34 presents measurement results at 10 cm. Most of the persons have their worst case of signal power in a range from 10 MHz to 20 MHz except the human3. The result except human3 is as the same as the depiction we discussed.

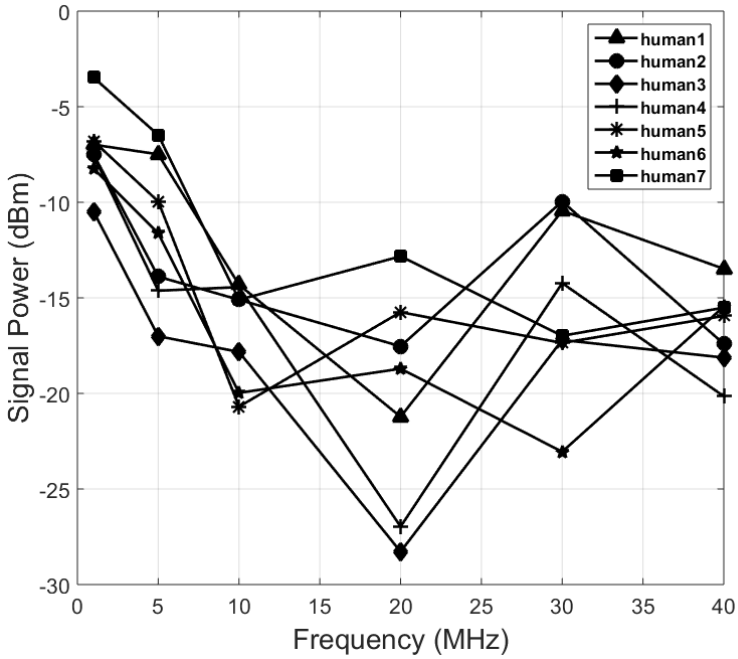


Figure 1.34 Frequency domain measurement results of with 7 persons at 10 cm.

The measurement results at 140 cm is shown in Figure 1.35 and the signal power also decreases while frequency increases. But the human3 has a better signal power than other persons, the signal power difference is about 7 dBm to 13 dBm.

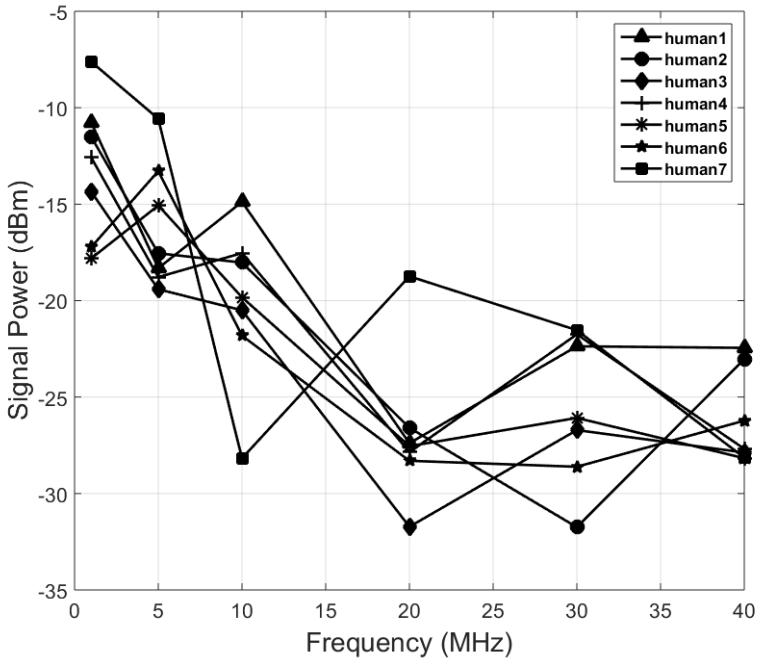


Figure 1.35 Frequency domain measurement results of 7 persons at 140 cm.

Next, we measure the effects of motion situation. The RMS period jitter of still/moving situation is measured on different transmission distance and frequency, as shown in Table 1.4. In still cases, the test person sits on a chair with his hands placed on a table. As for moving case, the test person sits on a chair with his hands swinging regularly. We can observe that jitter in two case is almost the same.

Table 1.4 Summary of BCC motion measurement results [24]

		RX Period Jitter RMS	
Distance	**Frequency**	**Still**	**Moving**
10 cm	1 MHz	1.7 (ns)	1.1 (ns)
	40 MHz	734.2 (ps)	667.1 (ps)
140 cm	1 MHz	4.3 (ns)	3.2 (ns)
	40 MHz	472 (ps)	515.7 (ps)

Table 1.5 shows the effect of interferences to the human body communication. We radiate a signal by using a wireless intercom to measure whether human body channel is sensitive to the interference in the nearby environment. According to results of Table 1.5, we can observe that wireless intercom causes a little interference on body channel communication.

Table 1.5 Summary of the interferences to the human body communication [24]

		RX Period Jitter RMS	
Distance	**Frequency**	**W/O Interference**	**With Interference**
10 cm	1 MHz	3.21 (ns)	2.71 (ns)
	40 MHz	456.2 (ps)	510.3 (ps)
140 cm	1 MHz	2.51 (ns)	1.87 (ns)
	40 MHz	287.8 (ps)	347.4 (ps)

1.5 Motivation

We introduce different modulation methods of the BCC and the measurement results for the BCC characteristics is also shown. In the previous design of our lab, the WBS BCC transceiver can't provide the correct random data transmission at 3.12 Mbps. However, when transmitting the regular 01 data through 140 cm BCC, the data rate can achieve 50 Mbps. The issues can deduced that the jitter occurred or the CID caused no correct transmission. The data reliability is the important issue of our design. Another, for the purpose of applications, a BCC transceiver which can transmit multimedia such as photos or videos is our target, too. A high data rate and high data reliability are essential for the BCC design. Therefore, we use Walsh codes to enhance data reliability. Apart from modulation, we implement BCC by using a FPGA board with an AFE board. An FPGA-based transceiver with Walsh code modulation is proposed which is aim to achieve high data rate and high data reliability.

Chapter 2 Architecture of the BCC Transceiver using Walsh codes

2.1 Overview

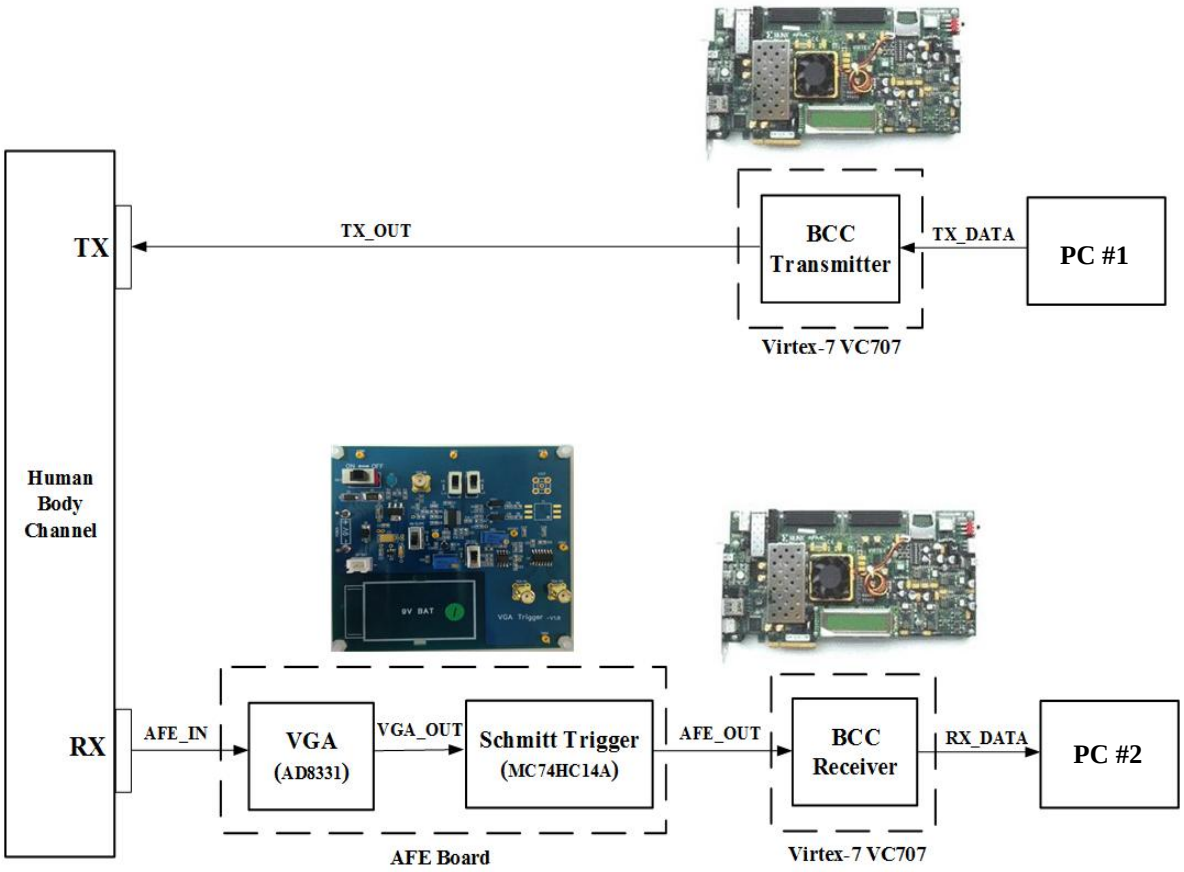


Figure 2.1 Architecture of the FPGA-based BCC transceiver

The proposed BCC transceiver using Walsh codes is implemented on the Virtex-7 VC707 evaluation boards, as shown in Figure 2.1. Personal computer (PC #1) generates TX_DATA and sends data to the transmitter through the universal asynchronous receiver/transmitter (UART). TX_OUT is output of transmitter. Next, data are sent to

the human body through an SMA cable and a medical electrode. The received data (AFE_IN) will be amplified and be recovered by a VGA and a Schmitt trigger of the AFE board. Subsequently, AFE_OUT which outputs from AFE board is sent to the FPGA_based BCC receiver. Finally, output data of the FPGA_based receiver will be sent to PC #2.

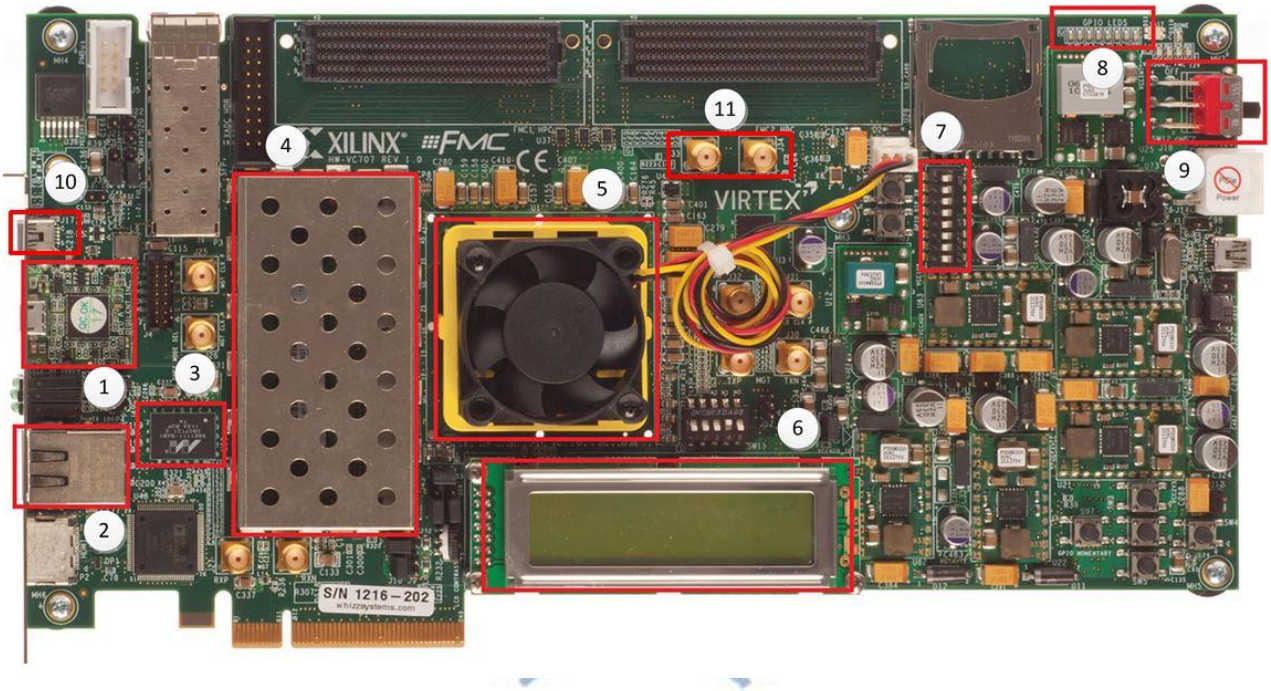


Figure 2.2 Overview of the Virtex-7 VC707 [28]

Figure 2.2 show the overview of the Virtex-7 VC707 evaluation board (EVB) and Table 2.1 lists the description of components of the VC707. Number 1 is a JTAG interface between FPGA and the PC. JTAG interface can be used to loads bit stream to the FPGA. Number 2 and 3 are the Ethernet connector and the Ethernet physical layer (PHT) IC, respectively. Number 4 is a 1GB DDR3 memory. Number 5 is Virtex-7 FPGA with a cooling fan. Number 6 is a LCD display. Number 7 are user DIP switches and number 8 are user LEDs. Number 9 is a power switch for a FPGA. Number 10 is a USB-UART bridge. Number 11 is SMA connector ports for connecting FPGA I/O pins

to the AFE board of the RX or to the TX electrode. In the proposed FPAG-based BCC transceiver using Walsh codes, USB-UART bridge communicates between PC and transceiver.

Table 2.1 VC707 EVB components description

Locations	Component Description
1	USB JTAG interface
2	Network cable port
3	10/100/1000 Mb/s Ethernet PHY
4	DDR3 SODIMM memory (1 GB)
5	Virtex-7 FPGA with cooling fan
6	LCD character display
7	User DIP Switch
8	User LEDs
9	Power on/off switch
10	USB to UART bridge
11	User SMAs

2.2 Introduction to the Walsh codes

The Walsh codes are a set of perfect orthogonal codes with the length n and can be generated from Hadamard matrix. Hadamard matrix is a square matrix which consists of 1 and -1. Assuming that a Hadamard matrix H of order k, Equation 2.1 shows a Hadamard matrix of order 2k. That is a formula of the Hadamard matrix. Walsh codes are generated by Hadamard matrix of order 2^k which are shown in Equations 2.2, 2.3, and 2.4.

$$H(2k) = \begin{bmatrix} H & H \\ H & -H \end{bmatrix} \quad (2.1)$$

$$H(2^1) = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (2.2)$$

$$H\left(2^2\right) = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \quad (2.3)$$

$$H(2^k) = \begin{bmatrix} H(2^k-1) & H(2^k-1) \\ H(2^k-1) & -H(2^k-1) \end{bmatrix} \quad (2.4)$$

In code division multiple access (CDMA) techniques, the Walsh code consists of 0 and 1. We can get a Walsh matrix by replacing the Hadamard matrix's 1 and -1 to 0 and 1, respectively. Then, each row of Walsh matrix is a Walsh code of length k. For example, Equation 2.5 is a Walsh matrix of order 4. From the matrix, four code words of the 4-bit Walsh codes can be found. Equation 2.6 is a Walsh matrix of order 8 and eight code words of the 8-bit Walsh codes can be obtained.

$$W(4) = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \tag{2.5}$$

4-bit Walsh codes:

Code 1 : [0 0 0 0],

Code 2 : [0 1 0 1],

Code 3 : [0 0 1 1],

Code 4 : [0 1 1 0]

$$W(8) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix} \tag{2.6}$$

8-bit Walsh codes:

Code 1 : [0 0 0 0 0 0 0 0]

Code 2 : [0 1 0 1 0 1 0 1]

Code 3 : [0 0 1 1 0 0 1 1]

Code 4 : [0 1 1 0 0 1 1 0]

Code 5 : [0 0 0 0 1 1 1 1]

Code 6 : [0 1 0 1 1 0 1 0]

Code 7 : [0 0 1 1 1 1 0 0]

Code 8 : [0 1 1 0 1 0 0 1]

The characteristic of the Walsh code is orthogonal to other code word [28].

Because of the orthogonal characteristic, each Walsh code is different with other Walsh codes which have the same length. Every Walsh code has half bits difference with each other. In other words, a received Walsh code can be correctly recovered back if the number of corrupted data bits is less than half bits of the code word.

After definition of Walsh codes, we introduce that how to demodulate the Walsh codes. Hamming distance is a simple method and it is easy to be implemented. This method performs bit-wise operation with the recovered data and all Walsh codes. We use exclusive or (XOR) to detect whether a data bit is equal to the corresponding bit of the Walsh code. If the bit operation is true, the result is “0”. Otherwise, the result is “1”. After that, all temporal results are added and the Hamming distance between the recovered data and the Walsh code can be calculated. Finally, the minimum Hamming distance is found, the Walsh code which has minimum Hamming distance to the received data is the desired code word.

Figure 2.3 illustrates the detail of the Hamming distance calculation. Assume that we use eight code words of 8-bit Walsh codes in data transmission. Now, there are 8 bits data are received in the BCC transceiver and we want to detect which one is the correct Walsh code sent by the transmitter. First, all Hamming distances with all possible Walsh codes are calculated. Then, the decode result is the corresponding Walsh code with the minimum Hamming distance. In Figure 2.3, assuming that the transmitter sends code 2, 01010101. Because of bit errors, the received data is 01011101. Figure 2.3 (a) performs the bit-wise operation by XOR and gets the comparing results of 8 bits data. The Hamming distance of code 2 is 1 by adding comparing results of each bit. Figure 2.3(b) shows eight Hamming distances of all code words of 8-bit Walsh codes. Finally, the decode result is code 2.

	Data	XOR	Walsh code (code 2)	=	Comparing result
	01011101		01010101		
Bit7	0	XOR	0	=	0
Bit6	1	XOR	1	=	0
Bit5	0	XOR	0	=	0
Bit4	1	XOR	1	=	0
Bit3	1	XOR	0	=	1
Bit2	1	XOR	1	=	0
Bit1	0	XOR	0	=	0
Bit0	1	XOR	1	=	0

(a)

8-bit Walsh codes	Hamming distance
Code 1	5
Code 2	1
Code 3	5
Code 4	5
Code 5	3
Code 6	3
Code 7	3
Code 8	3

(b)

Figure 2.3 An example of Hamming distance calculation (a) Comparing Code 2 and the received data (b) Hamming distances of eight code words

2.3 Walsh Code BCC Transmitter

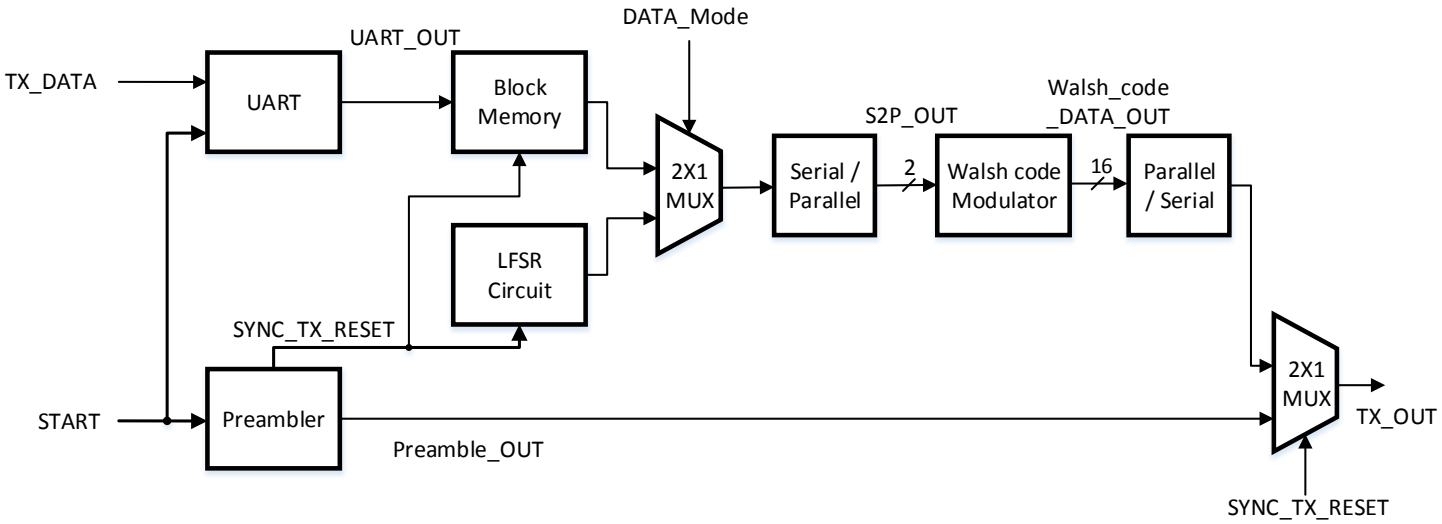


Figure 2.4 Architecture of Walsh code transmitter

Figure 2.4 shows the architecture of the proposed FPGA-based BCC transmitter. The transmitter has two modes and the signal DATA_Mode can choose the random data mode or the image mode. In random data mode, the linear feedback shift register (LFSR) circuit generated the random data for the transmitter. The LFSR circuit is composed of twenty registers with a XOR gate. It can generate the random pattern with every 2^{20}-1 repetition. Another mode of the transmitter is the image mode. In this mode, image data from PC are sent to the FPGA. We use MATLAB of the PC to convert image into binary sequence, then transmit these binary data through the UART interface to the block memory of FPGA. When we start transmitting, the binary data will be sent to the transmitter as inputs. After choosing one DATA_mode in the beginning, the transmitter generates the preamble data by the Preambler block. The preamble data include 12 bits preamble pattern and 8 bits start frame delimiter (SFD) for packet synchronization. When Preamble pattern are sent, the Preambler block sends the SYNC_TX_RESET signal to the LFSR circuit and block memory. Then, LFSR circuit or the block memory

will send the data for transmission. Every two bits of the data are combined as a 2-bit parallel data (S2P_OUT) and are sent to the Walsh code modulator. The modulator maps two bits data (S2P_OUT) to the corresponding 16-bit Walsh code according to the mapping table. In the modulator, we use 16-bit Walsh codes as the modulation code. Since 2-bit input to the Walsh code modulation, four among sixteen code words of 16-bit Walsh codes are chosen. Table 2.2 shows the mapping table used in the proposed Walsh code modulator. To avoid too long CID, the code words match the rule that the maximum CID is equal to two. Finally, the Walsh code outputs as TX_OUT.

Table 2.2 Proposed 16-bit Walsh code mapping table

Input parallel bits	Walsh code
00	0110_0110_0110_0110
01	0101_1010_0101_1010
10	0101_0101_1010_1010
11	0110_1001_1001_0110

Figure 2.5 shows the packet format used in the proposed transceiver. The packet includes 12 bits preamble pattern and an 8-bit SFD, and the following data are 1000 bits payload. The Walsh code demodulator demodulates after receiving a code word and outputs the result when demodulator receives the next packet. Therefore, the 12 bits preamble pattern is used to wait the output of the last demodulated result. In addition, in the first packet, there are additional 512 bits preamble pattern. The reason is that there are hundreds of received data with incorrected pulse width in the first packet at the highest data rate due to the power-on of the AFE board. The preamble

pattern and SFD will be sent in the beginning of the packet. These steps will be repeated until all data are transmitted.

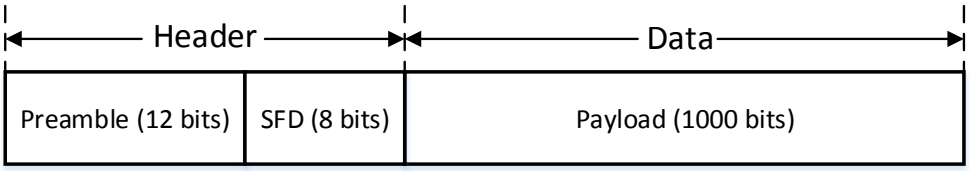


Figure 2.5 Packet format used in the proposed transceiver

2.4 8x Oversampling BCC Receiver

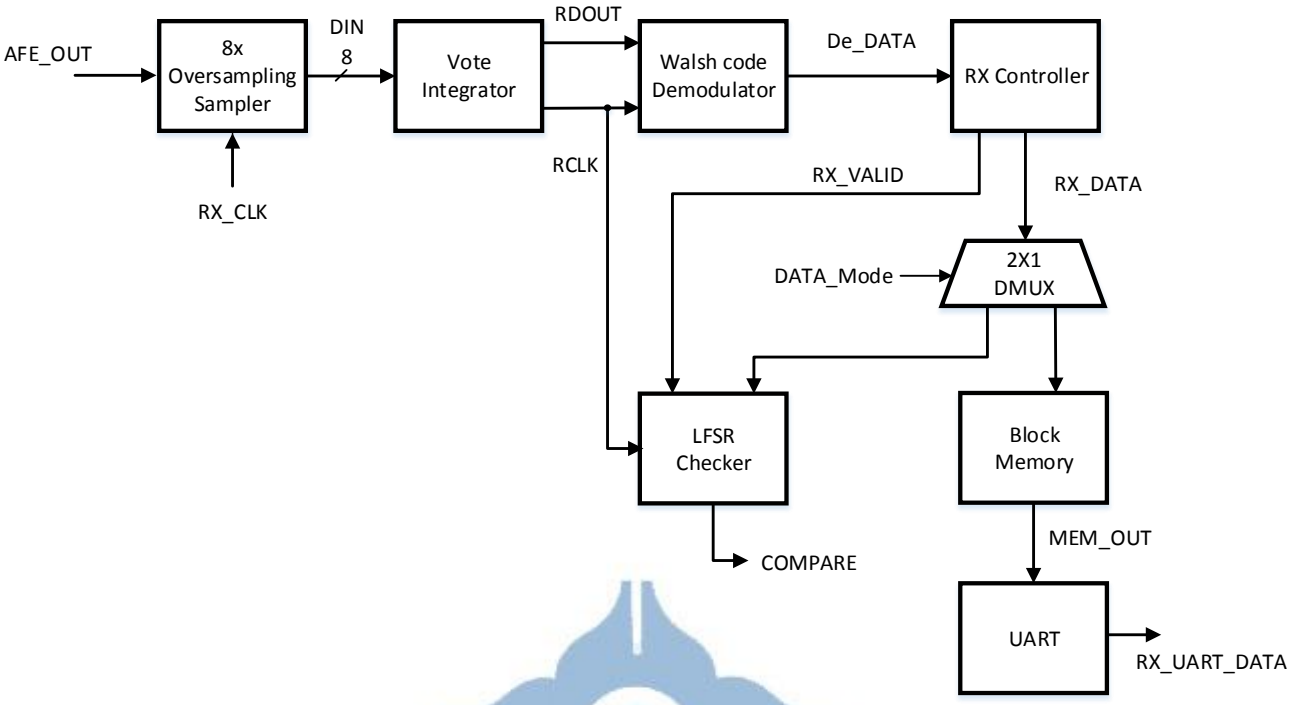


Figure 2.6 Architecture of the 8x oversampling receiver

Figure 2.6 presents the architecture of the proposed 8x oversampling BCC receiver. The 8x oversampling sampler and vote integrator are used to recovery clock and data from AFE_OUT. The 8x oversampling sampler use RX_CLK to sample eight data at one symbol period. The vote integrator uses these data to determine the recovery data (RDOUT) and produces the recovery clock (RCLK). The Walsh code demodulator demodulates 16-bit data to 2-bit original data after Hamming distance calculator. If the data mode is set to the random data mode, the RX controller will send the RX_VALID and the RX_DATA to the LFSR checker. Then, the LFSR checker outputs the COMPARE signal by comparing the RX_DATA and the LFSR data. If the RX_DATA is equal to the LFSR data, the COMPARE is set to 0. Otherwise, COMPARE is set to 1. If the image mode is set, the RX_DATA will be stored in the block memory. Subsequently, the data are transmitted through the UART interface to the PC. In LFSR

checker, the same random data sequence is generated by the LFSR circuit. Thus, the LFSR checker can determine whether there has bit errors.

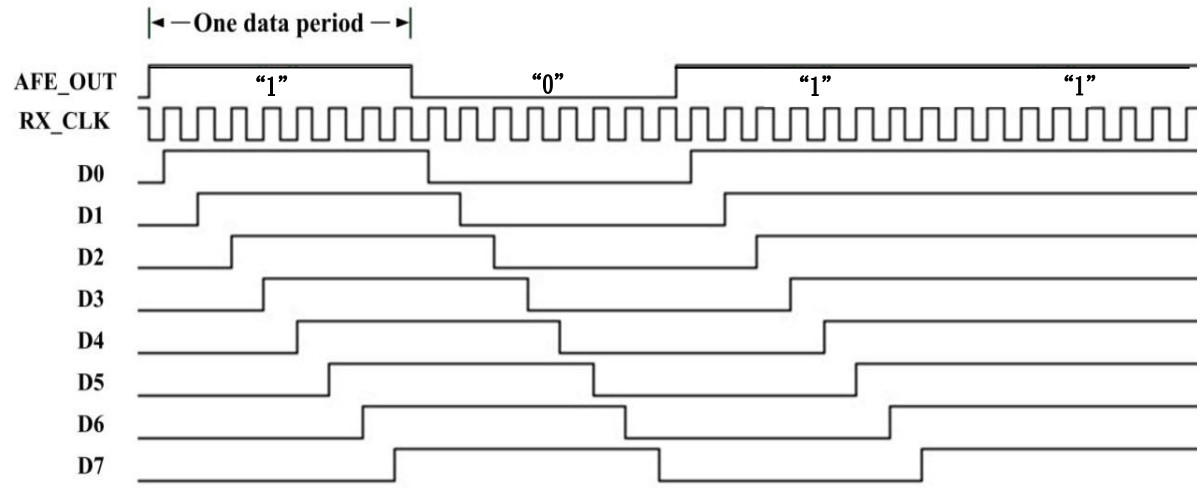


Figure 2.7 Illustration of the Vote integrator mechanism

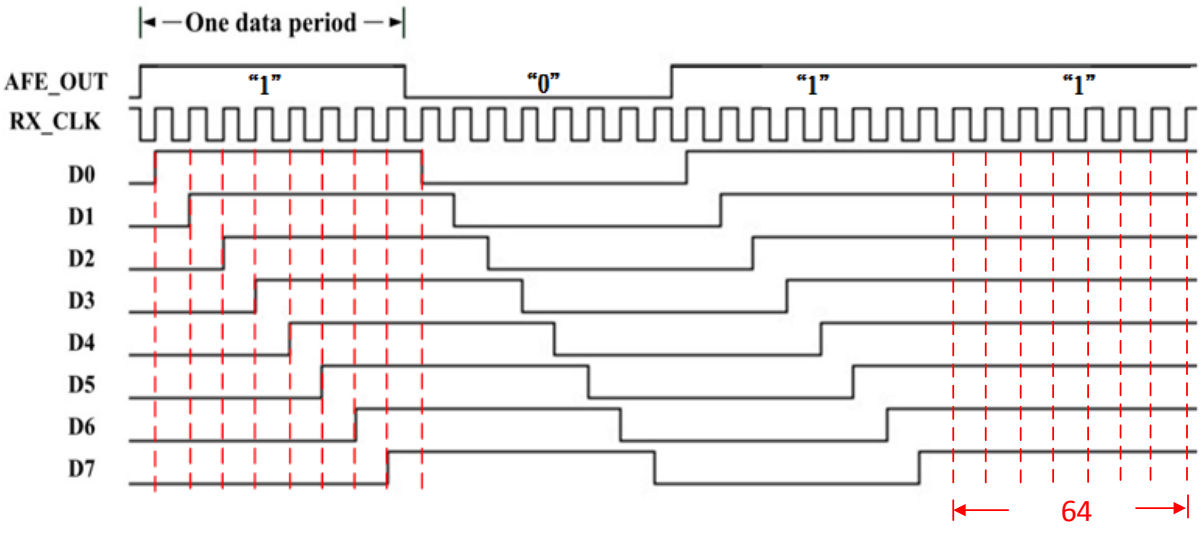


Figure 2.8 Detailed illustration of the Vote integrator mechanism

Figure 2.7 presents the illustration of the vote integrator mechanism. The 8x oversampling sampler uses RX_CLK to sample eight data in one data period as DIN[D7:D0] signal. The vote integrator computes the number of "1" from these 8-bit data within a data period. The eight clock periods of DIN are stored into the register (value_integrator). If the two data of "1" is coming, the value_integrator will be fulfilled by "1". Therefore, the value of the value_integrator is 64 (Figure 2.8), and this is the maximum value of the value_integrator. To recovery data and clock, the threshold of value_integrator is set to 32 because the value is half of value_integrator and the result is stored in over_threshold. Therefore, the over_threshold will be set to "1" if the value of value_integrator is over 32. Otherwise, over_threshold will be set to "0". To recovery the data, Rise_edge and Fall_edge show the data transition according to over_threshold. When Rise_edge is "1", RDOUT (signal of recovery data) is set to "1". When Fall_edge is "1", RDOUT is set to "0" (Figure 2.9).

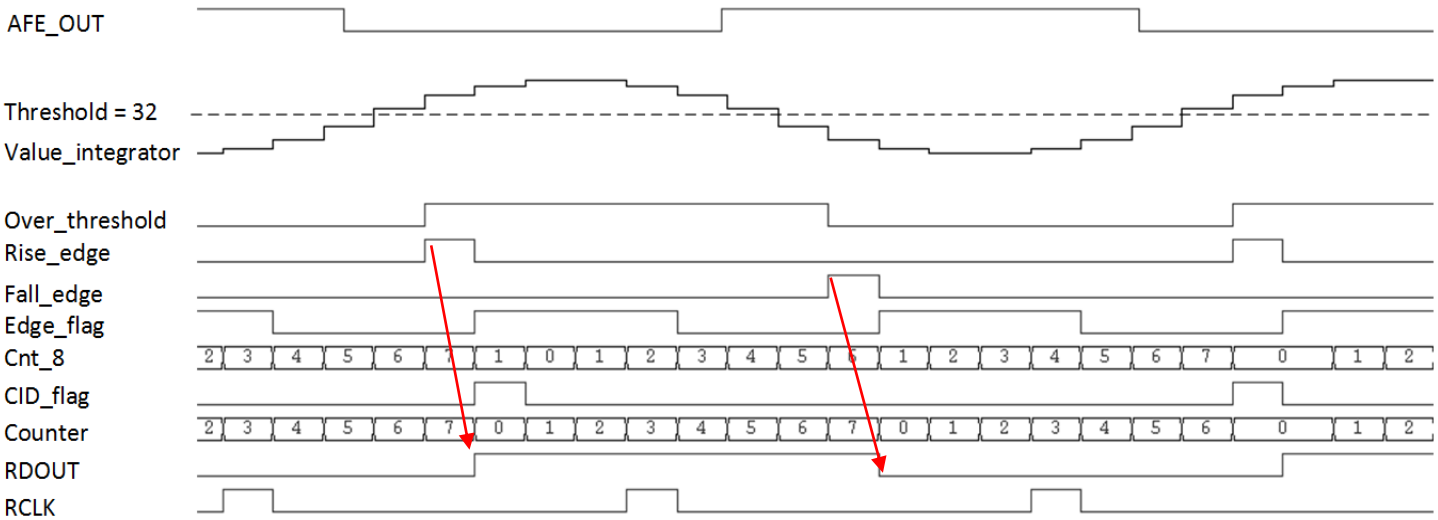


Figure 2.9 Illustration of recovery data

To recovery clock, some situations needs to be considered. According to data transition, the vote integrator has three mechanisms to produce the recovery clock. First, the normal situation (Figure 2.10) shows the situation of data transition. The signal Rise_edge and Fall_edge represent the data transition. The Edge_flag indicates that the transition is occurred and a clock should be recovered. The counter is used to count the clock cycles for RCLK (recovery clock). To sample in the middle of RDOUT, the RCLK rises after the counter is “2”. When Rise_edge or Fall_edge is “1”, the Edge_flag is set to “1” and the counter is reset to 0. After the RCLK falls, the Edge_flag is set to “0”. In the same time, the Rise_edge or Fall_edge is set to “0”, too.

Second, the CID situation (Figure 2.11). CID means that more than two consecutive data which have no transition. A counter (cnt_8) is used to count eight RX_CLK cycles. There are eight sampling data in a data period and thus cnt_8 counts from 0 to 7, CID_flag will be set to 1 for one RX_CLK period when the cnt_8 is equal to “7”. Finally, the falling edge of the RCLK resets the CID_flag.

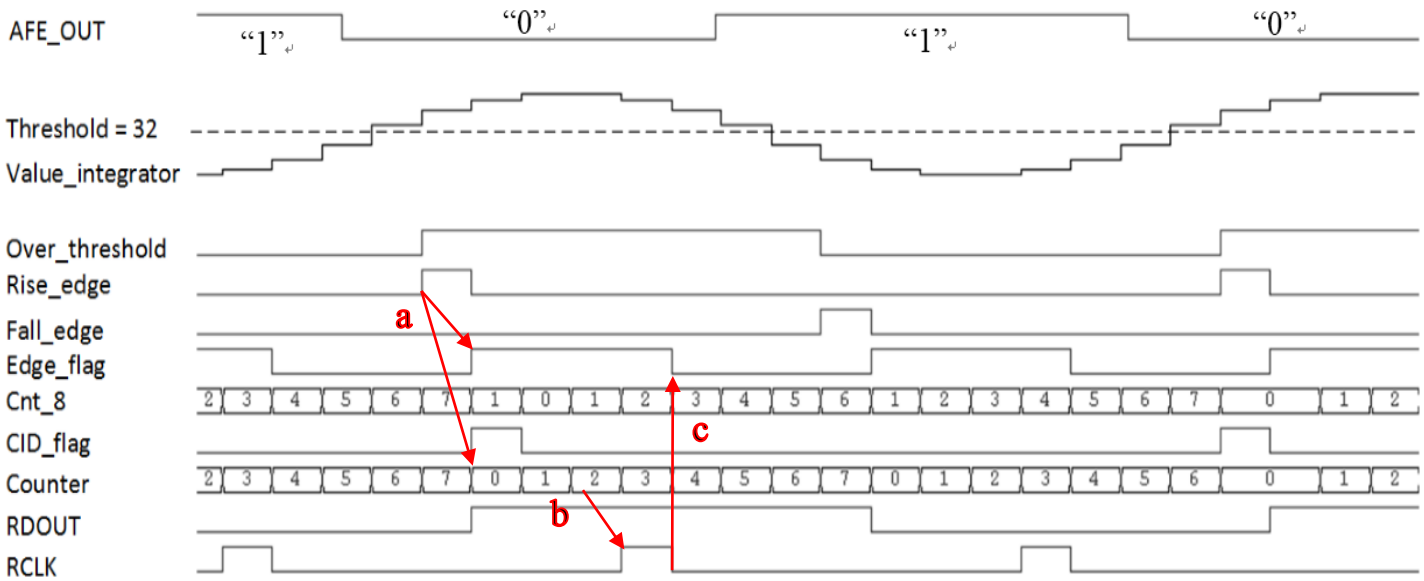


Figure 2.10 Normal situation in the vote integrator (a) the Rise_edge sets the Edge_flag and resets the counter (b) the RCLK is set to "1" after counter counts to "2" (c) Edge_flag is set to "0" when RCLK falls.

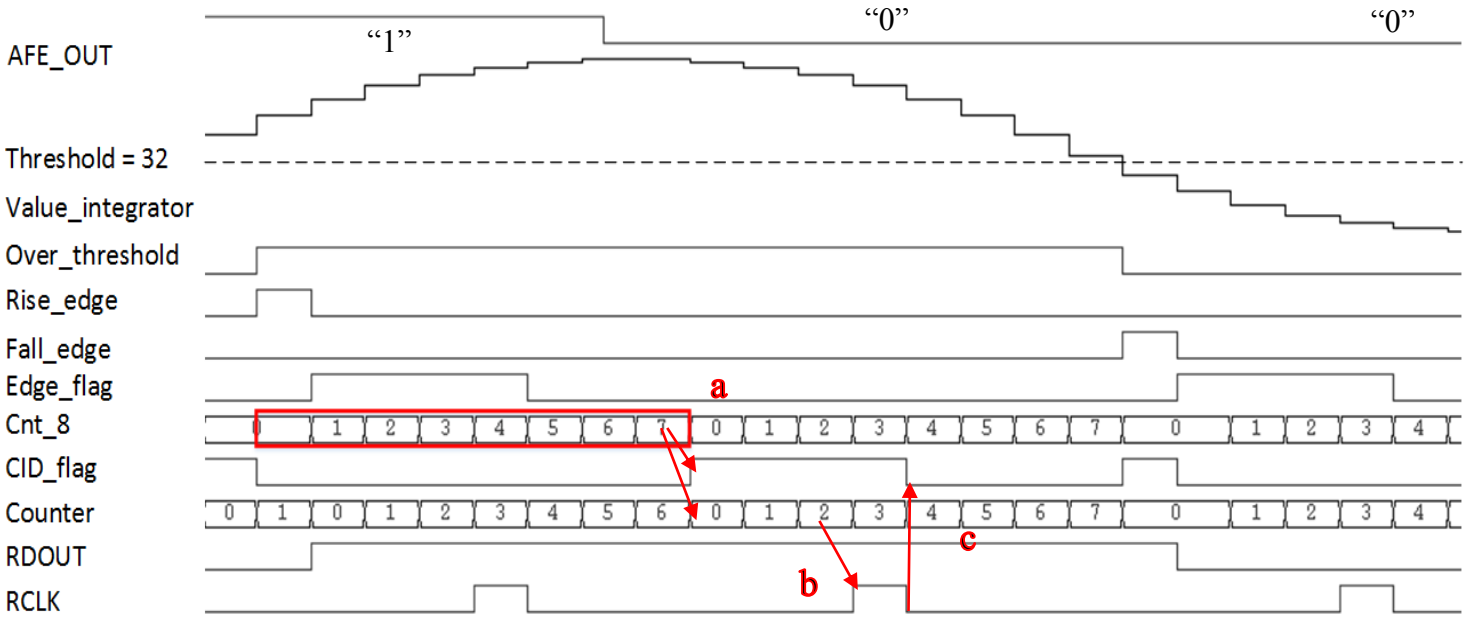


Figure 2.11 CID situation in the vote integrator (a) the CID_flag is set to "1" and counter is set to "0" when the cnt_8 counts to "7" (b) the RCLK is set to "1" after counter counts to "2" (c) CID_flag is set to "0" when RCLK falls.

To avoid conflicting of above two mechanisms, we add two rules and they have higher priority than the operation in the normal and CID situation. The first mechanism is shown in Figure 2.12. The Rise_edge and the Fall_edge can set the CID_flag to “0” and cnt_8 to “1”. The reason of cnt_8 is set to “1” rather than “0” is that the clock cycle of Rise_edge is the first cycle. The mechanism is obviously that the CID situation does not happen. The second mechanism is shown in Figure 2.13. If the CID_flag has risen and the value of value_integrator is in the range from 16 to 48, the CID_flag and the cnt_8 will be set to “0”. The second rule presents a situation that the CID_flag has risen so that the RCLK will rise soon. In this moment, Edge_flag will later rise in several RX_CLK cycles. The RCLK possibly rises two times because of rising of both two flag. However, the RCLK which is triggered by CID_flag is redundant. For this reason, we set CID_flag to “0” if value of value_integrator approaches to threshold (i.e. 16 to 48).

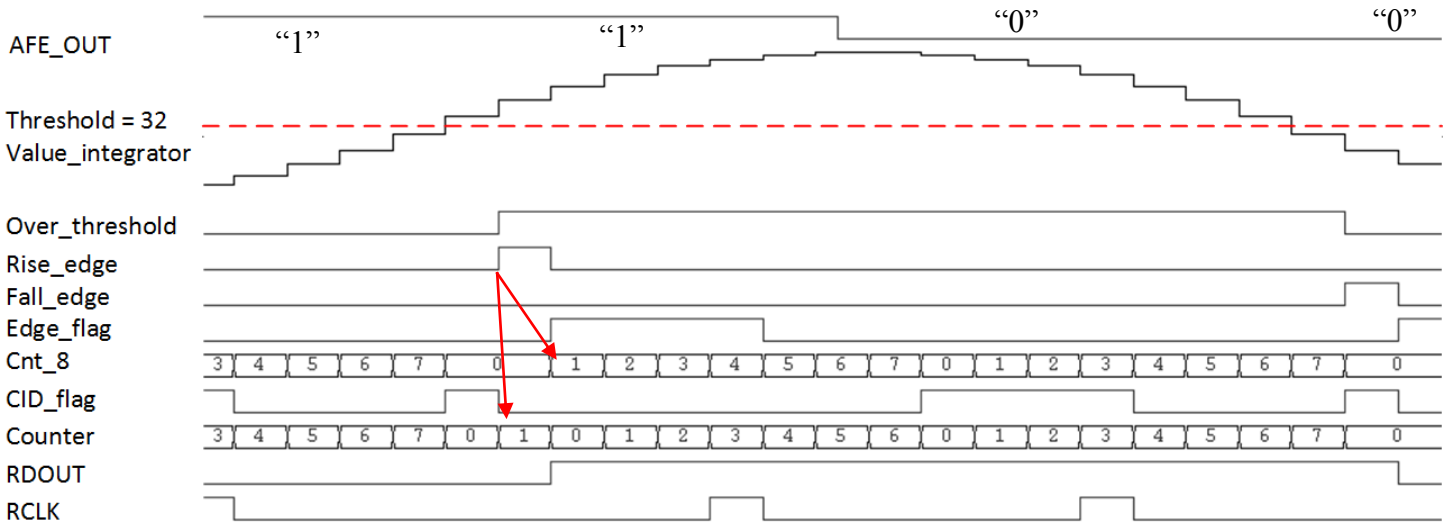


Figure 2.12 Rise_edge and Fall_edge can set CID_flag to “0” and cnt_8 to “1”

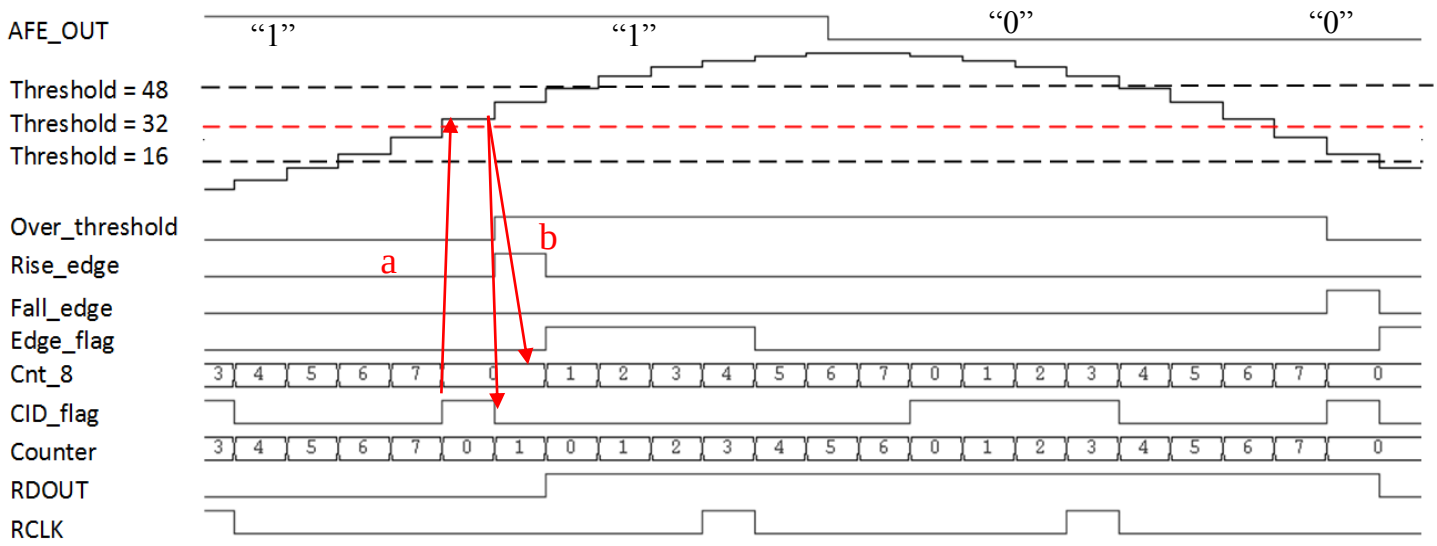


Figure 2.13 The CID_flag and the cnt_8 will be set to "0" when (a) CID_flag rised and the value of value_integrator is in the range from 16 to 48 (b) the CID_flag and the cnt_8 will be set to "0"

The Walsh code demodulator starts to demodulate when received the SFD. The counter continuously counts sixteen clocks which mean a code word of Walsh code is received. In every clock period, the demodulator performs the bit-wise operation and calculates the Hamming distance to all possible code words. When sixteen clocks are counted, the minimum operation operates and finds the code word which has minimum Hamming distance to the received code word. In the next cycle, the demodulated data bits are stored in the register. Finally, the Walsh_code_output_valid signal is raised then the data are outputted serially.

2.5 Implementation of the BCC transceiver on FPGA boards

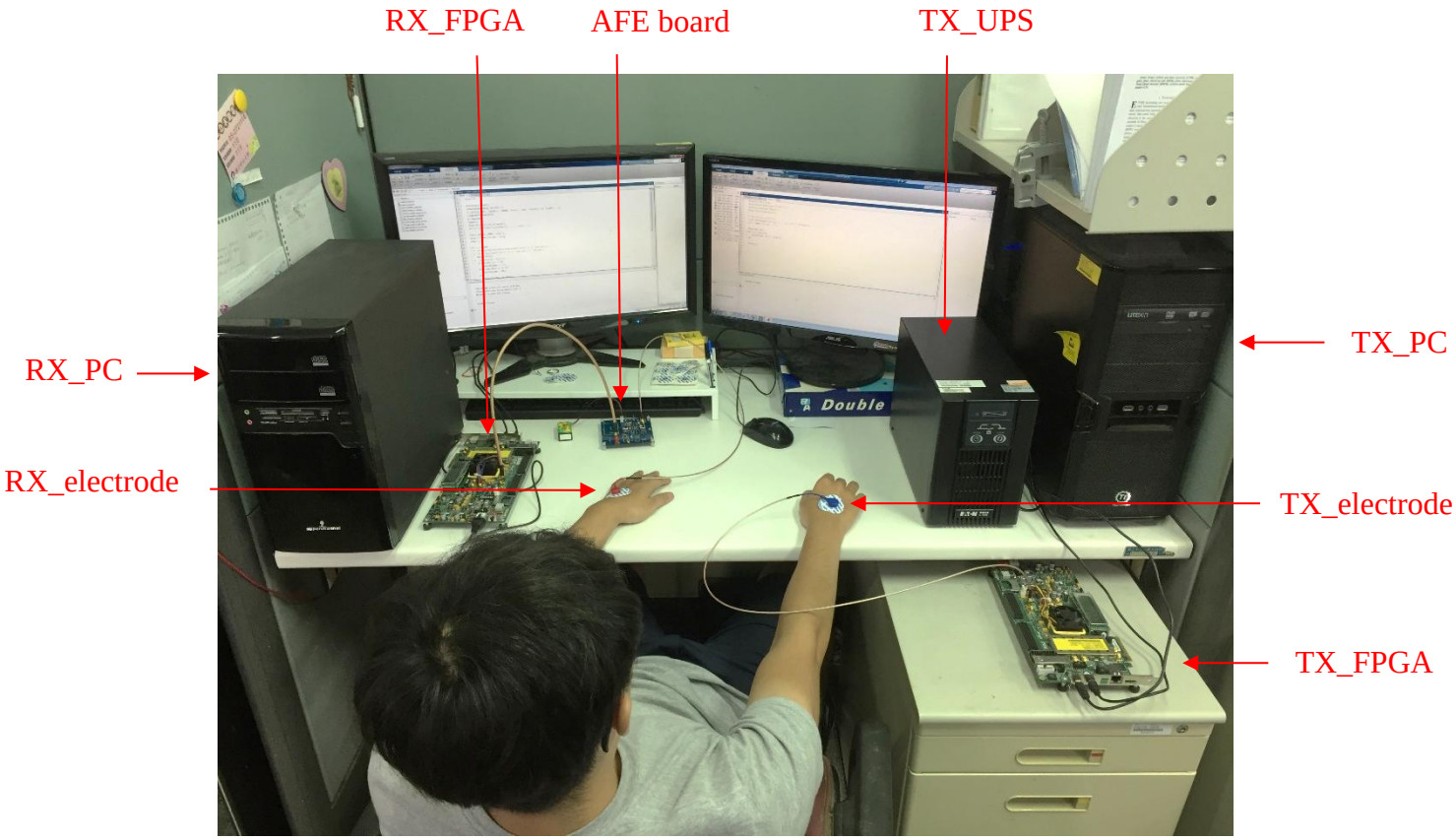


Figure 2.14 Implementation of the BCC transceiver on FPGA boards

Figure 2.14 shows the implementation platform of the proposed BCC transceiver with Walsh code. The designed RTL codes of TX and RX can be synthesized, implemented, and generated the bit stream by the ISE program. Thus, the transceiver is implemented on Virtex-7 EVB by downloading the bit stream to the FPGA. Next, we use MATLAB to generate the binary data of an image. The TX_PC transmits an image data as the TX_DATA to TX_VC707 through the UART interface. The TX_VC707 outputs data through the SMA port, the SMA cable, and the TX_Electrode to the human

body channel. The output data from the human body will be connected to the RX_AFE board first. The RX_VC707 receives recovering digital waveforms from the RX_AFE board, and then the data are recovered by the proposed FPGA-based BCC receiver. In the end, the recovery data are transmitted to the RX_PC through the RX_UART. Then, MATLAB on PC rebuild these data back to the original image. To make sure the grounds in TX and RX are air coupling, the power source of the TX_VC707 is powered by a UPS, and the power source of the RX_VC707 is directly connected to the power outlet

3 Implementation Results of the proposed BCC transceiver

3.1 Implemented Information of VC707 EVB

The implementation information shows that how many resource the proposed Walsh code BCC transceiver has used on FPGA. Table 3.1 and Table 3.2 show that the FPGA pins are used by the proposed BCC transmitter and receiver, respectively. Except a single pair of clock pins, most of the pins are input or output of the data. An LED lights when the data are transmitted completely from UART interface to the block memory of the TX.

Table 3.1 Usage of FPGA pins by the transmitter

BCC Transmitter			
Net Name	**I/O**	**FPGA Pin**	**Description**
clk_in_p	Input	E19	A signal pair provides create 200 MHz clock on VC707
clk_in_n	Input	E18	
RESET	Input	AV40	A CPU RESET button.
TX_DATA	Input	AU33	An input port for UART.
FIFO_VALID	Input	BA30	A DIP Switch to start the transmission of TX.
Walsh_Code_Data	Output	AP31	An SMA port for output data.
LED	Output	AR37	An LED for the state of the storage

Table 3.2 Usage of FPGA pins by the receiver

BCC Receiver			
Net Name	**I/O**	**FPGA Pin**	**Description**
clk_in_p	Input	E19	A signal pair provides create 200 MHz clock on VC707
clk_in_n	Input	E18	
RESET	Input	AV40	CPU RESET button
SWITCH	Input	BA30	A DIP Switch to start the transmission from RX to PC.
AFE_OUT	Input	AN31	An SMA port for the data from the AFE board
RX_DATA	Output	AU36	An output port for UART.
LED	Output	AR37	An LED for the state of the storage

Table 3.3 shows the resource utilization of the proposed BCC transceiver. The utilization of the proposed transceiver uses only 1% of all available resources of the FPGA. A slice is a basic implementation unit. A slice contains a number of LUTs, flip-flops, and logic elements. An LUT means the look-up table for Boolean function implementation. A large number of occupied slices represent that occupied LUTs or flip-flops or logic elements are distributed in FPGA. This situation cause redundancy of clock tree. The number used as memory means the number of LUTs which are used as the memory.

Table 3.3 Resource utilization of the BCC transceiver

Slice Logic Utilization	Used	Available	Utilization
BCC Transmitter			
Number of Slice Registers	1887	607200	1%
Number of Slice LUTs	2261	303600	1%
Number of Occupied Slices	932	75900	1%
Number used as Memory	215	130800	1%
BCC Receiver			
Number of Slice Registers	1389	607200	1%
Number of Slice LUTs	1286	303600	1%
Number of Occupied Slices	711	75900	1%
Number used as Memory	306	130800	1%

3.2 Implemented Information of Xilinx Integrated Synthesis Environment Design Suite

The Xilinx Integrated Synthesis Environment (ISE) design suite is a software tool which can generate the bit stream for FPGAs. It supports the devices which are 7-series FPGAs of Xilinx and their previous generation families. Among the tools, the ISE project navigator, iMPACT, and ChipScope Pro analyzer are used to design, implement, and debug the proposed BCC transceiver.

In the beginning, a new project needs to be created on ISE project navigator. To success generating the bit file, the RTL codes, implementation constraints file, and ChipScope definition and connection file need to be created. The RTL codes are the design of the proposed BCC transceiver. The implementation constraints file shows the connection between the input/output port of the top module of the design and the required pins on the FPGA. For example, it is assumed that the switch 6 of the 8-pole dual in-line package (DIP) switch is used in the design (Table 3.4), and named as "switch" which is an output port in the top module of the design. The command "NET switch LOC="BA30" | IOSTANDARD=LVCMOS18" should be added in the implementation constraints file. The "IOSTANDARD=LVCMOS18" means that the DIP switch uses LVCMOS18 I/O standard. The I/O standard and the mapping tables of FPGA pins are listed in Appendix C of [28].

Table 3.4 8-pole DIP switch connections to FPGA [28]

FPGA Pin	Schematic Net Name
AV30	GPIO_DIP_SW0
AY33	GPIO_DIP_SW1
BA31	GPIO_DIP_SW2
BA32	GPIO_DIP_SW3
AW30	GPIO_DIP_SW4
AY30	GPIO_DIP_SW5
BA30	GPIO_DIP_SW6
BB31	GPIO_DIP_SW7

After completing the RTL codes and implementation constraints file, the debug pins should be connected. The ChipScope definition and connection file is needed to be added. The file uses integrated logic analyzer (ILA) and integrated controller (ICON) to implement the debug cores [30]. Figure 3.1 shows the diagram of the debug core. The ICON connects the JTAG boundary scan port which can connect to the host computer through a JTAG download cable with at most 15 ILAs [30]. The ILA includes trigger ports and data ports and clock port (Figure 3.2). If the trigger ports are triggered, the data ports will save the data immediately into the registers of the ILA. The number of data which can be saved in the register is decided by the setting in the ChipScope definition and connection file. The steps of setting the file are setting the number of trigger ports and data ports (Figure 3.3, Figure 3.4), then setting the trigger ports, data ports, and clock port (Figure 3.5). Finally, the ChipScope definition and connection file is complete.

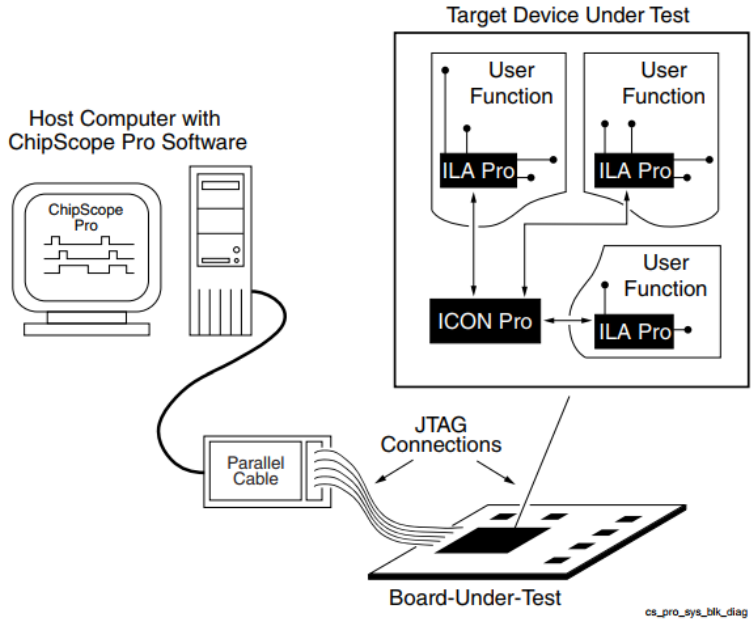


Figure 3.1 Debug core of ChipScope Pro System Block Diagram [30]

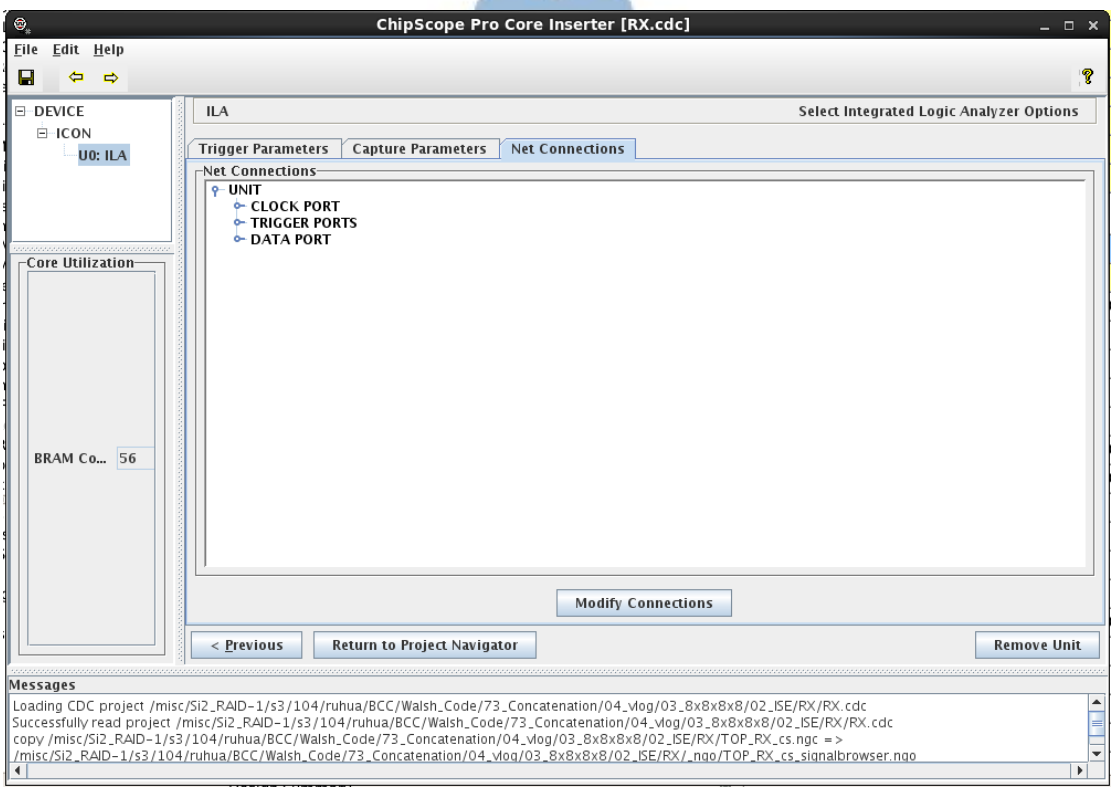


Figure 3.2 An ILA includes trigger ports, clock port, and data ports

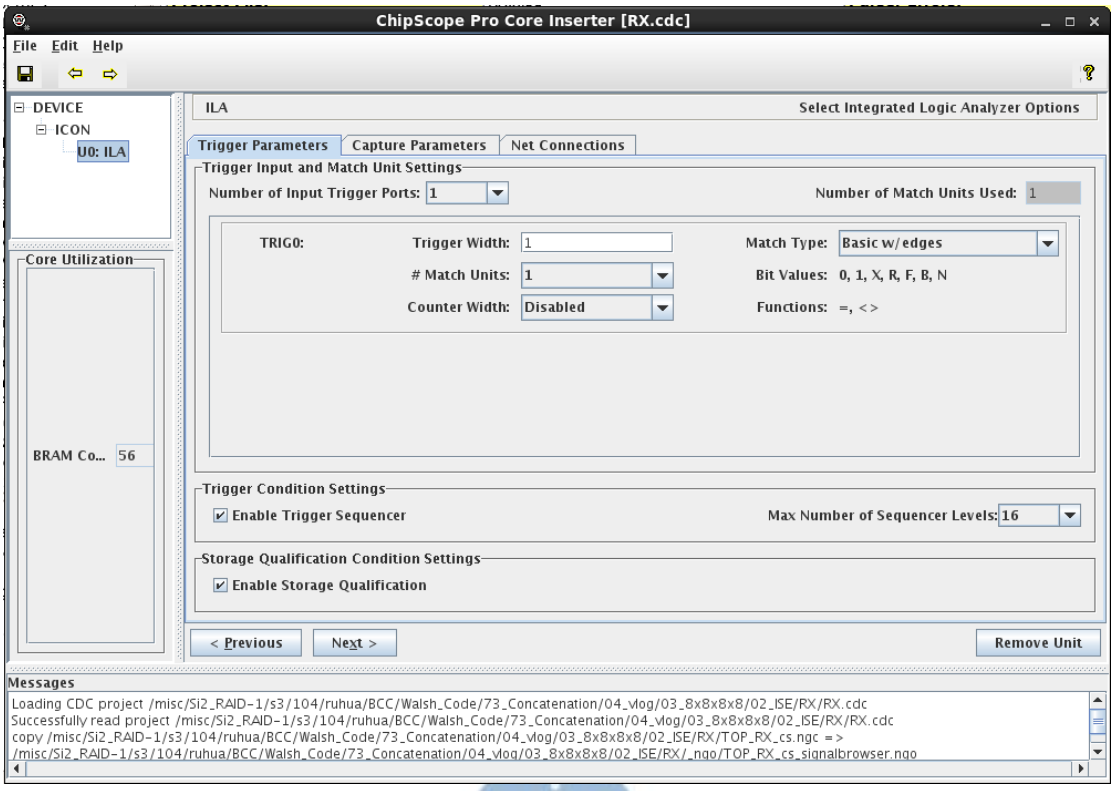


Figure 3.3 Number of trigger ports setting

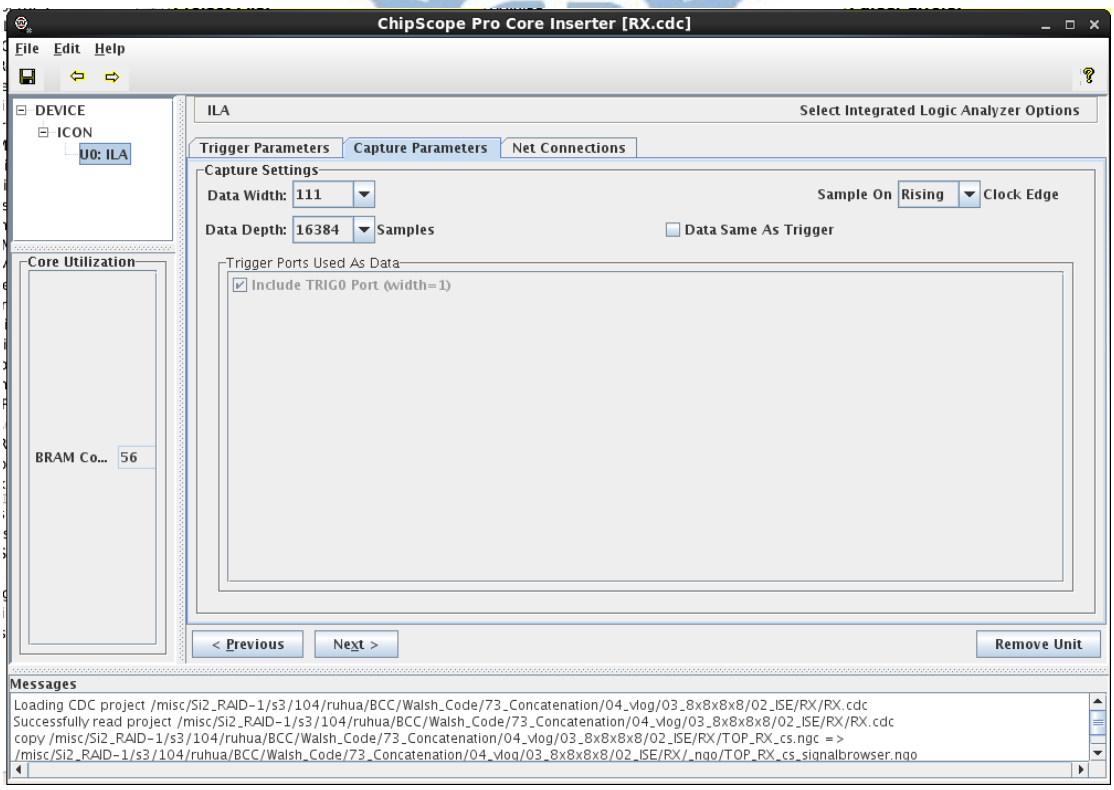


Figure 3.4 Number of data ports setting

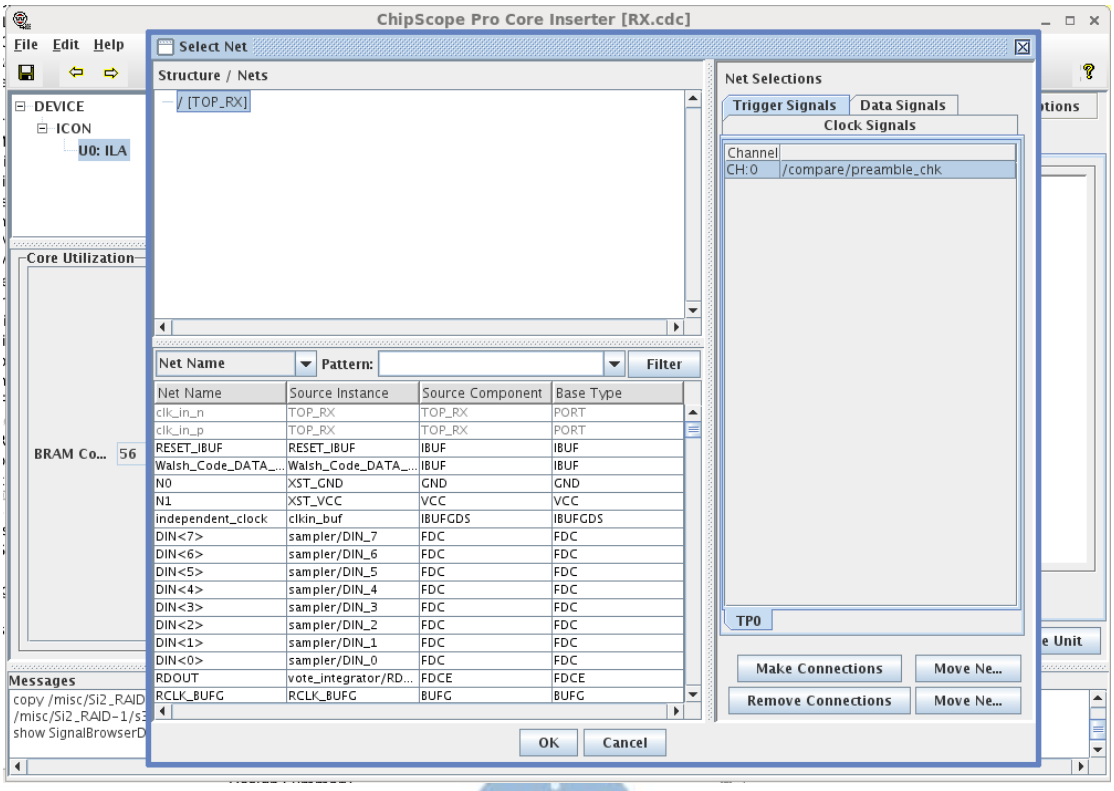


Figure 3.5 The clock port, the trigger ports, and the data ports setting

3.3 Implementation Results

Figure 3.6 shows the BER measurements of the proposed FPGA-based BCC transceiver in RTL simulation with data jitter. There are three lines about using different CID limitation in data transmission without Walsh codes. The line Walsh-code means the performance of the proposed BCC transceiver with Walsh codes. The CID of the proposed design is equal to 2. Figure 3.6 means the data reliability of the proposed design with Walsh codes is much better than the others. At 25 ns peak-to-peak jitter, the proposed BCC transceiver with Walsh codes can achieve BER < 10^{-8}. However, the BCC transceiver with CID=2 can only achieve BER < 10^{-5}.

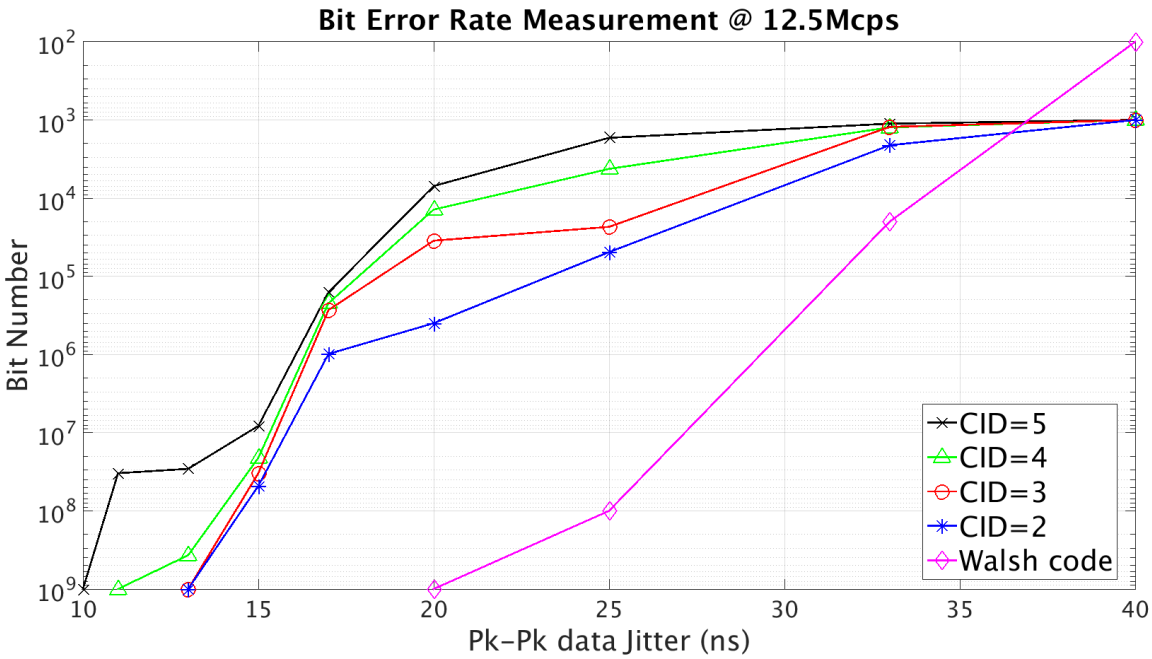


Figure 3.6 Bit error rate measurement of the proposed BCC transceiver in RTL simulation at 12.5 Mcps

Figure 3.7 shows the simulated power spectral density (PSD) of the Walsh codes. In the proposed BCC transceiver, four 16-bit Walsh code are used for data transmission. The PSD shows that the proposed BCC transceiver with Walsh codes has less opportunity to interfere with the other devices.

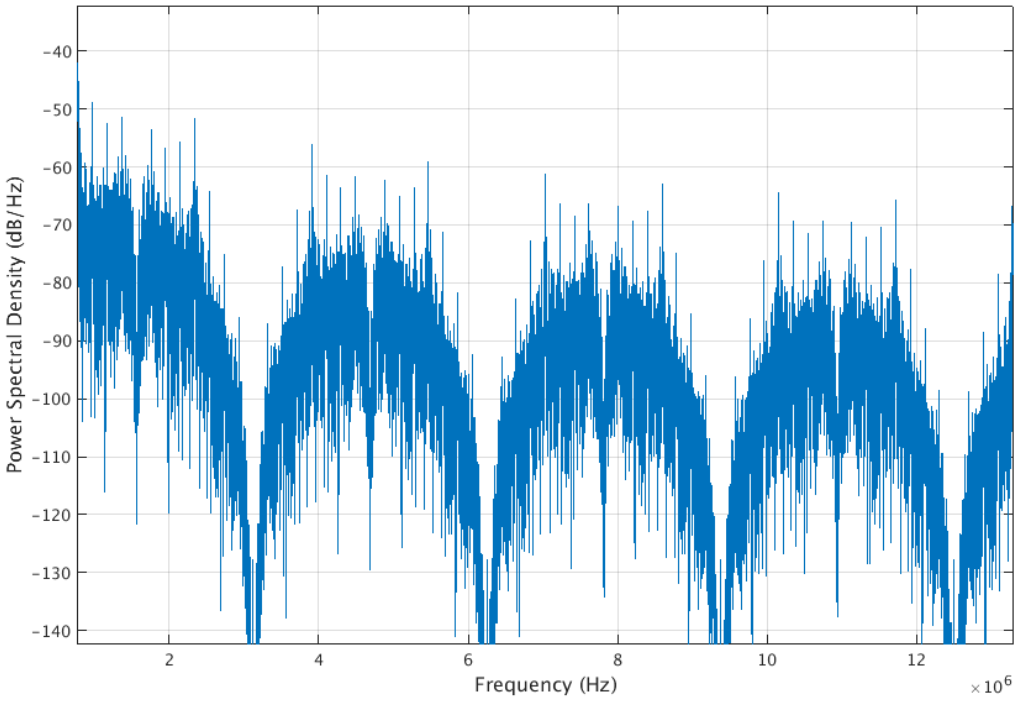


Figure 3.7 The simulated power spectral density of Walsh codes at 6.25 Mcps

Figure 3.8, Figure 3.9, and Figure 3.10 show the measurement result of the received packet number and error bits at 391 Kbps, 781 Kbps, and 1.56 Mbps, respectively. Each packet contains 1000 bits payload and the number of the transmitted packets are over 10^5. The total bits which are transmitted are over 10^8. The error bit at data rate less than 781 Kbps is zero. Although there are error bits at 1.56 Mbps, they are less than 1000 bits and results in a BER < 10^{-5}.

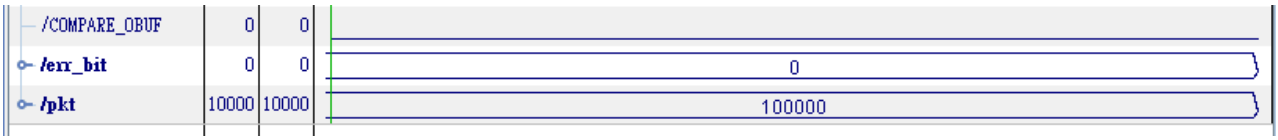


Figure 3.8 Number of packets and error bit at 391 Kbps

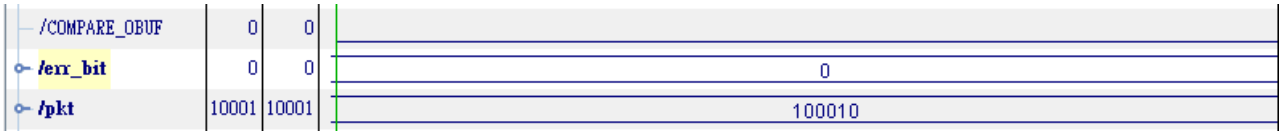


Figure 3.9 Number of packets and error bit at 781 Kbps

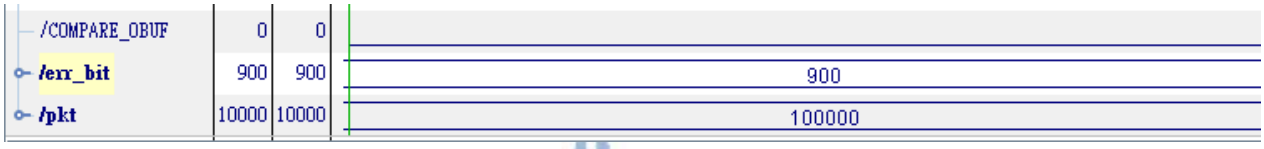


Figure 3.10 Number of packets and error bit at 1.56 Mbps

According to the proposed design, the Walsh code modulator (Table 2.2) raises the data reliability but it also reduces the data rate. In addition, the code rate is $\frac{1}{8}$ ($\frac{length\ of\ modulated\ data}{length\ of\ modulated\ code}$). Therefore, the concatenated methods of Walsh code are presented to solve the problem of data reliability with relatively high data rate. The 4-bit and 8-bit Walsh codes are used in the concatenated methods. Considering of CID limitations, there are three code words can be used from the 4-bit Walsh codes and six code words can be used from the 8-bit Walsh codes (Table 3.5). Then, the new 16-bit modulated codes are concatenated by four 4-bit Walsh codes (Figure 3.11) or two 8-bit Walsh codes (Figure 3.12). The new code words are shown in Table 3.6 and Table3.7. In Figure 3.13, the BER of the four 4-bit Walsh code concatenated method is better than 16-bit Walsh code when pk-pk jitter less than 25 ns. Table 3.8 shows the code rate and Hamming distance of the 16-bit Walsh code and two concatenated methods. The BER

of the four 4-bit Walsh code concatenated method is better than the others. However, the Hamming distance of the four 4-bit Walsh code concatenated method is less than the 16-bit Walsh code. In this situation, the error bits should be often separated in the packet rather than continuous bit errors. The BER simulation result shows that the four 4-bit Walsh code concatenated method has better data reliability than the others even this method has smaller Hamming distance. To verify the BER performance, the four different random data patterns are generated and the simulated BER performance is shown in Figure 3.14. The BER performance is similar with different random data. Figure 3.15 shows the simulated BER of the concatenated method with 16-bit and 24-bit code word. The BER performance of 24-bit concatenated method is similar to 16-bit concatenated methods (Table 3.9). Considering the cost of the concatenated method and the code rate, the 16-bit, four 4-bit Walsh code concatenated method is the best choice.

Table 3.5 Chosen code words of 4-bit Walsh codes and 8-bit Walsh codes for concatenated method

Length of Walsh codes	Code Words
4-bit Walsh codes	0001
	0011
	0110
8-bit Walsh codes	01010101
	00110011
	01100110
	01011010
	00111100
	01101001

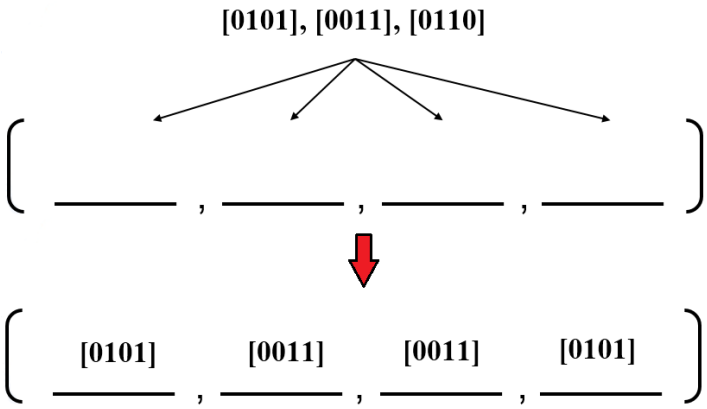


Figure 3.11 An example of 16-bit modulated codes are concatenated by four 4-bit Walsh codes

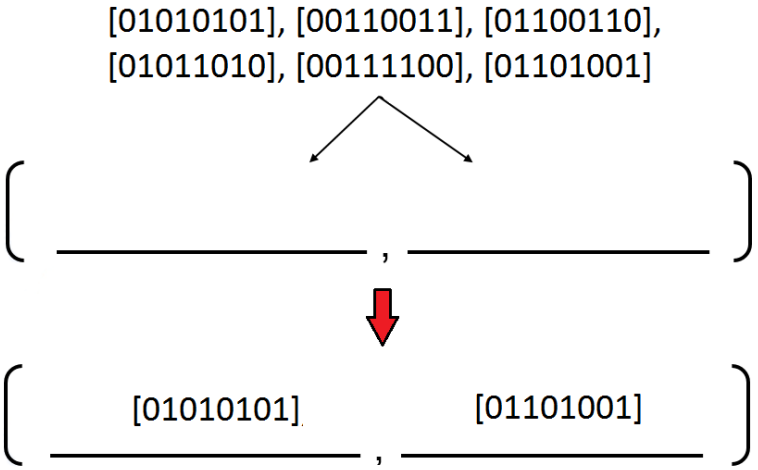


Figure 3.12 An example of 16-bit modulated codes are concatenated by two 8-bit Walsh codes

Table 3.6 The code words of 16-bit, four 4-bit Walsh codes

	Four 4-bit Walsh codes		Four 4-bit Walsh codes
Code 0	0101_0101_0101_0101	Code 16	0101_0110_0101_0101
Code 1	0101_0101_0101_0011	Code 17	0101_0110_0101_0011
Code 2	0101_0101_0101_0110	Code 18	0101_0110_0101_0110
Code 3	0101_0101_0011_0101	Code 19	0101_0110_0110_0101
Code 4	0101_0101_0011_0011	Code 20	0101_0110_0110_0110
Code 5	0101_0101_0011_0110	Code 21	0110_0101_0101_0101
Code 6	0101_0101_0110_0101	Code 22	0110_0101_0101_0011
Code 7	0101_0101_0110_0110	Code 23	0110_0101_0101_0110
Code 8	0101_0011_0101_0101	Code 24	0110_0101_0011_0101
Code 9	0101_0011_0101_0011	Code 25	0110_0101_0011_0011
Code 10	0101_0011_0101_0110	Code 26	0110_0101_0011_0110
Code 11	0101_0011_0011_0101	Code 27	0110_0101_0110_0101
Code 12	0101_0011_0011_0011	Code 28	0110_0101_0110_0110
Code 13	0101_0011_0011_0110	Code 29	0110_0110_0101_0101
Code 14	0101_0011_0110_0101	Code 30	0110_0110_0101_0011
Code 15	0101_0011_0110_0110	Code 31	0110_0110_0101_0110

Table 3.7 The code words of 16-bit, two 8-bit Walsh codes

	Two 8-bit Walsh codes		Two 8-bit Walsh codes
Code 0	01010101_01010101	Code 8	01011010_01010101
Code 1	01010101_01100110	Code 9	01011010_01100110
Code 2	01010101_01011010	Code 10	01011010_01011010
Code 3	01010101_01101001	Code 11	01011010_01101001
Code 4	01100110_01010101	Code 12	01101001_01010101
Code 5	01100110_01100110	Code 13	01101001_01100110
Code 6	01100110_01011010	Code 14	01101001_01011010
Code 7	01100110_01101001	Code 15	01101001_01101001

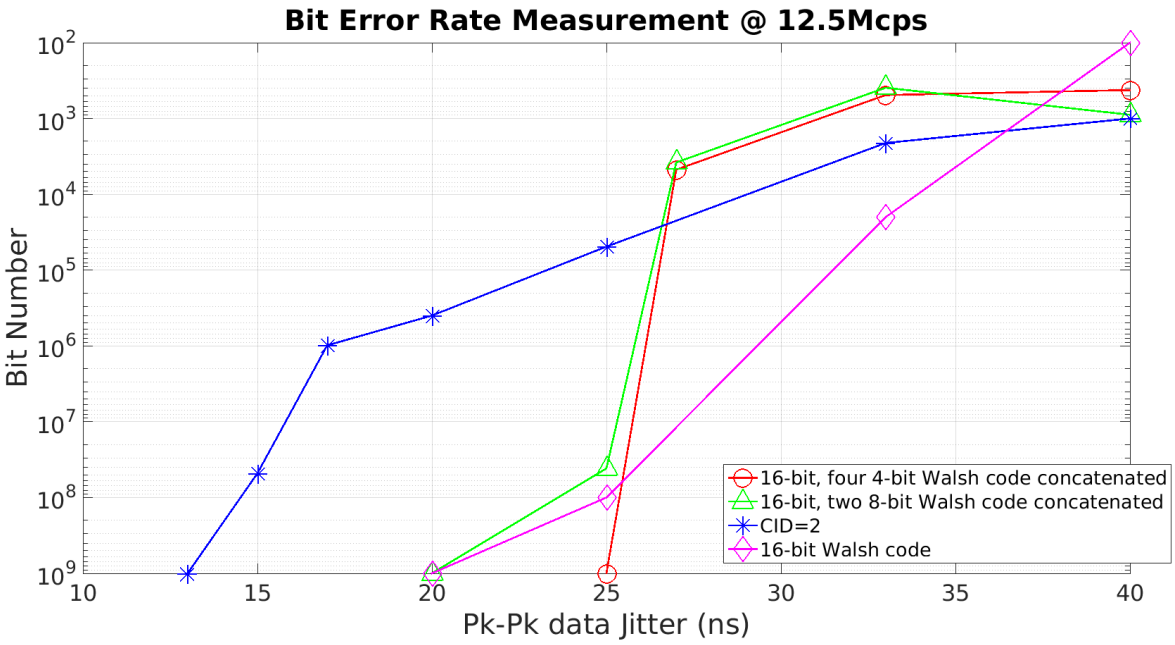


Figure 3.13 Simulated BER of the new concatenated methods and 16-bit Walsh codes

Table 3.8 Code rate and Hamming distance of 16-bit Walsh code, four 4-bit Walsh code concatenated method, and two 8-bit Walsh code concatenated method

	16-bit Walsh code	16-bit, Four 4-bit Walsh code concatenated method	16-bit, two 8-bit Walsh code concatenated method
Code rate	$\frac{1}{8}$ (or $\frac{2}{16}$)	$\frac{5}{16}$	$\frac{1}{4}$ (or $\frac{4}{16}$)
Hamming distance	8	2~8	4~8

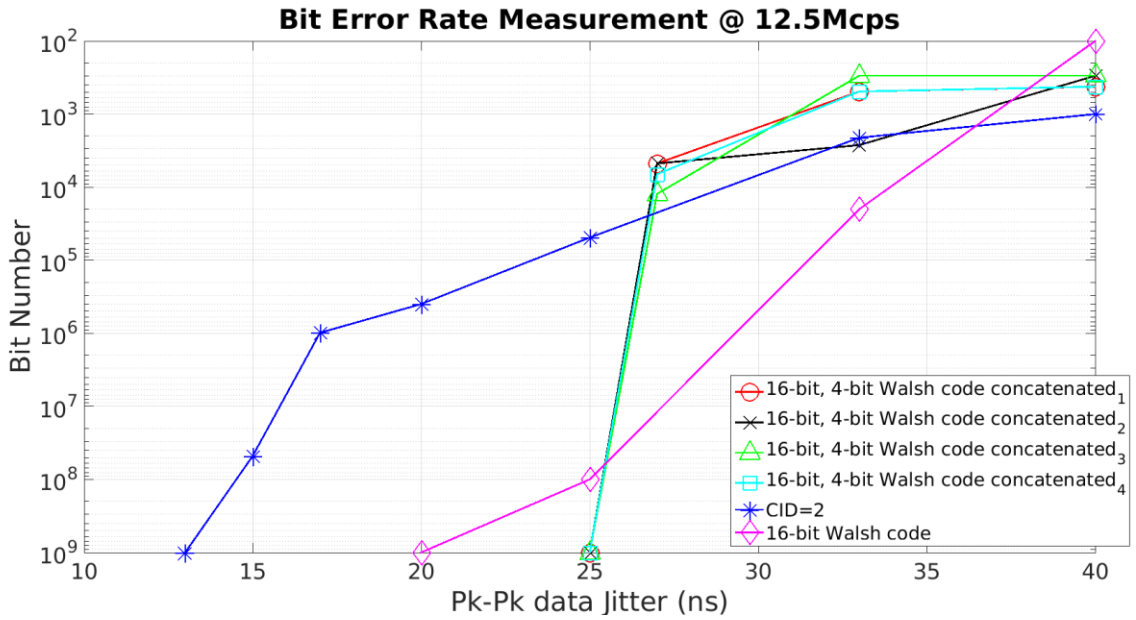


Figure 3.14 Simulated BER of different random data pattern of 16-bit, 4 concatenated method

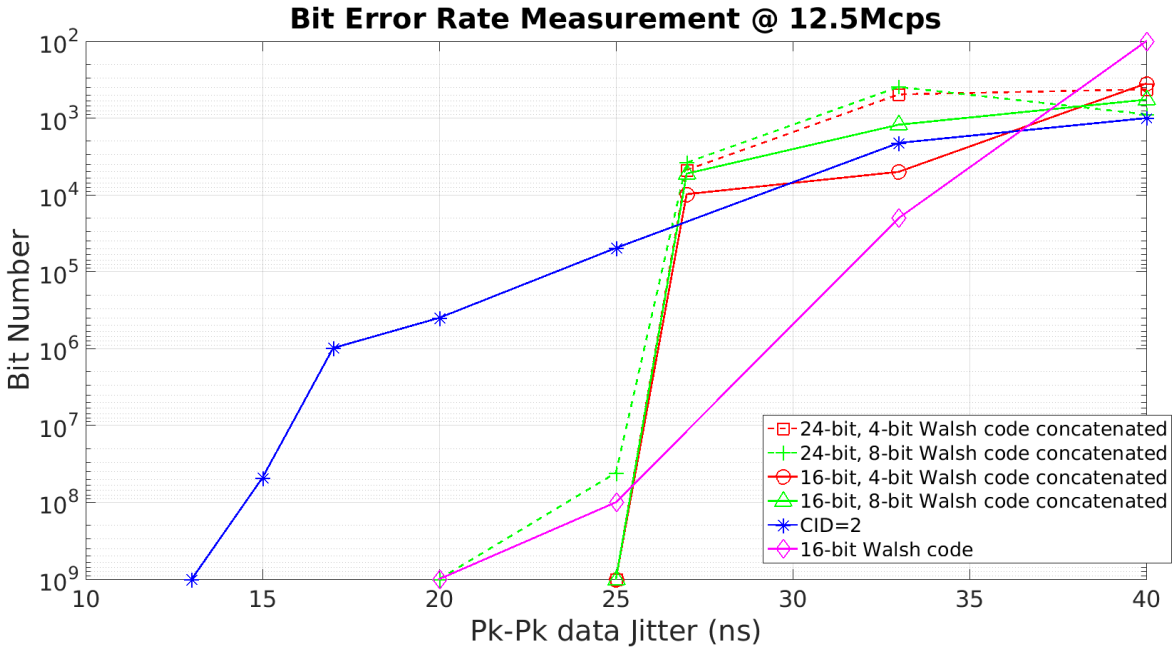


Figure 3.15 Simulated BER of 16-bit, 4/8-bit Walsh code concatenated method and 24-bit, 4/8-bit Walsh code concatenated method

Table 3.9 Code rate and Hamming distance of 24-bit (six 4-bit Walsh code) concatenated method, and three 8-bit Walsh code concatenated method

	24-bit, six 4-bit Walsh code concatenated method	24-bit, three 8-bit Walsh code concatenated method
Code rate	$\frac{7}{24}$	$\frac{1}{4}$
Hamming distance	2~8	4~8

We implement 16-bit, four 4-bit Walsh code concatenated method in replacing the original 16-bit Walsh code in the proposed BCC transceiver. Figure 3.16, Figure 3.17, Figure 3.18, and Figure 3.19 show the measurement results of the received packet number and error bits at 488 Kbps, 976 Kbps, 1.95 Mbps, and 3.9 Mbps, respectively. Each packet contains 1000 bits payload and the number of the transmitted packets are over 10^5. The total bits which are transmitted are over 10^8. The error bit at the data rate less than 1.95 Mbps is zero. Although there are error bits at 3.9 Mbps, they are less than 1000 bits and results in a BER < 10^{-5}.

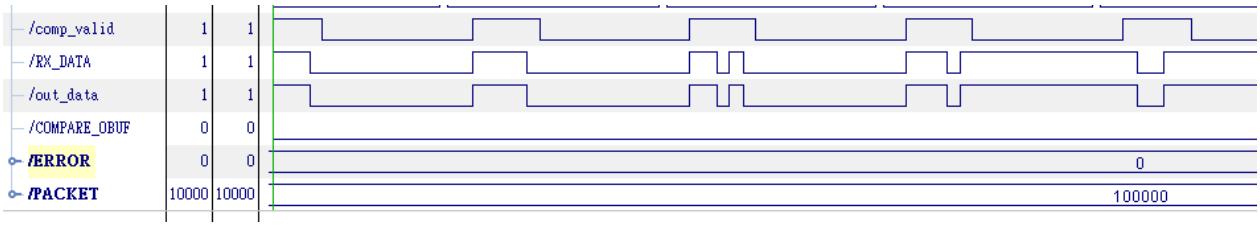


Figure 3.16 Number of packets and error bits at 488 Kbps

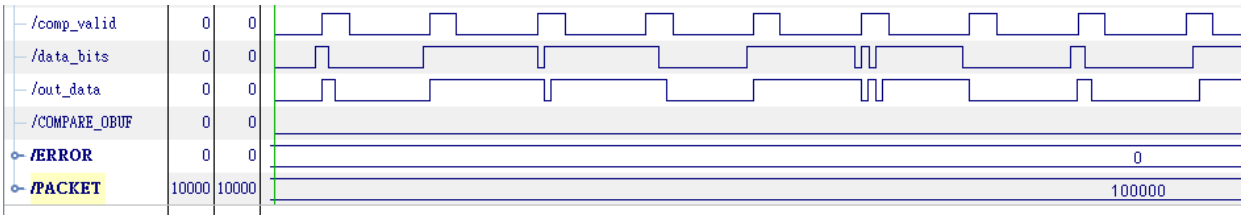


Figure 3.17 Number of packets and error bits at 976 Kbps

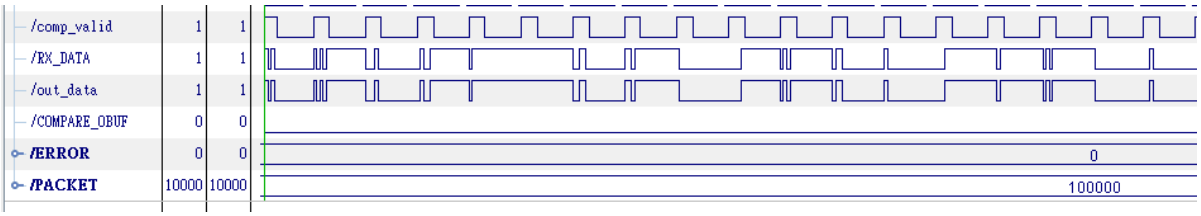


Figure 3.18 Number of packets and error bits at 1.95 Mbps

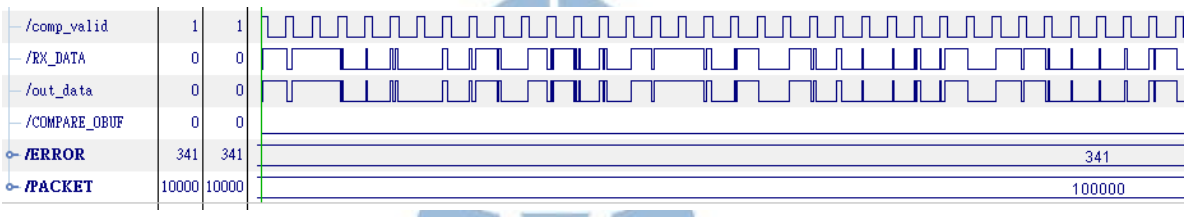


Figure 3.19 Number of packets and error bit at 3.9 Mbps

3.4 Summary

Table 3.10 Summary of proposed 16-bit Walsh code BCC TRX

Data rate	195 Kbps ~ 781 Kbps	1.56 Mbps
Chip rate	1.56 Mcps ~ 6.25 Mcps	12.5 Mcps
Transmission Distance	10 ~ 140 cm	10 ~ 140 cm
Core Voltage	1.0 V (for FPGA)	1.0 V (for FPGA)
Power Consumption	13.5 W (TX) 13.7 W (RX) 0.441 W (AFE circuit)	13.5 W (TX) 13.7 W (RX) 0.441 W (AFE circuit)
Sensitivity	-18.87 dBm	-18.87 dBm
BER	No bit error @ transmitting 10^8 bits	$< 10^{-5}$
Energy/bit	35.391 μJ/b	17.5 μJ/b

Table 3.10 shows the summary of the proposed Walsh code BCC transceiver with original 16-bit Walsh code. The range of data rate is from 195 Kbps to 1.56 Mbps. When data rate is from 195 Kbps to 781 Kbps and there is no bit error after transmitting 10^8 bits. The data rate at 1.56 Mbps have error bits and the BER is 10^{-5}. The maximum transmission distance is 140 cm. The core voltage of VC707 FPGA is 1.0 V. The total power consumption is 27.641 W. The sensitivity is -18.87 dBm and is determined by the AFE board. The energy per bit at two data rate ranges are 31.391 μJ/b and 17.5 μJ/b, respectively.

Table 3.11 Summary of 16-bit, four 4-bit Walsh code concatenated method BCC TRX

Data rate	488 Kbps ~ 1.95 Mbps	3.9 Mbps
Chip rate	1.56 Mcps ~ 6.25 Mcps	12.5 Mcps
Transmission Distance	10 ~ 140 cm	10 ~ 140 cm
Core Voltage	1.0 V (for FPGA)	1.0 V (for FPGA)
Power Consumption	13.5 W (TX) 13.7 W (RX) 0.441 W (AFE circuit)	13.5 W (TX) 13.7 W (RX) 0.441 W (AFE circuit)
Sensitivity	-18.87 dBm	-18.87 dBm
BER	No bit error @ transmitting 10^8 bits	$< 10^{-5}$
Energy/bit	14.174 μJ/b	7.08 μJ/b

Table 3.11 shows the summary of the four 4-bit Walsh code concatenated method of length of 16-bit BCC transceiver. The range of data rate is from 488 Kbps to 3.9 Mbps. When data rate is from 488 Kbps to 1.95 Mbps and there is no bit error after transmitting 10^8 bits. The data rate at 3.9 Mbps have error bits and the BER is 10^{-5}. The maximum transmission distance is 140 cm. The core voltage of VC707 FPGA is 1.0 V. The total power consumption is 27.641 W. The sensitivity is -18.87 dBm and is determined by the AFE board. The energy per bit at two data rate ranges are 14.174 μJ/b and 7.08 μJ/b, respectively.

The proposed BCC transceiver can be applied for the real applications. The data rate of the proposed BCC transceiver using Walsh code and concatenated method is 199 Kbps to 1.56 Mbps and 488 Kbps to 3.9 Mbps, respectively. Table 3.12 shows the data rate of different application. The data rate of the EEG, ECG, video (SDR, 480p), and the video calling.

Table 3.12 Data rate of the applications

	ECG[31]	EEG[32]	Video[33] (SDR, 480p)	Video calling[34]
Dara Rate (Mbps)	0.012	0.5	2.5	1.2

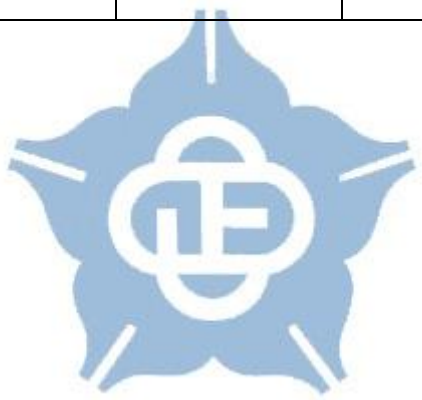


Table 3.13 Comparison table

	[3]	[5]	[27] JSSC'12	[13] ISSCC'13	[15] ISSCC'14	[29] ISSCC'15	Proposed
Process	90 nm	0.13 μm	0.18 μm	0.13 μm	65 nm	65 nm	FPGA
Supply	1V	1.2V	1V	1V	1.1V	1.2V	1.0V
Data Rate	1Mb/s ~ 40Mb/s	5Mb/s	1kb/s ~ 10 Mb/s	164, 328, 656, 1312.5 kb/s	5 Mb/s ~ 60 Mb/s	80 Mb/s	488 Kb/s ~ 3.9 Mb/s
Modulation	Wideband Signaling	Wideband Signaling	Double FSK	FSDT	3-level Walsh Code	Binary Phase Shift Keying	Walsh Code
Sensitivity	-29 dBm	9.6 mV	-66 dBm	N/A	-59 dBm @ 10^{-5} BER	-58 dBm	-18.87 dBm
Power Consumption	1.21 mW (w/o AFE circuit)	0.82 mW	2.4 mW	5.5 mW	1.85 mW	8.9 mW	27.6 W
Area	0.14 nm^2	0.26 nm^2	12.5 mm^2	12.5 mm^2	0.072 mm^2	5.76 mm^2	N/A
BER	< 10^{-8} @ 40Mb/s	N/A	10^{-5} @ 10Mb/s	N/A	10^{-5} @ 30 MHz	< 10^{-5} @40Mb/s	< 10^{-8} @ 1.95 Mb/s < 10^{-5} @3.9 Mb/s
Energy/bit	0.03nJ/b	0.2 nJ/b	0.24 nJ/b	4.19 nJ/b	31 pJ/b	0.079 nJ/b	14.174 μJ/b

In Table 3.13, the proposed BCC transceiver using Walsh codes has better BER than most of the others. However, the data reliability is dependent on transmitting redundant bits of the Walsh codes. For this reason, the data rate of proposed BCC transceiver is lower than others.

4 Conclusion and Future Work

4.1 Conclusion

To design the transceiver for body channel communication, the measurements about BCC characteristics are performed. According to the measurement results, the AFE board is constructed and it includes the voltage gain control and the DC level offset control. Then, the received signals are amplified and recovered the back to the digital waveform.

With the aim of data reliability, the Walsh codes are applied to modulate the output signal from the transmitter. The Walsh codes have the characteristic of orthogonality that each code which has the same length is different in half of the total bits. If the received Walsh code data have the error bits which are less than half of Walsh code length, the data can be recovered back to the correct Walsh code.

The proposed FPGA-based BCC transceiver using Walsh codes has a random data mode and an image mode. In random data mode, the LFSR circuit generates random data as transmitter's input data. In the image mode, the image is transferred as the binary sequence and then sent to the transmitter through UART as input data. The input data are partitioned into 2-bit parallel data then modulated by a 16-bit Walsh code. The code is the output of the transmitter and sent to AFE board through BCC. The receiver will receive the recovered data from AFE board. The 8x oversampling sampler and vote integrator will recover clock and data from receiving signal. Next, the Walsh code demodulator demodulates each 16-bit data into two bits original data. If the random data mode is set, the LFSR checker will compare the demodulated data and the random

data. Otherwise, the data will send to PC through UART and formed to an image.

The Virtex-7 VC707 EVB is used to implement the proposed BCC transceiver. The EVB has a reliable clock generator used as the transceiver system's clock. The EVB supports SMA ports which are the communication bridge between the BCC, the AFE board, and the transceiver. Moreover, the UART port is supported that the PC can send data to EVB that the image can be sent from PC the transmitter or PC to the receiver.

The maximum transmission distance is 140 cm. The maximum data rate of the proposed BCC transceiver using the original Walsh code is achieved at 1.56 Mbps. And the maximum chip rate is achieved at 12.5 Mcps. The tolerance P_k-P_k jitter is less than 100 ns (31.25% UI) and has no error bits. The BER of implementation results is 0 (No error bit) when transmitting at 195 Kbps (1.56 Mcps), 390 Kbps (3.12 Mcps), and 781 Kbps (6.25 Mcps). The BER is less than 10^{-5} when transmitting at 1.56 Mbps (12.5 Mcps).

A Walsh code concatenated method is proposed. This transceiver is achieved at 3.9 Mbps, and the range of data rate is from 488 Kbps to 3.9Mbps. There is no error bit happened when transmits at 488 Kbps(1.56 Mcps) to 1.56 Mbps(6.25 Mcps). The BER is less than 10^{-5} when transmitting at 3.9 Mbps (12.5 Mcps).

4.2 Future Work

The Walsh code modulation raises the data reliability and the maximum chip rate is achieved at 12.5Mcps. However, the data rate still not well enough. To increasing the data rate, the convolution code can be tried to use as the modulated code. The classical convolution codes calculate the input data and the module-2 adders as an output data (Figure 4.1). Therefore, the output data have the relationship to previous data. This characteristic is called memory property and raises the data reliability. The Viterbi algorithm is a simple method to demodulate the convolution code. This algorithm uses the maximum likelihood principle to find the original data pattern.

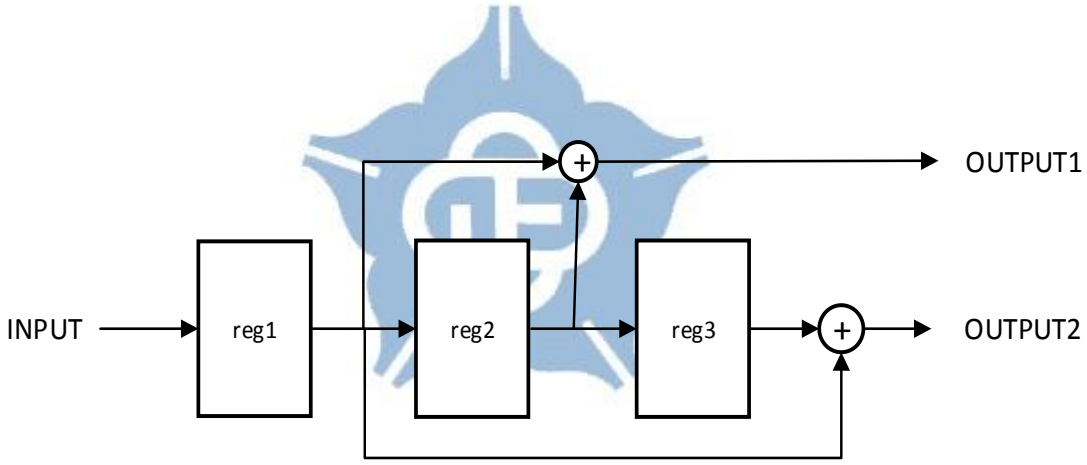


Figure 4.1 A hypothesized convolution code diagram

There are jitters occurred when raising the operating frequency. For the reason, the re-transmitting mechanism can be a choice to solve the bit error pattern. If the error bits are received, the receiver can send the request to the transmitter. The transmitter should transmit the data again by the request from the receiver.

Besides, the utilization of proposed BCC transceiver on VC707 FPGA EVB is very low (Table 3.3). The integrated EVB which has an Artix-7 FPGA, the elements in demand, and the AFE board can be implemented in the new platform of proposed BCC transceiver. The new integrated FPGA EVB has the advantage of the small volume which is the convenience to be carried, low interference by wire between FPGA EVB and AFE board, and low cost. In the new platform, the Bluetooth can be used. The video or image data can be sent from mobile to the transmitter through the Bluetooth interface. Then, the transmitter sends the data through human body to the receiver. Subsequently, the receiver sends the data to another mobile with Bluetooth. This can be a new demonstration system of the BCC transceiver platform.

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