# 國 立 中 正 大 學

## 資訊工程研究所碩士論文

# 可應用於人體通道傳輸且具有快速相位追蹤功能的無參考時脈全數位資料與回復電路設計

# A Fast Phase Tracking Reference-Less All-Digital CDR Circuit for Human Body Channel Communication

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可應用於人體通道傳輸且具有快速相位追蹤功能的無參考時脈全數位資料與回復電路設計A Fast Phase Tracking Reference-Less All-D igital CDR Circuit f or Human Body Channel Communication

經本委員會審查，符合 碩 士學位論文標準。

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# 摘要

隨著科技進步，穿戴式的裝置與個人醫療照護的裝置蓬勃發展。在傳統上，許多醫療的設備，如心電圖、肌電圖皆使用電線來傳遞訊號，對病人來說造成許多不方便，因此無線的人體區域網路開始發展，目前的無線人體區域網路技術透過空氣來傳遞訊號如藍芽、ZigBee，然而都有功率過高以及傳輸速率慢的缺點，因此人體通道傳輸的技術被用於解決這些問題，人體通道傳輸使用人體當成傳輸媒介。人體通道傳輸具有較低的訊號衰減且不容易遭受周遭環境的干擾，此外，人體通道傳輸能達到較高的傳輸速率。

本論文介紹一個寬帶訊號傳收器。在傳送端，資料會使用 NRZI 編碼與位元填充增加資料的變化，且使用封包式傳輸。在接收端，我們採用無參考時脈的資料與回復電路設計，因此可以降低功率的消耗以及減少電路的複雜度，且我們利用多相位來量化相位誤差的方法能夠增加資料與回復電路追蹤能力以及快速的補償相位誤差。此外，在不同的製程、溫度、電壓的變異下，我們所提出的自動校正相位追蹤量方法，能夠計算出補償碼並提供給全數位資料與回復電路控制器，保證在不同的環境變異下，動態地進行控制碼調整增益的補償。

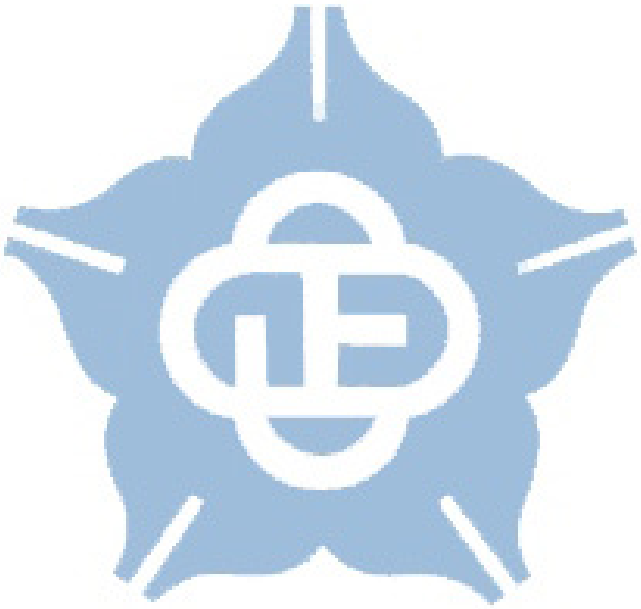
**關鍵字：**人體通道傳輸、資料回復電路、傳收器、全數位鎖相迴路

# Abstract

As technology advances, the wearable personal entertainments and personal healthcare devices are booming. Traditionally, the medical healthcare devices such as electromyography (EMG) and electrocardiography (ECG) use the wireline to transfer the physiological signals, it leads to inconvenient for patients. Therefore, the wireless communication techniques are used to solve this problem. The common type of wireless body area network (WBAN) realization transmits data through the air, such as Bluetooth and ZigBee. However, they have relatively high power consumption and relatively low data rate. Therefore, the body channel communication (BCC) is proposed to solve this problem. The wireless communication transmits the data through the air, but the BCC uses the human body as the communication channel to transmit the data. Moreover, the BCC has relatively low signal attenuation and relatively few interferences in the nearby environment. Furthermore, the BCC can achieve a high data rate.

In this thesis, a wideband signaling (WBS) transceiver is proposed. In transmitter part, the data are modulated by a non-return to zero inverted (NRZI) encoder with a bit stuffer. The data are transmitted in the packet format. In the receiver part, the proposed reference-less clock and data recovery circuit (CDR) can reduce the power consumption and circuit complexity. Moreover, the proposed phase error calculation method uses the multi-phase signals to quantize the phase error. The proposed method can enhance the CDR phase tracking ability and compensate for phase error quickly. The proposed automatically phase track gain calibration method can calculate the gain value for the all-digital CDR (ADCDR) controller. In different process, voltage and temperature (PVT) variations, the gain value will be automatically calibrated.

**Keywords：Body Channel Communication (BCC), clock and data recovery (CDR), transceiver, all-digital phase-locked loop (ADPLL)**



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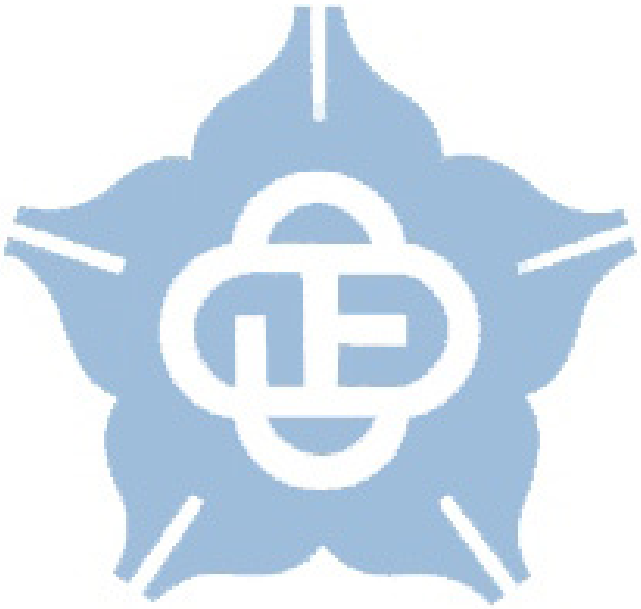

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# Chapter 1 Introduction

## 1.1 Introduction to Body Area Network

As technology advances, the wearable personal entertainments and personal healthcare devices are booming. Traditionally, the medical healthcare devices such as electromyography (EMG) and electrocardiography (ECG) use the wireline to transfer the physiological signals, it leads to inconvenient for patients. Therefore, the wireless communication techniques are used to solve this problem. In addition, IEEE 802.15 Task Group 6 formulated a body area network (BAN) standard [1] which defines the multimedia transportation protocols and the industrial scientific medical (ISM) around the human body.

The common type of wireless BAN (WBAN) realization, such as radio frequency (RF) transmission, transmits data through the air. The most widely used technologies of RF transmission such as Bluetooth and ZigBee which adopting 2.4 GHz ISM band for transmission. ZigBee has low power consumption and is simple in implementation. The data rate of ZigBee is 250Kbps at 2.4GHz, 40Kbps at 915MHz and 20Kbps at 868MHz [2]. However, the transmission distance of ZigBee ranges from 10 meters to 70 meters so it is only suitable for small area transmission. In addition, ZigBee is no for high-speed transmission because its low data rate. Therefore, Bluetooth is more popular than the ZigBee for the RF transmission. However, the RF wireless techniques face some problems, such as high power consumption and interferences with other devices which also using the 2.4GHz ISM band. Moreover, the RF transceiver also suffered from the body shadowing effect [26]. Thus, the body channel communication (BCC) was proposed to solve these problems.

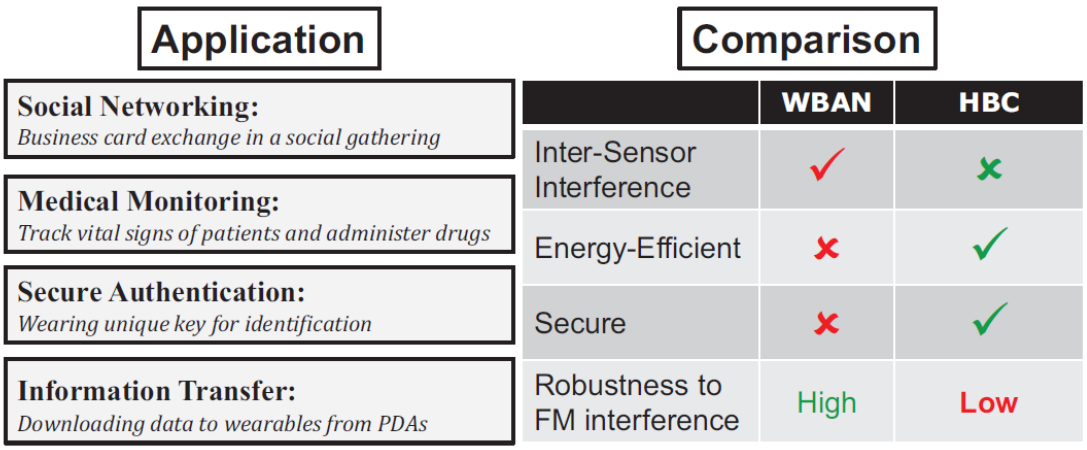



Fig. 1.1 the application of BCC and comparison with WBAN [3]

The BCC is different from the wireless transmission. The wireless transmission transmits the data through the air but the BCC uses the human body to transmit the data. Moreover, the BCC has relatively low signal attenuation and fewer interferences in the nearby environment. Fig. 1.1 shows the applications of the BCC and the comparison with WBAN [3]. Furthermore, the BCC is almost insensitive to the motion of a human [4] and it can achieve a high data rate. The concept of the body channel communication is shown in Fig. 1.2. The model consists of a transmitter (TX) and a receiver (RX), one or two electrodes are attached to the human body. The signal is transmitted through the human body channel from the TX to the RX. The RX recovers the data when it receives the signals sent from the TX.

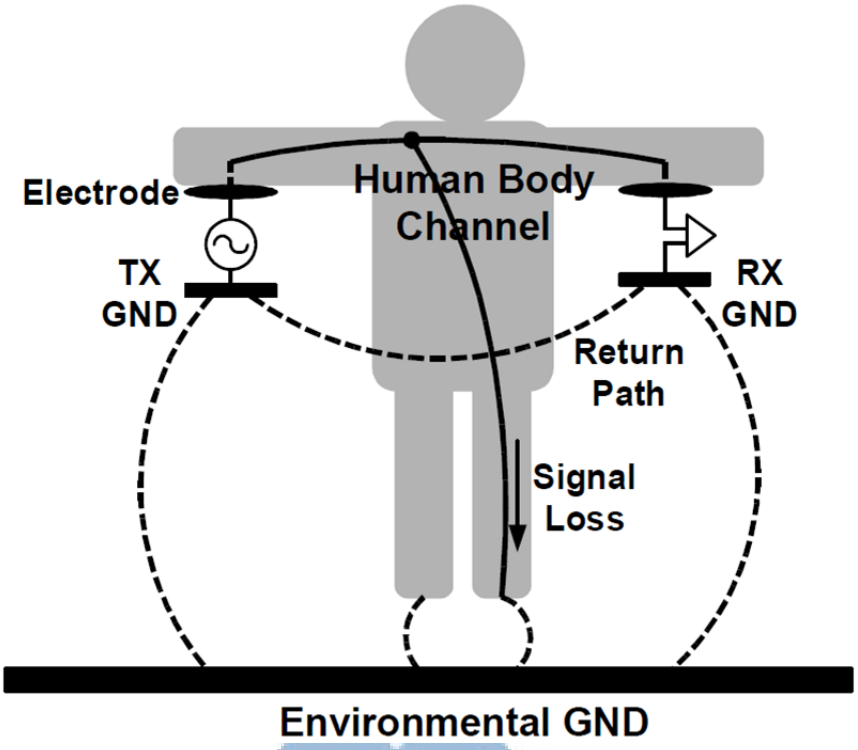



Fig. 1.2: The concept of the body channel communication [5]

One of the BCC applications for binaural hearing aids (BHAs) is shown in Fig. 1.3, and its power distribution is also shown. The wireless transceiver (TRX) for communicating between two ears consumes 80% of the total power of the device because the wireless communication such as Bluetooth and ZigBee have relatively high power consumption. Therefore, the BHAs with the BCC is proposed in [10].

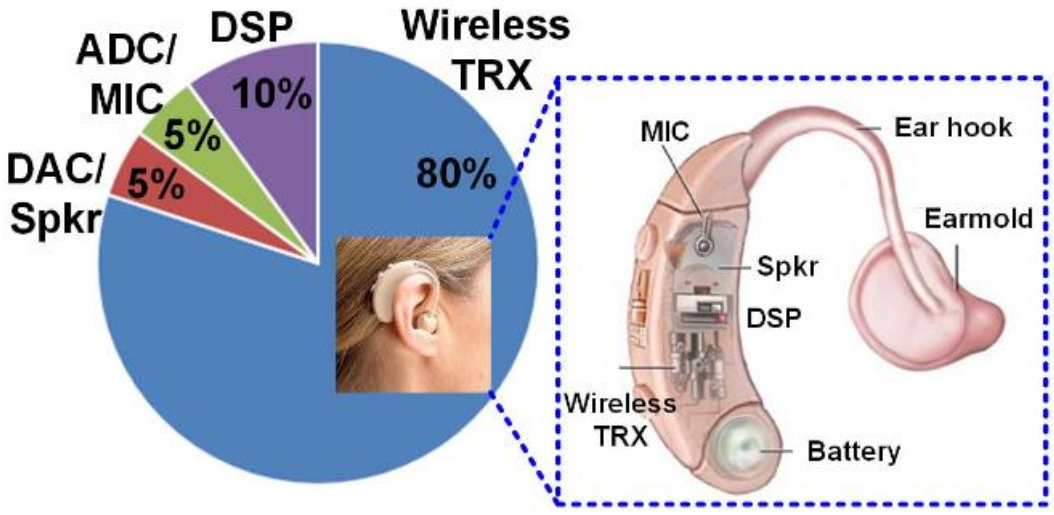



Fig. 1.3: BHAs application and power distribution [10]

Another application of the BCC for on-body communication using the fingerprint sensor on a smartphone is shown in Fig. 1.4. The smartphone can securely send information to the doorknob or the glucose sensor over the body.

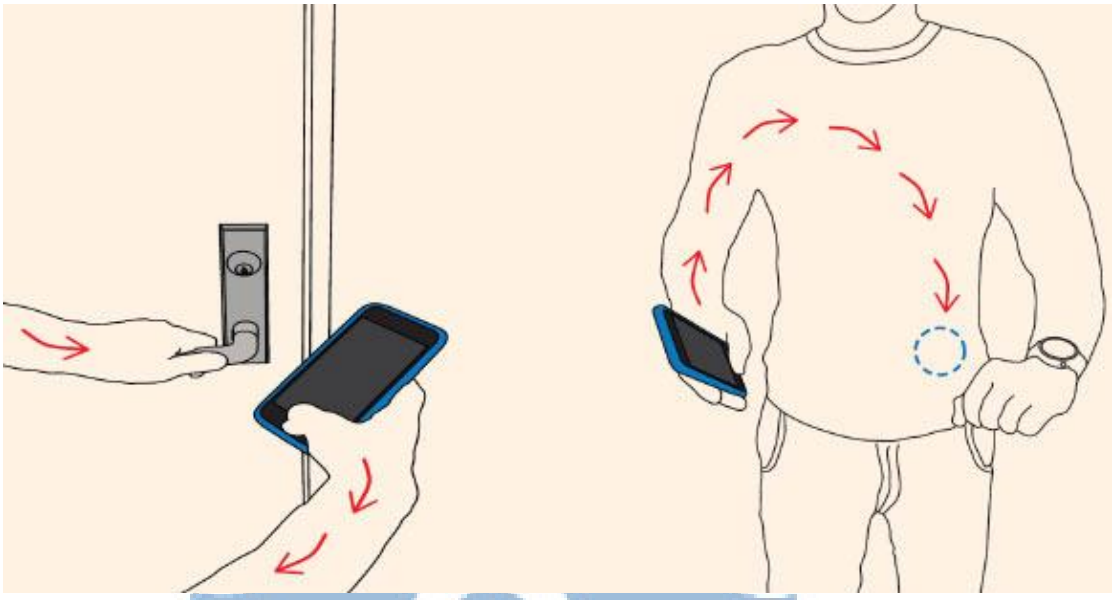


Fig. 1.4: The cell phone applications of the BCC [6]

Table 1.1 shows the requirements for data rate of the biomedical signal processing and multimedia signals. In the biomedical signal processing, the IEEE 802.15.4 standard lists the data rate of the ECG is 0.012 Mbps [41]. In the other application [42], the data rate of the EEG is 0.5Mbps. Therefore, the biomedical signal processing only use a data rate lower than 1Mbps.

However, the multimedia signals must have a high data rate, such as the DVD format, it uses the MPEG2 standard to encode the movie and the demand for the data rate is 10Mbps. When the picture quality increases, the requirement of the data rate will increase accordingly.

Table 1.1: Requirements for data rate of the medical signals and multi-media signals

| | ECG[41] | EEG[42] | MP3 | DVD |
|---|---|---|---|---|
| Data Rate (Mbps) | 0.012 | 0.5 | 0.3 | 8 |

# 1.2 Characteristics of Human Body Channel

In order to build the BCC model for simulation, many researches had analyzed the characteristics of human body channel, such as [7-8, 11-12]. These researches show that the BCC is deeply affected by transmission distance, frequency, and types of the transmission signal. The capacitive coupling HBC model which based on distributed RC topology is in [9], as shown in Fig. 1.5. The transmitted signal is directly coupled to the body skin through an electrode from the TX. The TX ground is floating since one wire communication mechanism is adopted. The return loop is realized by the parasitic capacitor of the surrounding environment. The signal passes through the human body in the form of an electric field and is decoupled by the electrode at the RX ended with the same mechanism. The number of *RC* unit segments depends on the transmission distance.

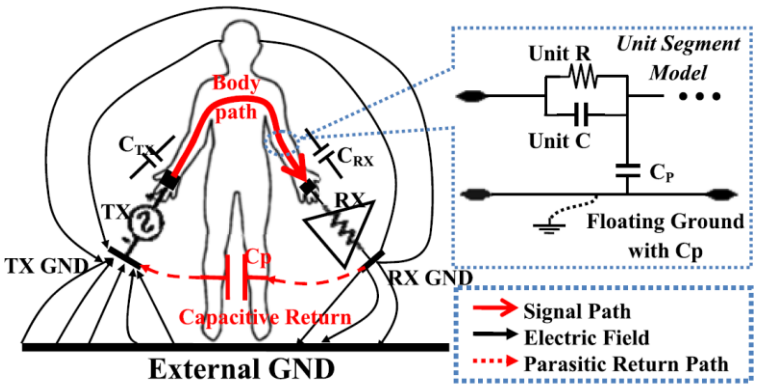



Fig. 1.5: Conventional RC distributed body channel model and IBC scheme [9]

The frequency-domain characteristic of the human body is shown in Fig. 1.6. It measures the BCC transmission with different transmission distance and frequency range, and the signal power is attenuated by the human body channel. Fig. 1.6 shows the measured results and it shows that the signal power attenuation at different transmission distance is very similar at the frequencies lower than 4MHz. This is because the impedance of the human body is extremely small as compared to the impedance of the capacitive return path at low frequencies. However, when the frequencies are higher than 10MHz, the power attenuation are quite different at different transmission distance. The reason is that the impendence of the human body dominates the signal loss at higher frequencies. Therefore, we can know that the BCC is affected by the signal frequency and the transmission distance.

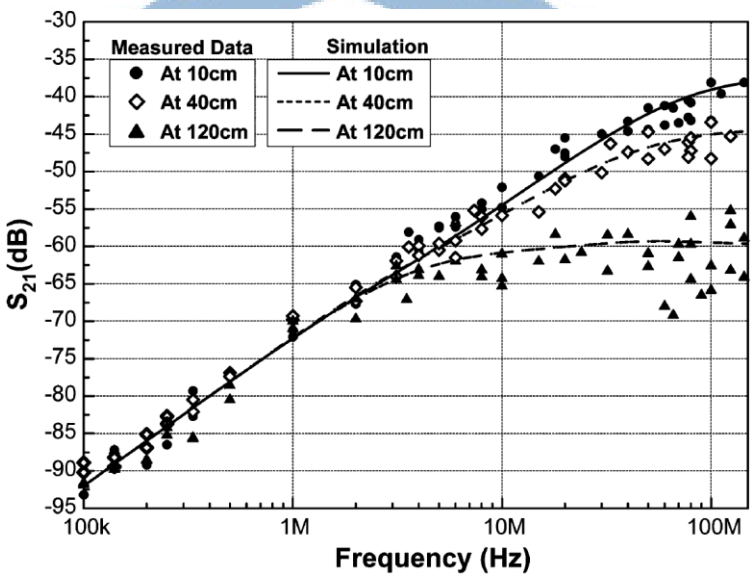



Fig. 1.6: The frequency-domain characteristics of the human body [7]

We also measure the characteristics of the human body to realize the BCC transceiver. The time-domain characteristics with different frequencies at 10 cm transmission distance are shown in Fig. 1.7. The signal generator generates a 1.0 Vpp square waveform signal and then transmits to the human body. The received signal through human body has the lower peak value at the higher frequency and looks like a

shark fins waveform. Thus, the received signal requires an analog front-end (AFE) circuit to amplify and recover the signal. The AFE circuit consists of a variable gain amplifier (VGA) and a Schmitt trigger. Firstly, the received signal must be amplified by the VGA. Then, by setting the threshold voltage of the Schmitt trigger, the received signal can be recovered back to digital waveforms, as shown in Fig. 1.8.

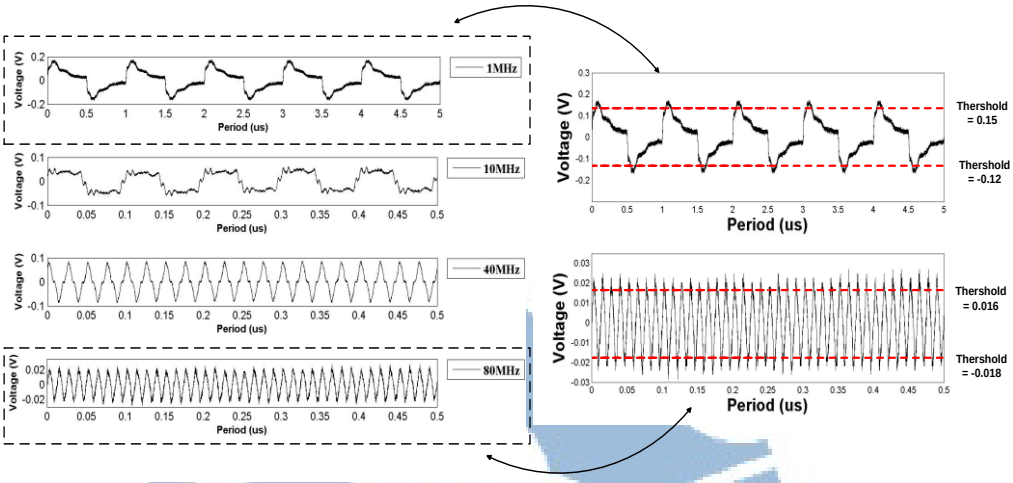



Fig. 1.7: The time-domain characteristics with different frequencies at 10 cm [24]

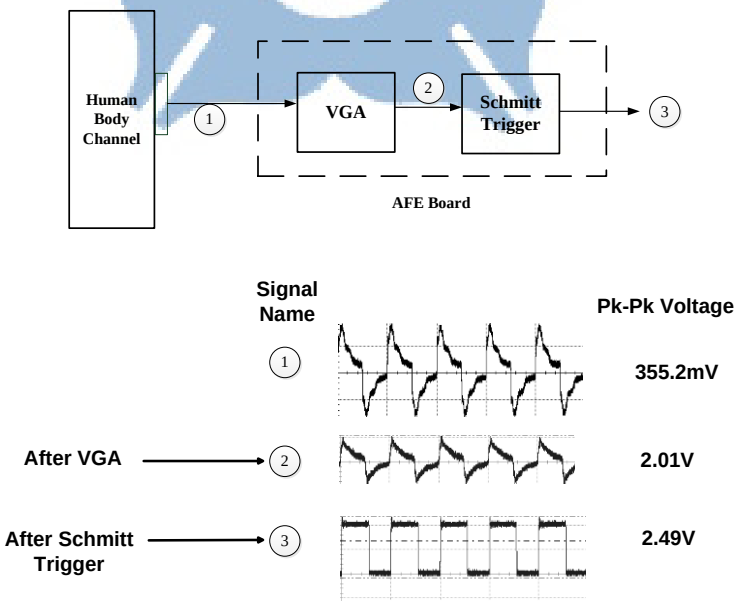



Fig. 1.8: The block diagram and the recovery operation of the AFE circuit [24]

Fig. 1.9 shows the frequency-domain characteristics of six different individuals at 10 cm transmission distance. Fig. 1.10 shows the frequency-domain characteristic of six different individuals at 140cm. The signal generator generates the 1.0 Vpp square waveform signal and then sent to human body channel, and then we measure the received signal at RX electrode. According to the measurement result, we know there has relatively large power attenuation at 20-30MHz.

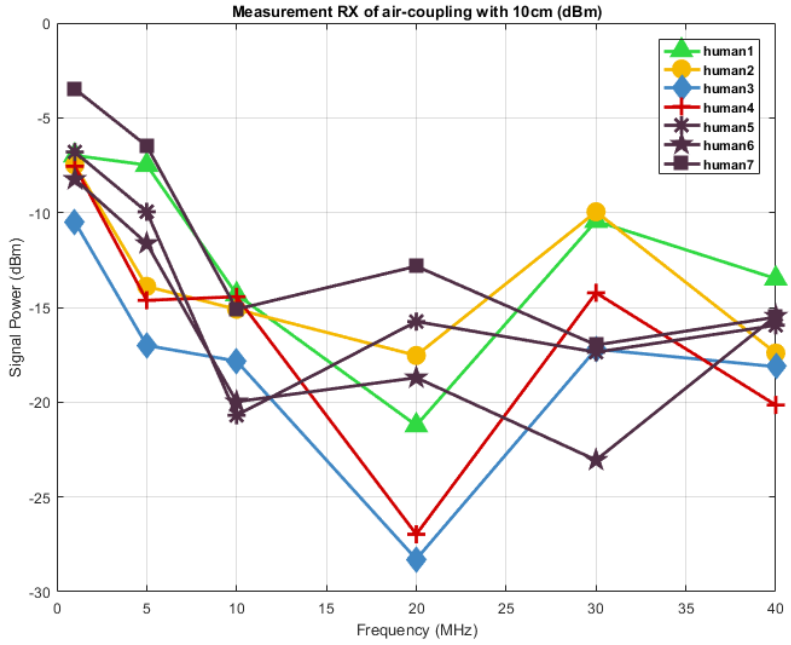



Fig. 1.9: Frequency-domain characteristic with different individuals at 10 cm

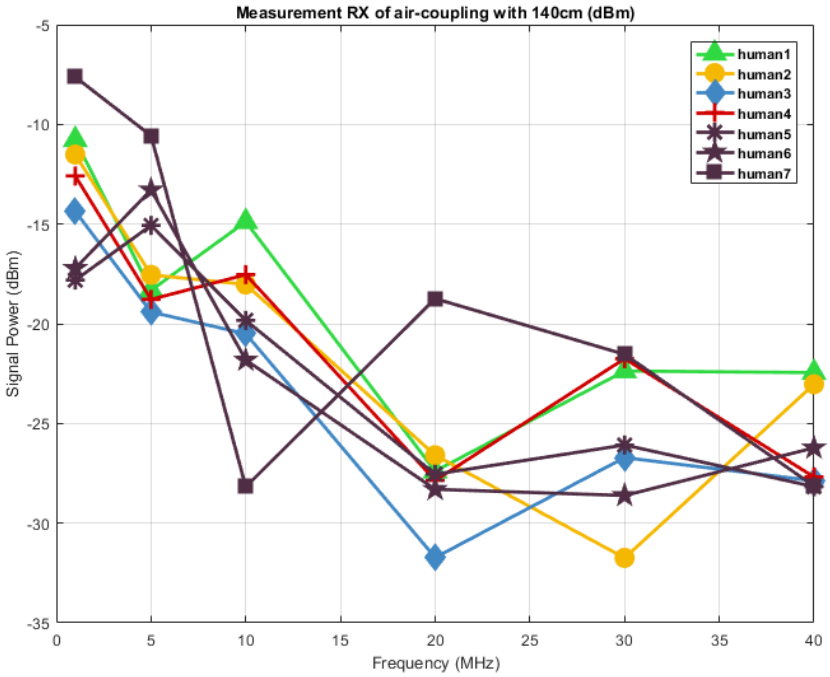



Fig. 1.10: Frequency-domain characteristic with different individuals at 140cm

In time domain analysis, a clock signal is transmitted to the human body and then recovered by the AFE circuit. Therefore, we measure the jitter effect of the received the signal which recovered by the AFE circuit in different frequencies and distances. Furthermore, we can use the result to build the jitter model of the BCC for realizing the BCC transceiver. Table 1.2 shows the summary of the jitter measurement results [13]. The result shows the magnitude of the jitter effect in different frequencies and distances. The peak-to-peak jitter is specified in Unit Intervals (UI), and one UI is equal to the symbol period.

Table 1.2: Summary of the jitter measurement results [13]

| **Distance** | **Frequency** | **Input Voltage** | **Period** | **Period Jitter Peak-to-Peak** | **Period Jitter RMS** | **Cycle-to-Cycle Jitter RMS** |
|---|---|---|---|---|---|---|
| 10 cm | 1 MHz | 1.0 Vpp | 999.99 ns | 3.9 ns (3.9% UI) | 471.7 ps (0.05% UI) | 849.92 ps (0.08% UI) |
| | 10 MHz | | 99.99 ns | 3.65 ns (3.65% UI) | 271.3 ps (0.27% UI) | 465.09 ps (0.47% UI) |
| | 20 MHz | | 49.99 ns | 3.05 ns (6.01% UI) | 314.4 ps (0.63% UI) | 485.63 ps (0.97% UI) |
| | 30 MHz | | 33.33 ns | 1.5 ns (4.50% UI) | 160.1 ps (0.48% UI) | 295.92 ps (0.89% UI) |
| | 40 MHz | | 25.01 ns | 2.6 ns (10.39% UI) | 155.6 ps (0.62% UI) | 845.55 ps (3.38% UI) |
| 140 cm | 1 MHz | | 999.88 ns | 43.5 ns (4.35% UI) | 3.5 ns (0.35% UI) | 5.63 ns (0.56% UI) |
| | 10 MHz | | 99.96 ns | 10 ns (10% UI) | 1.1 ns (1.1% UI) | 1.78 ns (1.78% UI) |
| | 20 MHz | | 49.99 ns | 3.4 ns (6.8% UI) | 253.6 ps (0.5% UI) | 467.95 ps (0.94% UI) |
| | 30 MHz | | 33.35 ns | 1.72 ns (5.15% UI) | 219 ps (0.66% UI) | 2.13 ns (6.39% UI) |
| | 40 MHz | | 25.42 ns | 7.1 ns (27.93% UI) | 643 ps (2.53% UI) | 4.33 ns (17% UI) |

# 1.3 Prior Body Channel Communication Transceivers

## 1.3.1 Basic architecture of a BCC Transceiver

Fig. 1.11 shows the block diagram of the BCC transmitter. The transmitter consists of a data generator, an encoder, a modulator, a driver, and a transmitter (TX) electrode. Firstly, the data generator generates the data to the encoder and modulator. Then, the transmit data are encoded and modulated. Finally, the modulated data are transmitted to the human body channel through the driver and the TX electrode.

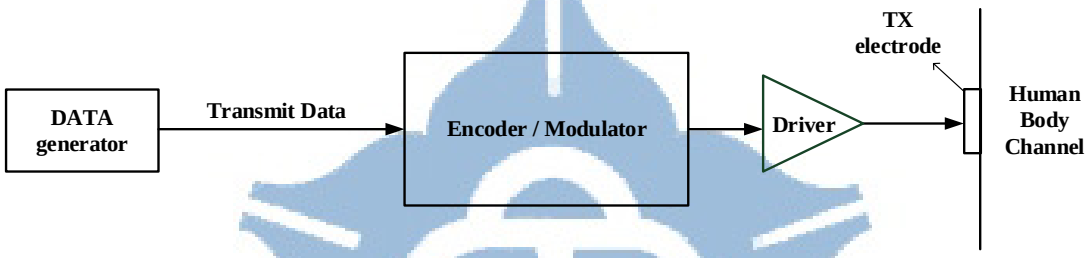



Fig. 1.11: Block diagram of BCC transmitter

Fig. 1.12 shows the block diagram of BCC receiver. The receiver is composed of a receiver (RX) electrode, an analog front end (AFE) circuit, a clock and data recovery (CDR) circuit, a demodulator, and a decoder. Firstly, the received signal is recovered to the digital waveform by the AFE circuit. Then, the CDR circuit recovers the clock and the incoming data. Finally, the demodulator and decoder can demodulate the encoded data to the original data.

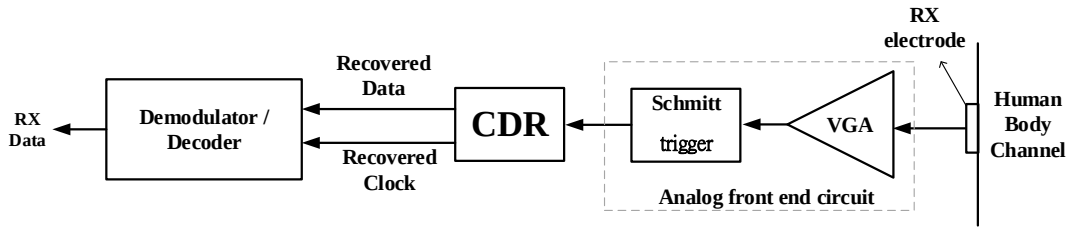



Fig. 1.12: Block diagram of BCC receiver

## 1.3.2 Modulation Scheme: Frequency/Amplitude - Shift Keying

The frequency-shift keying (FSK) is a modulation scheme which uses two different frequencies to represent two binary values. Many body channel communication transceivers based on FSK modulation have been proposed, such as [16], [21], [25].

Fig. 1.13 shows the architecture of the BCC with FSK modulation, in the receiving mode during the time period of t1, the 312 Kbps FSK-modulated signal (data 0: 72 MHz, data 1: 80 MHz) received from the electrodes is amplified by front-end amplifiers. According to the frequencies (72 and 80 MHz) of the amplified signal, the IL-DCO is injection-locked by 80 MHz or injection-pulled by 72 MHz signals. Then, the output of the oscillator is directly fed to the envelope detector to take advantage of the frequency-to-envelope conversion caused by the IL-DCO. Finally, the baseband circuit detect whether injection-locking occurs or not by means of the envelope signal and demodulates the data.

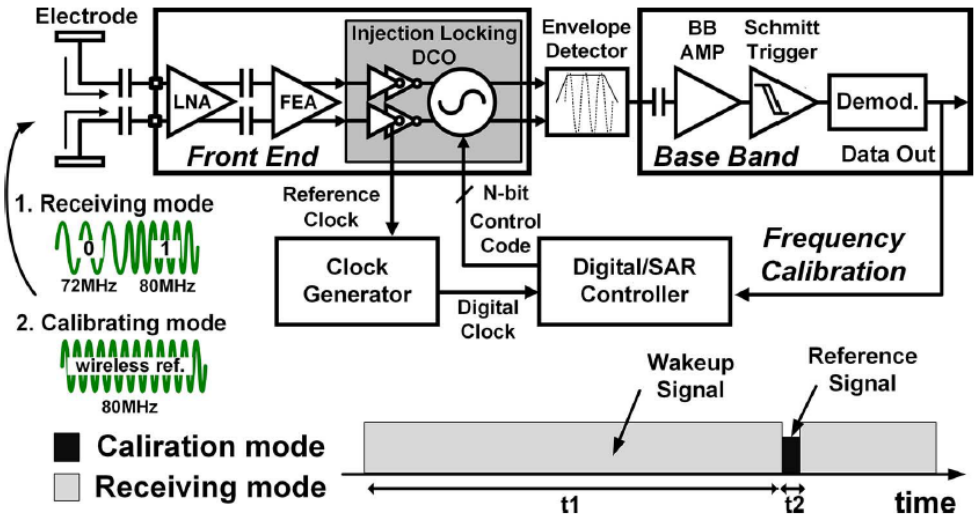



Fig. 1.13: Receiver architecture of the FSK modulation [21]

Fig. 1.14 shows another transceiver architecture of FSK modulation [16]. In the

transmitter, using the frequency synthesizer to generate the stable frequency to calibrate DCO frequency. Then, the TX data is modulated by the double-FSK modulator. In the receiver, the received signals are amplified by the LNA amplifier. Then, the received signals are converted and the low-frequency direct conversion receiver demodulates the sub-band signal into RX data. In addition, the injection-locking digitally controlled oscillator (IL-DCO) and injection-locking detector (IL-detector) are adopted for calibrating.

Fig. 1.15 shows the double-FSK modulation with frequency bands in [16]. The data are modulated with a low modulation index (500 kHz-2.5 MHz) by the sub-band FSK modulator. Then, by using the wideband FSK modulator, data are transformed to a high-modulation-index (40-120 MHz). Multiple users can share the same wideband signal, but distinguish themselves according to different subcarrier frequencies in the sub-band. Although the transceiver has higher data rate (10Mbps), it has a large chip area and has high power consumption.

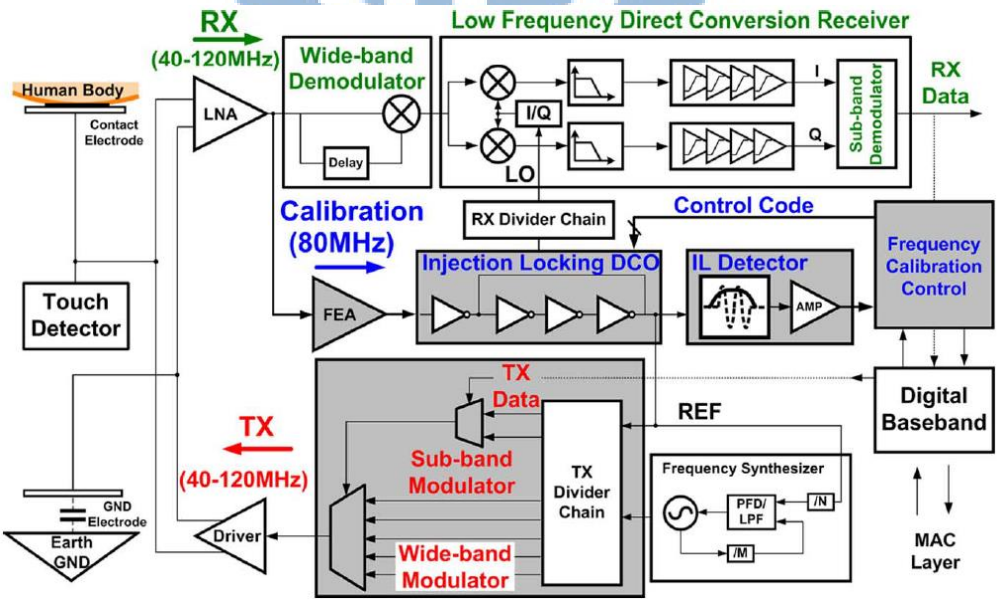



Fig. 1.14: Transceiver architecture of double-FSK modulation [16]

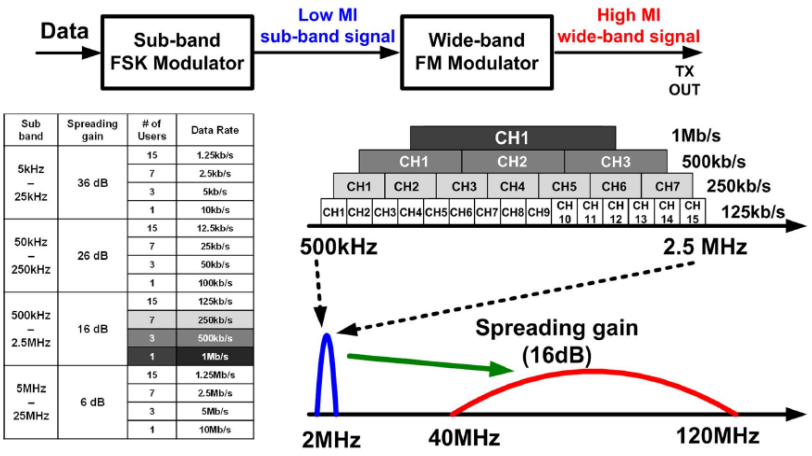



Fig. 1.15: Double-FSK modulation with frequency bands [16]

Another modulation is binary phase shift keying (BPSK). The BPSK is similar to FSK and it uses the phase to distinguish data. A full-duplex body channel communication transceiver with the BPSK is proposed in [19]. It has a low-speed mode and high-speed mode. It uses the 13.56 MHz ISM band to realize low-speed communication for healthcare mode (HC-mode). In addition, it uses two channels of 40 MHz, one centered at 40 MHz and the other at 160 MHz to realize the high-speed communication for entertainment mode (ET-mode), as shown in Fig. 1.16.

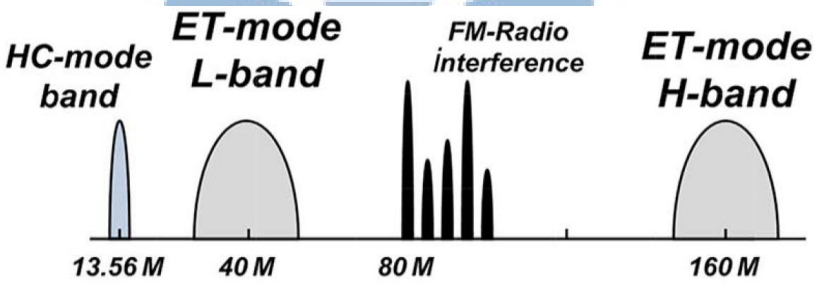



Fig. 1.16: Frequency plan [19]

Fig.1.17 shows the dual mode transceiver architecture in [19]. In HC-mode, the transmitter operates at the 100Kbps data rate based on-off keying (OOK) modulation. The OOK modulation uses with the frequency and without frequency to distinguish data. The super-regenerative receiver configuration with an RC oscillator is adopted to realize the receiver in order to achieve high-quality factor and low power consumption. In ET-mode, it provides full-duplex communication and achieves 80

Mbps data rate with BPSK modulation. When one of the band is set to the TX, another band is set to the RX. Both of 40 MHz band (L-band) and 160 MHz band (H-band) are combined in order to maximize the data rate and avoid the FM-radio (80MHz-100MHz) interferences. However, the L-band and H-band cost the much chip area.

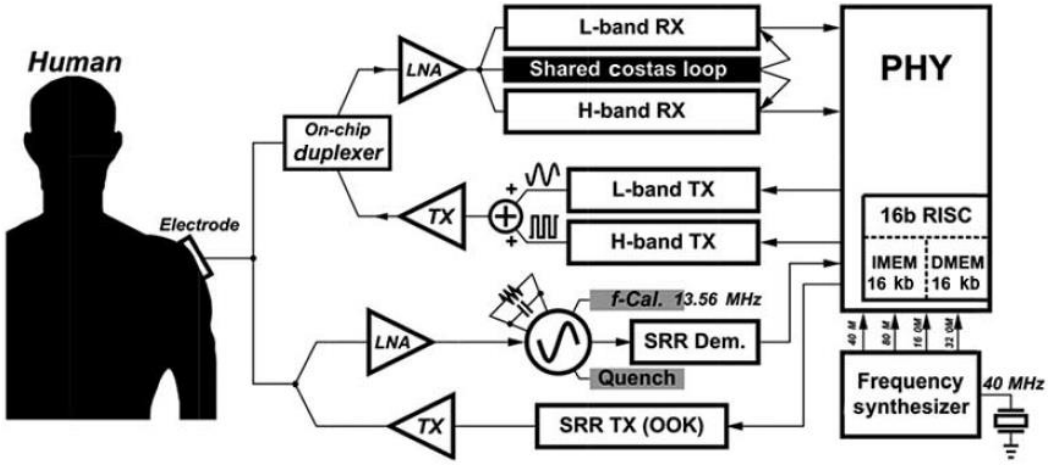



Fig. 1.17: Dual-mode transceiver architecture [19]

## 1.3.3 Modulation Scheme: OFDM

Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. An OFDM signal consists of a number of closely space modulated carriers. In [10], an OFDM-based BCC transceiver for the BHAs is proposed. Fig. 1.18 shows the pseudo OFDM (P-OFDM) baseband transceiver. In the transmitter, the input data are grouped into lower data rate streams that are transmitted concurrently over 64 subcarriers and generate the different constellation points using the 16-QAM. Then, these constellation points are modulated by the IFFT block and are sent to the receiver. Finally, the data can be demodulated in the receiver.

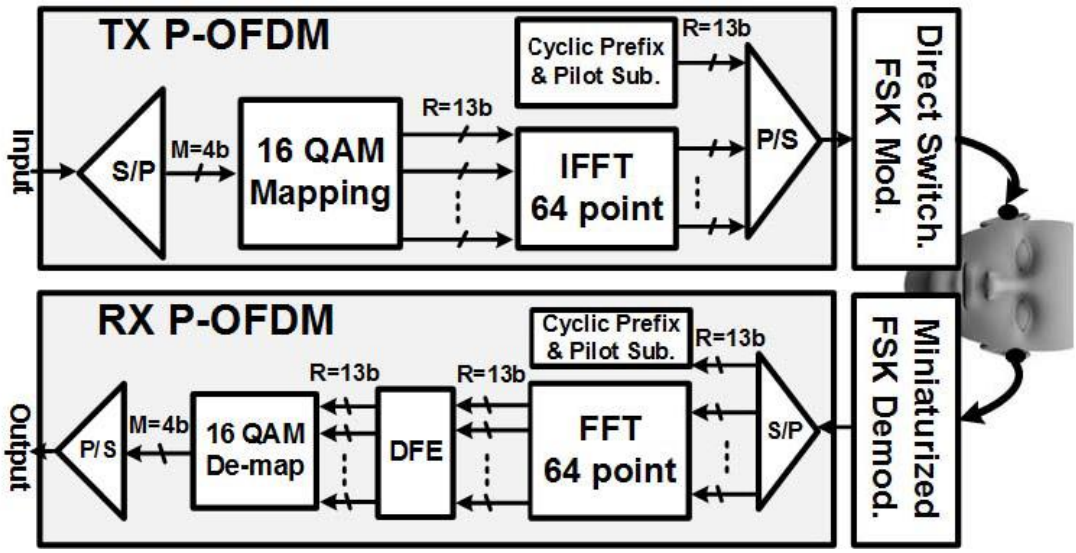



Fig. 1.18: The P-OFDM transceiver block diagram [10]

In addition, the OFDM modulation has the advantage of high data rate and high spectral efficiency properties. In [14], the transceiver uses the OFDM modulation to enhance data rate and it can support the data rate up to 29.1 Mbps. Fig. 1.19 shows the architecture of the OFDM-based transceiver. Before the transmission is started, the data will be encoded by the encoder. Then, it can select either lower order (QPSK) or higher order (16-QAM) modulation. Later, the data will be transformed by the IFFT and be sent to the receiver. In addition, most of the modules in the transceiver operates at the 0.5V environment, voltage scaling and clock-gating technique are adopted to reduce the power consumption. However, the OFDM-based BCC transceiver has high power consumption and occupies large chip area.

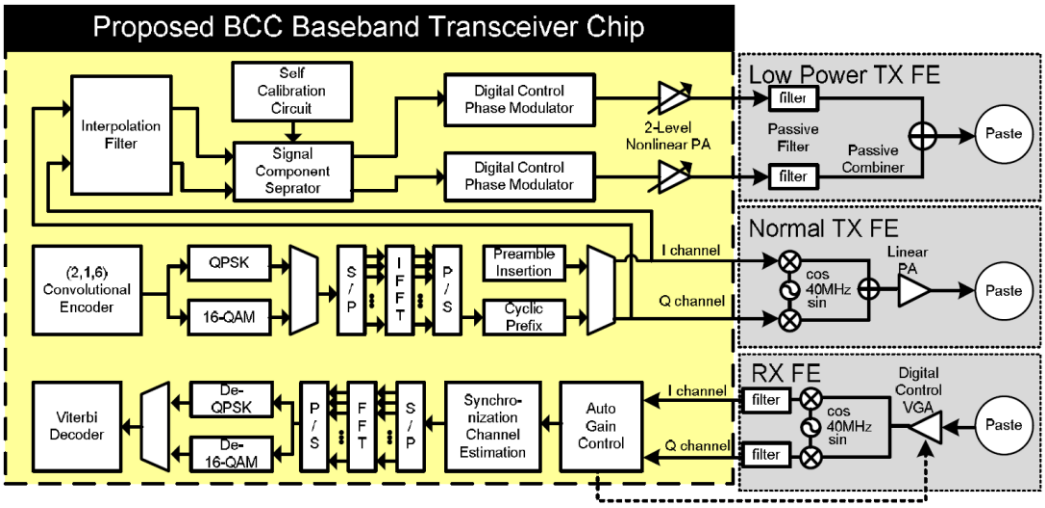



Fig. 1.19: OFDM baseband transceiver [14]

## 1.3.4 Modulation Scheme: Frequency Selective Digital Transmission

Another modulation scheme is called frequency selective digital transmission (FSDT) [39]. The FSDT is a modulation that selects some of the frequencies with characteristics and use the frequency to transmit the data. In [39], a highly flexible FSDT transmitter that supports both data scalability and low power operation with the aid of two novel implementation methods is presented. Fig. 1.20 shows the transceiver architecture of FSDT modulation. In the transmitter, the digital data will be spread with Walsh code and the digital data is amplified using a PA before the data is transmitted through an electrode to the body channel. In the receiver, the RX front end circuit and CDR will recover the Walsh-code data and uses the level detector to distinguish the data.

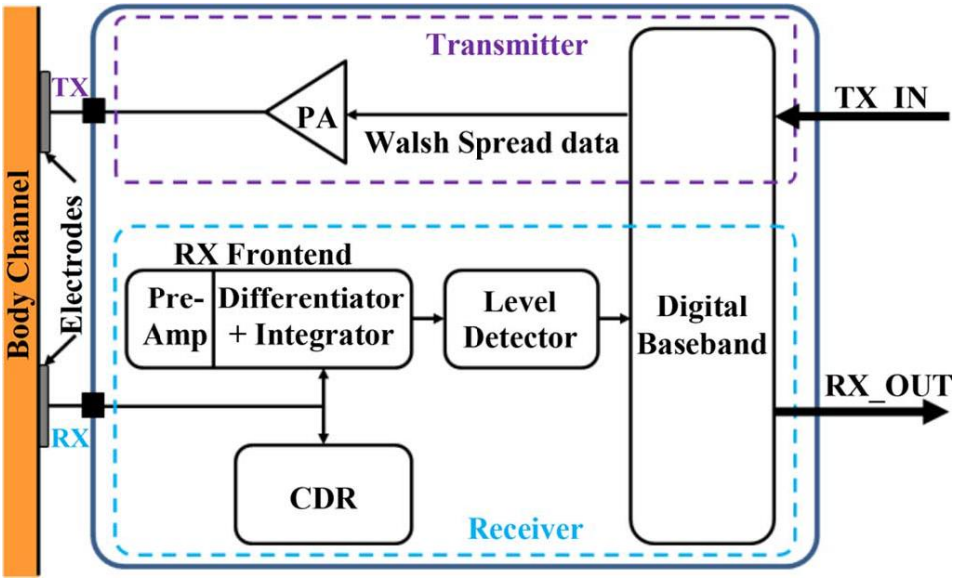
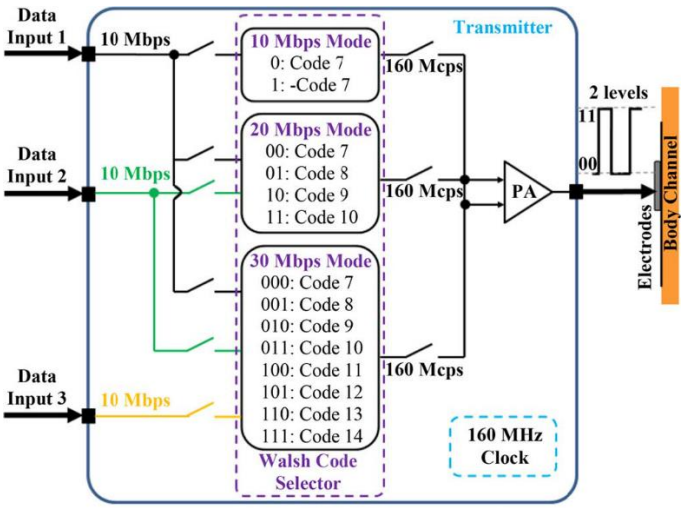


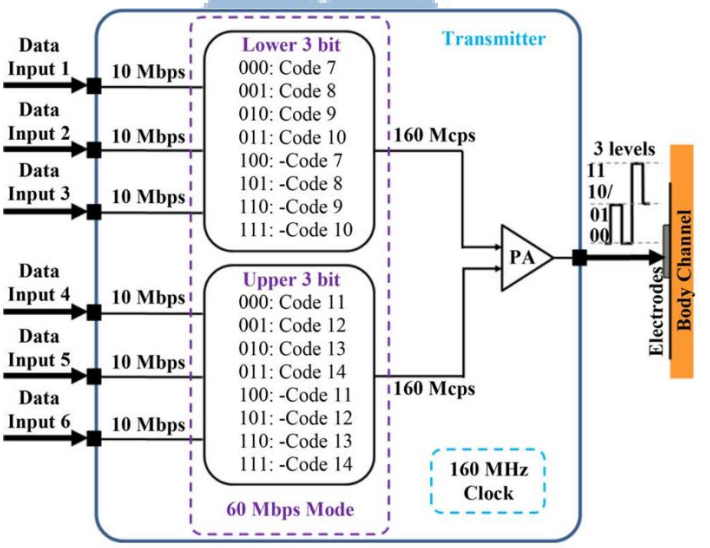

Fig. 1.20: Transceiver architecture of FSDT modulation [39]

The transceiver with FSDT has two modes in [39]. In the normal mode of operation, the clock operates at the 160 MHz, and the data rate is 10, 20, or 30Mbps. For the data rate of 10Mbps, only one Walsh code is required. For example, “1” is represented by Walsh code 7 and “0” is represented by the inverse of Walsh code 7. For the other data rate, different Walsh codes are used to represent multiple data bits, as shown in Fig. 1.21. In the high data rate mode, there are six data inputs in this mode, the lower three bits are mapped into code 7 to code 10 and the upper three bits are mapped into code 11 to code 14, as shown in Fig. 1.22. In addition, one Walsh code is used to represent three bits of data, and two Walsh codes are stacked together using the inverter PA to form a three-level signal. Furthermore, the system can support a data rate up to 60 Mbps.




| Bits/Symbol | Max Data Rate (Mbps) | Number of Walsh Code Required |
|---|---|---|
| 1 | 10 | 1 |
| 2 | 20 | 4 |
| 3 | 30 | 8 |

Fig. 1.21: Normal operation mode [39]




| Bits/ Symbol | Max Data Rate (Mbps) | Amplitude level | Number of Walsh Code Required |
|---|---|---|---|
| 3 | 60 | 3 | 8 + 8 inverse |

Fig. 1.22: High data-rate mode [39]

## 1.3.5 Modulation Scheme: Wide-Band Signaling

In [15], a body channel communication transceiver with wideband signaling (WBS) is proposed. The WBS transceiver and the CDR circuit are shown in Fig. 1.23. The data are encoded by non-return to zero inverted (NRZI) modulation and transmitted directly to the human body. Then the oversampling-based CDR circuit recovers the data

to the original data in the receiver. This wideband signaling transceiver supports maximum 40Mbps data rate. The DCO in the CDR circuit generates a 280MHz clock for the sampler to sample the data. However, in this architecture, if there is a large frequency drift between the transmitter and receiver, it may cause a high bit error rate(BER).

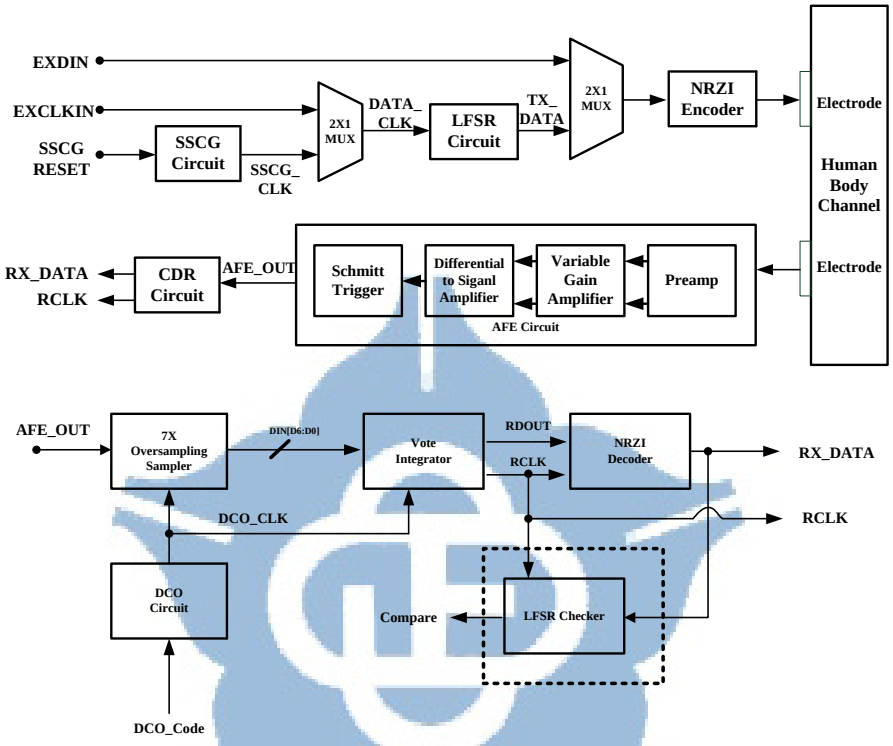



Fig. 1.23: The WBS transceiver and the CDR circuit [15]

# 1.4 CDR Circuit for NRZI Encoding

NRZI is a data recording and transmission method that ensures clock synchronization. The two level NRZI signal has a transition if the transmit signal is logical 1, and keep the previous signal voltage level if the transmit signal is logical 0. Moreover, the NRZI data will be attenuated after passing through the human body so that they require an AFE circuit and a CDR circuit to recovery the data. The CDR circuit can recover the clock and uses the clock to recover the data. We will introduce the common type of the CDR circuit in the following section.

## 1.4.1 Phase Interpolator Based CDR circuit

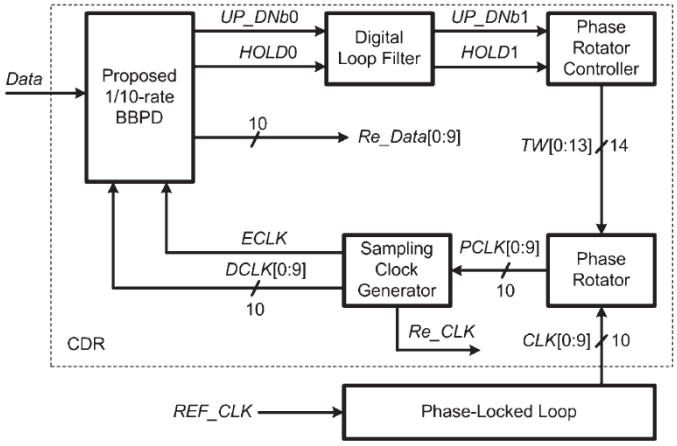



Fig. 1.24: Architecture of phase interpolator based CDR [18]

In [4, 18], the interpolator based CDR is proposed. Fig. 1.24 shows the architecture of the phase interpolator based CDR in [18]. The CDR consists of a 1/10-rate BBPD, a digital filter, a PR controller, a PR, and a sampling clock generator. The CDR uses 11 sampling clocks, ten clocks (DCLK0 to DCLK9) are for data sampling, and one clock (ECLK) is for edge tracking. According to BBPD output, the PR controller increases or decreases a 14-bit thermometer code which determines the phase of the sampling clocks. The sampling clock generator (SCG) generates ECLK and DCLKs. DCLKs are generated by interpolating two adjacent PCLK with the same weight. Finally, the multi-phase clock are used for data sampling and edge detection.

## 1.4.2 FLL/PLL-Based CDR circuit

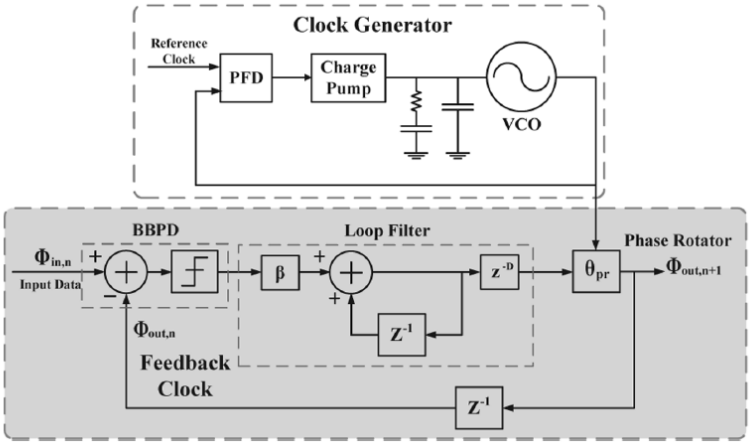



Fig. 1.25: Architecture of the PLL-based CDR [20]

The architecture of PLL-based CDR is proposed in [23], [20]. Fig. 1.25 shows the PLL-based CDR, the CDR consists a PLL loop and a CDR loop. In the PLL loop, according to the external frequency, the clock generator generates the clock to the phase rotator. The CDR loop only track phase because it has a stable frequency that is from the PLL loop.

## 1.4.3 Gated Oscillator CDR circuit

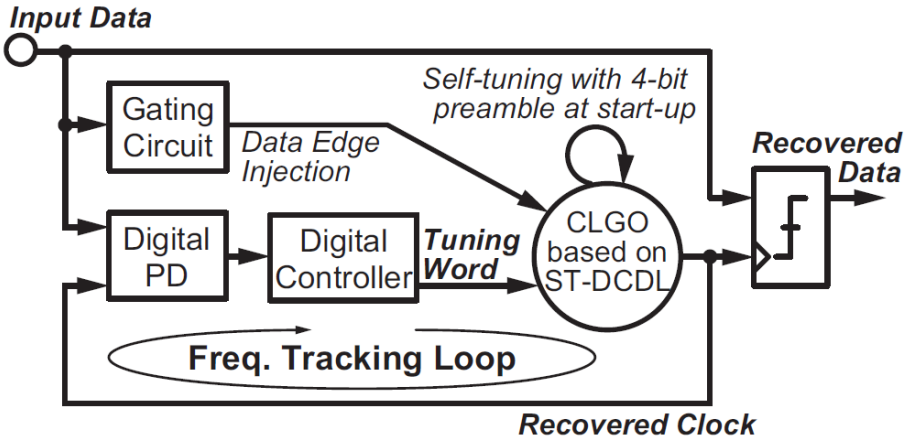



Fig. 1.26: Architecture of the Gated-Oscillator CDR [22]

The gated-oscillator CDR resets the oscillator to realign the phase between the clock and data. The architecture of gated-oscillator is proposed in [22], as shown in Fig. 1.26. Firstly, The CDR use the PD and controller and DCDL to track the frequency.

Then, the gating circuit is used to generate the data edge injection to reset the DCDL so the phase error can be compensated. However, the gated oscillator may cause the recovery clock has a glitch.

### 1.4.4 Blind Oversampling CDR circuit

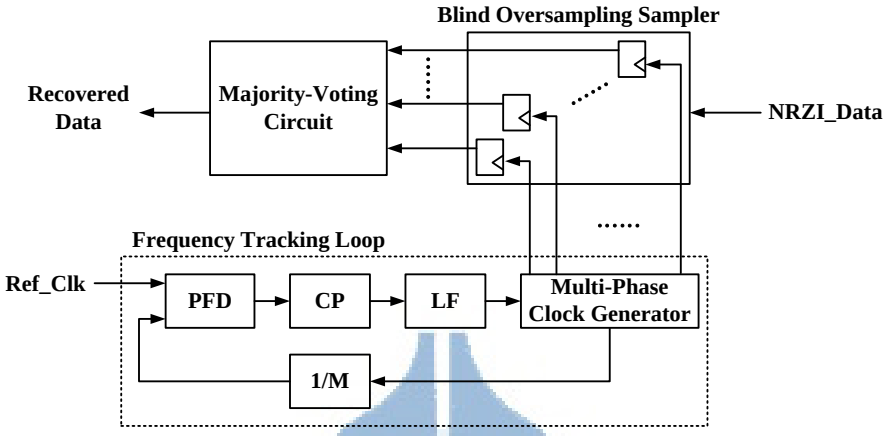



Fig. 1.27: Architecture of the blind oversampling CDR

The architecture of the blind oversampling CDR [26] is shown in Fig. 1.27. In the frequency tracking loop, it requires a reference clock to generate the high-speed multi-phase clocks. The blind oversampling sampler samples the data by using the multi-phase clocks. In this architecture, it uses the voting mechanism to distinguish the sampling data. The blind oversampling architecture has relatively large jitter tolerance because it has a stable frequency.

### 1.4.5 Summary

The common type of the CDR often uses the frequency synthesizer to provide a stable frequency to the CDR loop. Therefore, the CDR loop only needs to track the phase, and thus it has better jitter tolerance because the frequency is stable. However, the frequency synthesizer increases the area and power consumption of the CDR.

Moreover, because the phase interpolator based CDR circuit and oversample CDR circuit has a high sampling rate, and therefore, they have high power consumption. Furthermore, if the frequency synthesizer cannot generate the expected frequency, it

causes frequency drift. The frequency drift will cause bit errors in data recovery.

# 1.5 Motivation

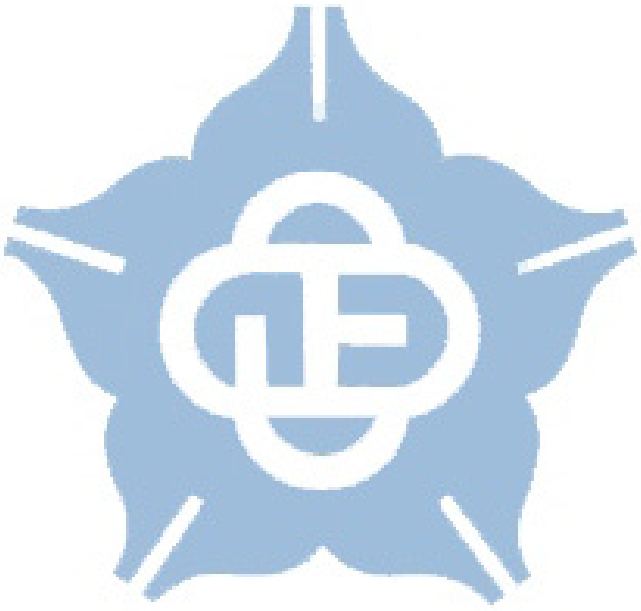
With new technological advances, the handled devices and healthcare devices become more and more popular now. The wireless BAN technique such as Bluetooth and ZigBee have relatively high power consumption and low data rate than the BCC. Therefore, they are not suitable for the low power devices. The BCC uses the human body as the medium to transmit the data so it is stable and has low power consumption. In addition, it can realize the high data rate easily.

In short distance transmission (< 60 cm), the healthcare devices can directly transmit to other devices and has high security. In long distance transmission (about 140 cm), for example, we can touch each other to transmit the data easily between two devices. Therefore, we want to realize a transceiver for human body channel communication, which can support different data rate of applications such as medical signals or multi-media signals and has different distance for these devices.

In the paper survey, there are several BCC transceivers are proposed. The OFDM-based architecture can achieve high data rate with a narrow channel frequency range. However, the OFDM increases the power consumption and the chip area. The FSK-based architecture and BPSK-based architecture use the different frequencies or phase to transmit the data. Therefore, the receiver can easily to be realized because it just distinguishes the two signals. However, the specific frequency of the FSK approach is easy to be interference by noise. The FSDT-based architecture [39], it achieves high data rate (60Mbps) by using the Walsh codes, but it requires a high signal-to-noise ratio (SNR) which is not available in real environment. The WBS-based architecture has small chip area and lower power consumption. Moreover, the WBS-based architecture can achieve high data rate easily. Therefore, we use the WBS-based architecture to

realize the transceiver for BCC and the energy per bit can be further reduced.

Moreover, the WBS-based architecture must have a CDR circuit in the receiver part. In the above paragraph, we have discussed several CDR circuits. The common type of the CDR circuits use the frequency synthesizer to generate the stable frequency. However, it increases chip area and power consumption and has low-frequency drift tolerance. Therefore, we adopt the reference-less CDR circuit to reduce the power consumption and circuit complexity, and the tolerance to frequency drift can be greatly improved.



# Chapter 2 Architecture of Wideband Signaling Transceiver

## 2.1 Architecture Overview

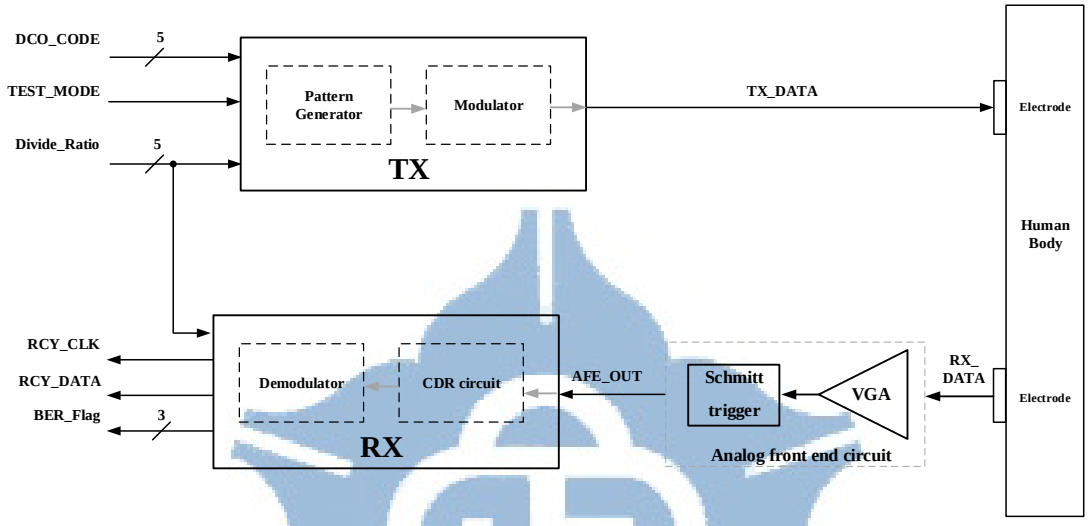



Fig. 2.1: Architecture of the proposed WBS transceiver

Fig. 2.1 shows the architecture of the proposed WBS transceiver. The transceiver consists of a transmitter (TX), a receiver (RX), and an analog front-end (AFE) circuit. In the transmitter part, we can set the DCO control code and the ratio of the divider to generate the desired frequency to the TX. The pattern generator and the modulator generate the TX_DATA. Then, the TX transmits the data (TX_DATA) to the human body. In the receiver part, the RX_DATA is amplified and converted to the digital signal by the AFE circuit. Subsequently, the RX will recover the data (AFE_OUT) to the original data (RCY_DATA) by the clock and data recovery (CDR) circuit and the demodulator. Finally, the BER_Flag signal will show the bit error rate information.

# 2.2 Wideband Signaling Transmitter Architecture

## 2.2.1 Wideband Signaling Transmitter Overview

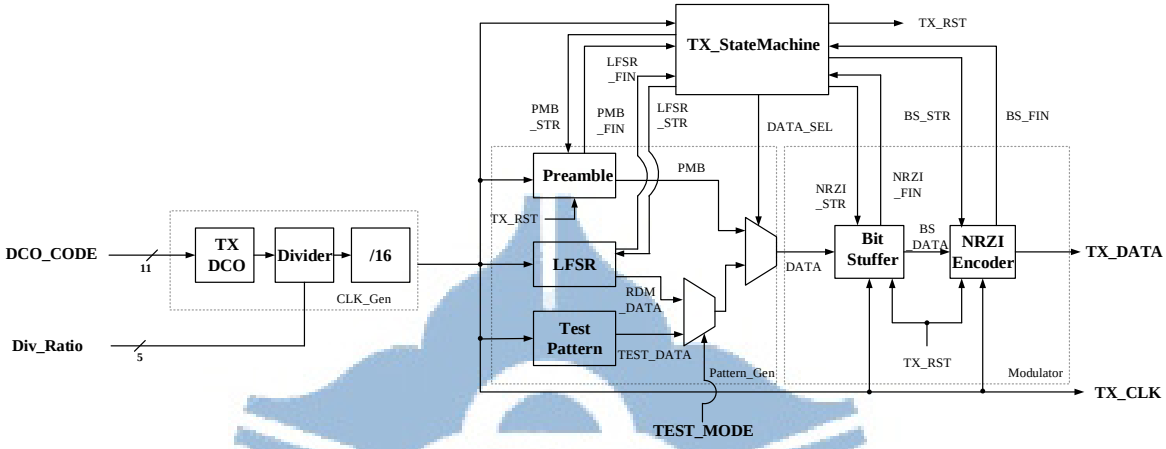



Fig. 2.2: Architecture of the proposed WBS transmitter

Fig. 2.2 shows the architecture of the proposed WBS transmitter. The transmitter consists of a clock generator (CLK_Gen), a pattern generator (Pattern_Gen), a modulator, and a TX state machine. Firstly, according to the input DCO control code, the CLK_Gen generates the clock (TX_CLK) to the other circuits. Secondly, the Pattern generator (Pattern_Gen) has a normal mode and a test mode. In the normal mode, the Pattern_Gen generates the preamble data and the random data. In the test mode, the Pattern_Gen generates the preamble data and regular data for chip debugging. Finally, the TX_DATA modulates the DATA to NRZI_DATA and the bit stuffer performs bit stuffing which limit the maximum continuous identical digits (CID) to 3. The TX_StateMachine can generate the start signal or the finish signal to control the state of the other circuit and select the output data of the Pattern_Gen.

## 2.2.2 Clock Generator

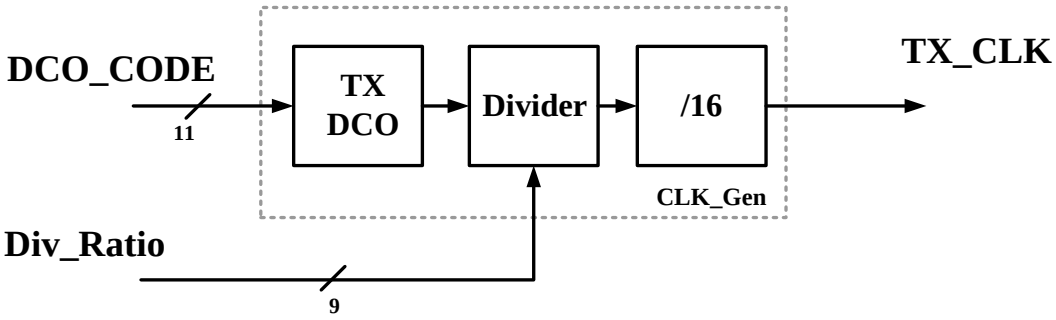



Fig. 2.3: Architecture of the clock generator

Fig. 2.3 shows the architecture of the clock generator. The clock generator consists of a TX_DCO, a frequency divider, and a divide-by-16 frequency divider. The DCO_CODE is used to control the output frequency of the TX_DCO. In addition, in order to generate wide frequencies (1MHz-20MHz), a frequency divider is adopted to increase the frequency range, and we can set the Div_Ratio to generate the target frequency. The architecture of the TX_DCO is the same as the RX_DCO and will be discussed in section 2.3.2.2.

## 2.2.3 Pattern Generator

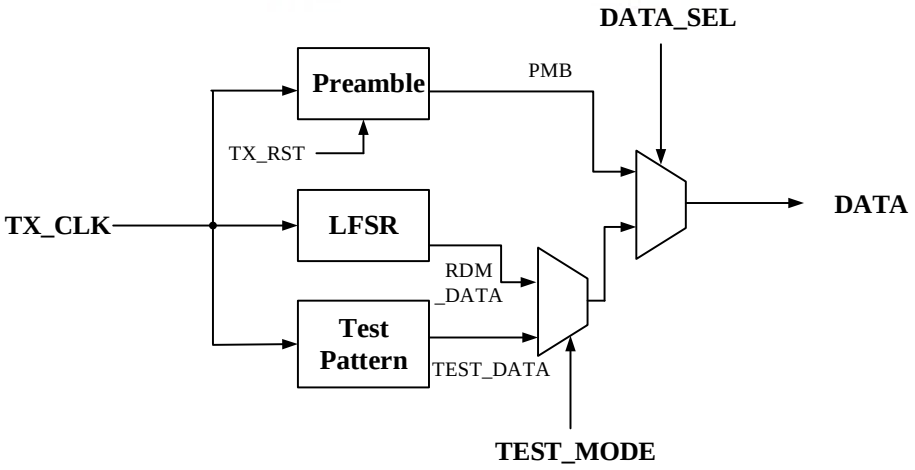



Fig. 2.4: Architecture of the pattern generator

The pattern generator consists of a preamble circuit, a linear feedback shift register

(LFSR) circuit, a test pattern circuit, and two 2-to-1 multipliers, as shown in Fig. 2.4. Firstly, the preamble circuit generates the preamble data for synchronization. Then, according to the TEST_MODE signal, the normal mode or test mode is selected. In the test mode, the Pattern_Gen generates the regular pattern for chip debugging. In the normal mode, the Pattern_Gen generates the random pattern. Fig. 2.5 shows the architecture of the LFSR circuit. It consists of twenty registers and a XOR gate. The feedback polynomial of the LFSR circuit is shown in Eq. 2.1.

$$1 + x^{19} + x^{20} \tag{2.1}$$

The random sequence is $2^{20}$ bits repetition and the longest CID are 20. In addition, we use the packet to transmit the data. Fig. 2.6 shows the packet format of the WBS transceiver. Firstly, 80 preamble bits are transmitted to the human body for synchronization. Subsequently, 4 bits start frame delimiter (SFD) which is used to detect the start bit of the random data are sent. Finally, 1000 bits random data are transmitted.

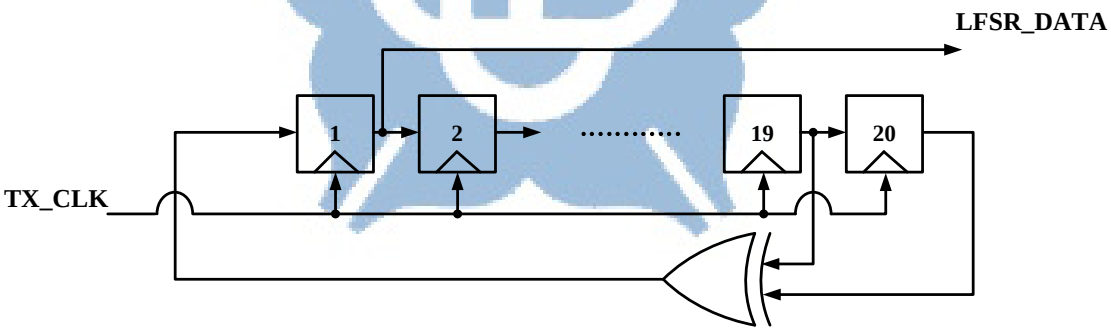



Fig. 2.5: Architecture of the LFSR circuit

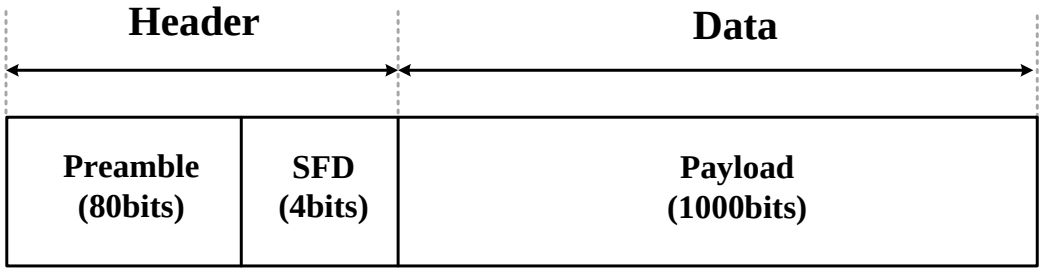



Fig. 2.6: The packet format of the WBS transceiver

## 2.2.4 Modulator

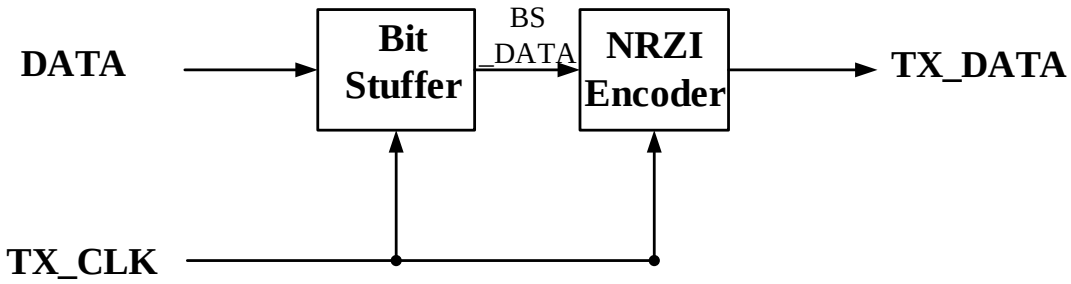



Fig. 2.7: Architecture of the modulator

Fig. 2.7 shows the architecture of the modulator. It consists of a bit stuffer and an NRZI encoder. Because the data (DATA) generated by the Pattern_Gen may have long CID, it implies the few data transitions. In addition, few data transitions are difficulty to recover the data because of the jitter accumulation. Therefore, the bit stuffer is used to increase the data transitions. In the proposed design, the maximum CID is set to 3. The bit stuffer will check the sequence of the DATA and inserts a transition after there is three identical digits. Moreover, because the NRZI encoder reverses the output data when the DATA is “0” to generate the transition, thus, the bit stuffer only insert the “0” after three continuous “1” and it does not need to insert the “1” after three continuous “0”. The NRZI encoder is used to encode the DATA to the NRZI_DATA. When the DATA is “1”, the NRZI encoder will keep the state of the previous NRZI_DATA. When the DATA is “0”, the NRZI encode will reverse the state of the state of the previous NRZI_DATA to generate the data transition.

## 2.2.5 TX State Machine

The TX state machine is used to control the enable or disable of the other circuits. Fig. 2.8 shows all I/O pins of the TX state machine. After the circuit resets, the preamble start signal (PMB_STR) is set to 1 and the TX starts to transmit the preamble data.

When the preamble data is transmitted completely, the LFSR start signal (LFSR_STR) is set to 1 and the TX starts to generate the random data and through the DATA_SEL signal to control the multiplier. Subsequently, when the random data is transmitted completely, the bit stuffer start signal (BS_STR) and NRZI start signal (NRZI_STR) are enabled and the TX starts to modulate the data. When the bit stuffer and NRZI modulation are finished, the TX_StateMachine generates the TX_RST signal to reset the TX.

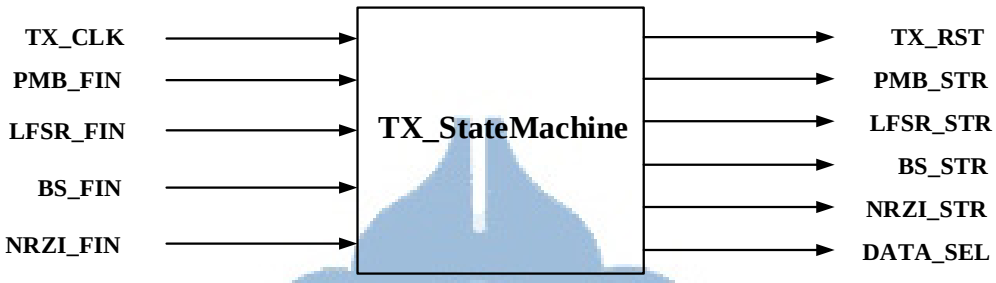



Fig. 2.8: All I/O pins of the TX state machine

## 2.2.6 TX Flowchart

Fig. 2.9 shows the flowchart of the TX. After TX is reset, the TX starts to transmit the preamble bits. When preamble bits are sent, the TX will detect the test mode signal. If the test mode is “0”, the LFSR circuit will generate the random data. If the test mode signal is “1”, the Test Pattern circuit will generate the regular pattern for debugging issue. Then, the bit stuffer will check the data and bit-stuffs the data to generate the transitions, and the NRZI encoder will encode the data to the NRZI format. Finally, the TX will wait 200 cycles before the self-operation reset because the RX needs to take some time to recover the clock and data. After that, the TX will generate the TX_RST signal to reset the circuits and start to send the next packet.

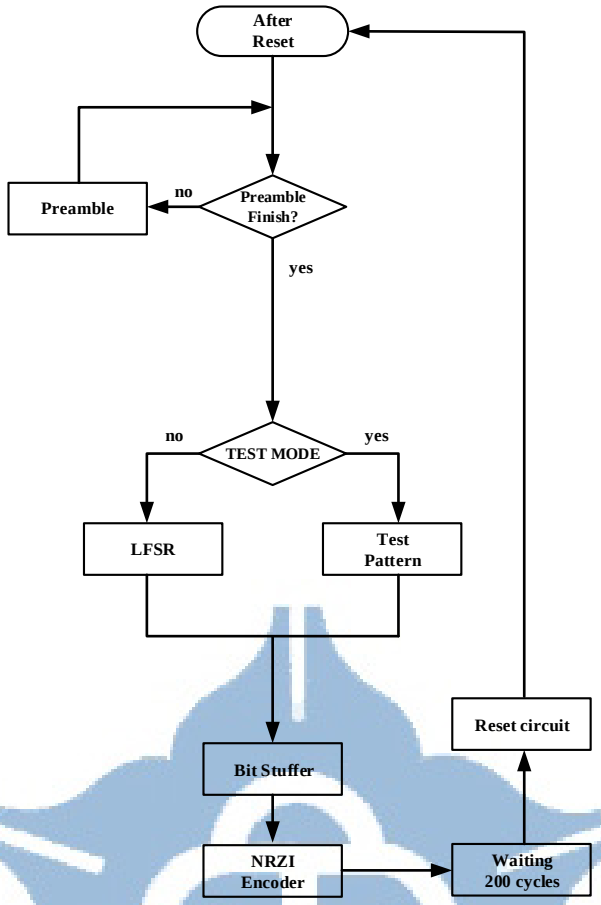



Fig. 2.9: TX flowchart

# 2.3 Reference-Less Receiver Architecture

## 2.3.1 Reference-Less Receiver Overview

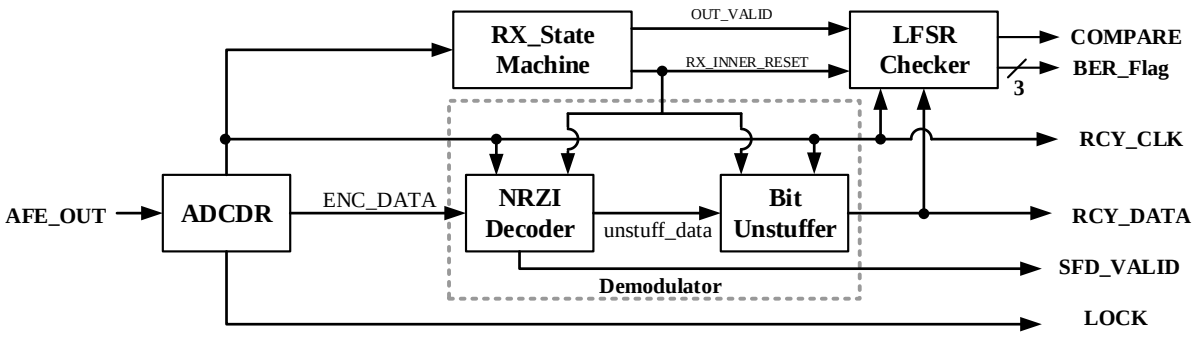



Fig. 2.10: Architecture of the reference-less receiver

Fig. 2.10 shows the architecture of the reference-less receiver. It consists of an all-

digital clock and data recovery (ADCDR), an RX state machine, a demodulator, and a LFSR checker. In the beginning, the gain calculator will use the AFE_OUT signal to calculate the gain value for the ADCDR controller. Consequently, the signal AFE_OUT will send to the ADCDR to perform the clock and data recovery. After that, the encoding data (ENC_DATA) will be demodulated by the demodulator and generate the recovery data (RCY_DATA). The RX state machine is used to reset the circuit if a packet is received. The LFSR checker circuit will generate the random pattern sequence which is the same as the LFSR circuit in the TX, and checks whether there are bit errors in the recovery data (RCY_DATA).

### 2.3.2 Demodulator and LFSR Checker

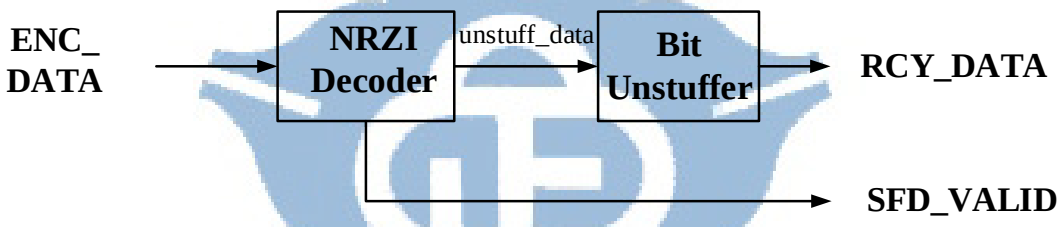



Fig. 2.11: Block diagram of the demodulator

Fig. 2.11 shows the block diagram of the demodulator. It consists of a bit unstuffer and an NRZI decoder. Firstly, the encoded data (ENC_DATA) from the ADCDR will be sent to the NRZI decoder to decode the stuffed data (BS_DATA). Then, the BS_DATA will take out the stuffing bits by the bit unstuffer and recover the original data (RCY_DATA). In addition, the RCY_DATA will be sent to the LFSR checker to check the bit error. The LFSR checker circuit is used to generate the random pattern which is same as the LFSR circuit in TX.

## 2.3.3 The Proposed Receiver Flow

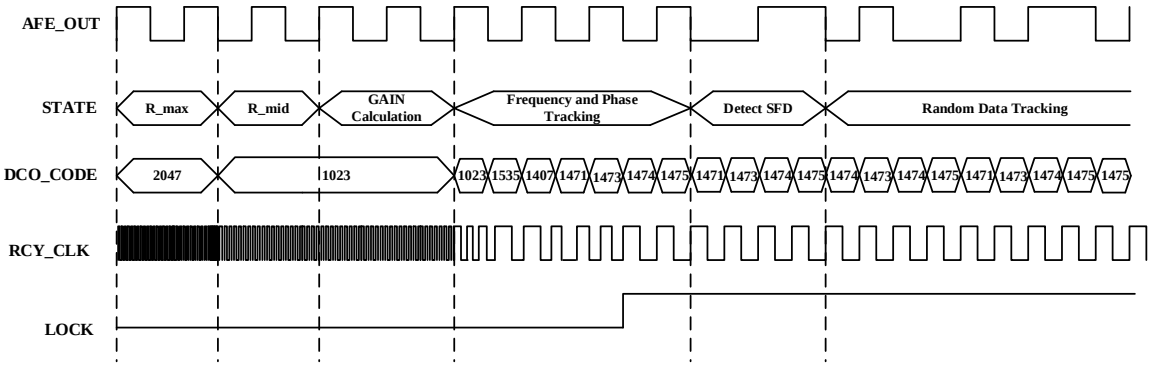



Fig. 2.12: Receiver timing diagram in preamble pattern

Fig. 2.12 shows the timing diagram of the receiver. Firstly, the DCO_CODE is set to 2047 to calculate the period ratio between the symbol period and the output of the DCO ($R_{max}$) at maximum DCO frequency output. Then, the DCO_CODE is set to 1023 to calculate another period ratio ($R_{mid}$) at medium DCO frequency output. Secondly, the gain calculator can calculate the gain value with the $R_{max}$ and $R_{mid}$ using Eq. 2.23 and sends to the ADCDR controller. Thirdly, the ADCDR start to perform the frequency and phase tracking. Finally, when the ADCDR detects SFD, the ADCDR start random data tracking.

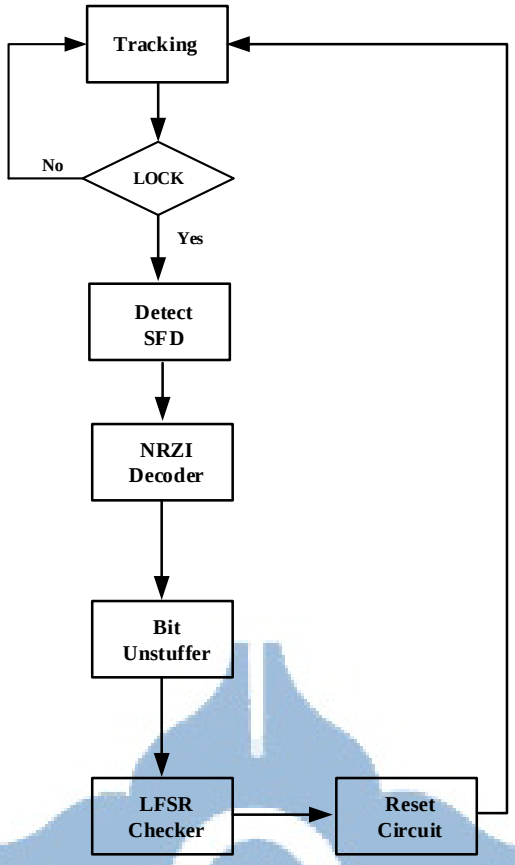



Fig. 2.13: Receiver flowchart in random data

Fig. 2.13 shows the receiver flowchart. Firstly, when the AFE_OUT is coming, the RX will track the frequency and phase of the incoming data. After frequency lock, the ADCDR starts to recover the data. Then, after detecting the SFD, the NRZI decoder and bit unstuffer will start to demodulate the data. Finally, the RCY_DATA will be sent to the LFSR checker circuit to check the bit error and the RX state machine will send the RX_RST signal to reset the circuit.

## 2.3.4 Clock and Data Recovery

### 2.3.4.1 CDR Overview

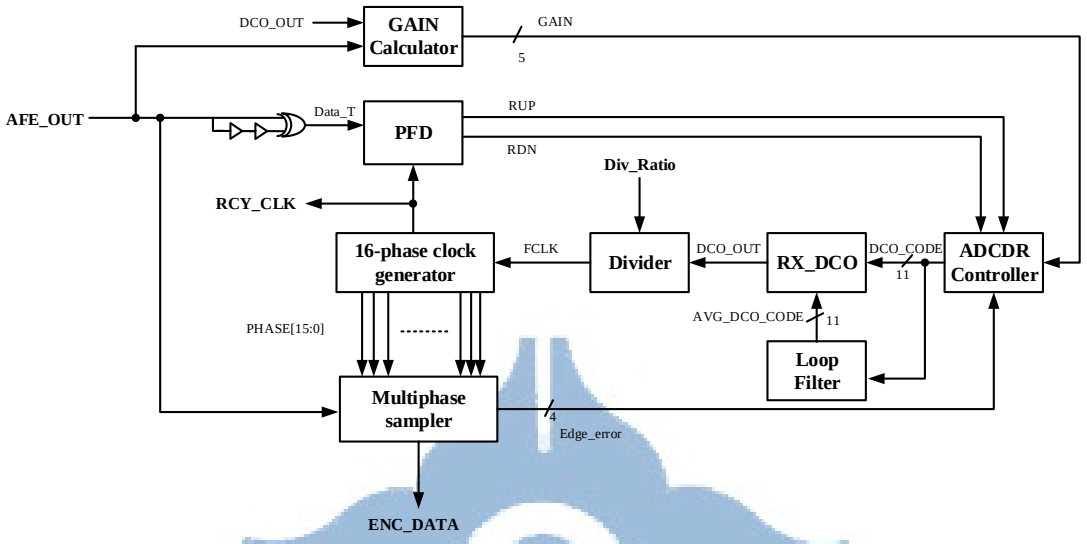



Fig. 2.14: The block diagram of the proposed ADCDR circuit

Fig. 2.14 shows the block diagram of the proposed ADCDR circuit. The proposed ADCDR circuit consists of a gain calculator, a phase and frequency detector (PFD), a monotonic digitally controlled oscillator (RX_DCO), a digital loop filter (DLF), an ADCDR controller, a frequency divider, a divided-by-16 frequency divider, a 16-phase clock generator, and a multiphase sampler.

Firstly, the input data (AFE_OUT) is delayed and exclusive-OR with the original data to generate the data transition signal (Data_T). Then, the PFD compares the phase and frequency error between the signal Data_T and the recovery clock and generates the signal RUP or RDN to the ADCDR controller. Before the frequency and the phase acquisition is complete, the ADCDR controller uses the binary search to adjust the DCO control code. When the frequency and the phase acquisition is complete, the frequency of the DCO clock will be sixteen times of the data rate, and the ADCDR will change to the phase tracking and disables the PFD circuit. In the phase tracking, the ADCDR will

generate the 16 phases and the multi-phase sampler will sample the AFE_OUT to detect the edge transition. According to the edge detection, we calculate the difference (Edge_error) between the current edge position and the ideal edge position. Therefore, we can compensate for the phase error. The method of the edge detection will discuss in detail in the session 2.3.4.6. In addition, the DCO control code is sent to the digital loop filter to generate the baseline DCO control code in order to stabilize the DCO output clock (DCO_OUT). Finally, the multiphase sampler will recover the data (ENC_DATA) and sends the data to the demodulator.

## 2.3.4.2 Monotonic Digital Controlled Oscillator

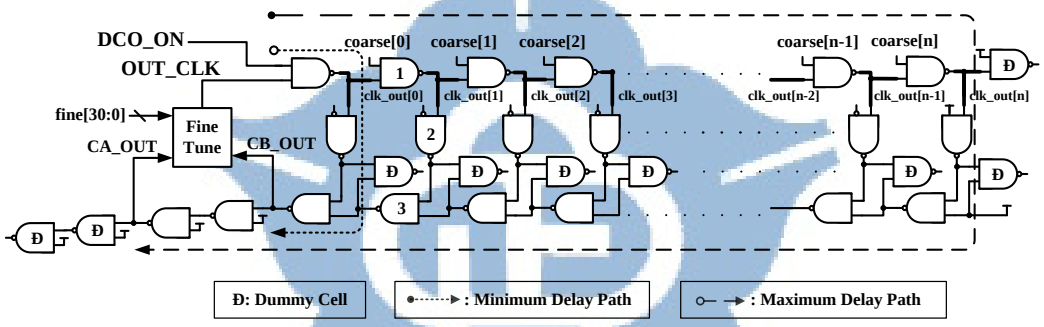



Fig. 2.15: The proposed DCO

Fig. 2.15 shows the architecture of the monotonic response DCO. The proposed DCO consists of a coarse-tuning delay line [27] and a fine-tuning delay [37]. The coarse-tuning delay line uses 63 coarse-delay cells (CDC), and each CDC is composed of four NAND gates. According to the 1st NAND gate to decide whether the CDC is enabled or disabled. Then, the 2nd and 3rd NAND gates are used to provide the delay. Therefore, the coarse-tuning resolution is the delay time of two NAND gates. In addition, to balance the rise time and fall time, the 4th NAND gate is used to be the dummy cell so that the duty cycle will not be distorted. The delay of the CDC is controlled by the 63 bits of the coarse control code (coarse [62:0]). If all of the 63 bits are set to the 1, the CDC will provide the maximum delay. Oppositely, if all of the 63

bits are set to 0, the CDC will provide the minimum delay.

Fig. 2.16 shows the fine-tuning architecture of the DCO. It consists of two parallel connected tri-state buffer arrays [37]. The two parallel connected tri-state buffer arrays are controlled by the 31 bits of the fine control code (Fine [30:0]). In addition, the total delay range of the fine-tuning stage should cover the resolution of the coarse-tuning stage [31, 32], or it may cause a large frequency gap. Therefore, the total delay controllable range of the fine-tuning range is equal to the resolution of the coarse-tuning stage. Table 2.1 shows the frequency range of the DCO in different PVT corners in the pre-layout simulation.

In addition, we use the DCO decoder to convert the DCO control code into the thermometer code. The DCO control code is 11 bits and the DCO_CODE [10:5] will be converted to coarse [62:0], and the DCO_CODE [4:0] will be converted to Fine [31:0].

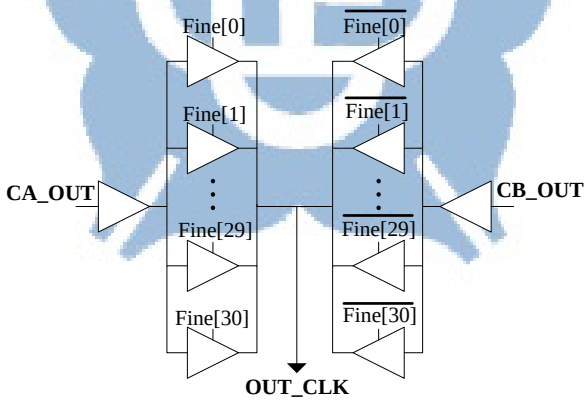



Fig. 2.16: The fine-tuning circuit of the proposed DCO [37]

Table 2.1: The DCO frequency range in different PVT corners

| PVT corner | Slow case | Typical case | Fast case |
|---|---|---|---|
| | (SS, 0.9V, 100°C) | (TT, 1.0V, 25°C) | (FF, 1.1V, 0°C) |
| Frequency Range (MHz) | 87 ~ 1547 | 122 ~ 2150 | 156 ~ 2785 |

## 2.3.4.3 Phase and Frequency Detector

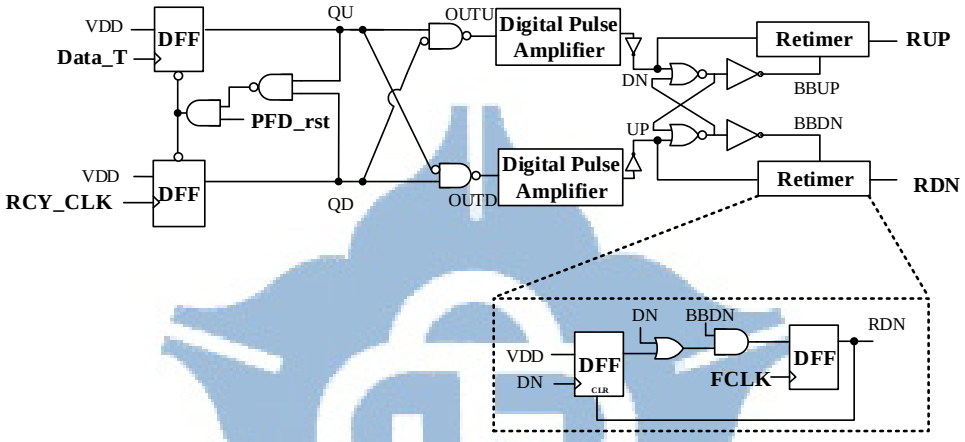



Fig. 2.17: Proposed dual mode PFD [29] and retimer architecture [30]

Fig. 2.17 shows the PFD and the retimer architecture. The PFD is a conventional three-state bang-bang PFD and can detect the frequency error and phase error with continuous data transition. The PFD will generate the UP or DN signal by comparing the rising edge of the Data_T and the recovery clock (RCY_CLK). In addition, the following SR_latch maintains the BBUP and BBDN signal. Finally, the retimer uses the FCLK to sample the UP or DN signal to generate the RUP or RDN signals which are synchronized with FCLK. Moreover, we only use the PFD and retimer during the frequency and phase acquisition with preamble pattern. When the frequency and phase acquisition is complete, the PFD and retimer circuits will be disabled.

## 2.3.4.4 Digital Loop Filter

The digital loop filter [33, 34] is used to stabilize the DCO control code and maintain the output frequency. Fig. 2.18 shows the architecture of the digital loop filter [33]. In the beginning, the DCO control code from the ADCDR controller is sent to the digital loop filter. When the digital loop filter receives the 4 DCO control codes, it generates the baseline DCO control code. Consequently, every two new DCO control codes are sent to the digital loop filter and the digital loop filter will sort the DCO control codes. Then, the digital loop filter removes the maximum and the minimum DCO control codes, and takes the average of the rest DCO control codes to generate a new baseline DCO control code. Finally, the average DCO control code (AVG_DCO_CODE) is used in the ADCDR when there has polarity change in phase maintaining.

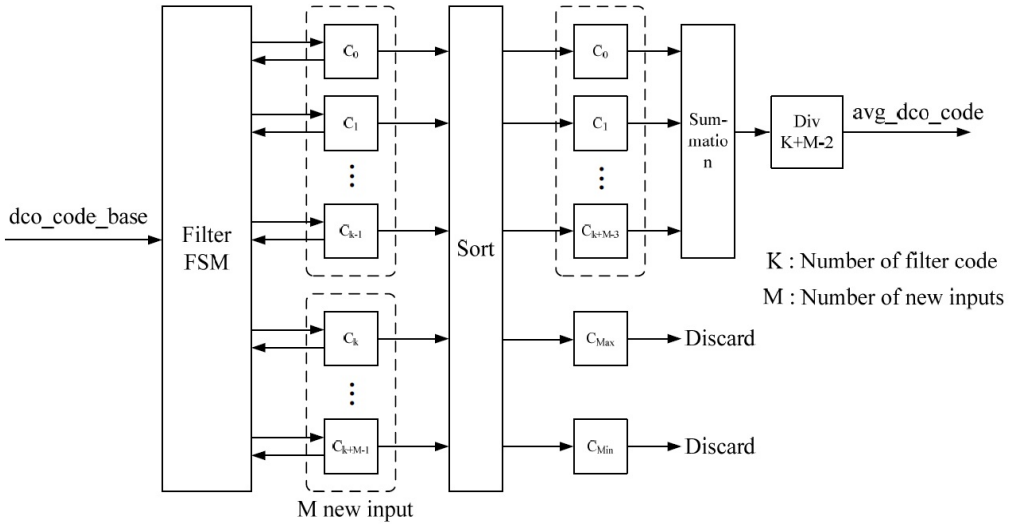



Fig. 2.18: The architecture of the digital loop filter [33]

### 2.3.4.5 Automatically Phase Track Gain Calibration

## Method

The gain calculator circuit is used to calculate the gain value. Due to the PVT variations, the DCO resolution varies with operating conditions. Therefore, we need a method to calibrate the gain value [35] and ensure the compensation for the same phase error is the same at different PVT conditions. In order to calculate the gain value, we denoted the $P_{mid}$, $P_{min}$, and $P_{ref}$ as follows. The $P_{mid}$ means the DCO period when the DCO control code is set to the medium value (i.e. DCO_CODE = 1023). The $P_{min}$ means the DCO period when the DCO control code is set to the maximum value (i.e. DCO_CODE = 2047). The $P_{ref}$ means the symbol period of the data. Then, the definition of the $R_{mid}$ and the $R_{max}$ is the ratio between the symbol period ($P_{ref}$) and the DCO clock (DCO_OUT) period at the median frequency and the maximum frequency, respectively. We can use the $P_{mid}$ and $P_{min}$ to calculate the $R_{mid}$ and the $R_{max}$ using the cyclic counters and the mathematical formulas of the $R_{mid}$ and $R_{max}$ are expressed in Eqs. 2.2 and 2.3. The $R_{mid}$ and $R_{max}$ are the symbol period divided by the medium DCO period and minimum DCO period, respectively.

$$R_{mid} = \frac{P_{ref}}{P_{mid}} \tag{2.2}$$

$$R_{max} = \frac{P_{ref}}{P_{min}} \tag{2.3}$$

Moreover, we assume that the period of the DCO is linear with the DCO code so $P_{mid}$ can be expressed with $P_{min}$ and DCO resolution ($\Delta$). Therefore, we can express the $R_{mid}$ in Eq. 2.4. The $\Delta$ is defined as the fine tuning resolution of the DCO.

$$R_{mid} = \frac{P_{ref}}{P_{min}+(2047-DCO\_CODE)\Delta} \tag{2.4}$$

In addition, the $R_{mid}$ is the period ratio when the DCO control code is set to 1023,

thus Eq. 2.5 is derived. Consequently, Eqs. 2.6 and 2.7 are derived. In Eq. 2.8, the $R_{mid}$ is expressed in terms of $R_{max}$, $\Delta$, and $P_{ref}$.

$$R_{mid} = \frac{P_{ref}}{P_{min}+1024\Delta} \tag{2.5}$$

$$R_{mid} = \frac{1}{\frac{P_{min}+1024\Delta}{P_{ref}}} \tag{2.6}$$

$$R_{mid} = \frac{1}{\frac{P_{min}}{P_{ref}} + \frac{1024\Delta}{P_{ref}}} \tag{2.7}$$

$$R_{mid} = \frac{1}{\frac{1}{R_{max}} + \frac{1024\Delta}{P_{ref}}} \tag{2.8}$$

According to Eq. 2.8, we can derive the Eqs. 2.9, 2.10, and 2.11.

$$\frac{1}{R_{max}} + \frac{1024\Delta}{P_{ref}} = \frac{1}{R_{mid}} \tag{2.9}$$

$$\frac{1024\Delta}{P_{ref}} = \frac{1}{R_{mid}} - \frac{1}{R_{max}} \tag{2.10}$$

$$\frac{\Delta}{P_{ref}} = \frac{(\frac{1}{R_{mid}} - \frac{1}{R_{max}})}{1024} \tag{2.11}$$

According to Eq. 2.11, we can derive the Eqs. 2.12, 2.13, and 2.14. Finally, we can get the ratio between the symbol period ($P_{ref}$) and the fine tuning resolution ($\Delta$) can be expressed in terms of $R_{mid}$ and $R_{max}$.

$$\frac{P_{ref}}{\Delta} = \frac{1024}{(\frac{1}{R_{mid}} - \frac{1}{R_{max}})} \tag{2.12}$$

$$\frac{P_{ref}}{\Delta} = \frac{1024}{(\frac{R_{max} - R_{mid}}{R_{mid} \times R_{max}})} \tag{2.13}$$

$$\frac{P_{ref}}{\Delta} = \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \tag{2.14}$$

On the other hand, after the frequency and phase acquisition is complete, the symbol period ($P_{ref}$) is 16 times of the DCO period (FCLK). Thus, the symbol period

($P_{ref}$) can be expressed in Eq. 2.15, where *N* is the divided ratio of the frequency divider.

$$P_{ref} = 16 \times P_{FCLK} = 16 \times (N \times (P_{min} + (2047 - DCD\_CODE) \times \Delta)) \quad (2.15)$$

Therefore, we can express the $\frac{P_{ref}}{\Delta}$ in another way as shown in Eq. 2.16. Also, the Eq. 2.17 is derived.

$$\frac{P_{ref}}{\Delta} = \frac{16\times (N\times(P_{min}+(2047-DCO\_CODE)\times\Delta))}{\Delta} \quad (2.16)$$

$$\frac{P_{ref}}{\Delta} = 16 \times N \times (\frac{P_{min}}{\Delta} + (2047 - DCO\_CODE)) \quad (2.17)$$

According to Eq. 2.17, we can get the ratio between the minimum DCO clock period ($P_{min}$) and the fine-tuning resolution ($\Delta$) as shown in Eq. 2.18.

$$\frac{P_{min}}{\Delta} = \frac{P_{ref}}{16\times N\times\Delta} - (2047 - DCO\_CODE) \quad (2.18)$$

The multi-phase generated from the FCLK are used to quantize the phase error. We assume that if the phase error (Edge_error) is K FCLK cycles. Therefore, the phase error is *K* multiplied by the period of the FLCK as shown in Eq. 2.19.

$$Phase\ \ Error = K \times (N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta)) \quad (2.19)$$

The value of K is changed at every phase error detection (edge detection). In Fig. 2.14, the DCO_OUT is divided by a frequency divider (N) and a divided-by-16 divider to generate multi-phase signals. Moreover, we compensate for eighth of the detected phase error in order to stabilize the DCO control code. Then, we can get the gain value (*GAIN*) that described as Eq. 2.20. Here GAIN means the required addition/subtraction value to the DCO control code when K=1.

$$GAIN = \frac{N\times(P_{min}+(2047-DCO\_CODE)\times\Delta)}{8\times16\times N\times\Delta} \quad (2.20)$$

$$GAIN = \frac{1}{8\times16} \times (\frac{P_{min}}{\Delta} + (2047 - \mathrm{DCO\_CODE})) \quad (2.21)$$

$\frac{P_{min}}{\Delta}$ in Eq. 2.21 can be substituted by Eq. 2.18, and then Eq. 2.22 can be derived.

$$GAIN = \frac{1}{8\times16} \times \frac{P_{ref}}{16\times N\times \Delta} \quad (2.22)$$

$\frac{P_{ref}}{\Delta}$ in Eq. 2.22 can be substituted by Eq. 2.14, and Eq. 2.23 can be derived.

$$GAIN = \frac{1}{8\times16\times16\times N} \times \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \quad (2.23)$$

The gain value is expressed in terms of the divide ratio of the frequency divider ($N$), $R_{mid}$ and $R_{max}$. Therefore, we can estimate the gain value by Eq. 2.23 with the preamble pattern, and we can have the same amount phase error compensation under PVT variations.

## 2.3.4.6 Phase Error (Edge Error) Detection Method

When the frequency and phase acquisition is completed, the 16-phase clock generator block uses the FCLK and a phase counter to generate the 16 multi-phases in one symbol period of the AFE_OUT. When the counter is 0, it means the PHASE0, and 1 is means PHASE 1, and so on.

Fig. 2.19 shows the timing diagram of the phase error detection in no phase error case. We use the negative edge of the multi-phase signals in the sampler. When there is no phase error, the PHASE0 (RCY_CLK) aligns the rising transition with the data transition of the AFE_OUT, so the negative edges of the PHASE0 will be in the center of the symbol period. Therefore, the data transition of the AFE_OUT will fall between the negative edges of the PHASE7 and PHASE8.

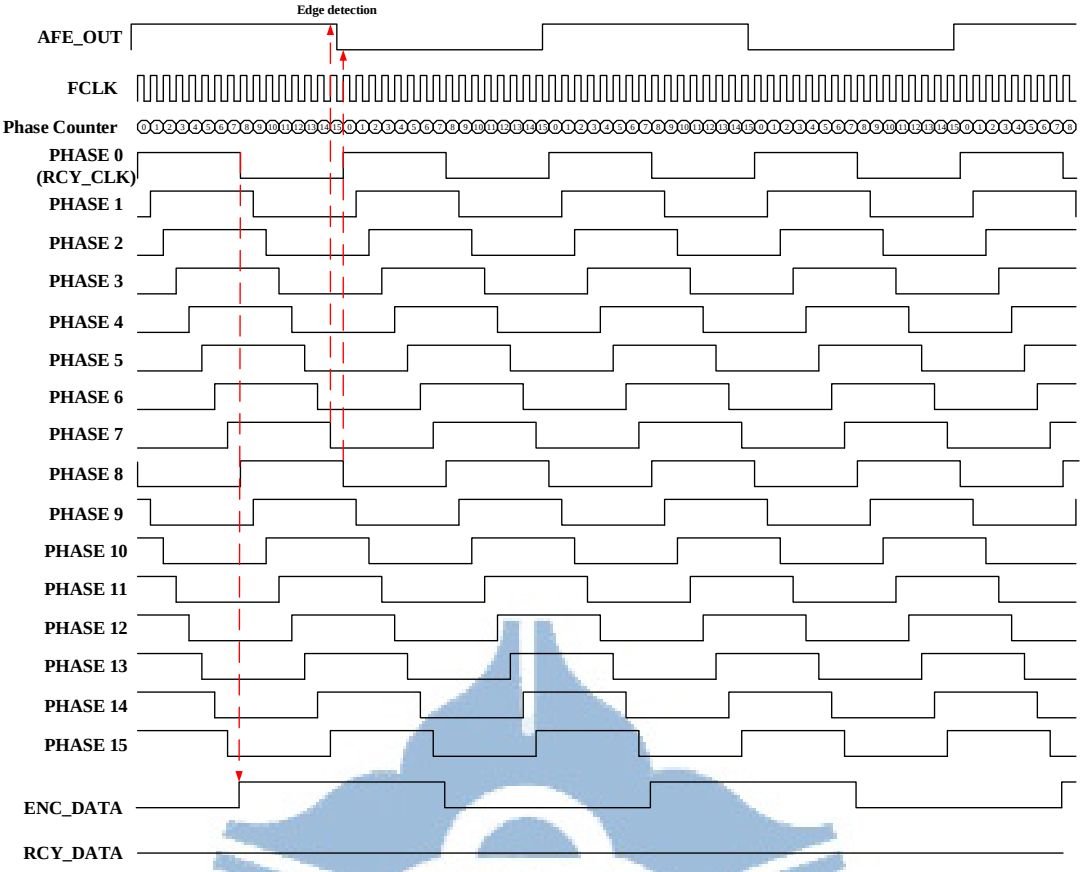



Fig. 2.19: Timing diagram of the phase error detection in no phase error case

As mentioned above, the phase error can be expressed as Eq. 2.19 and the value of the K is changed at every time of edge detection. Therefore, we use the multi-phase signals to quantize the phase error (Edge_error) (K). In the ideal case, the transition of the AFE_OUT will fall between the negative edges of the PHASE7 and PHASE8. If the data transition edge has phase drift, according to the position of the data transition edge, the phase error of the data transition edge can be expressed as the number of FCLK periods.

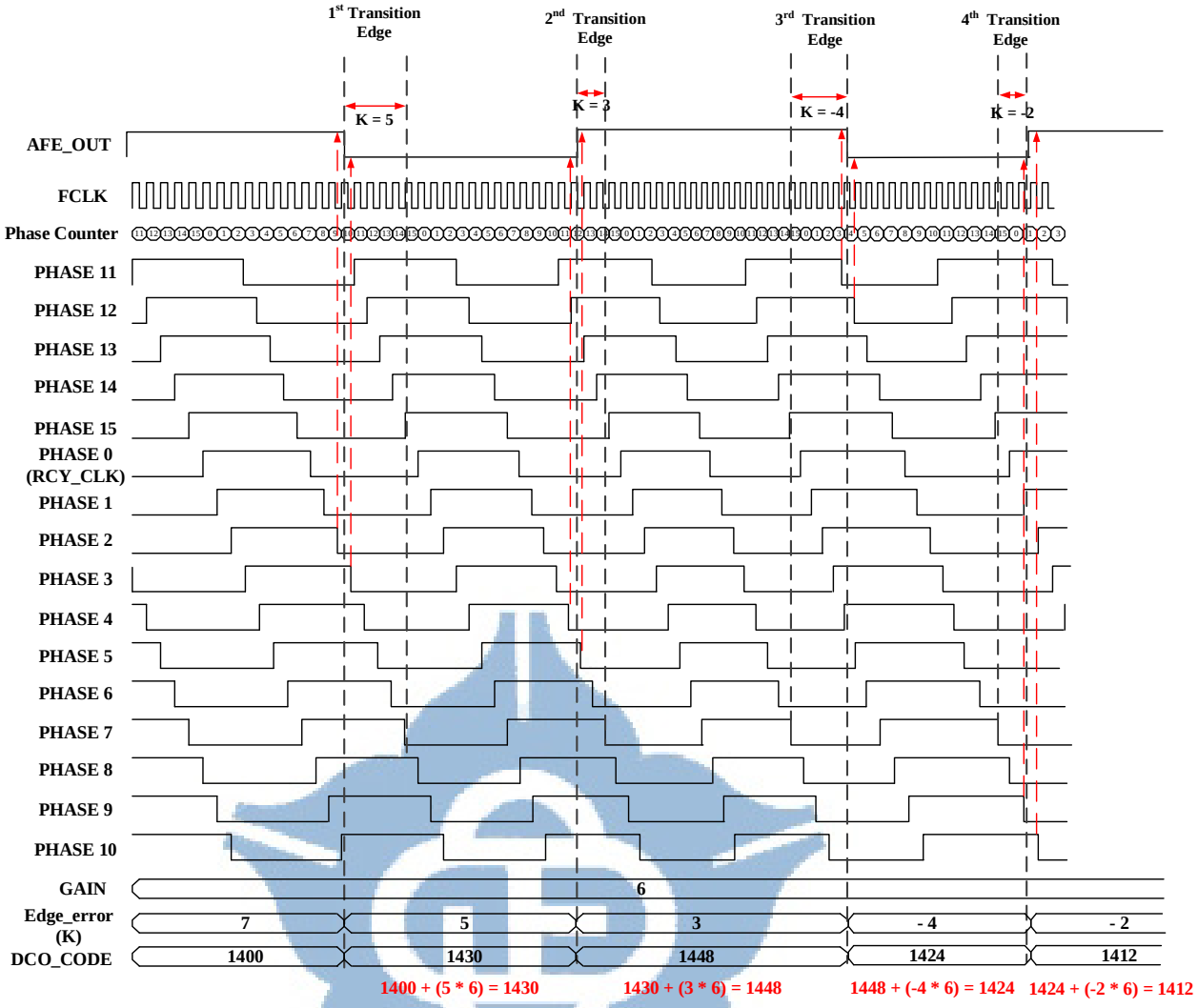



Fig. 2.20: Timing diagram of the phase error detection

Fig. 2.20 shows the timing diagram of the phase error detection. In the phase leading case, the data transition edge of the AFE_OUT leads the rising edge of the PHASE0 (RCY_CLK). As shown in Fig. 2.20, at first transition edge (1st Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE2 and PHASE3, and the phase error to the ideal data transition position ([PHASE7, PHASE8]) is 5 times the FCLK periods (K is 5). Then, the phase error (Edge_error) (K) will be multiplied by the GAIN and be added to the DCO control code. At second transition edge (2nd Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE4 and PHASE5, and it means the phase error is 3 times the FCLK periods. Then, the phase error (Edge_error)

(K) will be multiplied by the GAIN and be added to the DCO control code.

In the phase lagging case, the data transition edge of the AFE_OUT lags the rising edge of the PHASE0 (RCY_CLK). As shown in Fig. 2.20, at third transition edge (3rd Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE11 and PHASE12, the phase error (Edge_error) (K) is quantized as -4. Then, the phase error (Edge_error) (K) will be multiplied by the GAIN and be added to the DCO control code, and it makes the decrease of the DCO code. At fourth transition edge (4th Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE9 and PHASE10, and the phase error (Edge_error) (K) is quantized as -2. Then, the phase error (Edge_error) (K) will be multiplied by the GAIN and be added to the DCO control code.

Therefore, we can use the 16 multi-phases to detect the data transition edge and quantize the phase error and then quickly compensate for the phase error. In addition, when we detect the data transition edge, we can quantize phase error and update the DCO control code immediately. As compared to [34], because [34] uses the PFD to generate phase error signals then use the high frequency clock to quantize the phase error, it cannot update the DCO control code right after the data transition edge. As a result, it leads to a relatively slow response to the phase error.

## 2.3.4.7 Sampling Data

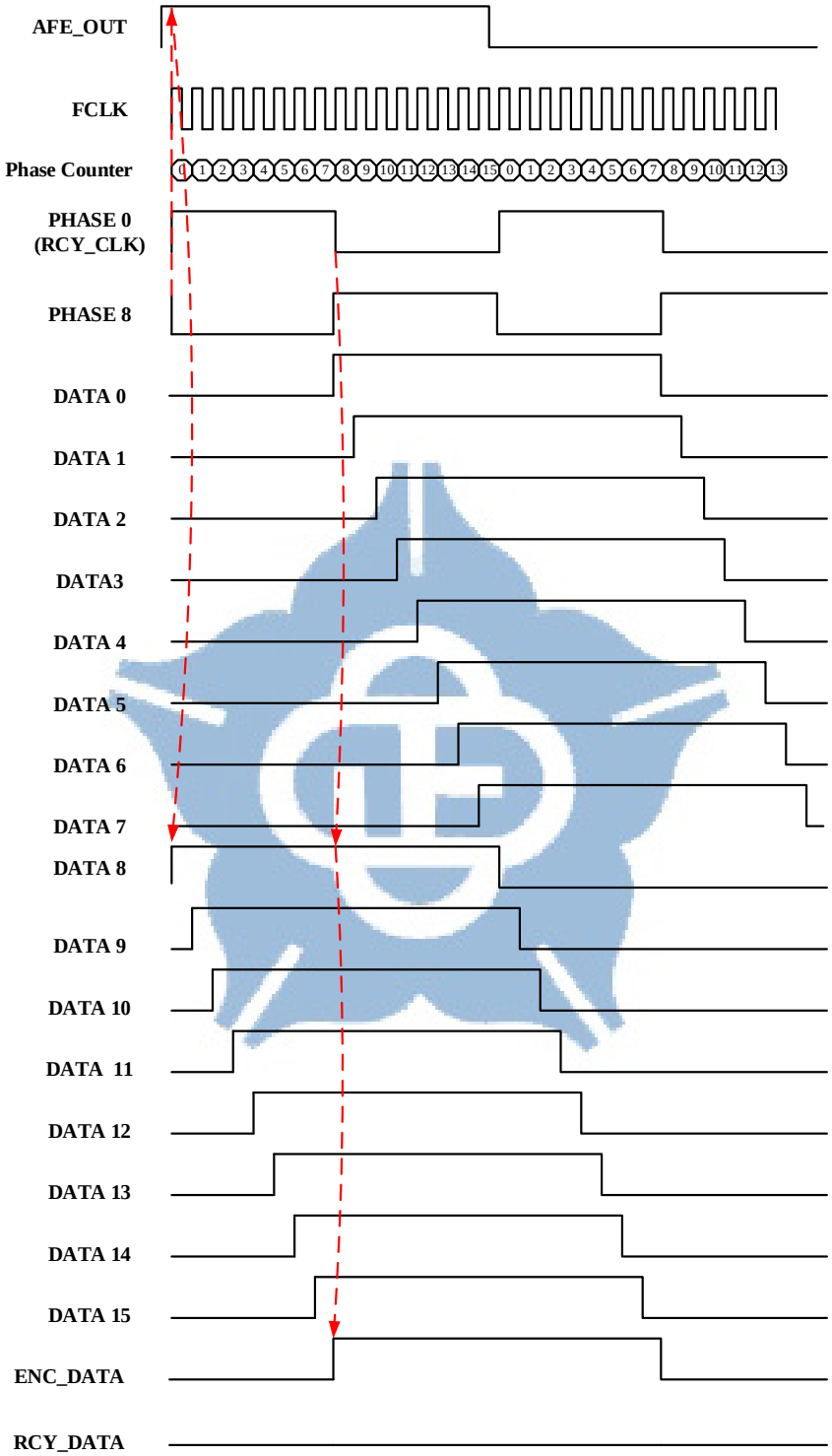



Fig. 2.21: The timing diagram of the sampling data

When the multi-phase sampler detects the data transition edge, we can ensure

the sampling data of the current phase is correct because the sampling point is right after the data transition edge. In addition, because the RX circuits operate at the PHASE0 (RCY_CLK) clock domain, we use the PHASE0 (RCY_CLK) to sample the data again in order to retime the data to the PHASE0 (RCY_CLK) clock domain. Fig. 2.21 shows the timing diagram of the sampling data. The PHASE[15:0] will sample the AFE_OUT, as denote as DATA[15:0]. For example, in the ideal case, the data transition edge of the AFE_OUT falls in the PHASE7 and PHASE8. Therefore, we select the DATA8 as the output data. Then, DATA8 will be sampled again by the PHASE0 (RCY_CLK) to retime to the PHASE0 (RCY_CLK) clock domain and output as ENC_DATA.

### 2.3.4.8 ADCDR Flowchart

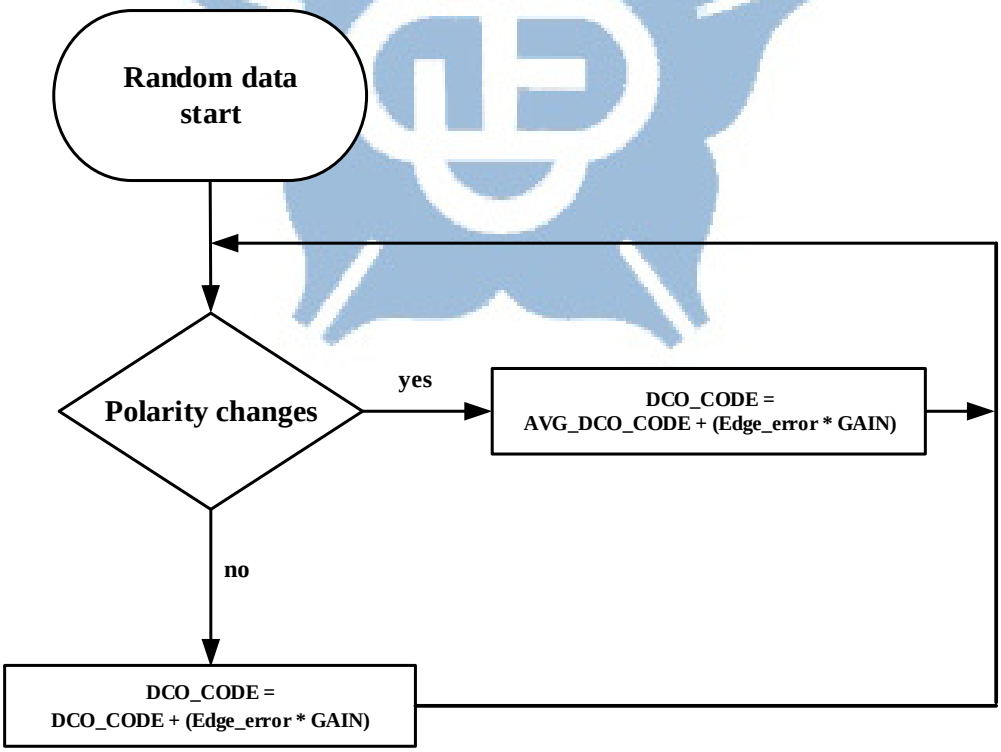



Fig. 2.22: Compensation flow with random data input

Fig. 2.22 shows the compensation flow of the controller with the random data input.

If there are phase polarity changes, the DCO_CODE will be restored to the AVG_DCO_CODE of the loop filter and adds by the Edge_error (K) multiplied by the GAIN. If there is no polarity change, DCO_CODE will add the current DCO_CODE by the Edge_error (K) multiplied by the GAIN.

# 2.4 Discussion

In [34]. When the frequency and phase acquisition is completed, the symbol period is 16 times of the FCLK. Continually, the PFD is used to generate the phase error pulse (RUP/RDN). Then, the FCLK quantizes the phase error pulse and calculates the phase error (K). Finally, the K multiplied by the GAIN to calculate the amount of DCO code for phase compensation. Fig. 2.23 shows the phase error detection method [34], in the RUP case, the RUP is quantized as two periods of the FCLK cycles (K = 2), then, the K will multiplied by the GAIN to calculate the adjustment of the DCO code. In the RDN case, the RDN quantized as three periods of the FCLK cycle (K = 3), then, the K will multiplied by the GAIN to calculate the adjustment of the DCO code.

However, [34] uses the PFD to generate the phase error pulse (RUP/RDN), it cannot update the DCO control code right after the data transition edge, and it leads to a relatively slow response to the phase error. Therefore, when the phase error is large, the compensation time of the proposed design is relatively short.

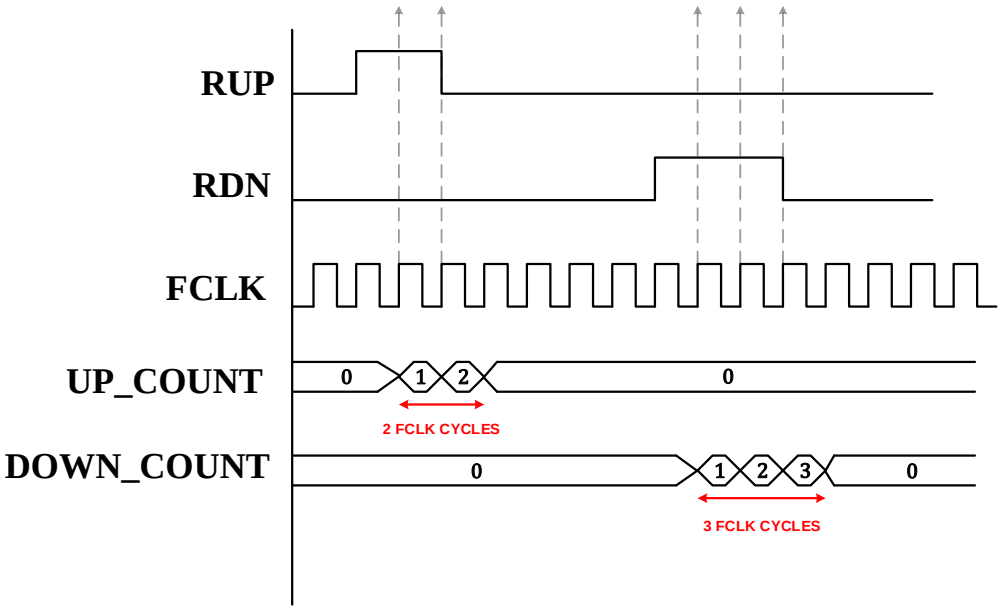



Fig. 2.23: The phase error detection method in [34]

Fig. 2.24 shows the Compensation flow with random data input in [34]. Because [34] uses the PFD to generate phase error signals then uses a high frequency clock to quantize the phase error, it cannot update the DCO control code right after the data transition edge, and it leads to a relatively slow response to the phase error. The controller also has except conditions to reduce the tracking ability when some special patterns are input. However, because the controller operates at 16 times the data rate, the complicated controller circuit will result in more power consumption.

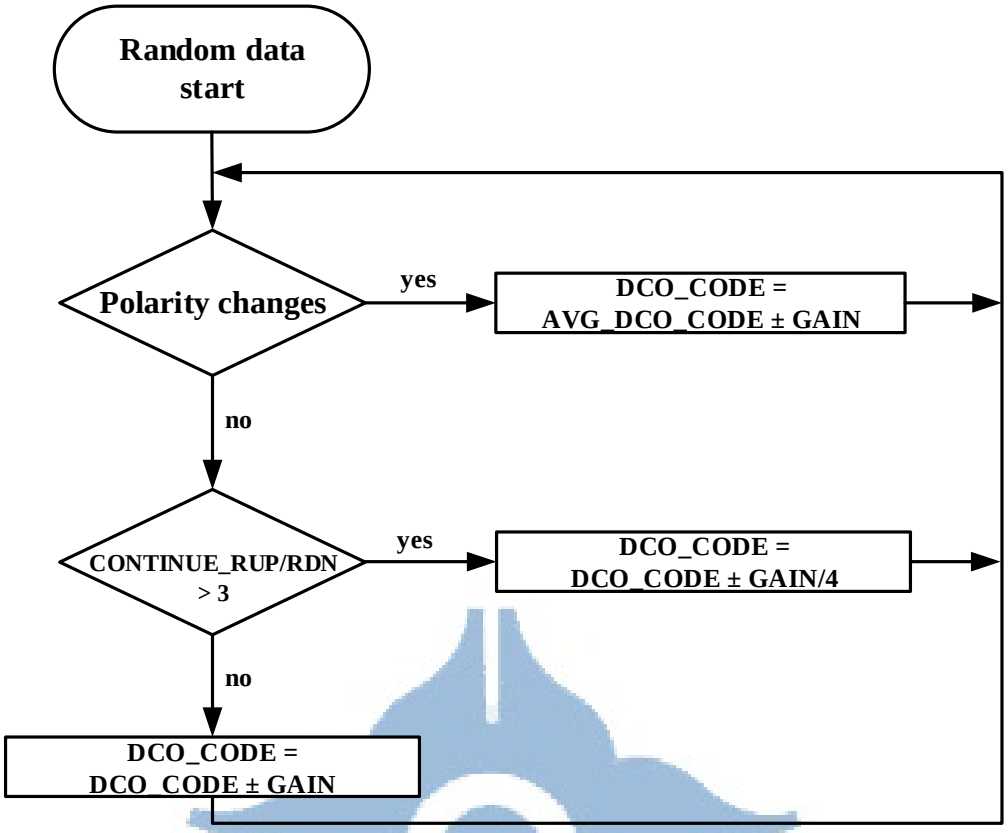


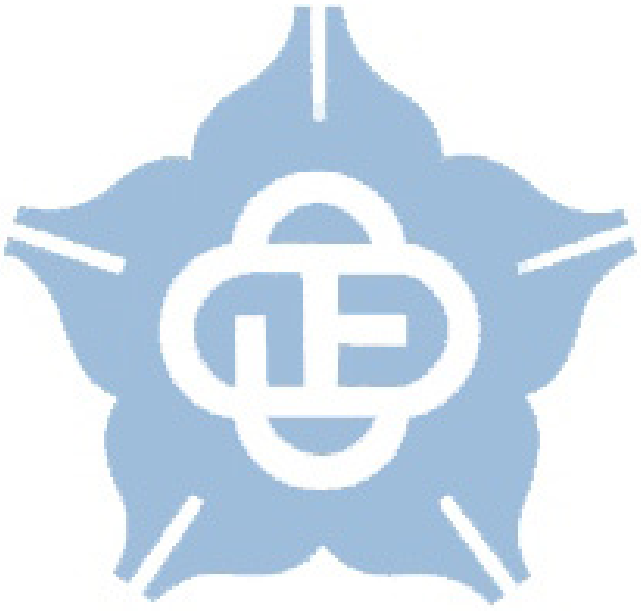

Fig. 2.24: Compensation flow with random data input in [34]

# 2.5 Summary

We use the NRZI format to transmit the data. In addition, because the random data may have long CID, we use the bit stuffer to insert the data transitions. Moreover, in above discussion, the wideband transceiver must have a CDR circuit, and the oversampling architecture of the CDR circuit requires an external reference clock or a frequency synthesizer to generate the stable frequency. Therefore, it has relatively high power consumption and relatively low frequency drift tolerance.

The proposed reference-less CDR circuit does not require a reference clock and a frequency synthesizer, and thus the power consumption is reduced. In addition, the gain calibration method can have the same amount of the phase error compensation with the same phase error under the PVT variations. Moreover, we use the 16 multi-

phases to quantize the phase error (Edge_error) and select the output data from the sampling data of the 16 phases signals. The performance of the proposed design will be discussed in the chapter 3.



# Chapter 3 Experimental Results

## 3.1 Test Chip Implementation

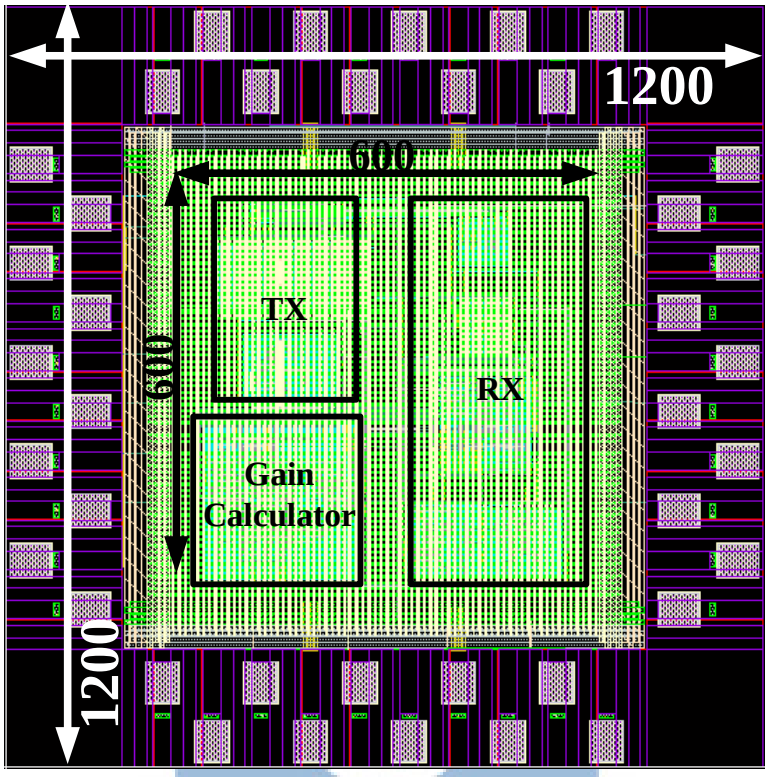



Fig. 3.1: Layout of the test chip

The layout of the test chip is shown in Fig. 3.1. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The core size of the chip is $600 \times 600 \mu m^2$. The chip size including I/O PADs is $1200 \times 1200 \mu m^2$.

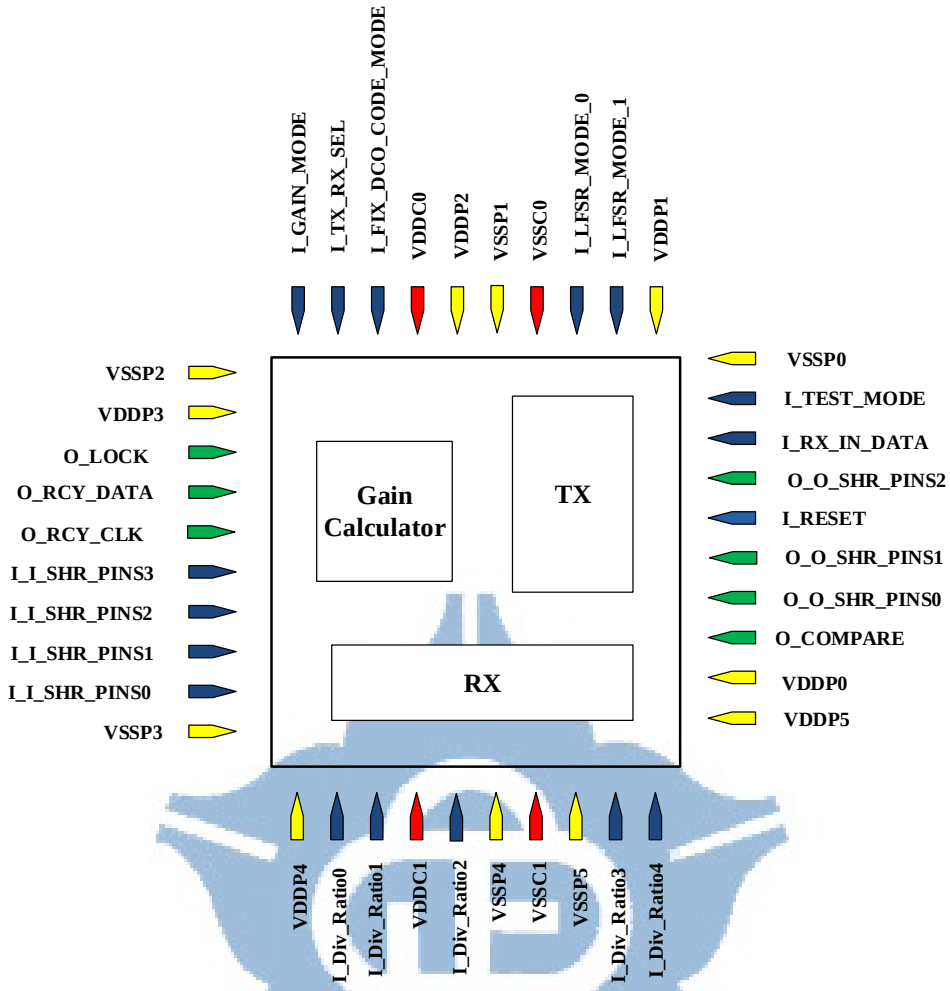



Fig. 3.2: Chip floorplan and I/O plan

Fig. 3.2 shows the test chip I/O planning and the floor planning of the proposed wideband signaling transceiver. There are 17 input pins, 7 output pins, and 16 power pins. The test chip consists of a TX circuit, an RX circuit, and a gain calculator. The detail I/O description is shown in Table 3.1.

Table 3.1: I/O PAD Description

| Input | Bits | Function |
|---|---|---|
| RESET | 1 | System reset |
| TX_RX_SEL | 1 | 0: TX<br>1: RX |

<table>
<tr><td>GAIN_MODE</td><td>1</td><td>0: Internal calculated<br>1: External input</td></tr>
<tr><td>TEST_MODE</td><td>1</td><td>0: Loopback test<br>1: Normal mode</td></tr>
<tr><td>LFSR_MODE</td><td>2</td><td>0: random data<br>1: 0101 repeat<br>2: 0011 repeat<br>3: 0001 repeat</td></tr>
<tr><td>FIX_DCO_CODE_MODE</td><td>1</td><td>0 : Normal mode<br>1 : fixed the DCO code when CDR frequency LOCK</td></tr>
<tr><td>I_SHR_PINS</td><td>4</td><td>TEST_MODE = 0<table><tr><td>Index</td><td></td></tr><tr><td>3</td><td>DCO_CODE[10]</td></tr><tr><td>2</td><td>DCO_CODE[9]</td></tr><tr><td>1</td><td>DCO_CODE[8]</td></tr><tr><td>0</td><td>DCO_CODE[7]</td></tr></table><table><tr><td colspan="3">TEST_MODE = 1</td></tr><tr><td>Index</td><td>TX</td><td>RX</td></tr><tr><td>3</td><td>DCO_CODE[10]</td><td>GAIN[3]</td></tr><tr><td>2</td><td>DCO_CODE[9]</td><td>GAIN[2]</td></tr><tr><td>1</td><td>DCO_CODE[8]</td><td>GAIN[1]</td></tr><tr><td>0</td><td>DCO_CODE[7]</td><td>GAIN[0]</td></tr></table></td></tr>
<tr><td>RX_IN_DATA</td><td>1</td><td>RX_IN_DATA</td></tr>
<tr><td>Div_R</td><td>5</td><td>Divide Ratio</td></tr>
</table>

| Output | Bits | Function | | | |
|---|---|---|---|---|---|
| RCY_CLK | 1 | CDR circuit recovery clock | | | |
| LOCK | 1 | CDR circuit LOCK | | | |
| RCY_DATA | 1 | CDR circuit recovery data | | | |
| COMPARE | 1 | Detect the error in the LFSR (1: has error , 0: No error) | | | |
| O_SHR_PINS | 3 | Index | TX | LFSR_MODE = 0 | LFSR_MODE = 1 2 3 |
| | | 2 | TX_DATA | BER_Flag[0] | SFD_VALID |
| | | 1 | TX_CLK | BER_Flag[1] | DECODE_DATA |
| | | 0 | STUFF_DATA | BER_Flag[2] | UNSTUFF_DATA |

## 3.2 Test Plan

Firstly, we set the TEST_MODE pin to the normal mode and the TX_RX_SEL pin is 0, and the test chip will operate at TX mode, and the O_SHR_PINS pins will show the TX_DATA, TX_CLK, and STUFF_DATA at TX mode. Therefore, we can observe the result by the O_SHR_PINS pins.

Then, when the TX mode works correctly, we will set the TEST_MODE pin to 0 and the test chip will operate in the loopback mode. In addition, at the TX mode and loopback mode, we can adjust the DCO_CODE [10:7] by I_SHR_PINS pins. Because the I/O pin number has limitation, we only adjust the coarse-tuning DCO control code to adjust the frequency of the TX_DCO.

Finally, when the loopback mode works correctly, we set the TEST_MODE pin to the normal mode and one of the test chip operates at TX mode, and the other test chip operates at RX mode. Then, the output data of the TX chip are connected to the human body then connects to RX_IN_DATA pin.

In addition, we can set the LFSR_MODE pin to generate different patterns. If the LFSR_MODE is 0, the TX will generate the random data and the O_SHR_PINS will be set to the BER_Flag[2:0]. Table 3.2 shows the BER_Flag information so that BER information of the proposed receiver can be obtained during chip testing. If the LFSR_MODE is 1, 2, or 3, the TX will generate the regular pattern and the O_SHR_PINS will be set to show the SFD_VALID, DECODE_DATA, and UNSTUFF_DATA for debugging. Moreover, in the RX, if there has error in the gain calculation, GAIN_MODE can be set to the external mode so that the external gain value can be input to the RX by the I_SHR_PINS pins.

Table 3.2: BER_Flag information

| BER_Flag | BER Performance |
|---|---|
| 3'd0 | Reset |
| 3'd1 | First bit error occurs before first packet finishes. |
| 3'd2 | BER < $10^{-3}$ |
| 3'd3 | BER < $10^{-4}$ |
| 3'd4 | BER < $10^{-5}$ |
| 3'd5 | BER < $10^{-6}$ |
| 3'd6 | BER < $10^{-7}$ |
| 3'd7 | BER < $10^{-8}$ |

# 3.3 Simulation Results

## 3.3.1 Post-layout Simulation

Figs. 3.3 – 3.5 show the one packet post-layout simulation of the proposed WBS

transceiver in the loopback mode at 20Mbps. Firstly, the TX generates the preamble data, the SFD, and the random data after the circuit reset. Then, the RX uses the preamble data to calculate the gain value and starts to perform frequency and phase acquisition. After the frequency and phase acquisition is complete, the frequency of the DCO clock is 16 times the frequency of the FCLK. Then, when the ADCDR detects the SFD pattern, it starts random data tracking and recovers the encoding data and the clock. Finally, the demodulator will demodulate the encoding data to recover the data. In addition, we use the LFSR circuit that is the same as the LFSR circuit used in the transmitter to generate the same random data sequence. The compare signal and BER_Flag[2:0] show the bit error. When the compare signal is 1, it means there has a bit error. Moreover, in TX, there has 200 cycles spacing between packets because the RX need time to recover and demodulate the data.

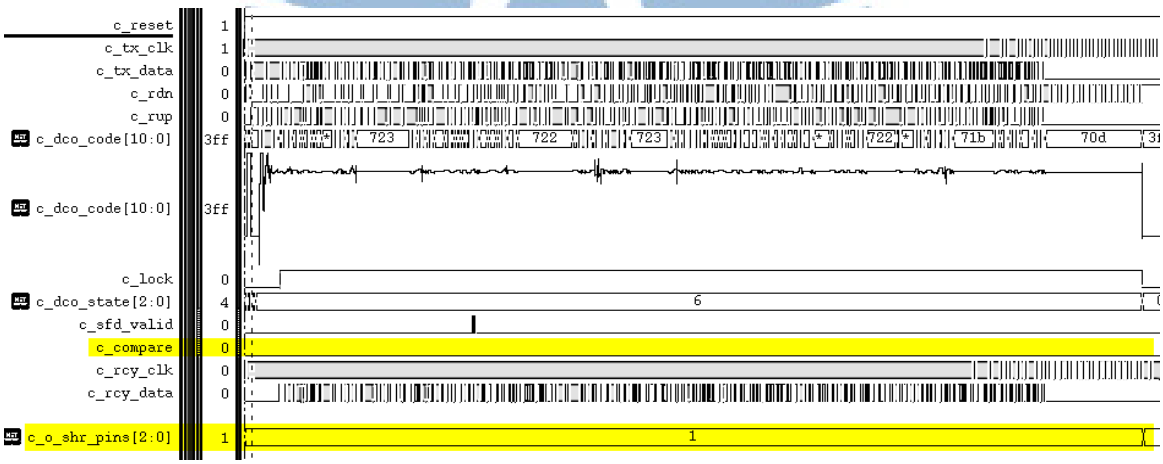



Fig. 3.3: Post-Sim at 1.0V, TT corner, 20Mbps


Fig. 3.4: Post-Sim at 1.1V, FF corner, 20Mbps

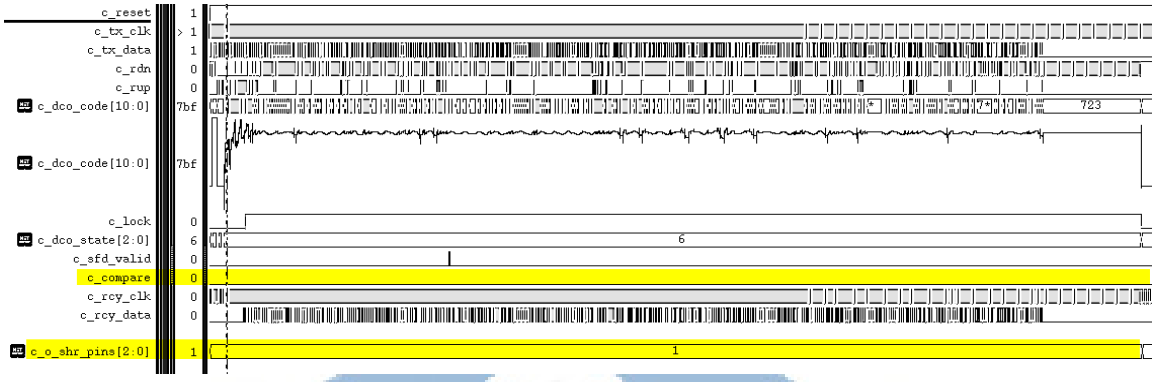



Fig. 3.5: Post-Sim at 0.9V, SS corner, 20Mbps

Figs. 3.6 - 3.8 show the post-layout simulation of the proposed WBS transceiver in regular pattern mode at 20Mbps. In order to provide debug information for testing the chip, we add several regular pattern modes in the TX because we cannot check the random data are correct or not with only recovery data. In this mode, the TX can generate the regular pattern (0101, 0011, 0001) and we can check the recovery data easily and confirm whether the circuits execute normally.

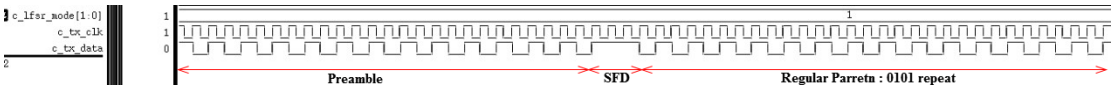



Fig. 3.6: Regular Pattern is ‘0101’, Post-Sim at 1V, TT corner, 20Mbps

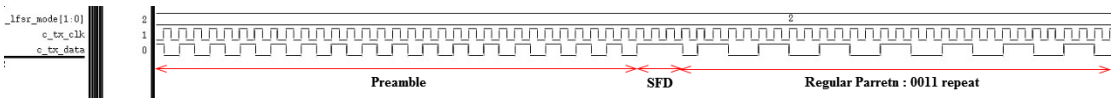



Fig. 3.7: Regular Pattern is ‘0011’, Post-Sim at 1V, TT corner, 20Mbps

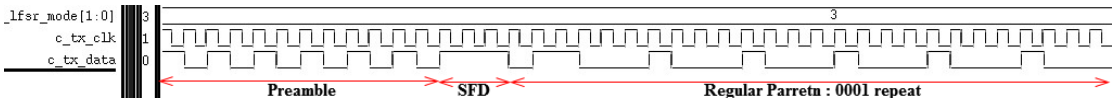



Fig. 3.8: Regular Pattern is '0001', Post-Sim at 1V, TT corner, 20Mbps

Fig. 3.9 shows the post-layout simulation of the proposed WBS transceiver in the fixed DCO control code mode. In this mode, we can fix the DCO control code after the frequency and phase acquisition is complete. Therefore, we can check whether the frequency of the recovery clock (RCY_CLK) is equal to the data rate.

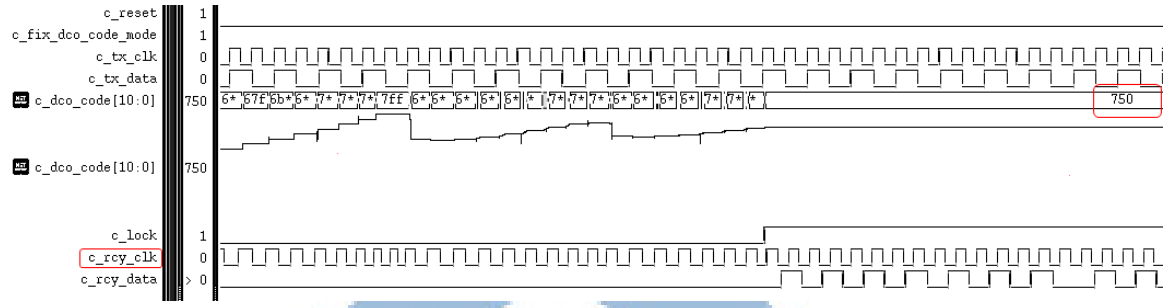



Fig. 3.9: Fixed DCO control code mode, Post-Sim at 1V, TT corner, 20Mbps

## 3.3.2 Simulation Result

Because the I/O pin count has limitation, we only adjust the coarse-tuning DCO control code. Table. 3.3 shows the adjustable DCO frequency range at the post-layout simulation and the ratio of the divider (N) is equal to 1.

Table 3.3: The adjustable DCO frequency range at the post-layout simulation.

| PVT corner | Slow case | Typical case | Fast case |
|---|---|---|---|
| | (SS, 0.9V,100°C) | (TT, 1.0V, 25°C) | (FF, 1.1V, 0°C) |
| DCO Frequency Range (MHz) | 81~372 | 110~512 | 141~640 |
| RCY_CLK Frequency Range (MHZ) | 5~23 | 7~32 | 9~40 |

Fig. 3.10 shows the gain value at different data rate of the proposed WBS transceiver by post-layout simulation. As the data rate increases, the gain value will be decreased. In addition, because the proposed DCO cannot generate the low frequencies directly. Thus, we add an external divider to increase the frequency range of the DCO. At high data rate, the ratio of the divider (N) equals to 1. However, at low data rate, the ratio of the divider (N) is not 1 and the gain value must be divided by the ratio of the divider (N). Therefore, the gain value has non-linear increasing as the data rate decreases.

Moreover, because the body temperature range is very narrow. Fig. 3.10 shows the gain value at the 36 ° C and 40 ° C with different supply voltage. At all listed conditions, the gain value are similar. Therefore, temperature and voltage violations will not greater affect the gain value. In the other word, the gain calibration is to calibrate the process violations.

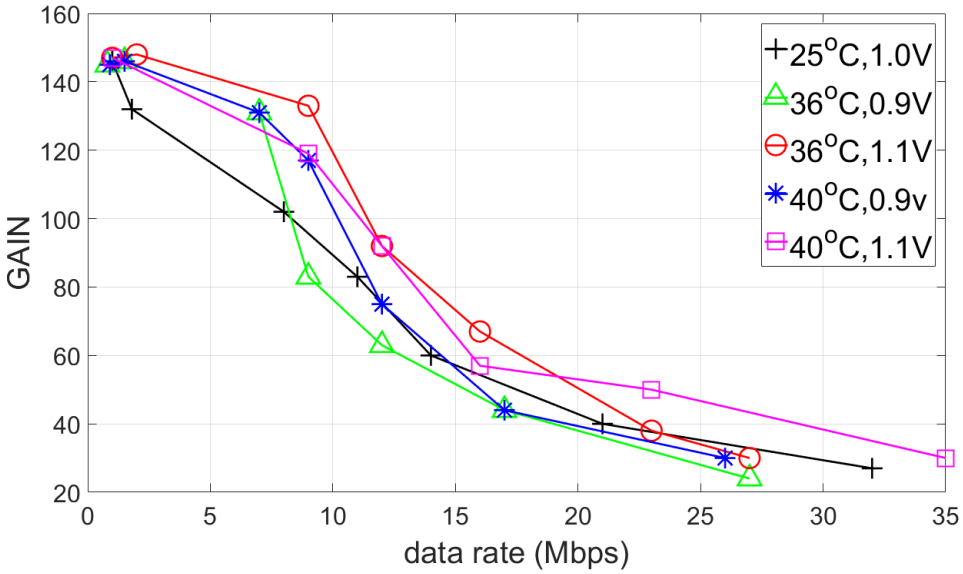



Fig. 3.10 The gain value at different data rate in post-layout simulation

Figs. 3.11 – 3.13 show the power spectral density (PSD) of the TX output with the regular pattern (Fig. 3.11) and random data (Figs. 3.12, 3.13) about 20Mbps (actually is at 19.4 Mbps due to only the coarse-tuning DCO control code is set). Fig. 3.12 shows the PSD of the random data without jitter about 20Mbps and Fig. 3.13 shows the PSD of the random data with 10ns $P_k$-$P_k$ jitter about 20Mbps. In addition, the signal below the -80 dB/Hz can be considered the noise. Therefore, the bandwidth that is used by the proposed WBS transceiver is about from 1 MHz to 40MHz. Because we use the NRZI format to transmit data, the data contain a variety of frequency components. Therefore, the NRZI data cause less interferences to the nearby environment.

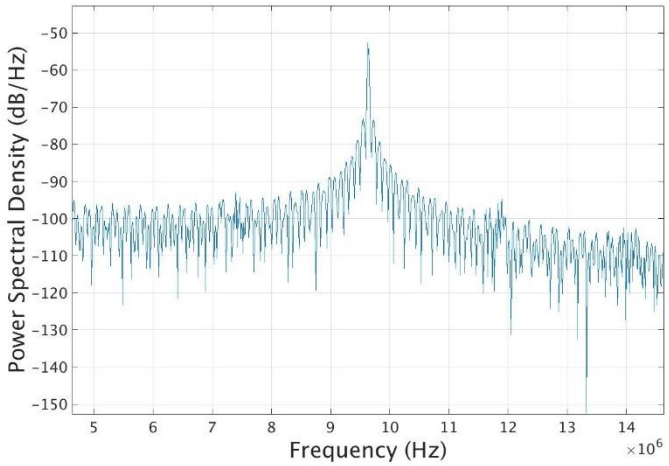



Fig. 3.11 The power spectral density (PSD) with the regular pattern

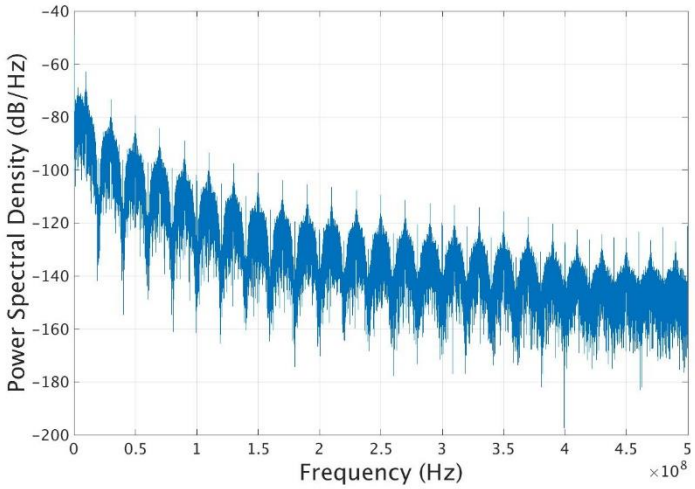



Fig. 3.12 The power spectral density (PSD) with the random pattern without jitter

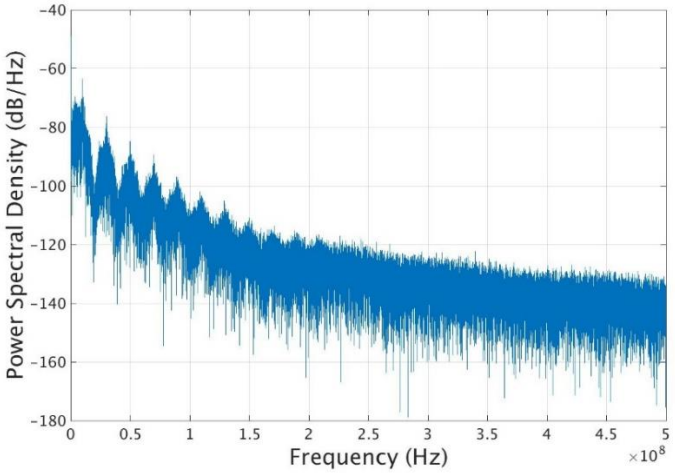



Fig. 3.13 The power spectral density (PSD) with the random pattern with 10ns $P_k$-$P_k$ jitter

Because the bit stuffer inserts the data transition when there are 3 continues identical digits (CID). Therefore, there are some harmonic components which can be found in Fig. 3.12. Fig. 3.14 shows the period histogram of the random data. The highest peak is at 100 ns because the preamble patterns in the packet. Therefore, the signal with 100ns period cause the peak frequency components at 10MHz in the PSD shown in Fig. 3.12.

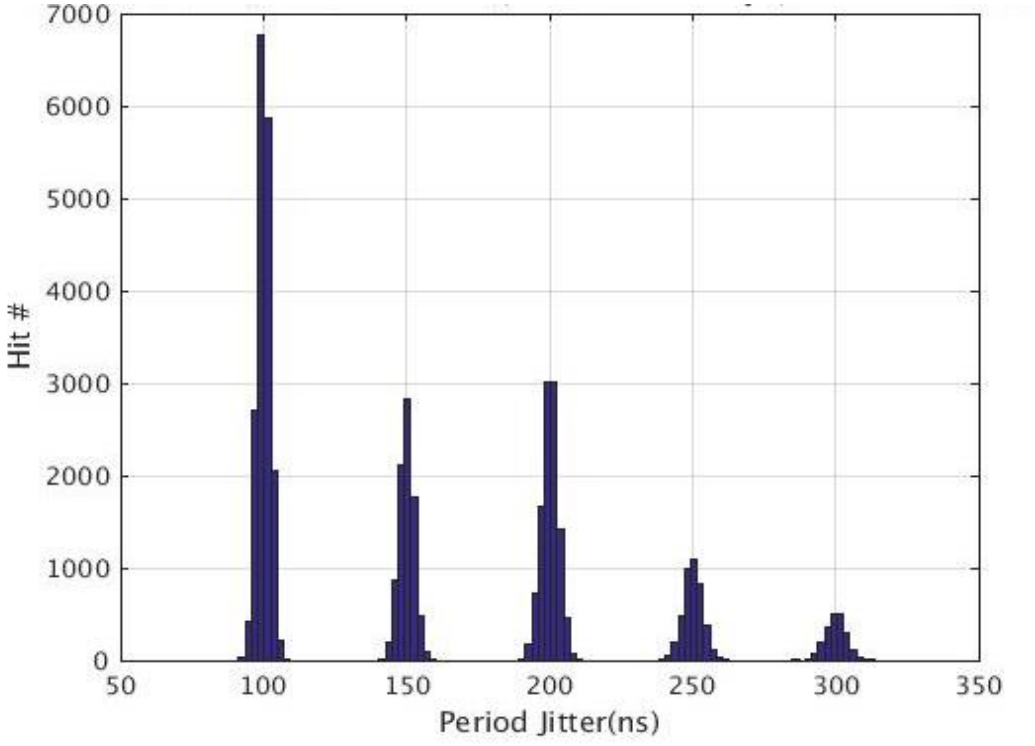



Fig. 3.14 The period histogram of the random data at 20 Mbps

Figs. 3.15 – 3.17 show the eye diagram of the transmitted random data pattern at 20Mbps. When the data has no jitter effects, the eye diagram is very clear. Oppositely, if the data has jitter effects, the transition edge has variations. The proposed ADCDR circuit can still recover the data with data jitter shown in Fig. 3.17. The BER performance of the proposed ADCDR is $< 10^{-7}$ with the $P_k$-$P_k$ jitter less than 10ns and the BER performance is $< 10^{-5}$ with the $P_k$-$P_k$ jitter less than 16ns.

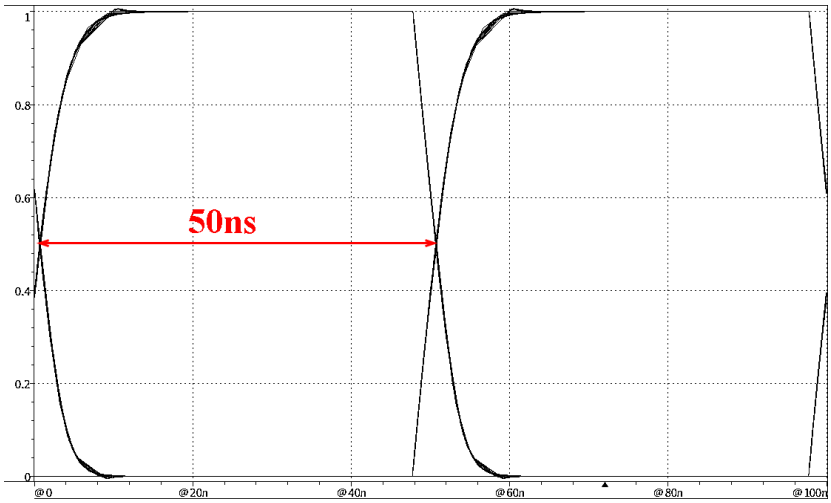



Fig. 3.15: Eye diagram of the transmitted random data without jitter at 20Mbps

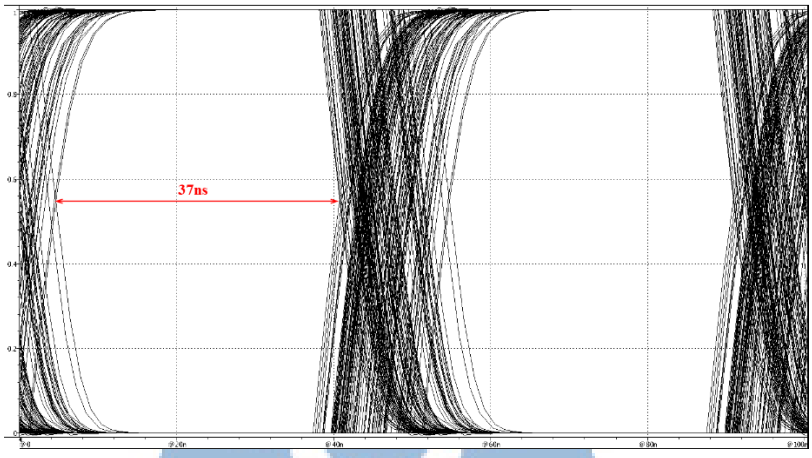



Fig. 3.16: Eye diagram of the transmitted random data with the jitter less than 10ns at 20Mbps

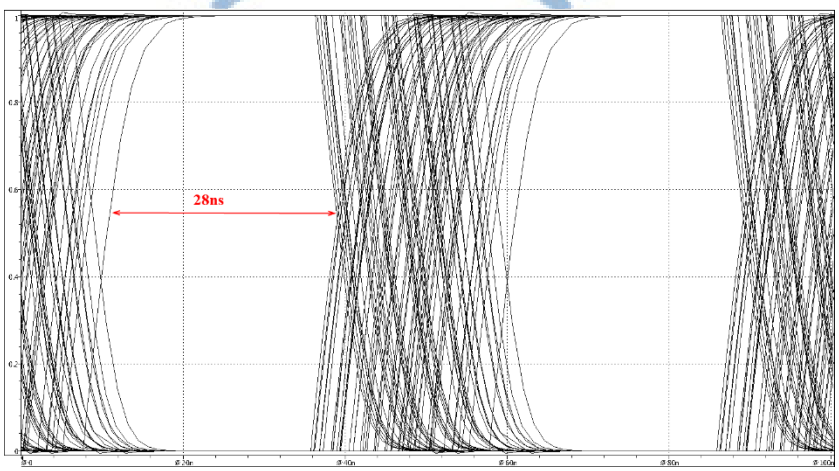



Fig. 3.17: Eye diagram of the transmitted random data with the jitter less than 16ns at 20Mbps

# 3.4 Error Free Measurement

## 3.4.1 Random Jitter Tolerance

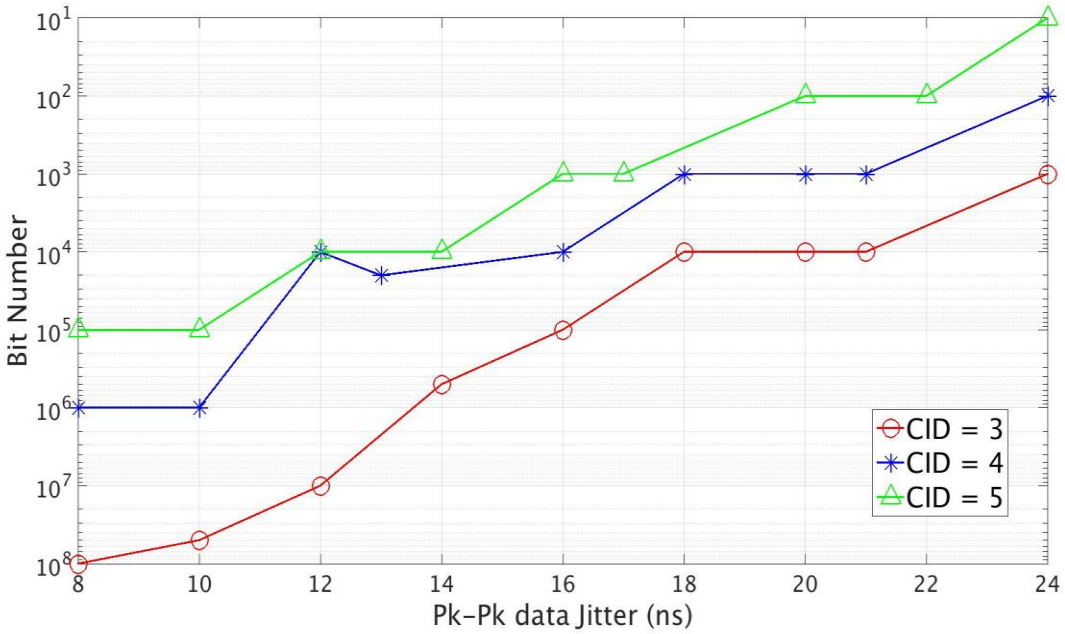



Fig. 3.18: Error-Free simulation result with different CID at 20Mbps

Fig. 3.18 shows the error-free simulation results with different CID at 20Mbps. If CID is reduced, there has more data transition. Therefore, the ADCDR can track phase more easily and it can improve the BER performance of the ADCDR. In the proposed ADCDR, the transceiver has a bit-error-rate (BER) < $10^{-7}$ with 10ns Pk-Pk random data jitter when the number of CID is 3.

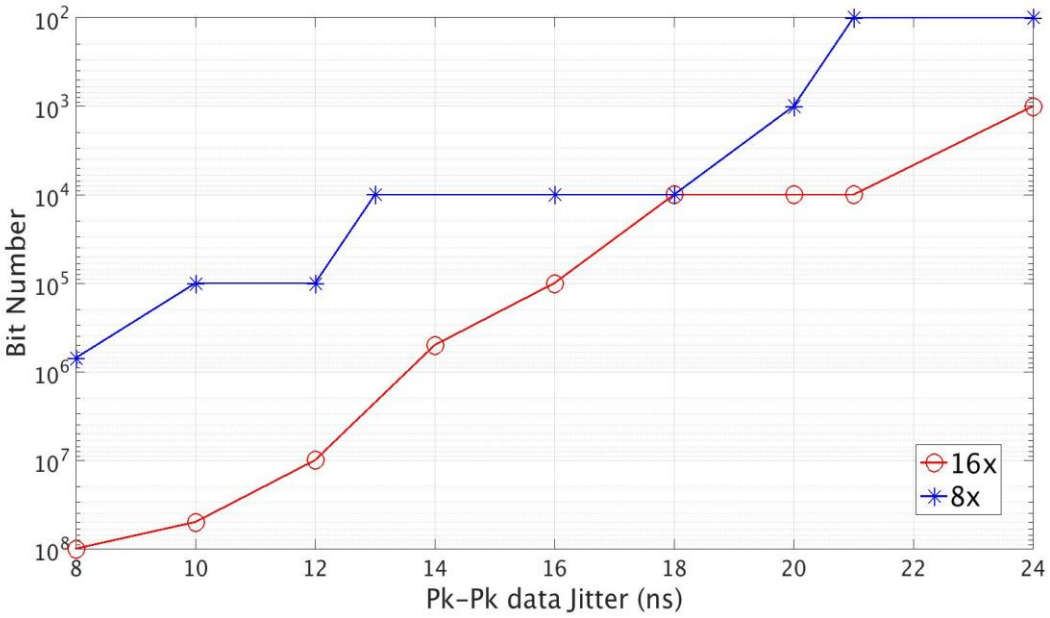



Fig. 3.19: Error-Free simulation result at 20Mbps with different oversampling rate

Fig. 3.19 shows the error-free simulation result at 20 Mbps with different oversampling rate in the ADCDR. The simulation result shows that the BER performance of the 16x oversampling rate is $< 10^{-7}$ and the BER performance of the 8x oversampling rate is $<10^{-5}$. Therefore, in the proposed ADCDR, the 16x oversampling rate is used.

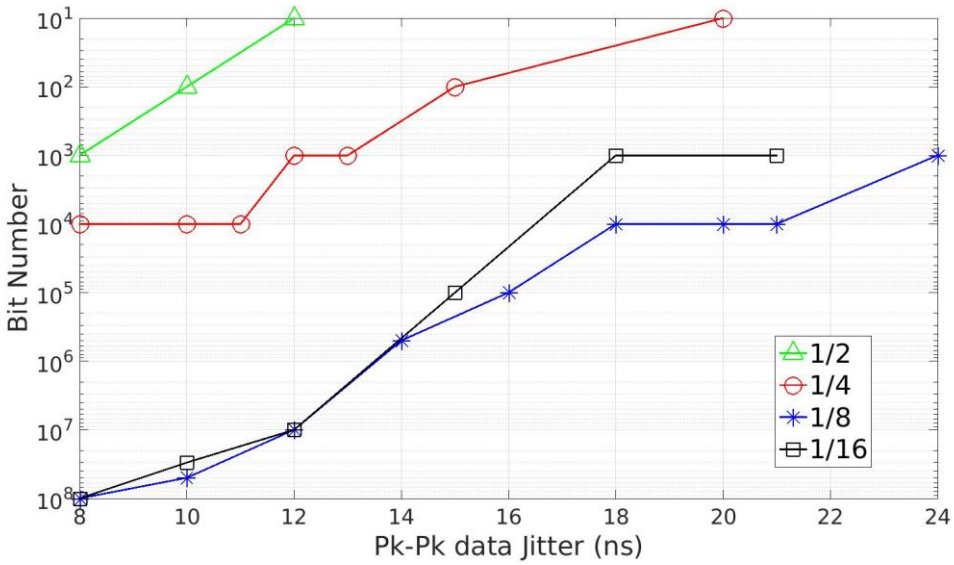



Fig. 3.20: Error-Free simulation result at 20Mbps with different gain ratio

In order to stabilize the DCO control code, the controller only compensates for

eighth of the detected phase error (gain ratio is 1/8). Fig. 3.20 shows the error-free simulation result at 20 Mbps with different gain ratio. If the gain ratio is too large, the DCO control code will have large variations and the jitter tolerance is decreased accordingly. In addition, when the gain ratio is increased, the jitter tolerance is converged, and thus the gain ratio 1/8 is chosen.

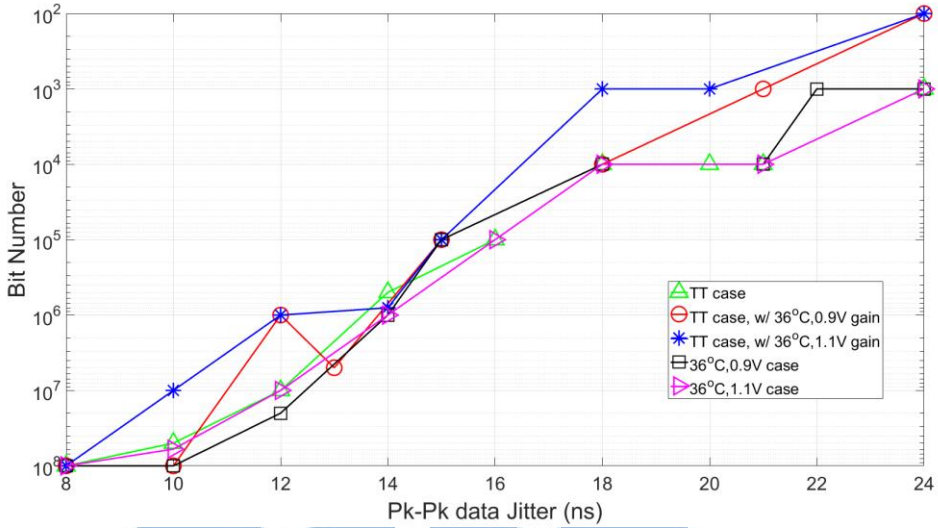



Fig. 3.21: Error-Free simulation result at 20Mbps with different gain value

Fig. 3.21 shows the error-free simulation result at 20 Mbps with different gain value. The automatically phase track gain calibration method is used to compensate for the DCO resolution variations under the PVT variations. In typical case (25℃, 1.0V), (36℃, 0.9V) case, and (36℃, 1.1V) case, the BER performance of the proposed ADCDR is almost the same with voltage and temperatures variations. When the gain calculation is complete, and if there has voltage and temperature variations, the BER performance is almost the same too. According to the simulation results shown in Fig 3.21, the voltage and temperatures variations have little effect on the gain value calculation. Therefore, the gain value does not require to be recalculated in each packet, and the gain calculation circuit can be turned off to reduce power consumption.

## 3.4.2 Sinusoidal Jitter Tolerance

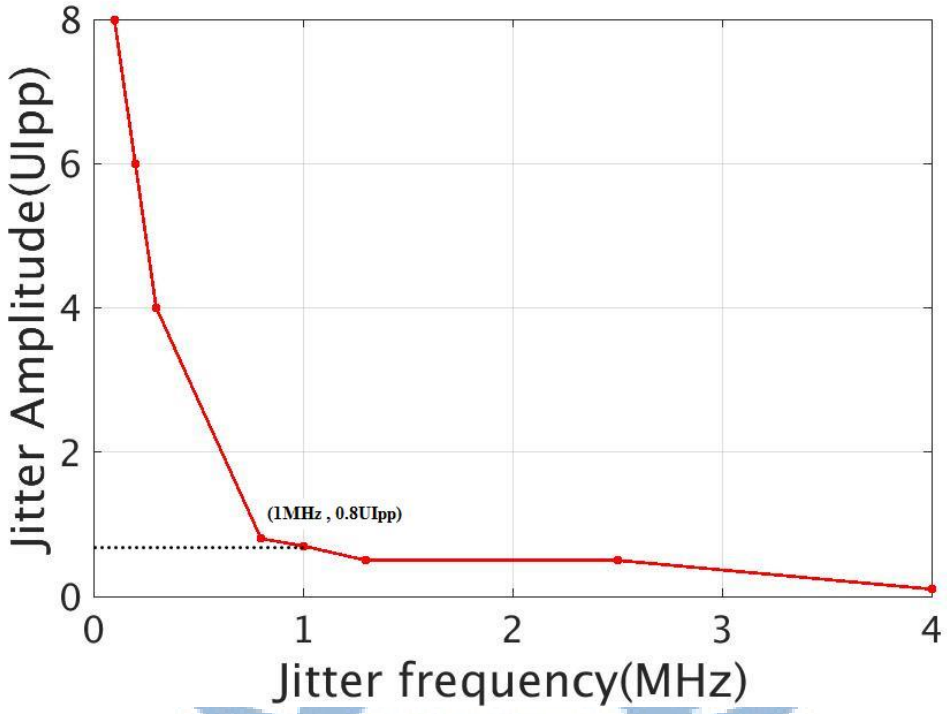



Fig. 3.22: Sinusoidal jitter tolerance performance

In jitter tolerance testing of the receiver, the data are modulated with a sinusoidal jitter. Therefore, the input data have a regular jitter frequency and data rate has variations. The sinusoidal jitter has three parameters, $UI_{jitter}$ (peak-peak), $\Delta f$ and $f_j$, as shown in Eq. 3.1. The $UI_{jitter}$ (peak-peak) is the total jitter accumulation in one sinusoidal modulation period. The $\Delta f$ is the maximum frequency variation during the sinusoidal modulation period. The $f_j$ is the modulation frequency of the sinusoidal jitter.

$$UI_{jitter}\ (peak-peak) = \frac{\Delta f}{f_{j*\pi}} \tag{3.1}$$

Fig. 3.22 shows the sinusoidal jitter tolerance of the ADCDR circuit at 20 Mbps. The corner frequency is at 1MHz with 0.2UI jitter tolerance.

### 3.4.3 Error Free Measurement with Frequency Drift

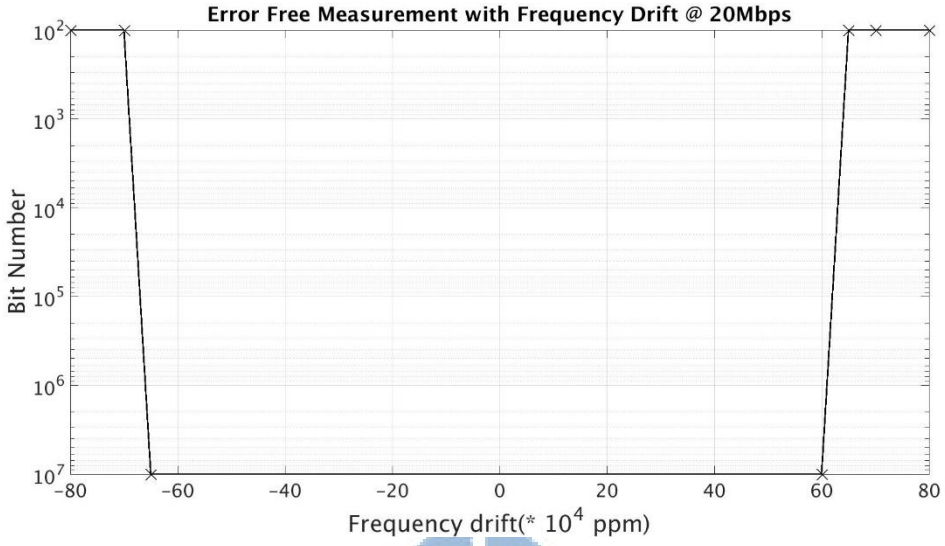



Fig. 3.23: Error-Free measurement with different frequency drift at 20Mbps

When the baud rate of the transmitter differs from the expected data rate, it causes the frequency drift problem in the receiver. Fig. 3.23 shows the error-free measurement with different frequency drift at 20Mbps. The performance of the ADCDR has a BER $< 10^{-7}$ within the frequency range from -650000 ppm to +600000 ppm at 20Mbps. At mentioned above, the adjustable DCO frequency range is from 110MHz to 512MHz. If the ratio of frequency divider is set to 1, the RCY_CLK frequency range is from 6.875MHz to 32MHz. Therefore, if the data rate of the TX is out of the range 6.875Mbps to 32Mbps, it may cause the bit errors. The proposed reference-less ADCDR circuit has the frequency and phase tracking ability. Thus, if the DCO can generate the required 16x oversampling clock, there are no bit errors in the proposed reference-less ADCDR circuit. However, for the oversampling architecture [24, 36], if there exists frequency drift, they are easy to have bit errors. In [24], the performance is BER $< 10^{-7}$ within the frequency drift ranging from -47200 ppm to +48600 ppm at 40Mbps.

## 3.5 Test Chip Summary and Comparison Table

Table 3.4: Chip Summary

| Parameter | Spec. | Post-sim(TT) | Post-sim(FF) | Post-sim(SS) |
|---|---|---|---|---|
| Power supply (V) | 1.0 | 1.0 | 1.1 | 0.9 |
| Operating Range | 1 Mbps ~ 20Mbps | 1 Mbps ~ 20Mbps | 1 Mbps ~ 20Mbps | 1 Mbps ~ 20Mbps |
| Power Consumption (mW) | 3@20Mbps | 2.2@20Mbps | 2.36@20Mbps | 1.83@20Mbps |
| Energy/bit | 0.15 nJ/b | 0.11 nJ/b | 0.118 nJ/b | 0.09 nJ/b |
| Core Area($mm^2$) | 0.6 * 0.6 | 0.6 * 0.6 | 0.6 * 0.6 | 0.6 * 0.6 |

The test chip summary is shown in Table 3.4. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The data rate of the proposed WBS transceiver is from 1Mbps to 20Mbps. The core area is 0.36 $mm^2$. The power consumption is 2.2 mW at 20Mbps without the AFE circuit in the typical case. The bit error rate (BER) is less than $10^{-7}$ at 20Mbps , and the energy consumption per bit is 0.11nJ/b at 20Mbps in the typical case.

Table 3.5: Power consumption table

| Parameter | TX | RX | GAIN | Total (TX+RX) |
|---|---|---|---|---|
| Power (mW) | **0.65** | **1.55** | **0.1** | **2.2** |

The power consumption table of the transceiver is shown in Table 3.5. When the test chip operates at the TX mode, the power consumption is 0.65mW. When the test chip operates at the RX mode, the power consumption of the RX circuit that includes

gain calculator circuit is 1.55mW. In addition, the power consumption of the gain calculator circuit of the RX circuit is 0.1mW because the gain calculator circuit only operate at the beginning of each packet. In the loopback mode, the power consumption of the test chip is 2.2mW.

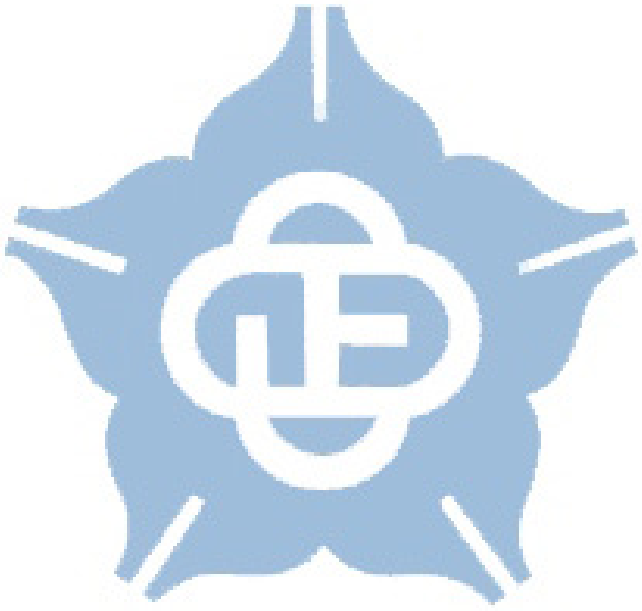
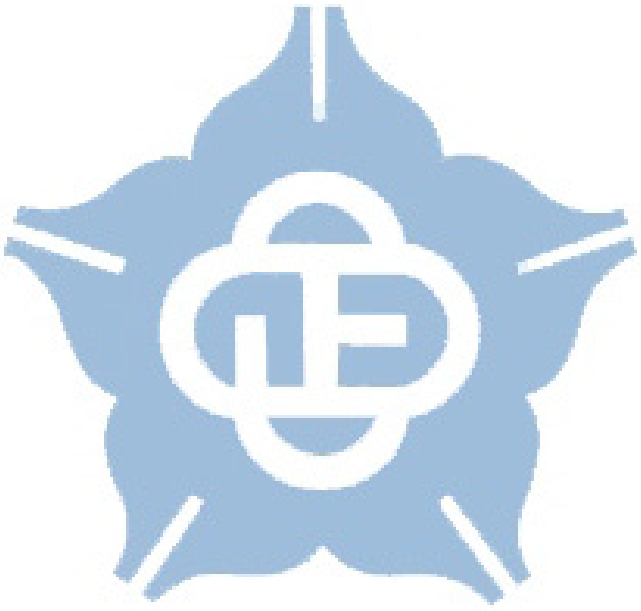


Table 3.6: Comparison table

| | [40] JSSC'07 | [38] JSSC'09 | [16] JSSC'12 | [17] ISSCC'14 | [14] VLSI-DAT'15 | [19] JSSC'16 | Proposed |
|---|---|---|---|---|---|---|---|
| Communication Method | Wideband Signaling | FSK | FSK | 3-level Walsh Coding | OFDM | BPSK | Wideband Signaling |
| Process | 0.25 μm | 0.18 μm | 0.18 μm | 65 nm | 90 nm | 65 nm | 90 nm |
| Frequency band | Wideband | 30-120 MHz | 40-120 MHz | 40-80 MHz | 35-45 MHz | 20-60 MHz、140-180 MHz | 1-40 MHz |
| Data Rate | 2 Mbps | 60 Kbps ~ 10 Mbps | 1 Kbps ~ 10 Mbps | 60 Mbps | 29.1Mbps | 80 Mbps | 1 Mbps ~ 20 Mbps |
| Modulation | No | Adaptive Frequency Hopping FSK | Double FSK | 3-level Walsh Coding | 16-QAM OFDM | Binary Phase Shift Keying | Non-Return-to-Zero-Inversed |
| Supply | 1 V | 1 V | 1 V | 1.1 V | 0.53 V | 1.2 V | 1 V |
| Sensitivity | -36 dBm | -65 dBm | -66 dBm | -58 dBm | N/A | -58 dBm | -18.87dBm |
| Power Consumption | 0.2 mW | 3.7 mW | 4.4 mW | 10.87 mW | 9.37mW | 6.3 mW | 2.2 mW (w/o AFE circuit) |
| Area | 0.85 $mm^2$ | 2.30 $mm^2$ | 4.5 $mm^2$ | 0.85 $mm^2$ | 5.2 $mm^2$ | 5.76 $mm^2$ | 0.36 $mm^2$ |
| BER | $1.1*10^{-7}$ | $10^{-5}$ (10Mbps) $<10^{-9}$(60Kbps) | $10^{-5}$(10Mbps) $10^{-12}$(10Kbps) | $<10^{-5}$ @ 60Mbps | N/A | $<10^{-5}$ @ 40Mbps | $<10^{-7}$ @20Mbps |
| Energy/bit | 2.5 nJ/b | 0.37 nJ/b | 0.44 nJ/b | 0.18nJ/b | 0.32 nJ/b | 0.079 nJ/b | 0.11nJ/b |

Table 3.6 shows the comparison table with other BCC designs. We have the smaller chip area than other BCC design. Although [17] and [19] achieve higher data rate, they have higher power consumption. In addition, they also use the high frequency band to transmit the data so they may interfere with other electronic products. Moreover, the proposed design also has higher data rate than [40], [38], and [16].



# Chapter 4 Conclusion and Future Works

## 4.1 Conclusion

In this thesis, a WBS transceiver is proposed. In the TX, the pattern generator can generate the random pattern or regular pattern. The data will be stuffed by the bit stuffer to limit the CID to 3 and then be modulated to the NRZI format. Moreover, the data are transmitted in the packet format. In the RX, a reference-less all-digital clock and data recovery (ADCDR) is proposed. In the preamble pattern, the ADCDR controller uses binary search to adjust the DCO control codes in the frequency and phase acquisition. After phase and frequency acquisition is completed, the ADCDR controller detects the SFD and start random data tracking. In random data tracking, the 16 phases will detect the transition edge position and quantize the phase error (Edge_error), and multiplied by the gain to get the value of the compensation.

In addition, because the DCO resolution varies under the PVT variations. Therefore, an automatically phase track gain calibration method is proposed to solve the problem. The proposed method uses the $R_{mid}$ and $R_{max}$ to calculate the gain value and the $R_{mid}$ and $R_{max}$ are the symbol period divided by the medium DCO period and minimum DCO period, respectively. Thus, in different PVT conditions, the gain value will be calibrated automatically and we can ensure the value of the compensation is same for the same phase error.

The test chip is implemented in TSMC 90nm process with standard cells. The core area is 0.36 $mm^2$ and the power consumption is 2.2mW at 20Mbps. In addition, the simulation result shows that the BER performance is < $10^{-7}$.

# 4.2 Future Works

The proposed ADCDR circuit has two loops. In the frequency loop, by using the PFD to generate the UP/DN signals to perform the frequency and phase acquisition with the binary search scheme. When the frequency and phase acquisition is completed, the PFD will be disabled and the 16-phase clock generator will generate the 16 phases to detect the transition edge and quantize the phase error (Edge_error). However, the PFD circuit only operate in the frequency and phase acquisition, thus, if the PFD is removed, the area will be reduce.

The method that used the multi-phase to perform the frequency and phase acquisition. According to the transition edge detection, the multi-phase can generate the information that current transition edge leads or lags the ideal transition edge position. Therefore, it has the similar phase error detection ability with the bang-bang PFD. Fig. 4.1 show the waveform of the frequency and phase acquisition by only using the multi-phase to detect the transition edge. According the transition edge detection, the multi-phase can be used to generate the LEAD/LAG signals to the controller to adjust the DCO code. As shown in Fig. 4.2, the frequency acquisition is also converged.

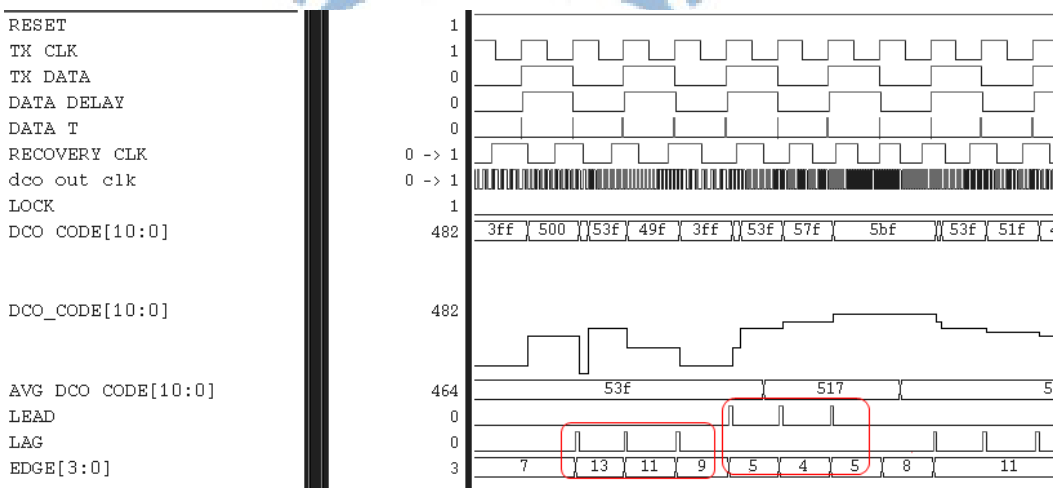



Fig. 4.1: The waveform of the frequency and phase acquisition by using the multi-phase

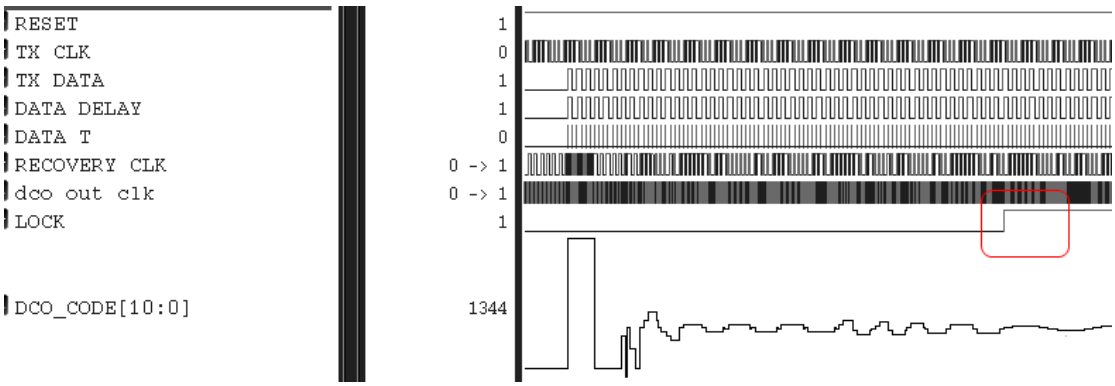



Fig. 4.2: The waveform of the frequency and phase acquisition is completed

Moreover, according to the simulation result shown in Fig 3.21, the gain value is not sensitive for temperature and voltage variations. Therefore, the gain value does not need to be recalculated at each packet and power consumption can be further reduced. In addition, the gain value is required after the frequency and phase acquisition is completed. Therefore, gain value can be computed in multi clock cycles. The divider used in the gain calculator can be changed to the divider which has the small area but the calculation time longer to reduce the area of the gain calculator shown in Fig. 3.1.

The data rate required for the medical signal devices are usually very slow, the DCO can be changed to the low-speed architecture, and the area and power consumption can be further reduced.

Furthermore, in this thesis, the AFE circuit does not integrate to the test chip. If the AFE circuit and the proposed transceiver circuit can be integrated to the single chip. Then the transceiver can operate without an external AFE board and the volume of the integrated system can be small and power can be reduced too.

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