國 立 中 正 大 學

資訊工程研究所碩士論文

可應用於人體通道傳輸之無參考時脈全數位資料與回復電路設計

A Reference-Less All-Digital CDR Circuit for Human Body Channel Communication

研究生： 蔡宜哲

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中華民國 一零五 年 八 月

國立中正大學碩士班研究生

學位考試同意書

本人所指導
資訊工程學系

研究生 蔡宜哲 所提之論文

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指導教授 鍾菁哲 簽章

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國立中正大學碩士學位論文考試審定書

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經本委員會審查，符合 碩 士學位論文標準。

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中華民國 105 年 7 月 5 日

摘要

近年來，穿戴式個人娛樂裝置與個人醫療照護裝置越來越流行。傳統上，許多醫療保健設備，如肌電圖、心電圖與血壓計需要使用實體電線來傳遞生理訊號，在長時間觀察上對病人非常不方便。因此，像人體通道傳輸這種無線傳輸技術可被用來收集這些生理訊號。與有線傳輸不同的地方是，人體通道傳輸使用人體當成傳輸媒介。然而，不同的人體通道會有不同的特性，這些特性也會造成不一樣的影響。在我們建立人體通道模型時，勢必也要將這些因素考慮進去。例如人體天線效應、傳輸距離、功率衰減與訊號頻率等等。

本論文介紹一個寬帶信號傳收器，且根據我們所量測之結果建立人體通道模型。在傳輸端，資料會使用 NRZI 編碼與位填充增加資料的變化，且使用封包式傳輸。在接收端，我們所介紹的相位與頻率偵測器與相位補償方法能夠增加頻率與相位的追蹤能力，且我們所提出之全數位資料與回復電路控制器能夠快速對相位誤差進行補償。我們所介紹的自動校正相位追蹤量方法能夠計算出補償碼並提供給全數位資料與回復電路控制器。在不同的製程、電壓、溫度變異下，補償碼也會自動調整。此外，此接收端之全數位資料與回復電路不需要參考時脈或多相位時脈產生器。因此能夠降低硬體設計之複雜度與硬體成本。

關鍵字：人體通道傳輸、資料回復、傳收器

Abstract

Nowadays, the wearable personal entertainments and personal healthcare devices become more and more popular. Traditionally, the medical healthcare devices such as electromyography (EMG), electrocardiography (ECG), and sphygmomanometers require wireline connections to transfer the physiological signals, it is very inconvenient for the patients in long time monitor. Therefore, wireless communication techniques, such as body channel communication (BCC), are used to gather the physiological signals. Different from the wireline transmission, the BCC transmits signals using the human body. However, different human body channel characteristics may have different effect. Therefore, there are some conditions must be considered in building up the human body channel model. For example, the body antenna effect, transmission distance, power attenuation, and signal frequencies are also need to be considered.

In this thesis, a wideband signaling (WBS) transceiver is proposed. The human body channel model is built up according to our measurement result. In transmitter part, the data are modulated by the NRZI encoder and the bit stuffer to increase the data transitions. Furthermore, the data is transmitted in a packet format. In receiver part, the proposed phase and frequency detector (PFD) and the phase compensation approach can enhance the frequency and phase tracking ability. The ADCDR controller can quickly compensate for the phase error. The automatically phase track gain calibration method is proposed to calculate the gain value for the ADCDR controller. In different PVT variations, the gain value will be automatically calibrated. Therefore, in the receiver part, the ADCDR circuit does not require a reference clock, or a multi-phase clock generator. As a result, the design complexity and hardware cost

can be further reduced.

Keywords：BCC、HBC、CDR

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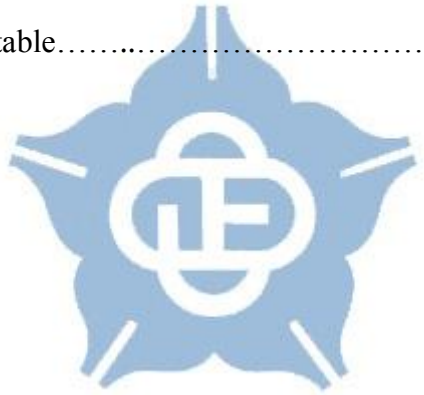


Chapter 1

Introduction

1.1 Introduction to Body Area Network

Nowadays, the wearable personal entertainments and personal healthcare devices become more and more popular. Traditionally, the medical healthcare devices such as electromyography (EMG), electrocardiography (ECG), and sphygmomanometers require wireline connections to transfer the physiological signals, it is very inconvenient for the patients. Therefore, wireless communication techniques are used to gather the physiological signals. Body area network (BAN) is a type of communication for wearable devices. The BAN is organized by IEEE 802.15 Task Group 6 (TG6) [1] to standardize the industrial scientific medical (ISM) bands and the protocols of multimedia communication around the human body.

Body area network can provide connectivity between each wearable device, which is distributed on the human body. In addition, these devices with BAN should be satisfied with low volume, low weight, and low power consumption. There are two main approaches to realize the BAN. The first approach requires external medium such as the air and a wire to transmit the data. The second approach uses the human body skin as the transmission medium.

The first approach generally knows as radio frequency transmission (RF) [2] [3], near field communication [5], and electromagnetic wave transmission. The RF wireless techniques are well developed. For example, Bluetooth and ZigBee transmit data in 2.4GHz ISM band. The typical RF transceiver is shown in Fig. 1.1. The RF transceiver is composed of an antenna, a TX/RX switch, a low noise amplifier (LNA),

a variable gain amplifier (VGA), a band pass filter (BPF), an analog to digital converter, a pulse generator, and a power amplifier (PA). The RF transceiver can both transmit and receive signals in a short range. In addition, it provides good performance in data rate. However, the RF wireless technique still exist some problems such as relatively high power consumption. Moreover, there may have interferences if someone also uses the 2.4GHz frequency band. Furthermore, the RF transceiver using 2.4GHz band is not suitable for BAN because of the large path loss affected by the body shadowing effect [6]. Thus, the second approach was proposed to solve these problems.

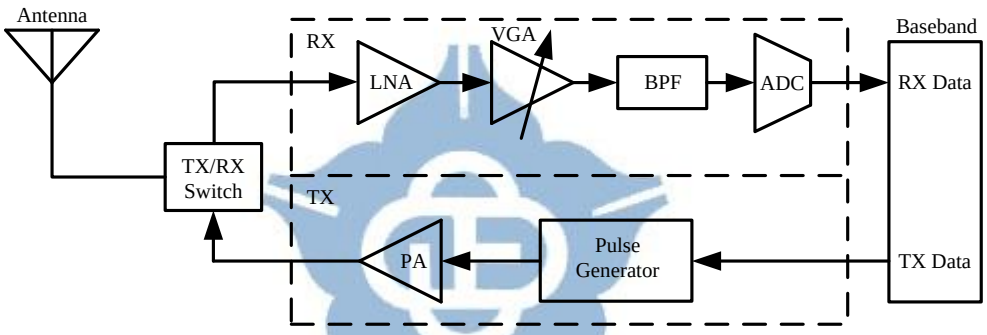


Fig. 1.1 Typical RF transceiver

The second approach generally known as body channel communication (BCC) which was first introduced in [4]. It is different from the wireline transmission. The wireline transmission uses metal lines to transmit signals but the BCC transmits signals using the human body. The concept of body channel communication is shown in Fig. 1.2. The BCC is composed of the transmitter electrode (TX), the receiver electrode (RX), the human body channel, and the return path. The physiological signals are transmitted through the human body channel from TX to RX. Then, the RX sends these physiological signals to the nearby devices and analyze immediately. Using the BCC has some advantages. First, the body channel communication transmitting data using the human body which has higher conductivity than the air.

Thus, the human body channel has lower path loss in comparison to the wireless transmission through the air. Second, the BCC does not require the external antenna because the data are transmitted into the human body so that the power consumption may be reduced as compared to the RF transceiver [7].

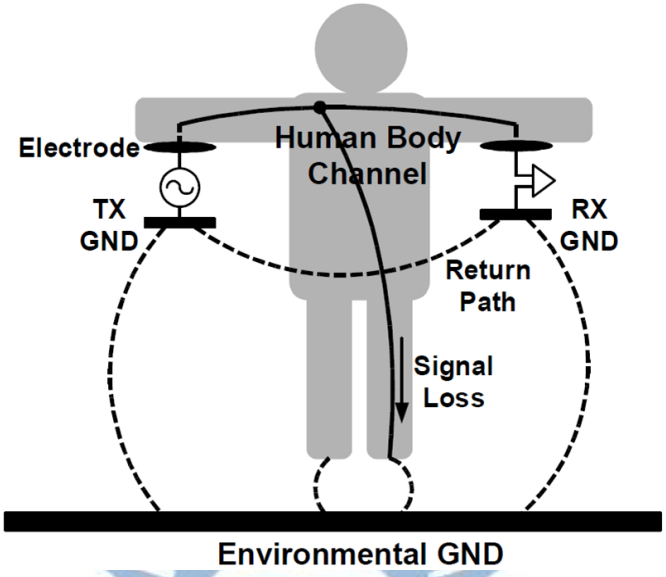


Fig. 1.2: The concept of body channel communication [6]

The BCC technique has lower path loss and more stable as compared to wireless transmission. In addition, the BCC may not be interfered by different body motions [20]. Another body channel communication application is shown in Fig. 1.3. The human can simply open or lock a door, or walk through the ticket gate without taking out the key or the smartcard.

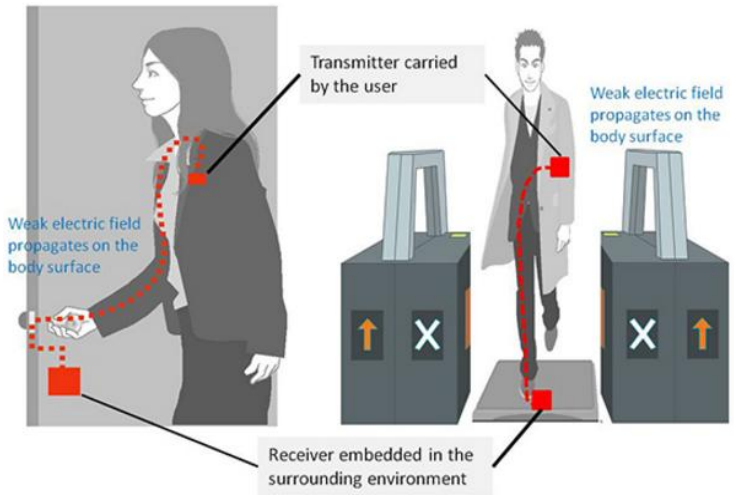


Fig. 1.3: Body channel communication applications [8]

1.2 Characteristics of Human Body Channel

Before using the human body as the transmission medium, it is necessary to know the characteristics of the human body channel. Many researches had analyze the characteristics of human body channel, such as [7], [9-10], [12], [17]. These researches show that the characteristics of the human body channel are related to the frequency and the transmission distance. Moreover, they also show that the human body channel can be simulated by a distributed RC model. Fig. 1.4 shows the distributed RC model of the human body channel [7]. In this RC model, the values of R and C are calculated from the electrical properties within 10-60MHz. If we want to analyze the properties in different transmission distance, we can cascade the N-stage unit blocks as the N×10 cm distance since each unit block is tread as 10-cm length of the human body. Besides, the capacitive coupling between TX GND and RX GND makes the return path.

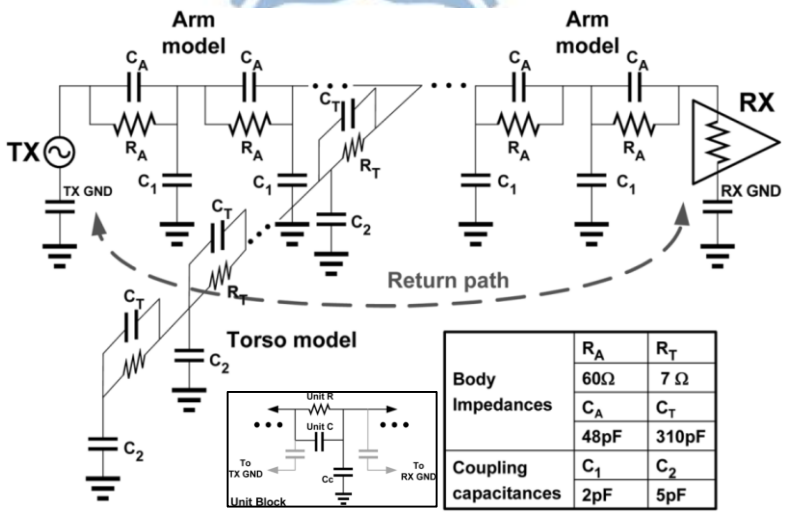


Fig. 1.4: The distributed RC model of the human body channel [7]

In order to understand the characteristics of human body channel better, we need

to investigate the time-domain and frequency-domain characteristic of the human body by transmitting signal through the human body [7], [11], [13]. In [7], a 2MHz, 10ns transition time and 3.5V peak-to-peak amplitude square wave is transmitted through the human body to analyze the time-domain characteristic of the human body, as shown in Fig. 1.5. After passing through the human body, the original square signal will turn into analog pulse. The increased transmitting distance may cause the wider pulse width and the lower peak value of the pulse. Thus, according to this measurement, we can find that the time-domain characteristic of the human body relate to different transmission distance.

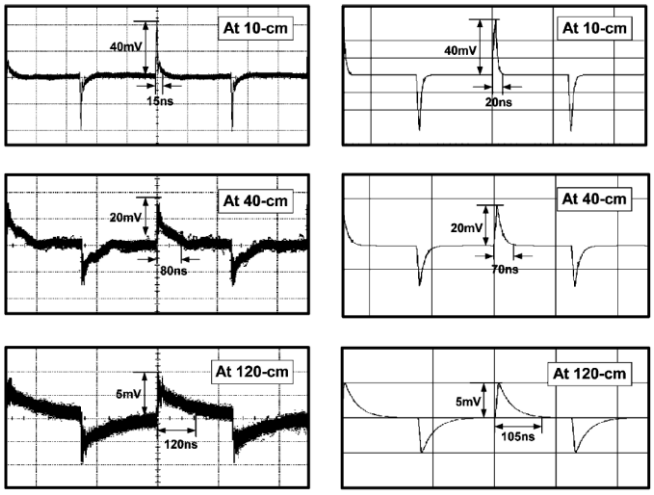


Fig. 1.5: The time-domain characteristics of the human body [7]

(a) Measured (b) Simulated

The frequency-domain characteristic of the human body is shown in Fig. 1.6 [7]. It measures that in different transmission distance and frequency range, the signal power attenuated by the human body channel. The measured results show that in different transmission distance, the power attenuation is very close at the frequencies lower than 4MHz. That is because the impedance of the human body is exceedingly small as compared to the impedance of the capacitive return path. Once the

frequencies are higher than 10MHz, the transmission distance has a great impact on power attenuation. The reason is that in long transmitting distance, the large capacitive coupling effect between the human body and the external ground causes the signal loss. Finally, in this measurement, we can learn that the frequency-domain characteristic of the human body depend on the signal frequency and the transmit distance.

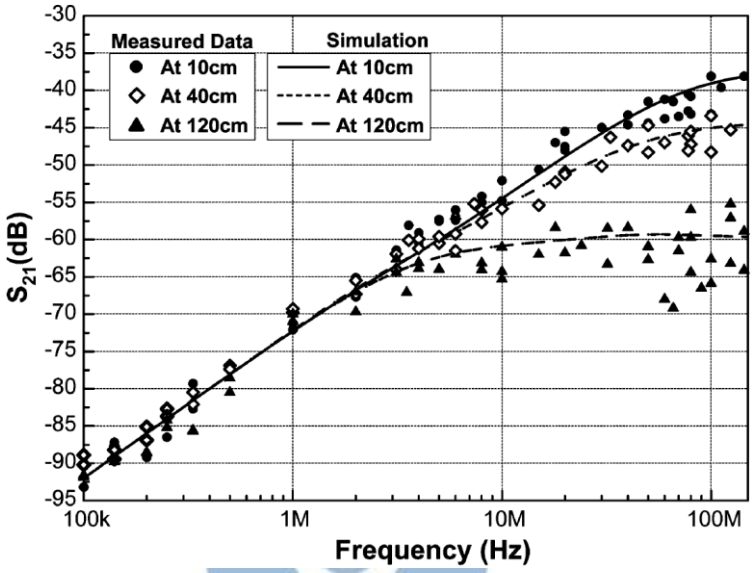


Fig. 1.6: The frequency-domain characteristics of the human body [7]

In order to achieve high data rate, it is necessary to transmit data using high frequencies. Nevertheless, the high frequencies cause electric field change rapidly and then generate the electromagnetic radiation around the human body. If there have some nearby electronic devices, it may be influenced by the electromagnetic radiation, generally known as electromagnetic interference (EMI). In [7], the electric field around the human body with a BCC transmitter has been measured. The distance from the transmitter to the measured location is 3m and the transmitter signal power is maintained at 3dBm. The measured result is shown in Fig. 1.7. It shows that the electric field strength becomes larger with the increased transmission frequency.

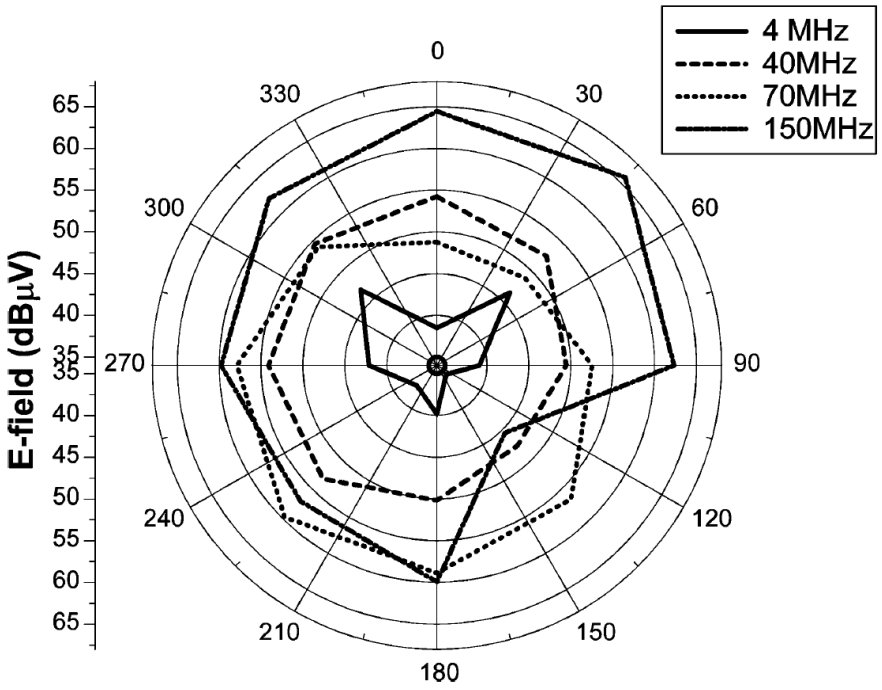


Fig. 1.7: Electric field measurement around the human body [7]

In order to realize the human body channel transceiver, we measure the characteristics of the human body by ourselves. Fig. 1.8 shows the time-domain characteristics at different frequencies in 10 cm transmission distance. The transmitting signal is a 1.0 Vpp square waveform generated by the signal generator. The measured results show that the received signal has the lower peak value at higher frequencies and looks like a triangle waveform. Thus, the received signal required an analog frond-end (AFE) circuit to amplify and recovery the signal. The AFE circuit is composed of a VGA and a schmitt trigger, the received signal must be amplified by the VGA, and then recovered back to digital waveforms by the Schmitt trigger, as shown in Fig. 1.9.

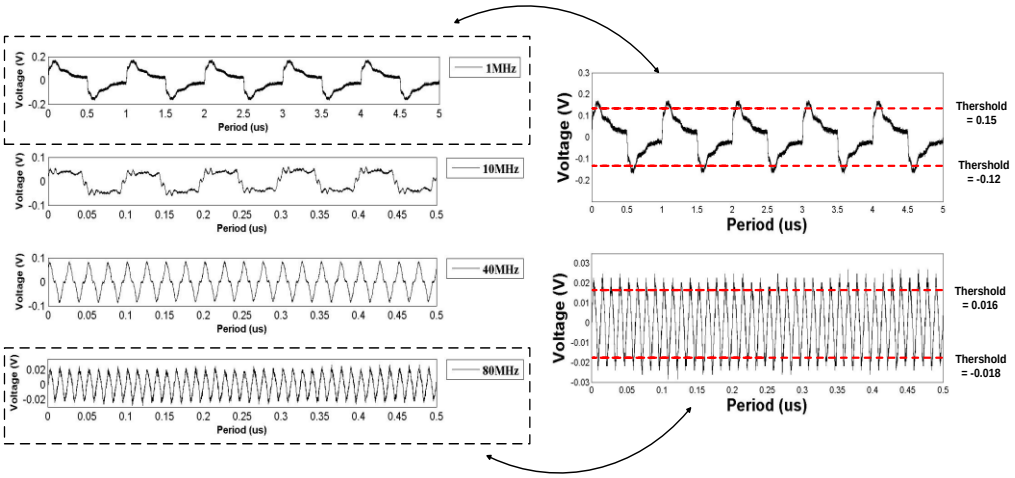


Fig. 1.8: The time-domain characteristics at different frequencies in 10 cm [36]

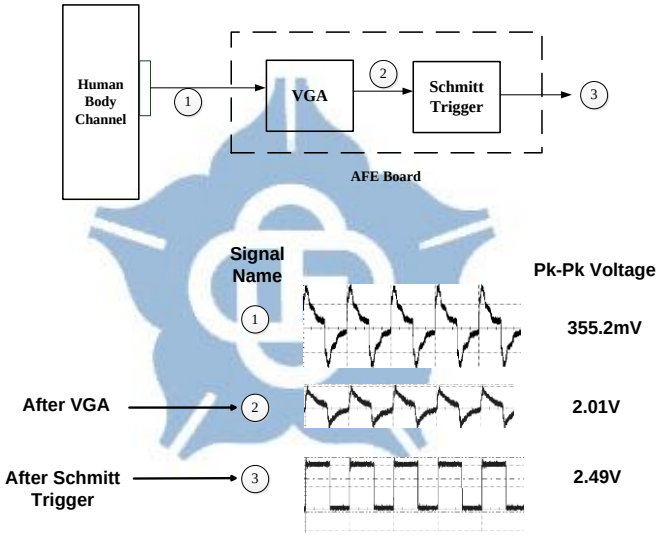


Fig. 1.9: The block diagram and the recovery operation of the AFE circuit [36]

Fig. 1.10 shows the frequency-domain characteristics of six different individuals in 10 cm transmission distance. The transmis signal is 1.0 Vpp generated by the signal generator. Human #1 is 158 cm in height and 51 kg in weight; Human #2 is 173 cm in height and 64 kg in weight; Human #3 is 176 cm in height and 90 kg in weight; Human #4 is 172 cm in height and 75 kg in weight; Human #5 is 180 cm in height and 70 kg in weight; Human #6 is 167 cm in height and 60 kg in weight. According to the measured result, we can know that in Human #3 and Human #6, there is a

maximum difference of signal power about 6dBm at 30MHz. Also, these six different individuals have similar tendency.

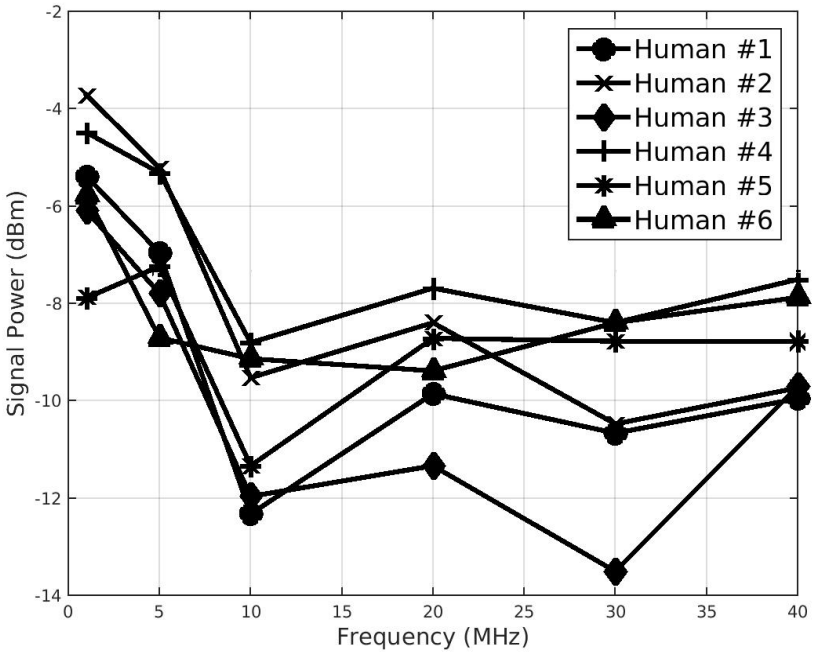


Fig. 1.10: Frequency-domain characteristic with different individuals in 10 cm

Fig. 1.11 shows the frequency-domain characteristic of six different individuals from left wrist to right wrist. We can figure out that in Human #3 and Human #6, there is a maximum difference of signal power about 6dBm at 30MHz. Also, these six different individuals have similar tendency.

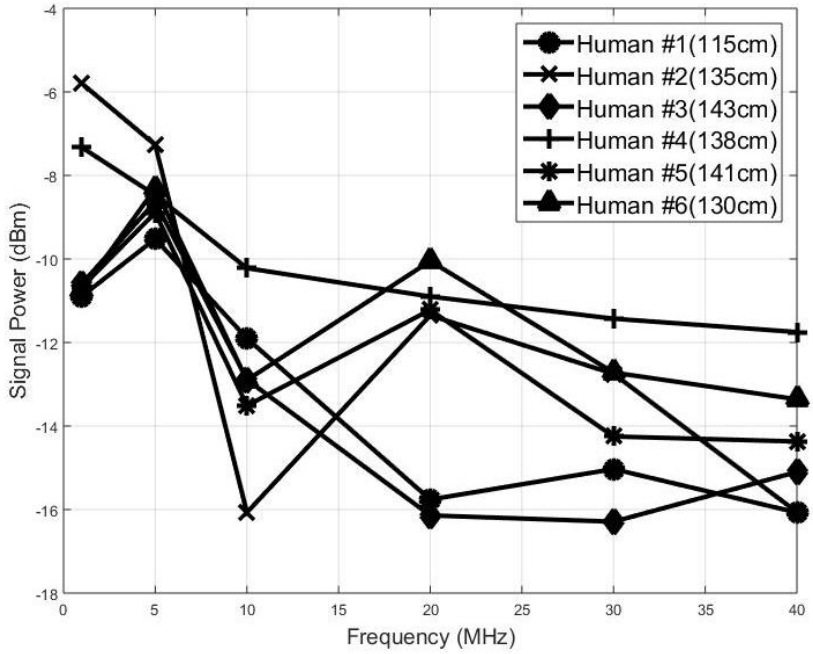


Fig. 1.11: Frequency-domain characteristic with different individuals from left wrist to right wrist

In time domain measurement, a clock signal is transmitted to the human body, and then recovered by the AFE circuit. We measure the jitter effect of the signal which recovered by the AFE circuit in various frequencies and distances. Table 1.1 shows the summary of the jitter measurement results [26]. The result shows that in different frequencies and distances, the magnitude of the jitter effect is also different. The peak-to-peak jitter is specified in Unit Intervals (UI), such that one UI of jitter is equal to the symbol time, irrespective of the data rate.

Table 1.1: Summary of the jitter measurement results [26]

Distance	**Frequency**	**Input Voltage**	**Period**	**Period Jitter Peak-to-Peak**	**Period Jitter RMS**	**Cycle-to-Cycle Jitter RMS**
10 cm	1 MHz	1.0 Vpp	999.99 ns	3.9 ns (3.9% UI)	471.7 ps (0.05% UI)	849.92 ps (0.08% UI)
	10 MHz		99.99 ns	3.65 ns (3.65% UI)	271.3 ps (0.27% UI)	465.09 ps (0.47% UI)
	20 MHz		49.99 ns	3.05 ns (6.01% UI)	314.4 ps (0.63% UI)	485.63 ps (0.97% UI)
	30 MHz		33.33 ns	1.5 ns (4.50% UI)	160.1 ps (0.48% UI)	295.92 ps (0.89% UI)
	40 MHz		25.01 ns	2.6 ns (10.39% UI)	155.6 ps (0.62% UI)	845.55 ps (3.38% UI)
140 cm	1 MHz		999.88 ns	43.5 ns (4.35% UI)	3.5 ns (0.35% UI)	5.63 ns (0.56% UI)
	10 MHz		99.96 ns	10 ns (10% UI)	1.1 ns (1.1% UI)	1.78 ns (1.78% UI)
	20 MHz		49.99 ns	3.4 ns (6.8% UI)	253.6 ps (0.5% UI)	467.95 ps (0.94% UI)
	30 MHz		33.35 ns	1.72 ns (5.15% UI)	219 ps (0.66% UI)	2.13 ns (6.39% UI)
	40 MHz		25.42 ns	7.1 ns (27.93% UI)	643 ps (2.53% UI)	4.33 ns (17% UI)

1.3 Prior Body Channel Communication Transceiver

1.3.1 Basic Components of a BCC Transceiver

Fig. 1.12 shows the block diagram of the BCC transmitter. The transmitter is composed of an encoder, a modulator, a driver, and a transmitter (TX) electrode. At first, the transmit data are encoded by the encoder. After that, the encoded data are modulated by the modulator. Finally, the modulated data are transmitted to the human body channel through the driver and the TX electrode.

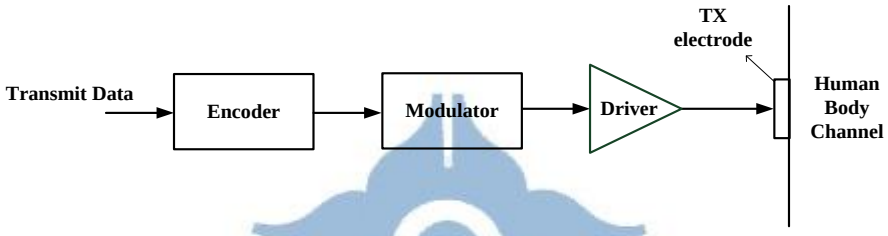


Fig. 1.12: Block diagram of BCC transmitter

Fig. 1.13 shows the block diagram of BCC receiver. The receiver is composed of a receiver (RX) electrode, an amplifier, a clock and data recovery (CDR) circuit, a demodulator, and a decoder. When the RX electrode receives the signal from the human body channel, the received signal is firstly amplified by the amplifier. Next, the CDR circuit extracts the clock and retimed the incoming data. After that, the demodulator and decoder can recover the retimed data to the original data.

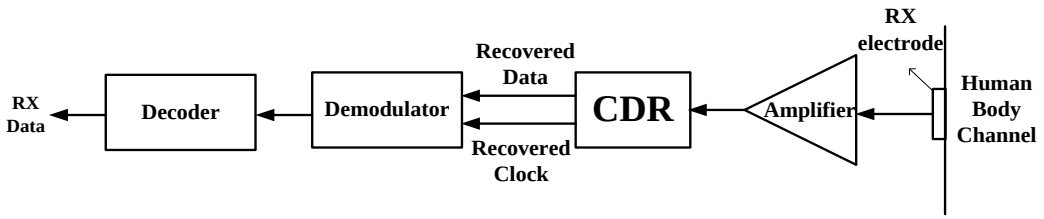


Fig. 1.13: Block diagram of BCC receiver

1.3.2 Modulation Scheme: Frequency/Amplitude -Shift Keying

The frequency-shift keying (FSK) is a modulation scheme of transmitting digital signals. The digital signal is transmitted through two different frequencies to represent two binary values. Recently, many body channel communication transceivers based on FSK modulation have been proposed, such as [14], [17].

Fig 1.14 shows the transceiver architecture of double-FSK modulation [14]. In the transmitter, the frequency synthesizer is phase-locked to the calibrated DCO frequency. Besides, the TX data is modulated by the double-FSK modulator. In the receiver, the received signals are amplified by the LNA amplifier. Then the received signals are converted to the sub-band signals by the wide-band FSK demodulator. After that, the low frequency direct conversion receiver with sub-band FSK demodulator coverts the sub-band signal into RX data. As for calibration, the injection-locking digitally controlled oscillator (IL-DCO) and injection-locking detector (IL-detector) are adopted.

Fig 1.15 shows the double-FSK modulation with frequency bands in [14]. The data would be modulated with a low modulation index (500 kHz-2.5 MHz) by the sub-band FSK modulator. Then, it is converted to a high-modulation-index (40-120 MHz) wideband signal by the wideband FSK modulator. The spreading gain between modulation indexes (80MHz / 2MHz) is 16dB. In low data rate, it provides several channels and has a high spreading gain. Multiple users can share the same wideband signal, but distinguish themselves according to different subcarrier frequencies in the sub-band. However, there is a high power consumption in the receiver (2.4mW). Moreover, the transceiver has a large chip area with only 10Mb/s data rate.

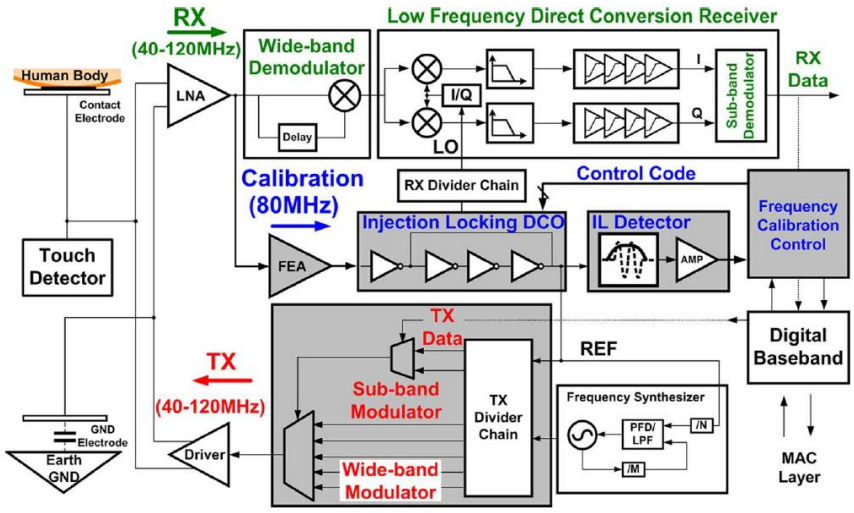
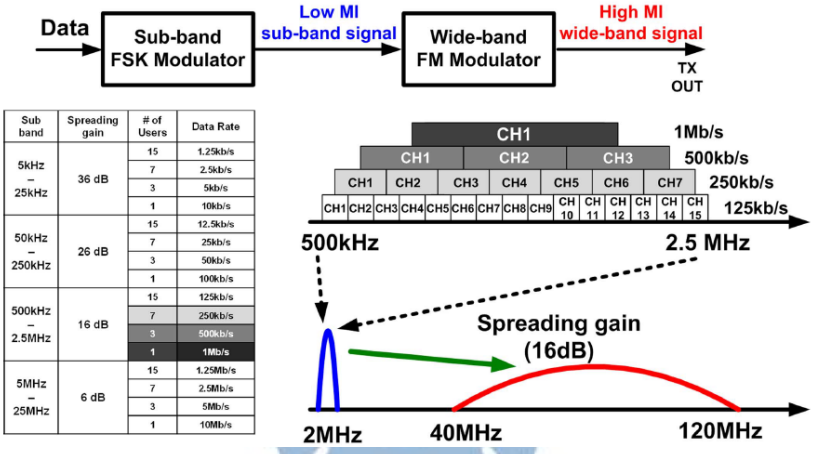


Fig. 1.14: Transceiver architecture of double-FSK modulation [14]



Sub band	Spreading gain	# of Users	Data Rate
5kHz – 25kHz	36 dB	15	1.25kb/s
		7	2.5kb/s
		3	5kb/s
		1	10kb/s
50kHz – 250kHz	26 dB	15	12.5kb/s
		7	25kb/s
		3	50kb/s
		1	100kb/s
500kHz – 2.5MHz	16 dB	15	125kb/s
		7	250kb/s
		3	500kb/s
		1	1Mb/s
5MHz – 25MHz	6 dB	15	1.25Mb/s
		7	2.5Mb/s
		3	5Mb/s
		1	10Mb/s

Fig. 1.15: Double-FSK modulation with frequency bands [14]

A full-duplex body channel communication transceiver for both healthcare and entertainment application is proposed in [16]. It uses the 13.56 MHz ISM band for healthcare mode (HC-mode). Also, it uses two channels of 40 MHz, one centered at 40 MHz and the other at 160 MHz to realize the high speed communication for entertainment mode (ET-mode). Fig. 1.16 shows the frequency plan in [16].

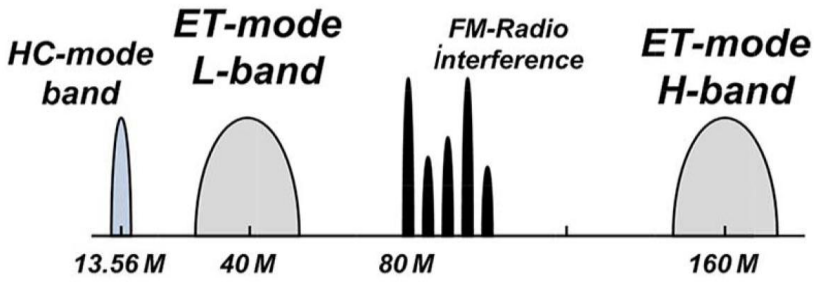


Fig. 1.16: Frequency plan [16]

Fig.1.17 shows the transceiver architecture in [16]. In HC-mode, the transmitter provides 100 kb/s data rate based on on-off keying (OOK) modulation. The super-regenerative receiver configuration with a RC oscillator is adopted to realize the receiver in order to achieve high quality factor and low power consumption. In ET-mode, it provides full-duplex communication and achieves 80 Mb/s data rate with coherent binary phase-shift keying (BPSK) modulation. Both of 40 MHz band (L-band) and 160 MHz band (H-band) are combined in order to maximize the data rate and avoid the FM-radio interference. However, the L-band and H-band are cost too much chip area.

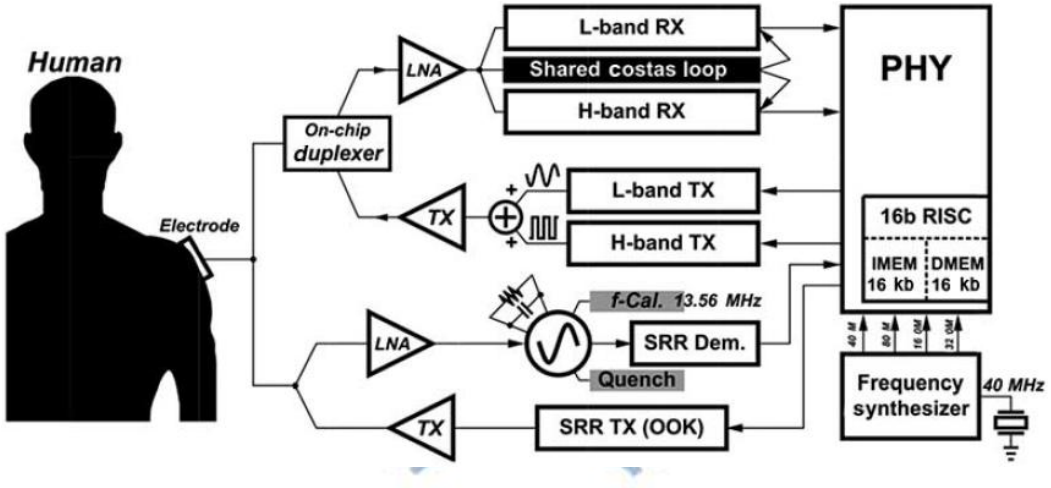


Fig. 1.17: Transceiver architecture [16]

1.3.3 Modulation Scheme: OFDM

Orthogonal frequency-division multiplexing (OFDM) is a modulation scheme that modulates the digital data on multiple carrier frequencies. The technology is used for wideband digital communication. In [18], an OFDM-based BCC transceiver is proposed in order to use the BCC technique for multimedia transmission. Fig. 1.18 shows the OFDM baseband transceiver. It uses the OFDM modulation to enhance data rate. The (2, 1, 6) convolutional encoder is adopted to remain the transmission reliability. Also, the Viterbi decoder is used to enhance the bit-error-rate (BER). Most modules in the transceiver work in 0.5V environment, and the uneven multi-level LINC technique, voltage scaling and clock-gating technique are adopted to reduce the power consumption. Although the OFDM-based transceiver can enhance the data rate, there is also a high power consumption and occupies large chip area.

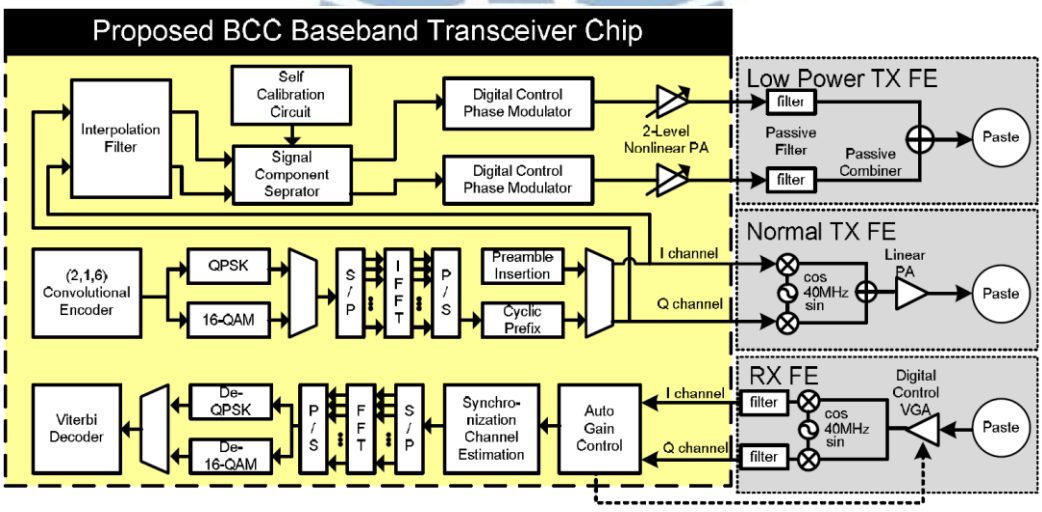


Fig. 1.18: OFDM baseband transceiver [18]

1.3.4 Modulation Scheme: Frequency Selective Digital Transmission

Another modulation scheme is called frequency selective digital transmission [13], [15]. Fig. 1.19 shows the transceiver architecture of FSDT modulation. The serial-to-parallel (S2P) circuit transfers the serial data to a 4-bit symbol. Then, the 4-bit symbol is converted to the index of the 16 codes out of 64 Walsh codes. By using the Walsh codes, the data is spread into different frequency. Then it increases the resistance to interferences and provides a high quality communication. The FSDT-based transceiver has the low sensitivity (-74 dBm) and wide dynamic range (82dB). However, the maximum data rate in [15] is only 2Mb/s, and the power consumption is quiet high (194.7mW).

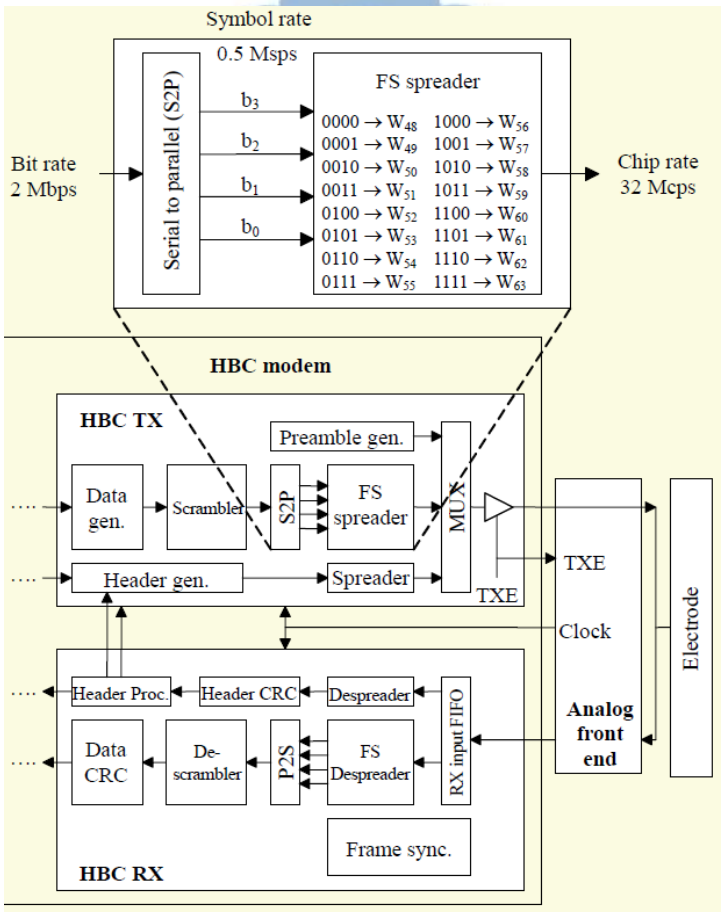


Fig. 1.19: Transceiver architecture of FSDT modulation [15]

1.3.5 Modulation Scheme: Wide-Band Signaling

A body channel communication transceiver with wideband signaling (WBS) is presented in [19]. Fig. 1.20 shows the WBS transceiver and the CDR circuit. The data are converted into the non-return to zero inverted (NRZI) data and transmitted directly to human body. Then the oversampling-based receiver circuit recovers the data to the original data. This wideband signaling transceiver supports 40Mb/s data rate. In addition, the energy per bit is 0.0485 nJ/b. However, the DCO in CDR circuit always generate 280MHz frequency for the sampler. If there is a large frequency drift, it may cause the lower BER.

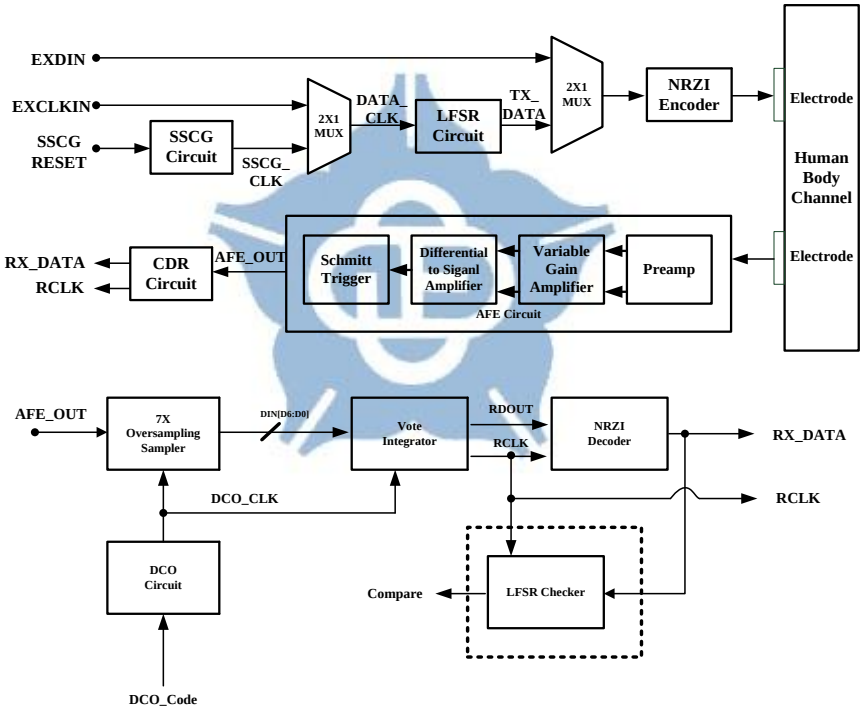


Fig. 1.20: The WBS transceiver and the CDR circuit [19]

1.4 CDR Circuit for NRZI Encoding

Non-return-to-zero-inversed (NRZI) is a method that used to map the binary signal to physical signal for transmission. The two level NRZI signal has a transition if the binary signal is logical 1, and does not have transition if the binary signal is logical 0. Because the NRZI data will be attenuated after passing through the human body, therefore, they require an AFE circuit and a CDR circuit to recovery the data.

1.4.1 Phase Interpolator Based CDR circuit

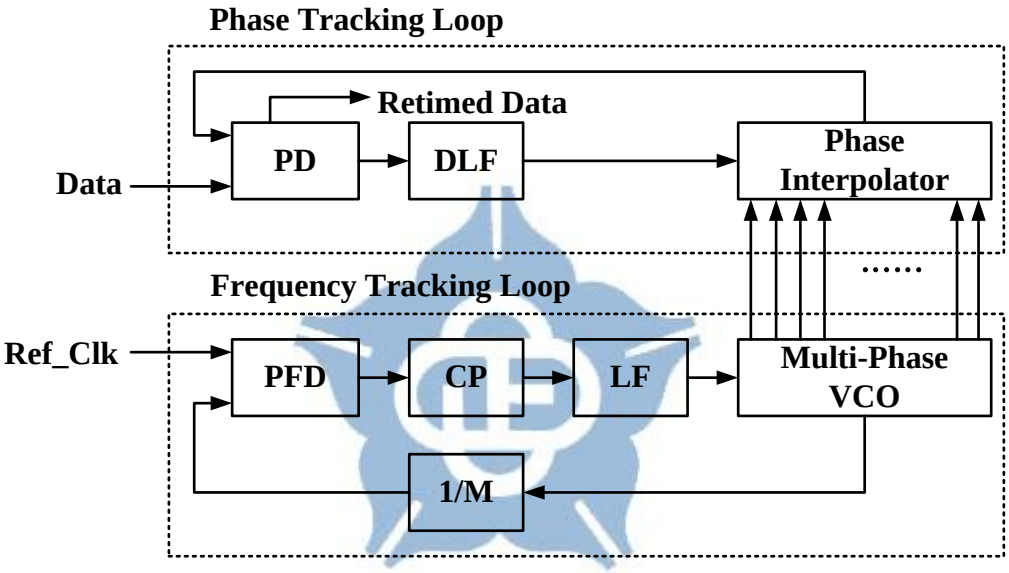


Fig. 1.21: Architecture of phase interpolator based CDR

Fig. 1.21 shows the architecture of phase interpolator based CDR. It is composed of a frequency tracking loop and a phase tracking loop. In frequency tracking loop, the high speed multi-phase signals are generated by the multi-phase VCO base on reference clock (Ref_Clk). In phase tracking loop, after the data transition phase and clock from the phase interpolator are phase-locked, the retimed data are generated by the PD. The phase interpolator base CDR is usually used in high speed applications [20], [21]. However, the phase interpolator based CDR requires a reference clock to generate the high speed multi-phase signals.

1.4.2 PLL-Based CDR circuit

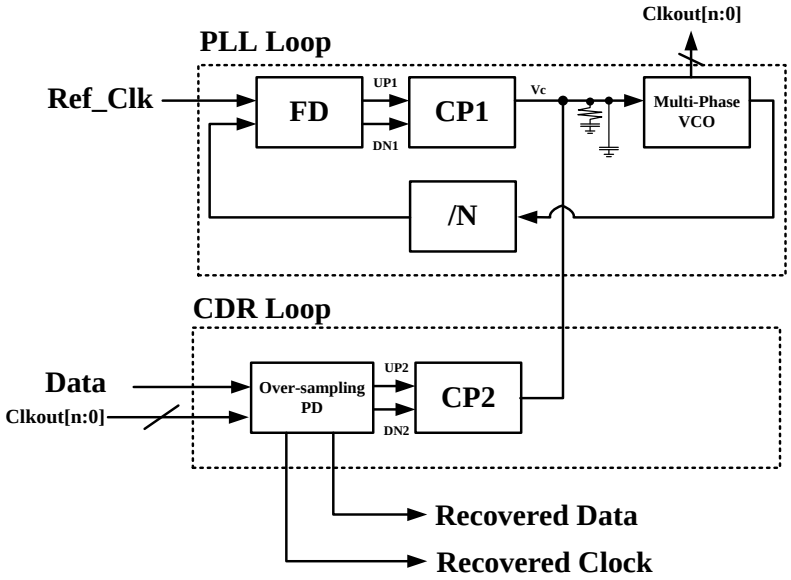


Fig. 1.22: Architecture of the PLL-based CDR

The architecture of PLL-based CDR is shown Fig. 1.22. It is proposed in [24], [25]. The PLL-based CDR consists of two loops. In PLL loop, the PLL uses the external reference clock to generate the multi-phase clocks. In CDR loop, the over-sampling PD uses the multi-phase clock to perform the clock and data recovery. In this architecture, the power consumption of the multi-phase VCO is decreased because the VCO clock rate could be half or quarter of the data rate. However, it also requires an external reference clock to generate multi-phase clocks. Moreover, the multi-phase clock generator and the over-sampling circuit may cause the higher design complexity.

1.4.3 Blind Oversampling CDR circuit

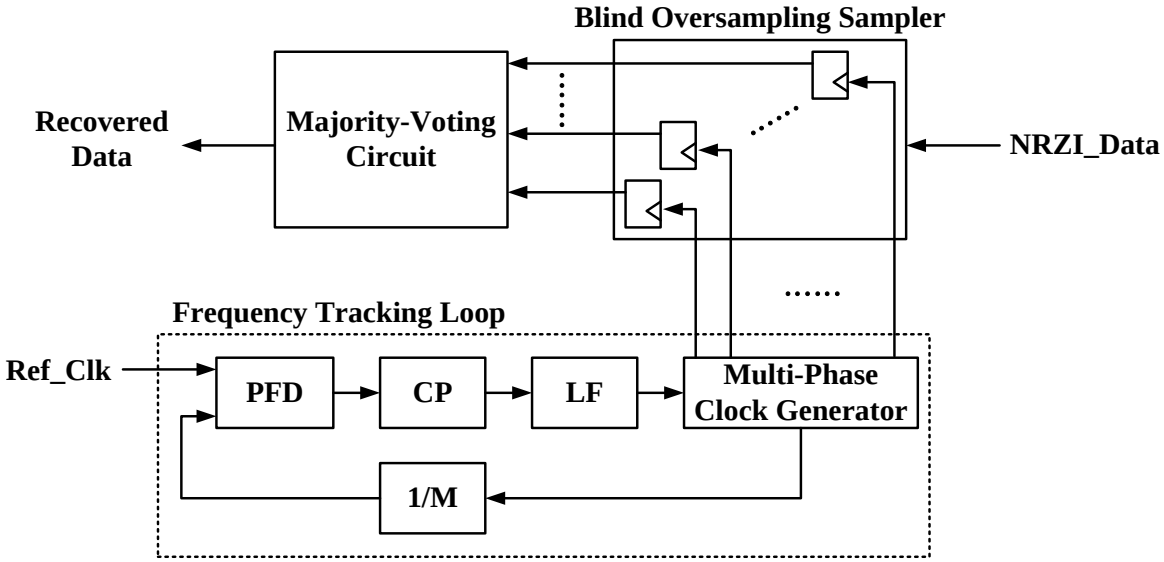


Fig. 1.23: Architecture of the blind oversampling CDR

The architecture of the blind oversampling CDR [26] is shown in Fig. 1.23. The frequency tracking loop requires a reference clock to generate the multi-phase clocks. The blind oversampling sampler samples the data by using the multi-phase clocks, and then the majority-voting circuit will decide the right value of the data. The blind oversampling architecture has large jitter tolerance. However, the high oversampling rate may cause the high power consumption. In addition, it has no feedback loop, if there is a large frequency drift, it may increase the BER.

1.5 Motivation

The wearable electronic devices and personal healthcare devices are popular now. We want to realize a human body channel transceiver which can support different data rate and different distance for these devices. Traditionally, many devices transmitted data by a wireline. That is very inconvenient. By using the BCC technique, the data are transmitted by the human body. In short distance transmission (< 60 cm), the physiological signals, which are gathered by the healthcare devices, can easily and directly transmitted to other devices. In long distance transmission (about 140 cm), for example, multimedia transmission between two devices, the transmission is easily performed by just touching these two devices.

There are several BCC transceivers we have discussed. They have some advantages and disadvantages. The OFDM-based architecture [18] can easily improve the data rate, however, it also increases the power consumption and the chip area. The FSK-based architecture [14] can share the same wideband signal for maximum 15 users, however, it is complicate and the maximum data rate is only 10Mbps. The FSDT-based architecture in [13], it reaches 60Mb/s without increasing the number of Walsh codes or the clock frequency. However, the power consumption is quiet high, i.e., 10.87mW. The WBS-based architecture [19] has advantages in chip area and power consumption. Moreover, it has low architecture complexity. Therefore, a wideband signaling transceiver is adopted to transmit data for healthcare and multimedia applications.

Chapter 2

Architecture of Wideband Signaling Transceiver

2.1 Architecture Overview

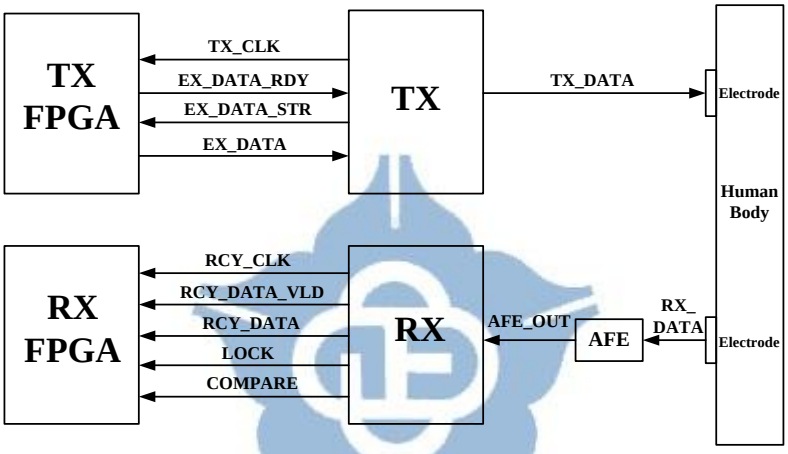


Fig. 2.1: Architecture of the proposed WBS transceiver

Fig. 2.1 shows the architecture of the proposed WBS transceiver. The transceiver consists of two field-programmable gate arrays (FPGAs), a transmitter (TX), a receiver (RX), and an AFE circuit. In transmitter part, the TX_FPGA prepares the data and sends to TX. After that, the data will be sent in a packet format and modulated by the TX. Then, TX transmits the data (TX_DATA) to the human body. In the receiver part, the RX_DATA is firstly amplified and converted to the digital signal by the AFE circuit. Then, the RX will recover the data (AFE_OUT) to the original data (RCY_DATA). Moreover, it also generates the recovery clock (RCY_CLK) and other signals to the RX_FPGA.

2.2 Wideband Signaling Transmitter Architecture

2.2.1 Wideband Signaling Transmitter Overview

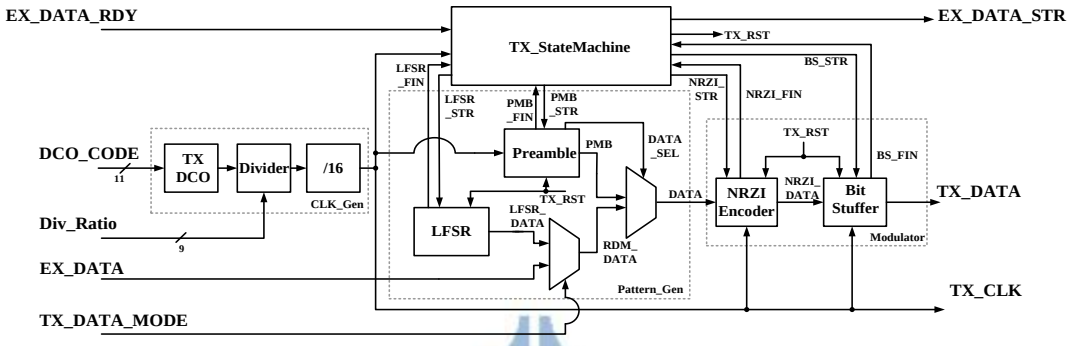


Fig. 2.2: Architecture of the proposed WBS transmitter

Fig. 2.2 shows the architecture of the proposed WBS transmitter. It consists of a clock generator (CLK_Gen), a pattern generator (Pattern_Gen), a modulator, and a TX state machine. Firstly, according to the input signal DCO_CODE, the CLK_Gen can generate the TX_CLK to other circuits. By monitoring the signal TX_CLK, we can know that the frequency of the TX_CLK. Secondly, the Pattern_Gen generates the preamble data (PMB) and random data (RDM_DATA) to the modulator. In addition, the Pattern_Gen supports the random data which is generated by the linear feedback shift register (LFSR) or external inputs (EX_DATA). The EX_DATA_RDY signal and EX_DATA_STR signal are used to communication with external devices. Finally, the modulator generates the TX_DATA by modulating the DATA to NRZI_DATA and performing bit stuffing to limit the maximum continuous identical digits (CID). The TX state machine is used to communicate with the external devices to transmit the data. Moreover, it manages the Pattern_Gen and the Modulator that works in different states by using the signals PMB_STR, LFSR_STR, NRZI_STR, BS_STR. The signals

DCO_CODE and Div_Ratio are fed by the other interface which present in section 2.4.

2.2.2 Clock Generator

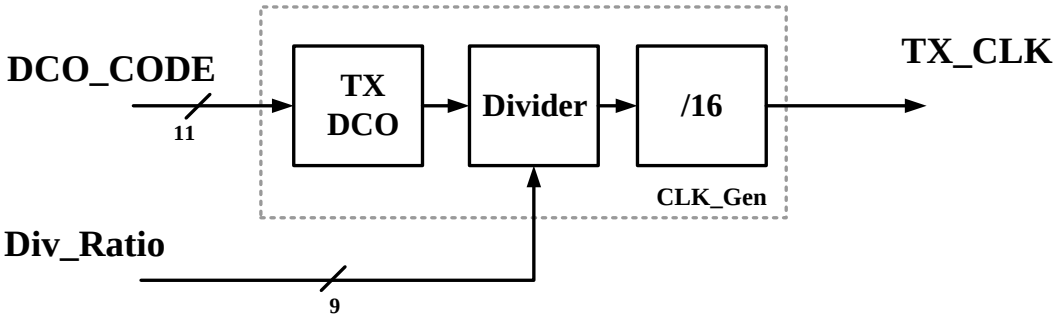


Fig. 2.3: Architecture of the clock generator

In order to generate a clock to trigger the circuits in the transmitter and sends data at specified baud rate, a clock generator is required. Fig. 2.3 shows the architecture of the clock generator. It composed of a TX_DCO, a frequency divider, and a divide-by-16 frequency divider. The DCO_CODE is used to control the output frequency of the TX_DCO. In order to generate different frequencies (1MHz-20MHz), a programmable frequency divider is adopted. We can set the Div_Ratio to generate the target frequency. The architecture of the TX_DCO is the same with the RX_DCO and will be discussed in section 2.3.2.2.

2.2.3 Pattern Generator

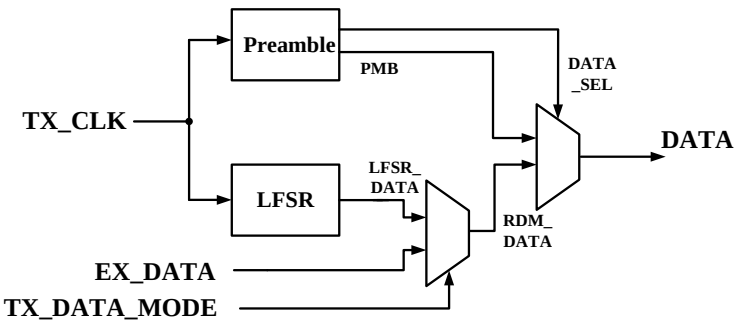


Fig. 2.4: Architecture of the pattern generator

The pattern generator consists of a preamble circuit, a LFSR circuit, and two 2-to-1 multipliers, as shown in Fig. 2.4. The signal DATA_SEL selects the data which are from the preamble circuit or the LFSR circuit. In preamble part, it is used to generate the preamble bits (PMB) for synchronization. In LFSR circuit part, it can generate the random data sequence. Fig. 2.5 shows the architecture of the LFSR circuit. It consists of twenty registers and a XOR gate. The feedback polynomial of the LFSR circuit is shown in Eq. 2.1.

$$1 + x^{19} + x^{20} \tag{2.1}$$

The random sequence with every 2^{20} bits repetition and the longest consecutive identical digits (CID) are 20. The package format is adopted in the transceiver. Fig. 2.6 shows the package format of the WBS transceiver. Eighteen preamble bits are first transmitted to the human body for synchronization, and followed by four bits start frame delimiter (SFD). Consequently, 1000 bits data are transmitted.

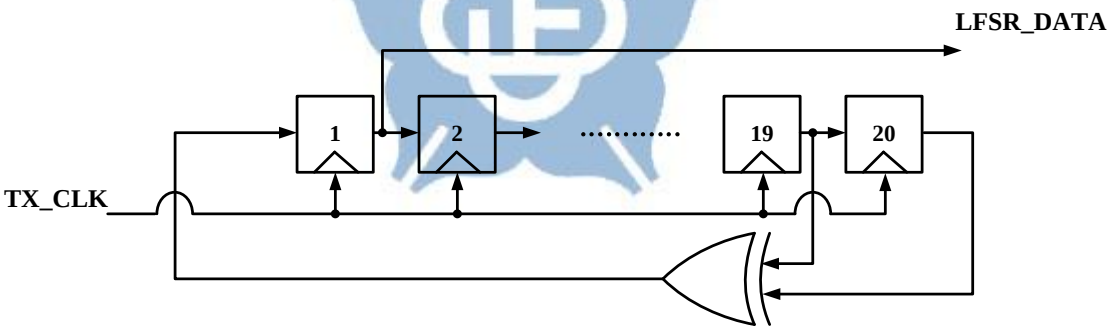


Fig. 2.5: Architecture of the LFSR circuit

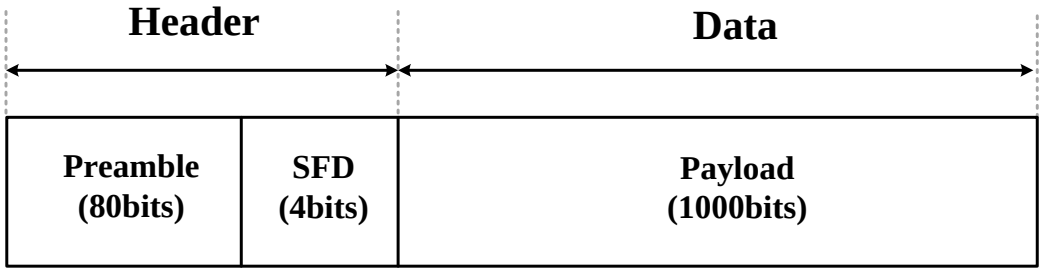


Fig. 2.6: The package format of the WBS transceiver

2.2.4 Modulator

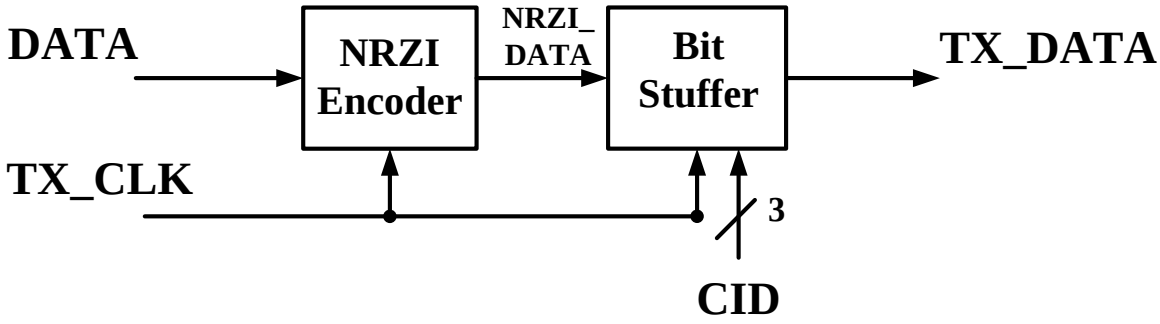


Fig. 2.7: Architecture of the modulator

The data (DATA) from the Pattern_Gen may have long CID. It implies the less data transitions and hard to recover the data due to the jitter accumulation and duty-cycle distortion. Therefore, the modulator is used to increase the data transitions. Fig. 2.7 shows the architecture of the modulator. It consists of a NRZI encoder and a bit stuffer. The NRZI encoder will reverse the previous NRZI_DATA if the DATA is "0". Otherwise, the NRZI encoder will keep the state of the previous NRZI_DATA if the DATA is "1". However, the NRZI_DATA may have long CID, thus, the bit stuffer will check the longest CID of the NRZI_DATA and insert a stuffing bit to make output has one transition. For example, if the longest CID is 3, a stuffing bit is inserted after three continuous "1". Fig, 2.8 shows the waveform of the NRZI encoder and the bit stuffer.

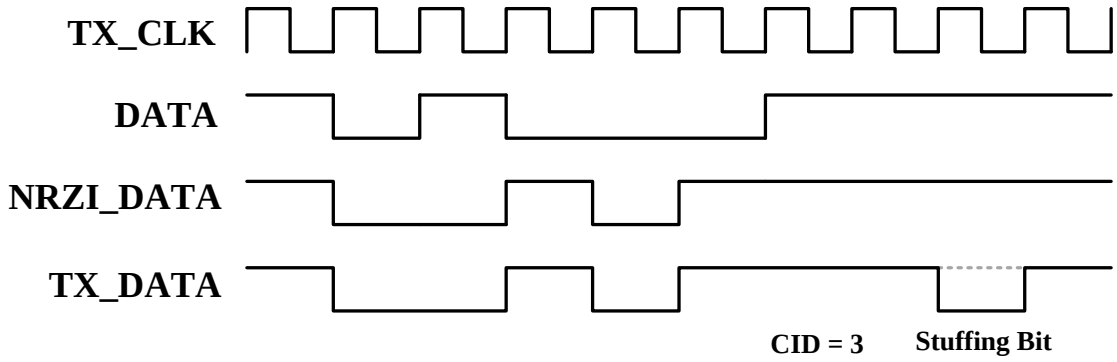


Fig. 2.8: Waveform of the NRZI encoder and the bit stuffer

2.2.5 TX State Machine

The TX state machine controls all the blocks inside the TX. Fig. 2.9 shows all I/O pins of the TX state machine. The TX state machine will start when the signal Setting_FIN is equal to “1”. The signal TX_DATA_MODE is used to select the data which are generated from the LFSR circuit or external devices. The signals EX_DATA_RDY and EX_DATA_STR are used to communicate with the external devices. The PMB_STR, LFSR_STR, NRZI_STR, and BS_STR signals control each block works or not. According to the PMB_FIN, LFSR_FIN, NRZI_FIN, and BS_FIN signals, the TX state machine can easily to change the state (TX_STATE). The signal TX_RST is used to reset the circuits.

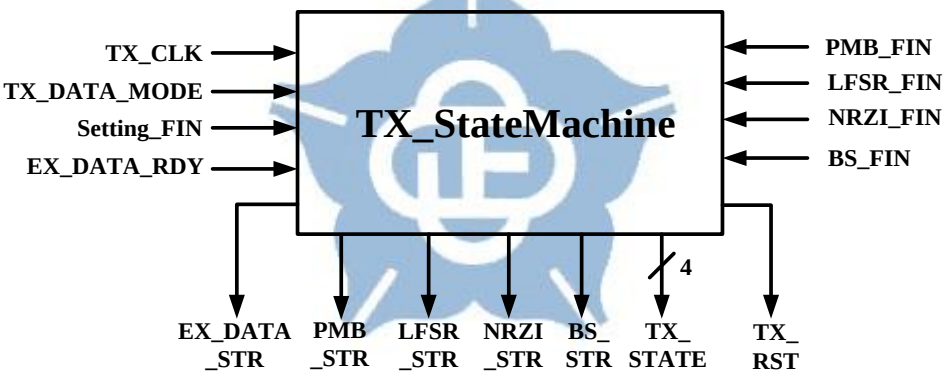


Fig. 2.9: All I/O pins of the TX state machine

Fig. 2.10 shows the flowchart of the TX state machine. After the setting of the circuit finished, the TX state machine will determine which data mode is selected. If the TX_DATA_MODE is “0”, it means that the data are generated by the LFSR circuit. In the beginning, the preamble bits are generated, and once the preamble bits is finished, the LFSR circuit starts to generate the random data. After that, the NRZI encoder and the bit stuffer will modulate the data and check the longest CID length. When the bit stuffing is finished, it means that all of the data are transmitted. The TX will wait for 200 cycles due to the latency between the TX and RX. Finally, the signal

TX_RST is sent to reset the circuits. If the TX_DATA_MODE is “1”, it means that the data are generated by the external inputs. Before generating the preamble bits, the TX state machine firstly wait for the EX_DATA_RDY signal rise to “1”. When the TX state machine detects that the signal EX_DATA_RDY is “1”, the preamble bits start to generate. After the preamble bits are sent, the TX state machine will send a signal EX_DATA_STR to the external device and the external device will now start to transmit the external data. The remaining flows are the same as in previous presentation.

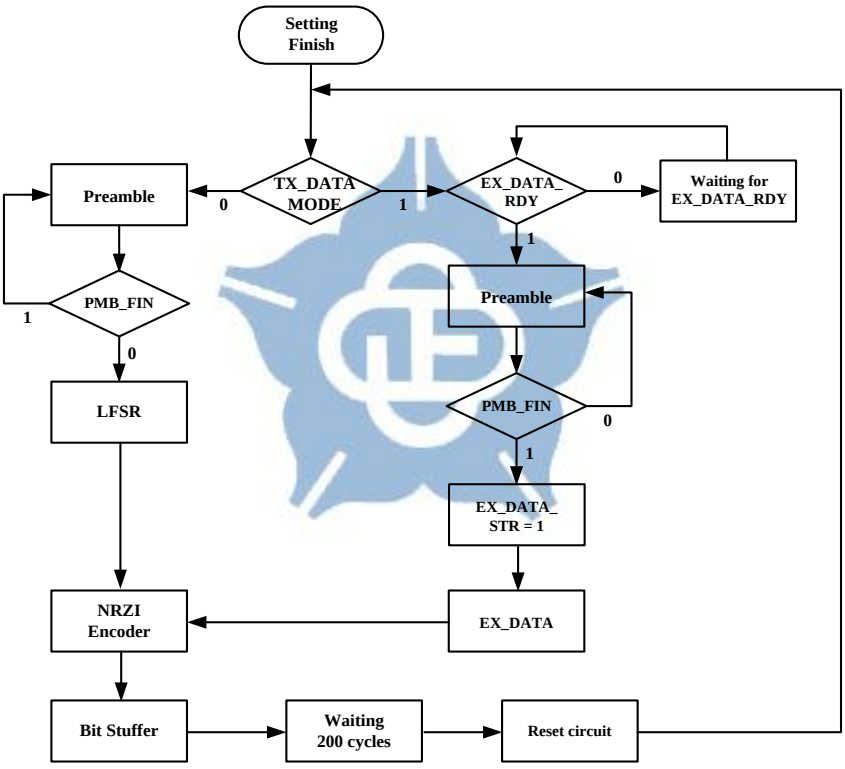


Fig. 2.10: TX flowchart

2.3 Reference-Less Receiver Architecture

2.3.1 Reference-Less Receiver Overview

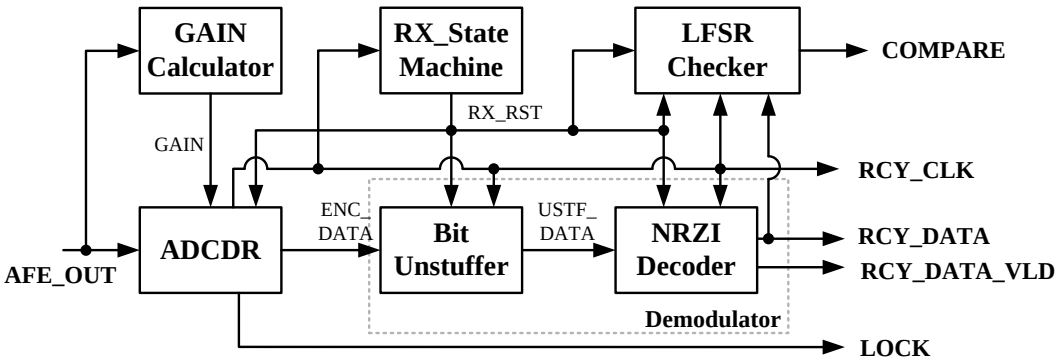


Fig. 2.11: Architecture of the reference-less receiver

Fig. 2.11 shows the architecture of the reference-less receiver. It consists of an all-digital clock and data recovery (ADCDR), a GAIN calculator, a RX state machine, a demodulator, and a LFSR checker. In the beginning, the GAIN calculator will use the AFE_OUT signal to calculate the gain value for the ADCDR controller. Consequently, the signal AFE_OUT will send to the ADCDR to perform the clock and data recovery. After that, the encoding data (ENC_DATA) will be demodulated by the demodulator and generate the recovery data (RCY_DATA). The RX state machine is used to reset the circuit if a packet is recovered. The LFSR checker circuit will generate the random pattern which is exact the same as the LFSR circuit in the TX, and check whether there are bit errors in the recovery data (RCY_DATA).

2.3.1.1 The Proposed Receiver Flow

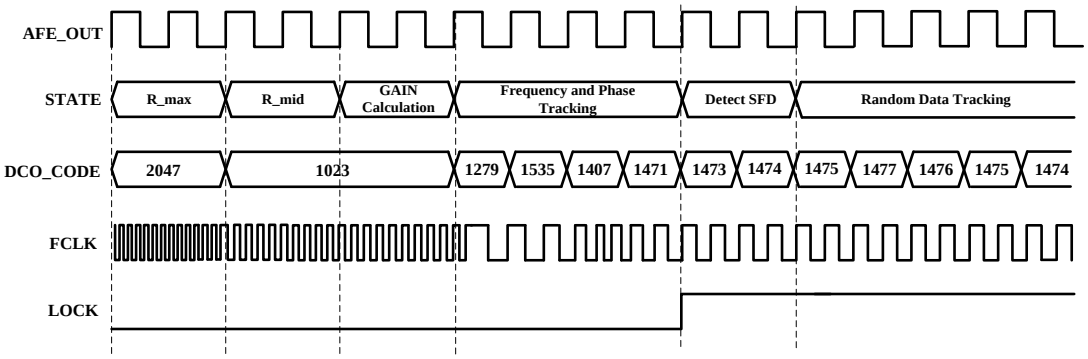


Fig. 2.12: Receiver timing diagram in preamble pattern

Fig. 2.12 shows the receiver timing diagram in preamble pattern. Firstly, the DCO_CODE is set to 2047 to calculate the period ratio between the symbol period and the output of the DCO (R_{max}). After that, the DCO_CODE is set to 1023 to calculate to calculate another period ratio (R_{mid}). Secondly, by using R_{max} and R_{mid}, the GAIN calculator can calculate the gain value for the ADCDR controller. Thirdly, the ADCDR start to operate the frequency and phase tracking. Finally, the ADCDR detects SFD and start random data tracking.

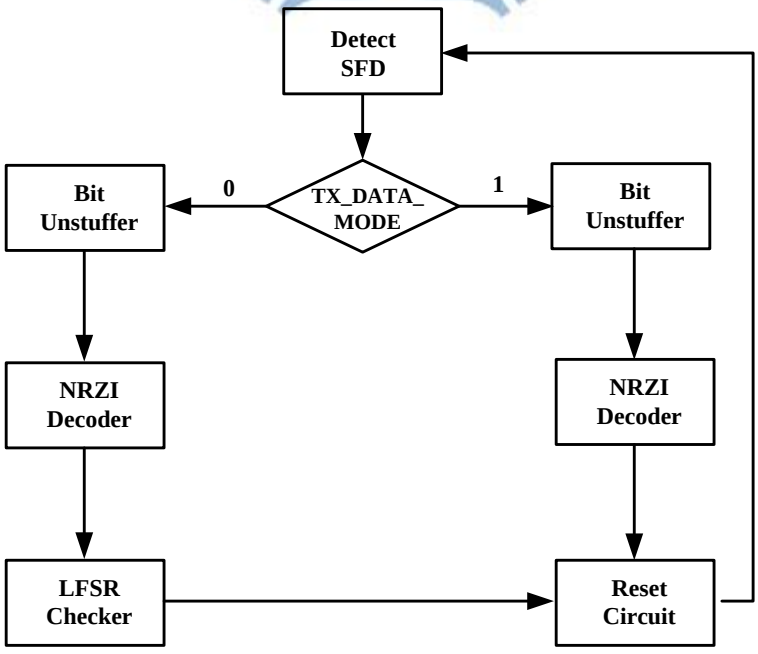


Fig. 2.13: Receiver flowcharts in random data

Fig. 2.13 shows the Receiver flowcharts in random data tracking. After detecting the SFD, the bit unstuffer will take out the stuffing bits and the NRZI decoder will decode the data. If the TX_DATA_MODE equals to “0”, it means that the random data is from the LFSR circuit of the TX. Thus, the LFSR checker will check the bit errors in the recovery data. Oppositely, the LFSR checker does not work. Finally, the RX state machine will send the signal RX_RST to reset the circuits.

2.3.2 Clock and Data Recovery

2.3.2.1 CDR Overview

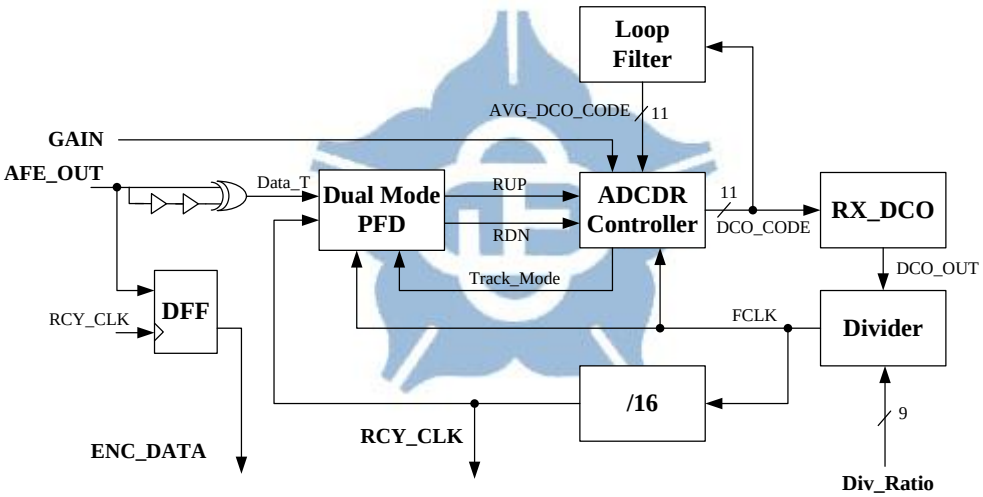


Fig. 2.14: The block diagram of the proposed ADCDR circuit

Fig. 2.14 shows the block diagram of the proposed ADCDR circuit. The proposed ADCDR circuit consists of a dual mode phase and frequency detector (PFD), a monotonic digitally controlled oscillator (RX_DCO), a digital loop filter (DLF), an ADCDR controller, a frequency divider, and a divided-by-16 frequency divider. In addition, the signal Div_Ratio is the same as the signal shown in Fig. 2.2.

In the beginning, the input data (AFE_OUT) is delayed and exclusive-OR with the original data to generate the data transition signal (Data_T). The PFD compares

the phase and frequency error between the signal Data_T and the recovery clock (RCY_CLK), and generates the signal RUP or RDN signal to the ADCDR controller. Before frequency and phase acquisition is complete, the ADCDR controller uses the binary search algorithm to adjust the DCO control code to compensate for the frequency error and phase error. Moreover, the DCO control code is sent to the digital loop filter to generate the baseline DCO control code in order to stabilize the DCO output clock (DCO_OUT). After frequency and phase acquisition is complete, the ADCDR controller sets the signal Track_Mode to “0”. In this mode, the PFD works as a PD and is suitable for phase error detection with random data. The pulse width of the signal RUP or RDN may be different according to the amount of the phase error. Thus, the ADCDR controller can quickly compensate for the large phase error. However, the DCO resolution in different process, voltage, temperature (PVT) variations is changed. Therefore, an automatically phase track gain calibration method is proposed to automatically adjust the phase track gain in different PVT variations.

In this architecture, the FCLK is 16 times of the RCY_CLK. The FCLK is used to sample the RUP or RDN signal to quantize the phase error. If the FCLK downs to 8 times of the RCY_CLK, the jitter tolerance will reduced. The simulation result is shown in Fig. 3.5 of the section 3.3.1.

2.3.2.2 Monotonic Digital Controlled Oscillator

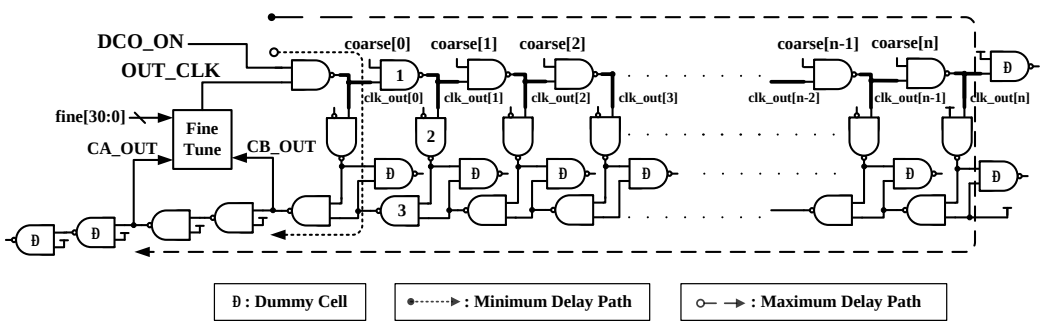


Fig. 2.15: The proposed DCO

Fig 2.15 shows the architecture of the monotonic response DCO. It is composed of a coarse-tuning delay line [29] and a fine-tuning delay line [30]. The coarse-tuning delay line consists of 63 coarse-delay cells (CDC), and each CDC is composed of four NAND gates. The 1st NAND gate is used as a switch that decides whether enable or disable the CDC circuits. The 2nd and 3rd NAND gate provide the delay time, therefore, the course-tuning resolution is the delay time of two NAND gates. The 4th NAND gate is the dummy cell which used to balance the rise time and fall time so that the duty cycle will not be distorted. The CDC is controlled by the coarse control code (coarse[n]). If the coarse control code is 63'hffff_ffff_ffff_ffff (coarse[0] ~ coarse[62] = 1), the DCO works at the lowest frequency. Oppositely, if the coarse control code is 63'h0 (coarse[0] ~ coarse[62] = 0), the DCO works at the highest frequency.

Fig. 2.16 shows the fine-tuning architecture of the DCO. It consists of two parallel connected tri-state buffer arrays [30]. The two parallel connected tri-state buffer arrays are controlled by the fine control code (Fine[n]), and it operates as an interpolator circuit. Traditionally, the total delay range of the fine-tuning stage should overlap the resolution of coarse-tuning stage [33], [34]. If this condition is not satisfied, it may cause large frequency gap. Therefore, the two parallel connected tri-state buffer arrays are adopted to enhance the resolution of the DCO. Moreover, the total delay controllable range of the fine-tuning range is always equal to the resolution of the coarse-tuning stage. Table 2.1 shows the frequency range of the DCO in different PVT corners in pre-layout simulation.

In addition, the DCO control code is 11 bits. The DCO decoder converts the 11 bits DCO control code into the thermometer codes. The DCO_CODE [10:5] will convert to coarse [62:0], and the DCO_CODE [4:0] will be converted to fine [31:0].

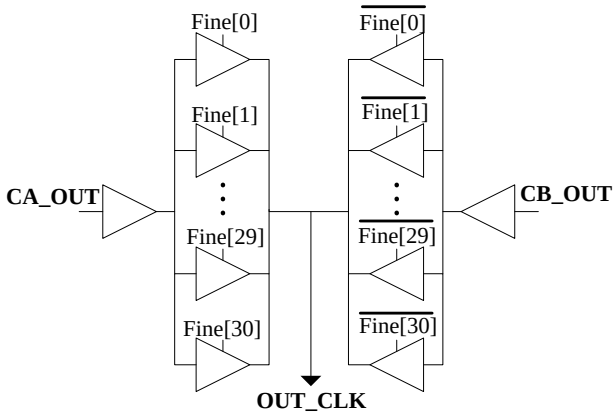


Fig. 2.16: The fine-tuning circuit of the proposed DCO [30]

Table 2.1: The DCO frequency range in different PVT corners

PVT corner	Slow case	Typical case	Fast case
	(SS, 0.9V, 100°C)	(TT, 1.0V, 25°C)	(FF, 1.1V, 0°C)
Frequency Range (MHz)	87 ~ 1547	122 ~ 2150	156 ~ 2785

2.3.2.3 Dual mode Phase and Frequency Detector

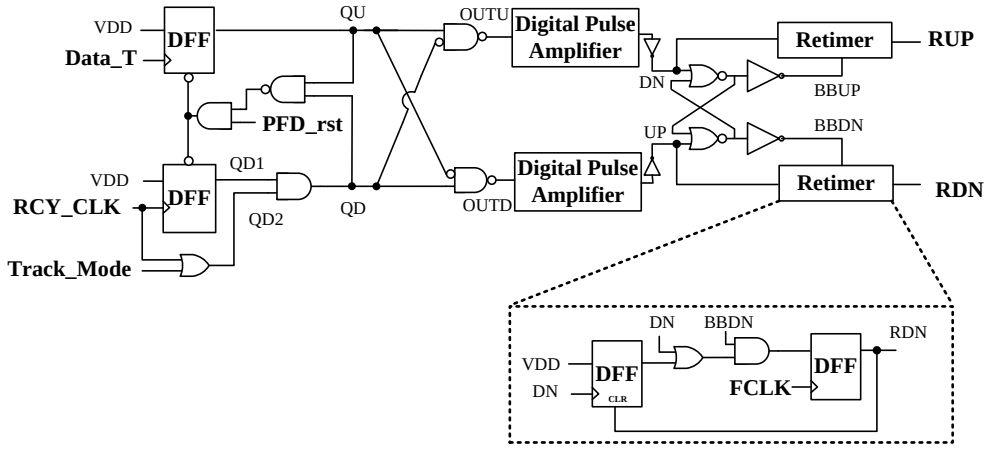


Fig. 2.17: Proposed dual mode PFD [27] and retimer architecture [28]

Fig. 2.17 shows the proposed dual mode PFD and the retimer architecture. It supports two modes: PFD mode for continuous data transition and PD mode for

random data detection. In PFD mode (Track_Mode = 1), the function of the PFD is similar to the conventional three-state bang-bang PFD to detect the frequency error and phase error with continuous data transition. The PFD will generate the signal UP or DN by comparing the rising edges of the recovery clock (RCY_CLK) and Data_T. The following SR-latch maintains the signal BBUP or BBDN until the polarity of input phase error changes. Then, the retimer generates the RUP or RDN signal by using the FCLK to sample the UP or DN signal. In addition, the frequency of the FCLK is 16x of the RCY_CLK. In PD mode (Track_Mode = 0), it is used to track the random data. Different from PFD mode, the QD signal is reset by the negative edge of the RCY_CLK. After sampled by the retimer, the maximum width of RDN signal is equal to half period of RCY_CLK. The timing diagram of the proposed dual mode PFD is shown in Fig. 2.18.

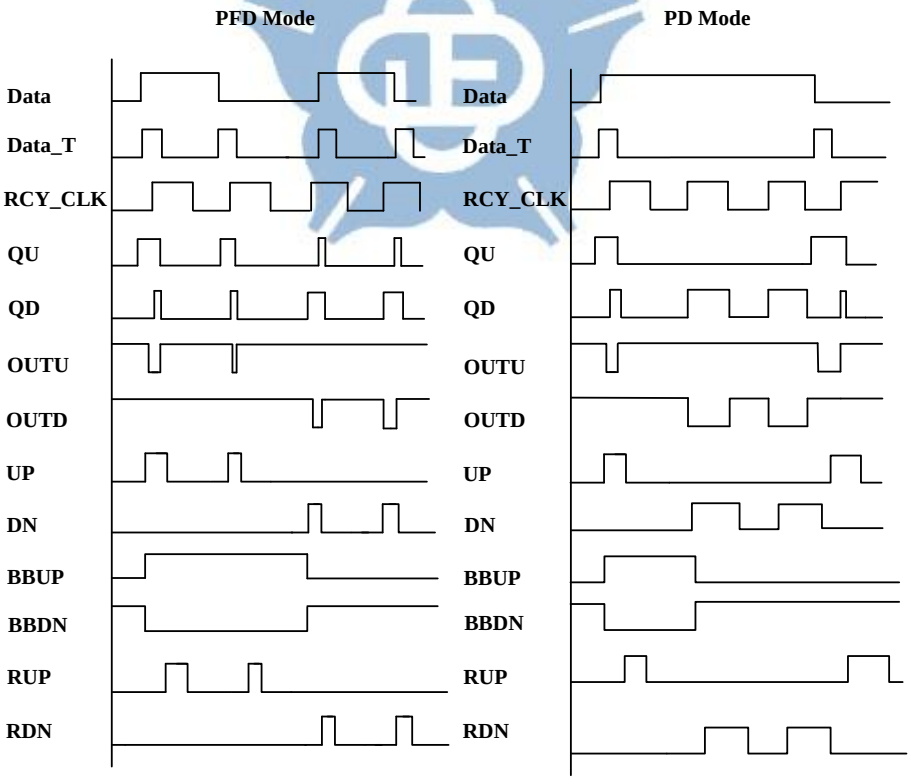


Fig. 2.18: Waveform of proposed dual mode PFD

Unlike the conventional bang-bang PFD architecture can only provide the

bang-bang information, the proposed PFD can generate different pulse width of the RUP or RDN signal according to the phase error. Fig. 2.19 shows the proposed PFD output with different phase error. There is a small pulse width of RUP or RDN signal if the phase error is small. Oppositely, a large pulse width of RUP or RDN signal is generated if there is a large phase error.

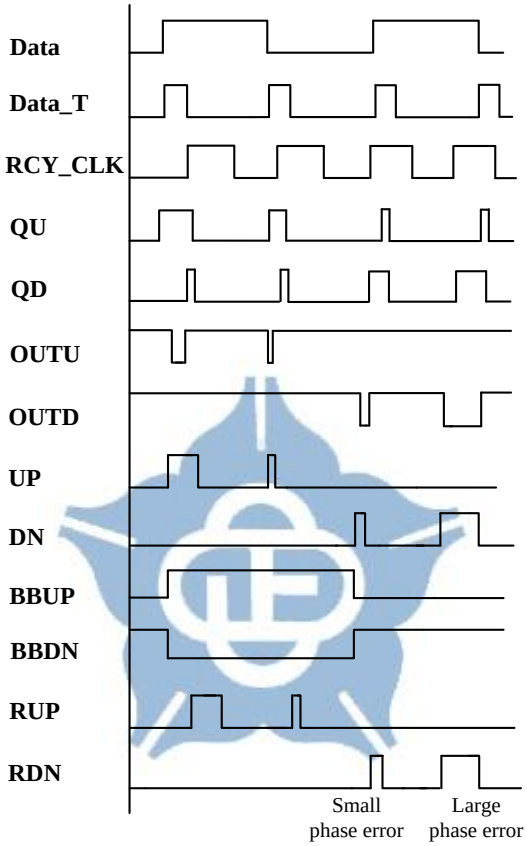


Fig. 2.19: Proposed PFD output in different phase error

2.3.2.4 Digital Loop Filter

The ADCDR will continue tracking the frequency and the phase between the data and the recovery clock. The digital loop filter [31], [32] is used to stable the DCO control code and maintain the output frequency. Fig. 2.20 shows the architecture of the digital loop filter [32]. The digital loop filter receives the DCO control code from the ADCDR controller. After the target DCO control code is sent to the DCO, the digital loop filter also stores the DCO control code. The digital loop filter stores 4

DCO control codes to generate the baseline DCO control code. Once the four DCO control codes are already stored in the digital loop filter, the baseline DCO control code is generated. Consequently, every two new DCO control codes are sent to the digital loop filter and the digital loop filter will sort the DCO control codes. Subsequently, the digital loop filter removes both the maximum and the minimum DCO control codes, and averages the rest of the DCO control codes to generate the baseline DCO control code. Thus, the baseline DCO control code is updated by the digital loop filter. The proposed digital loop filter updates the baseline DCO control code in short time and stabilizes the output frequency of the DCO.

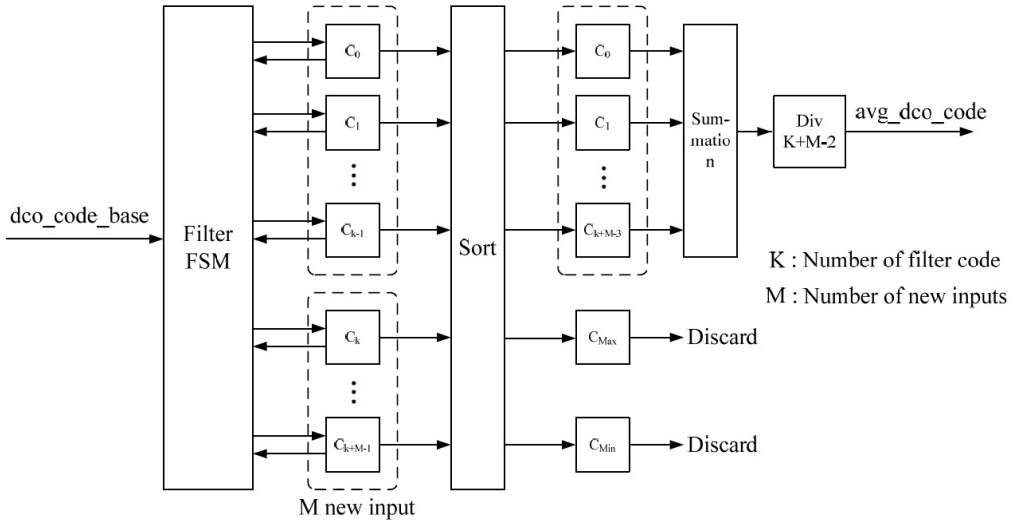


Fig. 2.20: The architecture of the digital loop filter [32]

2.3.2.5 Frequency and Phase Tracking

In conventional bang-bang CDR architecture, the PFD can only provide the bang-bang information to control the DCO. It causes the weak phase tracking ability. However, the frequency error will be accumulated in the CID region, and it may cause a large phase error in the end of the CID region. Therefore, the proposed PFD and the phase compensation approach can enhance the frequency and phase tracking ability.

In the preamble pattern, the frequency and phase tracking is according to the

signal RUP or RDN length to perform binary search. In coarse-tuning stage, once the FCLK samples that the RUP or RDN is “1”, the DCO control code will add or subtract one coarse-tuning step. In addition, if there is a polarity change, the search step will be divided by 2. When the coarse-tuning search step is equal to one, the fine tuning stage will be started. In the fine-tuning stage, the ADCDR controller adjusts the DCO control code by using the fine-tuning search step if the FCLK samples that the signal RUP or RDN is “1”. The fine-tuning search steps will be subtracted by one if the polarity is changed. In our design, the definition of the frequency locked is when fine-tuning search step is equal to one. The phase tracking will keep work until the ADCDR controller counts the preamble bits equals to seventy five. After that, the random data are input, and the ADCDR will change the other way to quickly compensate for the phase error. Fig. 2.21 shows the waveform of the tracking procedure in preamble pattern.

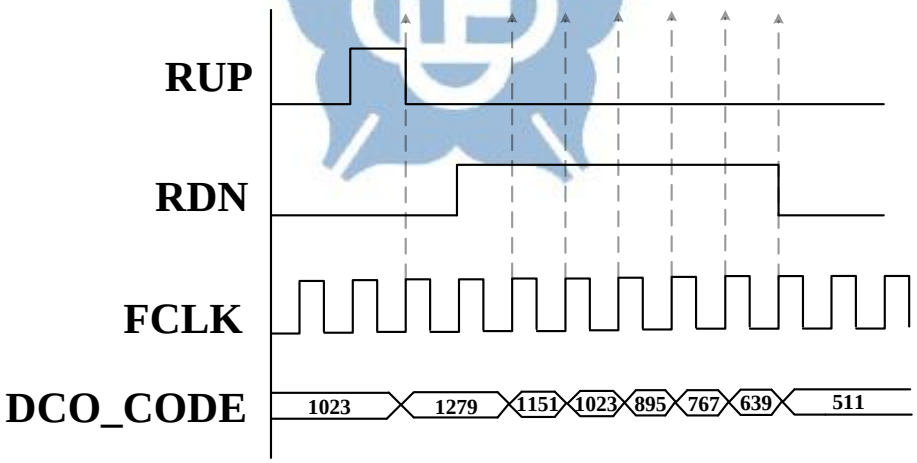


Fig. 2.21: Waveform of the tracking procedure in preamble pattern

In random data tracking, the FCLK also samples the signal RUP and RDN. According to different RUP or RDN length, the different phase track gain (GAIN) compensation is applied. Fig. 2.22 shows the compensation flow in random data. If the ADCDR controller detects the polarity changes, the baseline DCO control code (AVG_DCO_CODE) is restored and then added or subtracted by the GAIN.

Oppositely, if there is no polarity change, the ADCDR controller will check whether continuous RUP or RDN are more than three times. If there are RUP or RDN more than three times, the DCO control code will be added or subtracted by the quarter of GAIN. Oppositely, the DCO control code will be added or subtracted by the GAIN.

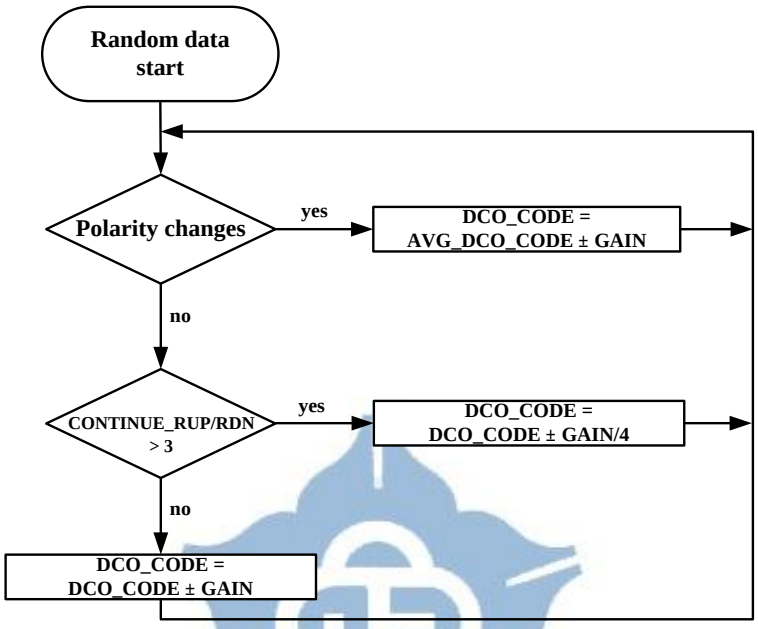


Fig. 2.22: Compensation flow in random data

When continuous RUP or RDN happen more than three times, the DCO control code may be over compensated and cause a large phase error, as shown in Fig. 2.23. There are four times RUP occur, and the DCO control code are adjusted for four times. The RCY_CLK frequency is faster than the DATA_T after consecutive updates to the DCO. After that, the data have no transition for several bit time. The DCO control code will not be updated with no data transition. Subsequently, in next data transition, a large phase error is occurred. Thus, we need to slow down the DCO control code adjustment after continuous RUP or RDN more than three times, as shown in Fig. 2.24. In Fig. 2.23, the 4th RUP only adjust the DCO control code with quarter of GAIN. Thus, in next data transition, the phase error may be small.

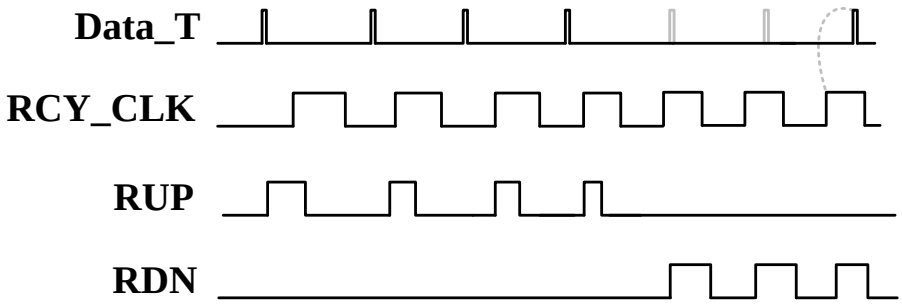


Fig. 2.23: Regular DCO control code adjustment with polarity change

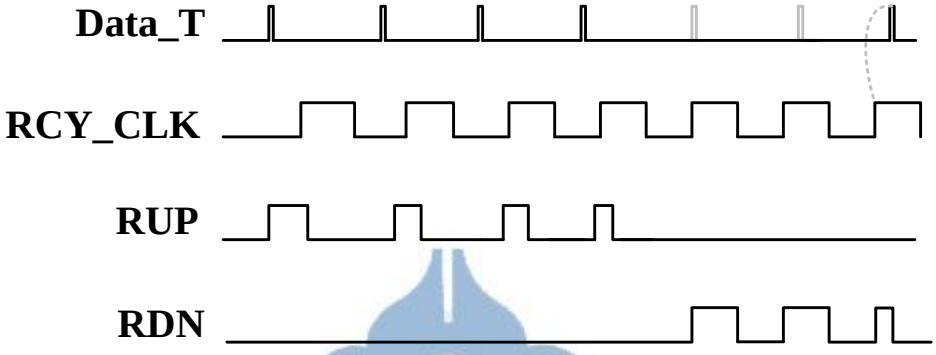


Fig. 2.24: Slow down DCO control code adjustment with polarity change

In another case, the condition is not suitable, as shown in Fig. 2.25 and Fig. 2.26. If there is no polarity change after no data transitions region, it means that the RCY_CLK must be keep adjusted to work at faster frequency. Thus, once we slow down the DCO control code adjustment, there will have a little larger phase error in next data transition as compare to regular DCO control code adjustment.

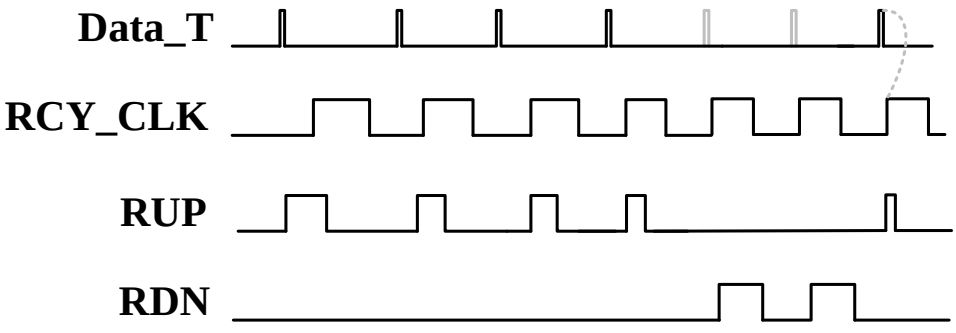


Fig. 2.25: Regular DCO control code adjustment with no polarity change

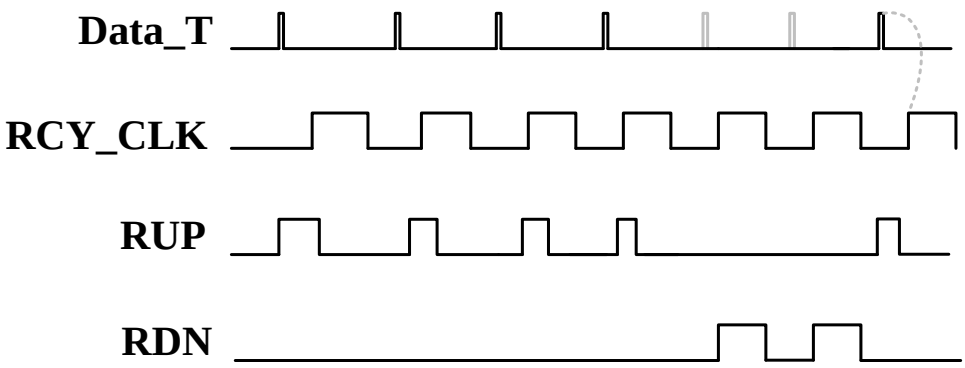


Fig. 2.26: Slow down DCO control code adjustment with no polarity change

We also simulate the BER performance in different condition, as shown in Fig. 3.6 in section 3.3.1. According to simulation result, the continuous RPU/RDN equal to 3 has larger jitter tolerance as compare to set the maximum continuous RUP/RDN to 4 or 5.

2.3.2.6 Automatically Phase Track Gain Calibration Method

Due to the PVT variations, the DCO resolution varies with operating conditions. Therefore, we need a method to calibrate the value of GAIN. The method is described below. In the beginning, the DCO control code is set to the medium value of the DCO control code (DCO_CODE = 1023), thus the DCO operates at the median frequency with the median period, denoted as P_{mid}. After that, the DCO control code is set to the maximum value of the DCO control code (DCO_CODE = 2047), and then the DCO operates at the maximum frequency with the minimum period, denote as P_{min}. Then, we can use the P_{mid} and P_{min} to calculate the R_{mid} and the R_{max} by using the cyclic counter. The definition of the R_{mid} and the R_{max} is the ratio between a symbol time (P_{ref}) and the DCO clock (DCO_OUT) period at the median frequency and the maximum frequency, respectively. The mathematical formula of the R_{mid} and R_{max} is expressed in Eqs. 2.2 and 2.3. The R_{mid} and R_{max} is the symbol time divided by the medium clock period and minimum clock period, respectively.

$$R_{mid} = \frac{P_{ref}}{P_{mid}} \tag{2.2}$$

$$R_{max} = \frac{P_{ref}}{P_{min}} \tag{2.3}$$

Because the P_{mid} is the DCO operate with the median period. We can express the R_{mid} in Eq. 2.4. The Δ is defined as the fine tuning resolution of the DCO.

$$R_{mid} = \frac{P_{ref}}{P_{min}+(2047-DCO\_CODE)\Delta} \tag{2.4}$$

As mentioned before, the R_{mid} is the period ratio when the DCO control code is set to 1023, thus the Eq. 2.5 is derived. Consequently, Eqs. 2.6 and 2.7 are derived. In Eq. 2.8, the R_{mid} is expressed in terms of R_{max}, Δ, and P_{ref}.

$$R_{mid} = \frac{P_{ref}}{P_{min}+1024\Delta} \tag{2.5}$$

$$R_{mid} = \frac{1}{\frac{P_{min}+1024\Delta}{P_{ref}}} \tag{2.6}$$

$$R_{mid} = \frac{1}{\frac{P_{min}}{P_{ref}}+\frac{1024\Delta}{P_{ref}}} \tag{2.7}$$

$$R_{mid} = \frac{1}{\frac{1}{R_{max}}+\frac{1024\Delta}{P_{ref}}} \tag{2.8}$$

According to Eq. 2.8, we can derive the Eqs. 2.9, 2.10, and 2.11.

$$\frac{1}{R_{max}} + \frac{1024\Delta}{P_{ref}} = \frac{1}{R_{mid}} \tag{2.9}$$

$$\frac{1024\Delta}{P_{ref}} = \frac{1}{R_{mid}} - \frac{1}{R_{max}} \tag{2.10}$$

$$\frac{\Delta}{P_{ref}} = \frac{(\frac{1}{R_{mid}}-\frac{1}{R_{max}})}{1024} \tag{2.11}$$

Eq. 2.12 can be easily derived because it is the reciprocal of the Eq. 2.11. Also, Eqs. 2.13 and 2.14 are derived. Then, the ratio between the symbol time (P_{ref}) and the fine tuning resolution (Δ) can be expressed in terms of R_{mid} and R_{max}.

$$\frac{P_{ref}}{\Delta} = \frac{1024}{(\frac{1}{R_{mid}} - \frac{1}{R_{max}})} \quad (2.12)$$

$$\frac{P_{ref}}{\Delta} = \frac{1024}{(\frac{R_{max} - R_{mid}}{R_{mid} \times R_{max}})} \quad (2.13)$$

$$\frac{P_{ref}}{\Delta} = \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \quad (2.14)$$

The resolution of the retimer of the PFD (*R_Resolution*) is the period of FCLK. Thus, it can be expressed in Eq. 2.15, where *N* is the divided ratio of the frequency divider.

$$R\_Resolution = N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta) \quad (2.15)$$

After frequency and phase acquisition is complete, the P_{ref} is 16 times of the retimer resolution. Therefore, we express the $\frac{P_{ref}}{\Delta}$ in another way as Eq. 2.16. Also, the Eq. 2.17 are derived.

$$\frac{P_{ref}}{\Delta} = \frac{16 \times (N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta))}{\Delta} \quad (2.16)$$

$$\frac{P_{ref}}{\Delta} = 16 \times N \times (\frac{P_{min}}{\Delta} + (2047 - DCO\_CODE)) \quad (2.17)$$

According to Eq. 2.17, we can get the ratio between the minimum DCO clock period (P_{min}) and the fine tuning resolution (Δ) as shown in Eq. 2.18.

$$\frac{P_{min}}{\Delta} = \frac{P_{ref}}{16 \times N \times \Delta} - (2047 - DCO\_CODE) \quad (2.18)$$

We assume that if the signal RUP or RDN length is *K* FCLK cycles. It represents that the phase error value is *K*. Thus, actual phase error is *K* multiplied by the retimer resolution as shown in Eq. 2.19.

$$Phase\ Error = K \times (N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta)) \quad (2.19)$$

In Fig. 2.14, the DCO_OUT will be divided by a frequency divider and a

divided-by-16 divider. Moreover, we only compensate for eighth of the actual phase error. Then, we can get the gain value (*GAIN*) that described as Eq. 2.20.

$$GAIN = \frac{K \times N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta)}{8 \times 16 \times N \times \Delta} \quad (2.20)$$

$$GAIN = \frac{K}{8 \times 16} \times \left(\frac{P_{min}}{\Delta} + (2047 - \text{DCO\_CODE})\right) \quad (2.21)$$

$\frac{P_{min}}{\Delta}$ in Eq. 2.21 can be substituted by Eq. 2.18, and then Eq. 2.22 can be derived.

$$GAIN = \frac{K}{8 \times 16} \times \frac{P_{ref}}{16 \times N \times \Delta} \quad (2.22)$$

$\frac{P_{ref}}{\Delta}$ in Eq. 2.22 can be substituted by Eq. 2.14, and Eq. 2.23 can be derived.

$$GAIN = \frac{K}{8 \times 16 \times 16 \times N} \times \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \quad (2.23)$$

The gain value is expressed in terms of the phase error value (*K*), the divide ratio of the frequency divider (*N*), R_{mid} and R_{max}. Therefore, we can estimate the gain value by Eq. 2.23. In addition, the gain value is used in the compensation flow shown in Fig. 2.22.

2.3.3 Demodulator and LFSR Checker

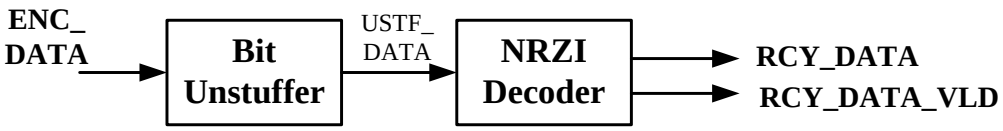


Fig. 2.27: Block diagram of the demodulator

Fig 2.27 shows the block diagram of the demodulator. It consists of a bit unstuffer and a NRZI decoder. The encoded data (ENC_DATA) from the ADCDR will firstly sent to the bit unstuffer to take out the stuffing bits. Then, the unstuffed data (USTF_DATA) will be transmitted to the NRZI decoder and generate the recovery data (RCY_DATA). At the same time, the LFSR checker will generate random pattern which is exact the same as the LFSR circuit in TX, and checks

whether there are bits errors in the (RCY_DATA).

2.4 Setting Interface

In order to set the parameters of the transceiver circuit, we need some signals from external devices. However, the pin counts of the chip are limited, we require an interface that helps to set the circuit. Fig 2.28 shows the block diagram of the setting interface. The setting clock (S_CLK), ENABLE signal, and the setting data (S_DATA) are sent to the setting interface. The setting interface will convert the serial signal S_DATA to parallel signals DCO_CODE, GAIN, CID, and Div_Ratio. The signal DCO_CODE is for TX to generate the target frequency. The signal GAIN is for the ADCDR controller to compensate for the phase error. The signals CID and Div_Datio are used to set the maximum CID and the divide ratio of the frequency divider, respectively. In addition, the interface only works when the signal ENABLE equals to "1". Fig 2.29 shows the waveform of the setting interface. The S_CLK is the clock signal that triggers the interface. When ENABLE is "1", it represents that the S_DATA is valid. The interface will catch the S_DATA and convert into the corresponding parameters. In the first 11 cycles, the S_DATA represent the 11-bits DCO_CODE of the TX_DCO. The following 7 cycles, the S_DATA represent the 4-bits GAIN and 3-bits CID, respectively. The finally 9 cycles, the S_DATA represent 9-bits Div_Ratio.

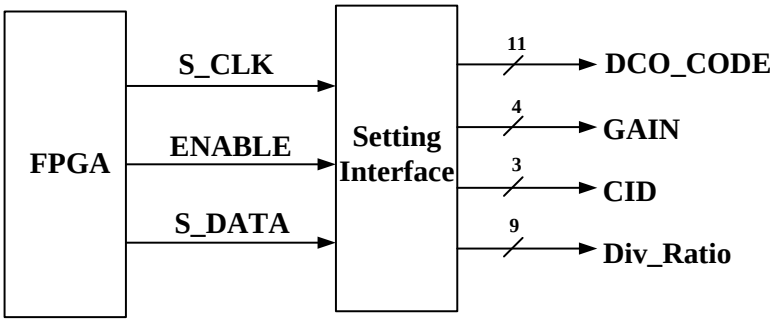


Fig. 2.28: Block diagram of the setting interface

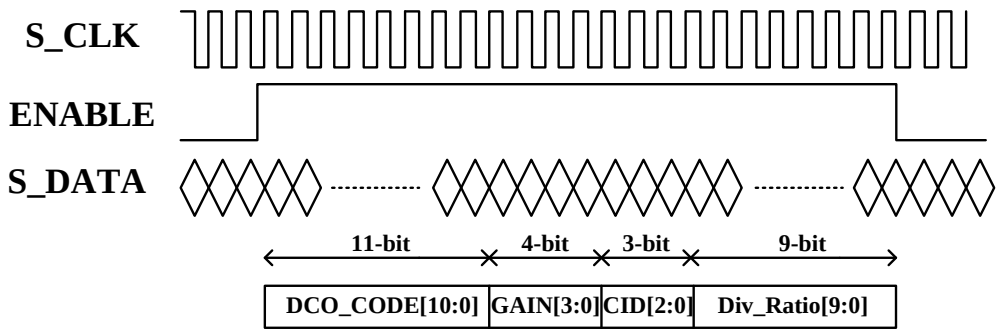


Fig. 2.29: Waveform of the setting interface

2.5 Tape-Out Chip Architecture

Fig. 2.30 shows the transceiver architecture of the tape-out chip. As compared to Fig. 2.1, the FPGAs are removed. Consequently, it can be set the parameters directly without the setting interface. In the begining, the TX will transmit the TX_DATA after circuit reset. After the AFE circuit convert the analog signal (RX_DATA) to digital signal (AFE_OUT), the RX will start to perform clock and data recovery, and generate recovery clock (RCY_CLK) and recovery data (RCY_DATA). In addition, the signal BER_Flag can show us that the BER performance.

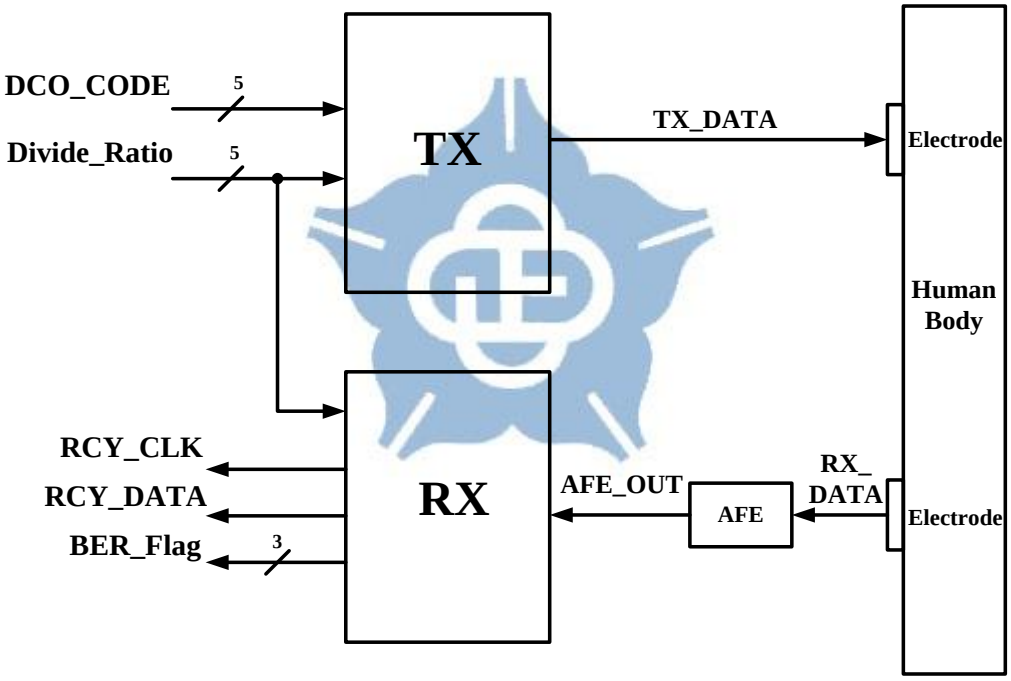


Fig. 2.30: Transceiver architecture of the tape-out chip

Fig. 2.31 shows the transmitter architecture of the tape-out chip. As compared to Fig. 2.2, the data can only be generated by the LFSR circuit, and the CID is 3. The TX flowchart of the tape-out chip is shown in Fig. 2.32. After the circuit reset, the TX will start to send the preamble pattern and the random data. After that the NRZI encoder and the bit stuffer will modulate the data. When the bit stuffing is finished, the TX will waiting for 200 cycles. Finally, the TX will be reset.

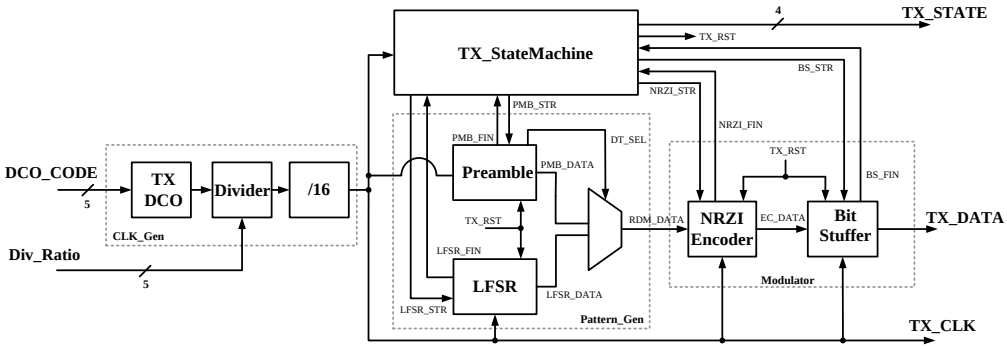


Fig. 2.31: Transmitter architecture of the tape-out chip

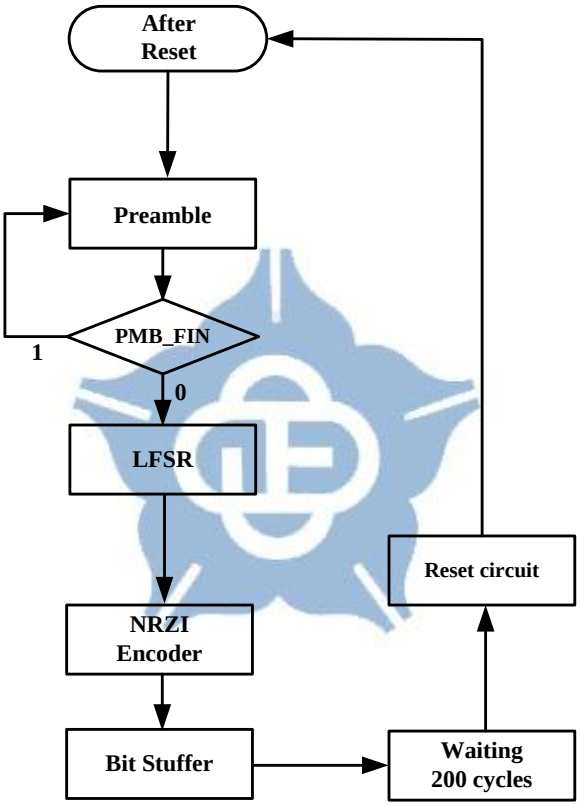


Fig. 2.32: TX flowchart of the tape-out chip

Fig. 2.33 shows the receiver architecture of the tape-out chip. Different to Fig. 2.11 is that the LFSR checker generates the 3-bits signal BER_Flag. The signal BER_Flag can help us to know the BER performance, as shown in table 2.2. The RX flowchart of the tape-out chip is shown in Fig. 2.34. After detect SFD, the bit unstuffer and the NRZI decoder will demodulate the data. Then the LFSR checker will check the bit errors. Finally, the RX will be reset, and wait for another packet.

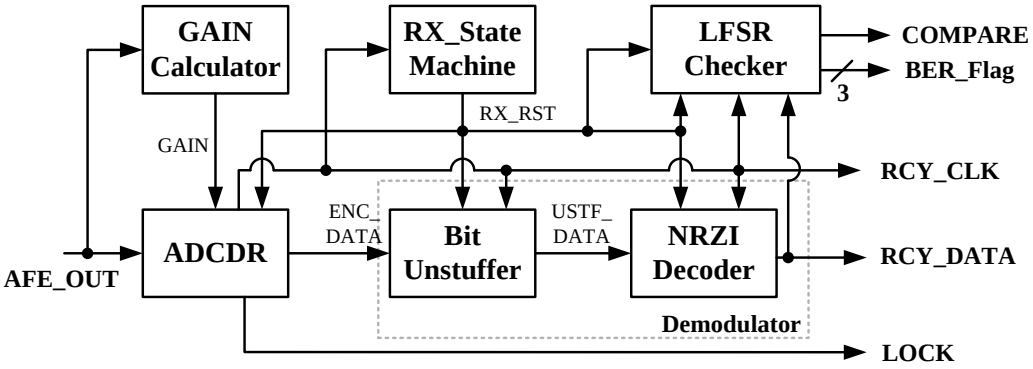


Fig. 2.33: Receiver architecture of the tape-out chip

Table 2.2: BER_Flag information

BER_Flag	BER Performance
3'd0	Reset
3'd1	First bit error occurs before first packet finishs.
3'd2	BER < 10^3
3'd3	BER < 10^4
3'd4	BER < 10^5
3'd5	BER < 10^6
3'd6	BER < 10^7
3'd7	BER < 10^8

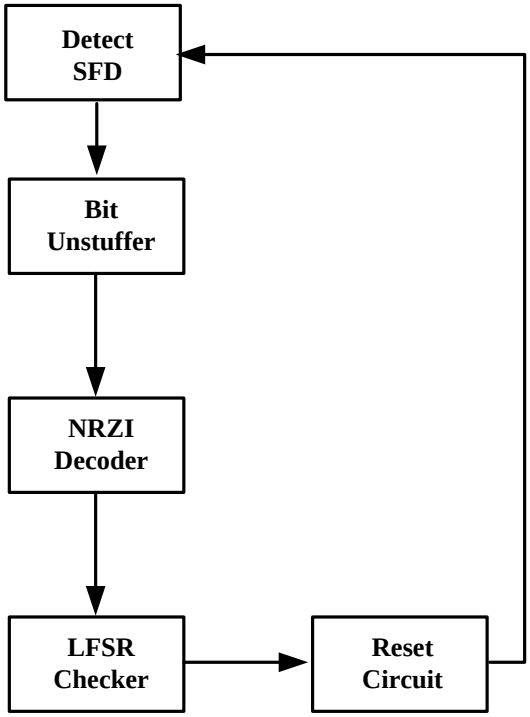


Fig. 2.34: RX flowchart of the tape-out chip

Chapter 3

Experimental Results

3.1 Test Chip Implementation

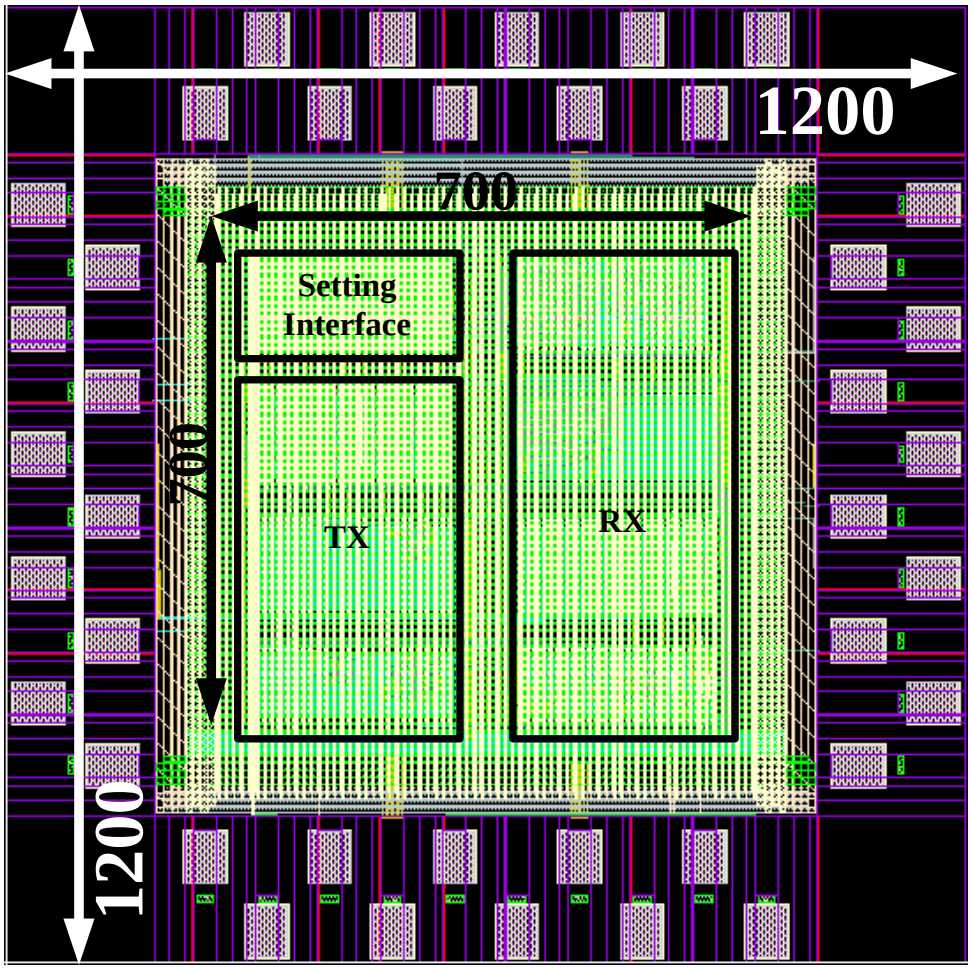


Fig. 3.1: Layout of the test chip

Fig. 3.1 shows the layout of the test chip. The test chip is implemented in TSMC 90nm CMOS process with standard cells and 1.0V power supply. The core size of the chip is $700 \times 700 \mu m^2$. The chip size including I/O PADs is $1200 \times 1200 \mu m^2$.

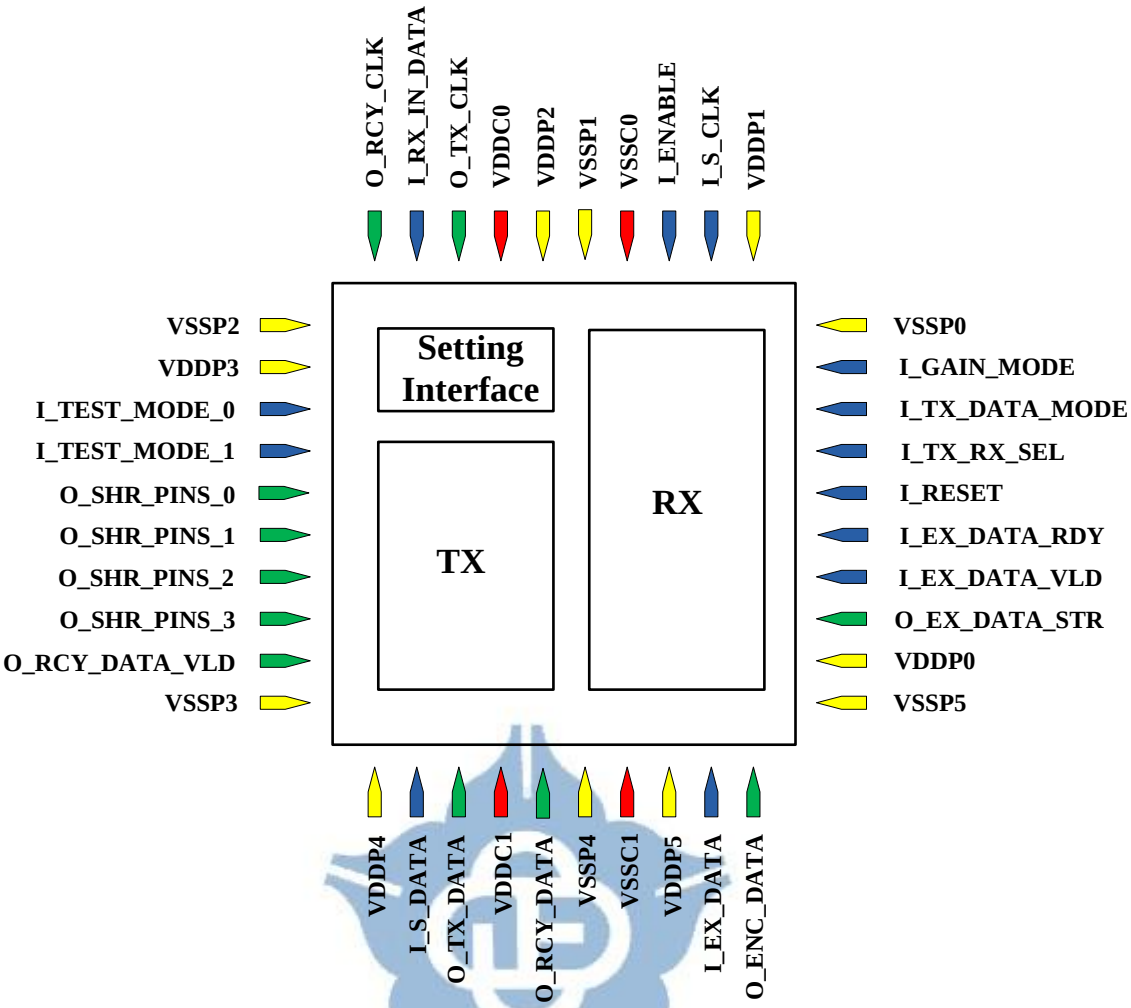


Fig. 3.2: Chip floorplan and I/O plan

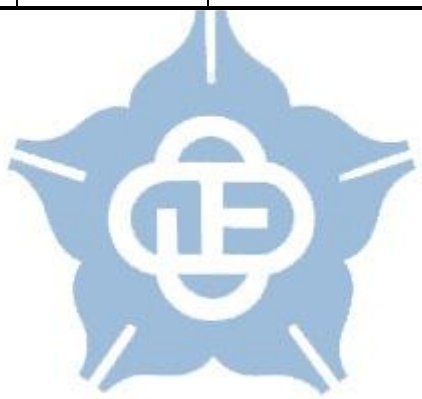
The test chip I/O planning and the floorplanning of the proposed transceiver are shown in Fig. 3.2. There are 13 input pins, 11 output pins, and 16 power pins. The detail I/O description is shown in Table 3.1.

Table 3.1: I/O PAD Description

Input	Bits	Function
RESET	1	System reset
S_CLK	1	Input clock for setting interface
S_DATA	1	Input data for setting interface
ENABLE	1	S_DATA valid

TX_RX_SEL	1	0: TX 1: RX
EX_DATA_RDY	1	External data ready
EX_DATA_VLD	1	External data valid
EX_DATA	1	External data
TX_DATA_MODE	1	Random data generated by 0: LFSR circuit 1: External device
GAIN_MODE	1	0: Internal calculated 1: External input
RX_IN_DATA	1	RX input data
TEST_MODE	2	0: Fixed TX_DCO at minimum frequency 1: Fixed TX_DCO at maximum frequency 2: Loopback test 3: Set by yourself
Output	**Bits**	**Function**
TX_CLK	1	TX clock output
EX_DATA_STR	1	External data start transmit
TX_DATA	1	TX data output
RCY_CLK	1	CDR circuit recovery clock
RCY_DATA_VLD	1	Recovery data valid
RCY_DATA	1	CDR circuit recovery data
ENC_DATA	1	Encoding data
SHR_PINS	4	TEST_MODE = 2
		Index

		3	COMPARE	
		2	LOCK	
		1	RX_STATE[1]	
		0	RX_STATE[0]	
		TEST_MODE = 3		
		Index	TX	RX
		3	TX_STATE[3]	COMPARE
		2	TX_STATE[2]	LOCK
		1	TX_STATE[1]	RX_STATE[1]
		0	TX_STATE[0]	RX_STATE[0]



3.2 Simulation Results

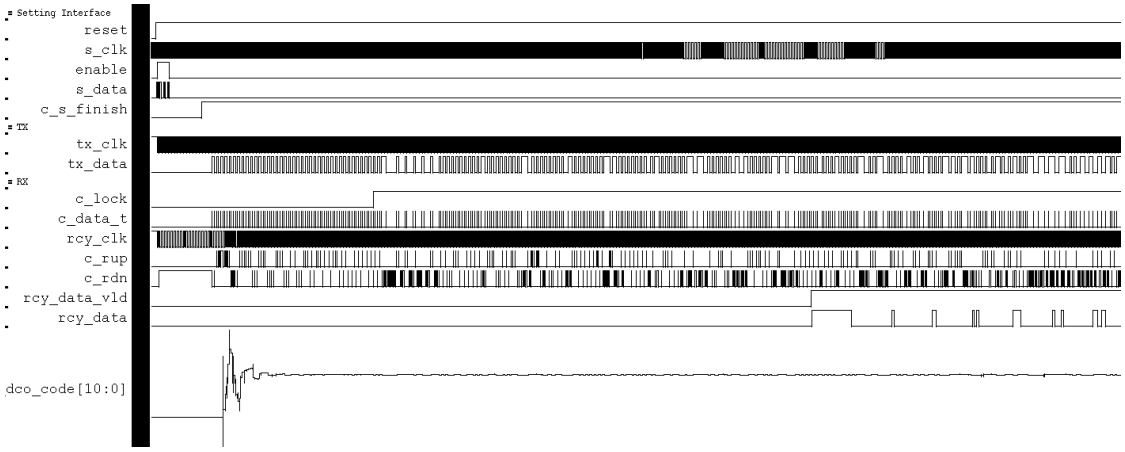


Fig. 3.3: Post-Sim at 1.0V, TT corner, 20Mps

Fig. 3.3 shows the post layout simulation of the proposed WBS transceiver in loop back mode at 20Mbps. After system is reset, the setting interface sets the parameter of the transceiver by external inputs. After setting parameters finished, the TX starts to the generate preamble pattern, SFD, and random data. In the receiver part, the RX will firstly start binary search during the preamble pattern to perform frequency and phase acquisition. After the frequency and phase acquisition is complete, the ADCDR will detect the SFD pattern and starts random data tracking. Finally, the demodulator will generate the recovery data and the valid signal (rcy_data_vld). In addition, there is a bit-unstuffing buffer in the demodulator and the recovery data are generated after the buffer is full. Therefore, there has 200 cycles latency between the TX and RX.

3.3 Error Free Measurement

3.3.1 Random Jitter Tolerance

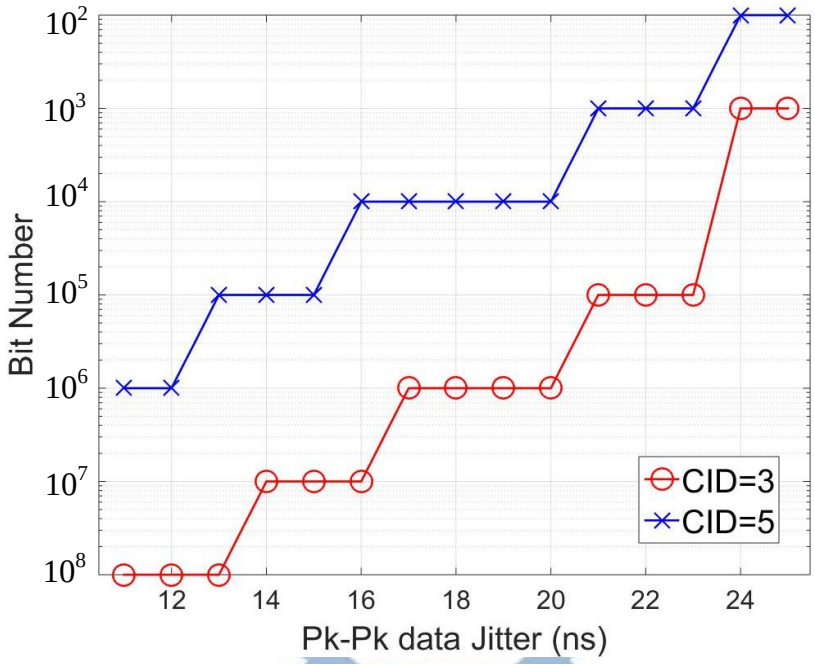


Fig. 3.4: Error-Free simulation result at 20Mbps

Fig. 3.4 shows the error-free simulation results at 20Mbps data rate. The transceiver has a bit-error-rate (BER) < 10^{-5} with 13 ns Pk-Pk data jitter when the number of CID is 5. If CID is reduced, it has a BER < 10^{-8}. For the ADCDR circuit, if there has more data transitions, it can improve the ADCDR performance in phase tracking. Therefore, in the proposed ADCDR, CID is equal to 3.

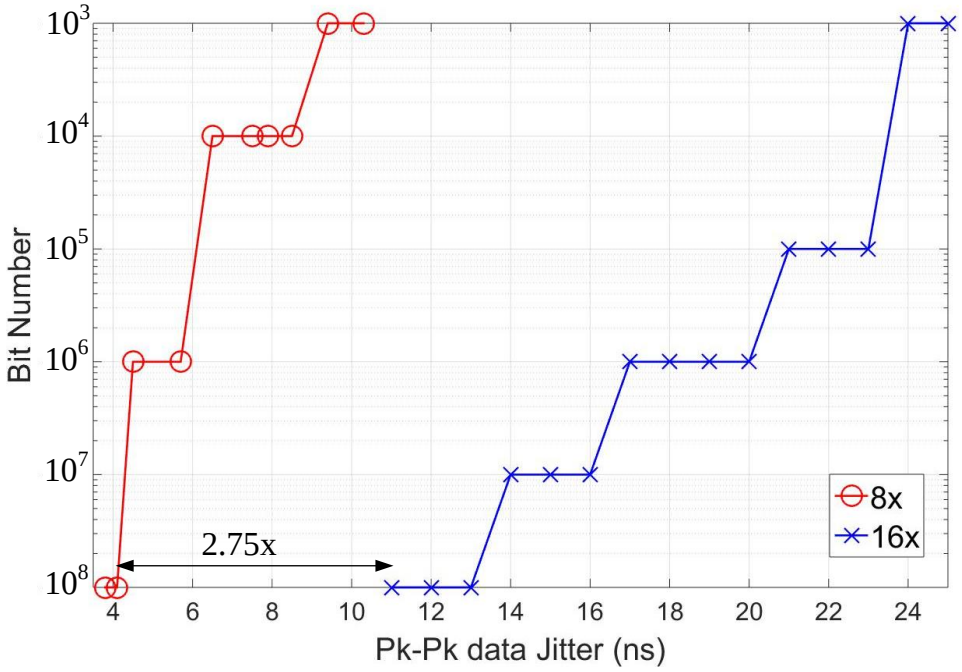


Fig. 3.5: Error-Free simulation result with different sample rate at 20Mbps

Fig. 3.5 shows the error-free simulation result at 20 Mbps with different sample rate. The simulation result shows that the 16x sample rate has 2.75 times jitter tolerance than the 8x sample rate with BER performance < 10^{-8}.

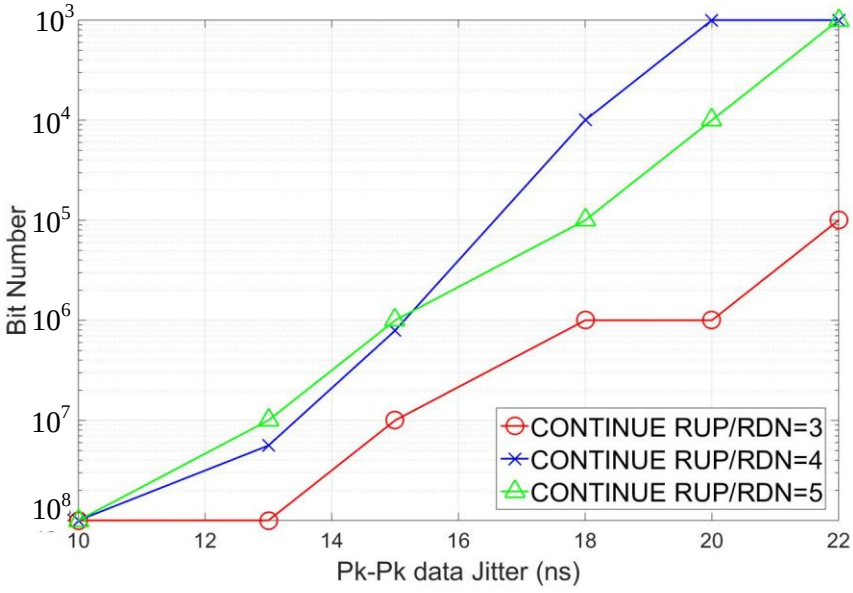


Fig. 3.6: Error-Free simulation result with different maximum continuous RUP/RDN at 20Mbps

In random data tracking compensation flow, as shown in Fig. 2.22 in section

2.3.2.5, if there are continuous RUP or RDN more than three times, the DCO control code will added or subtracted by the quarter of GAIN. Fig. 3.6 shows the error-free simulation result at 20 Mbps, CID equals to 3 with different maximum continuous RUP/RDN conditions. The simulation result shows that the continuous RUP or RDN equal to 3, the proposed ADCDR has large jitter tolerance as compare to maximum continuous RUP or RDN equal to 4 or 5.

3.3.2 Sinusoidal Jitter Tolerance

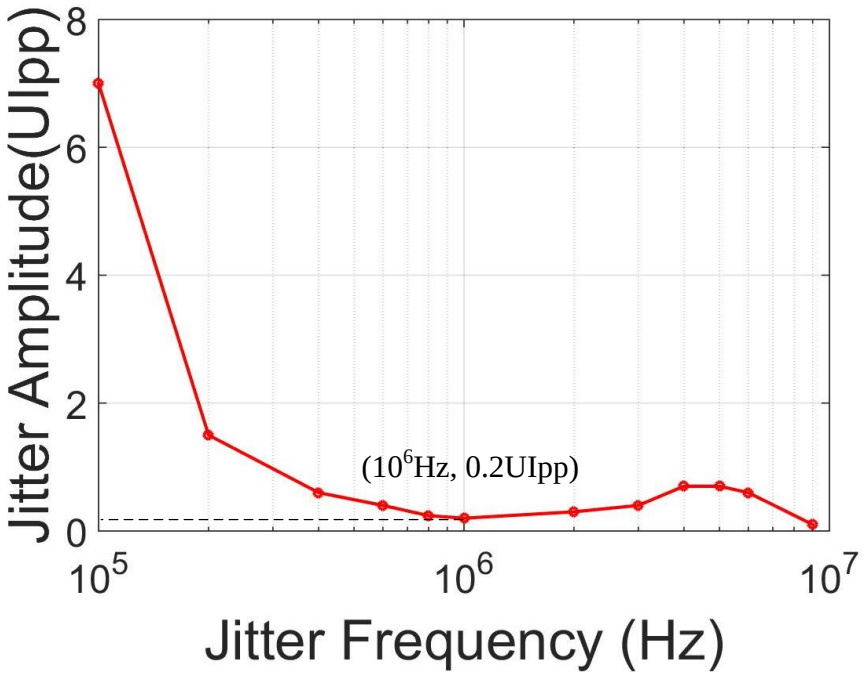


Fig. 3.7: Sinusoidal jitter tolerance performance

In jitter tolerance testing of the receiver, the input data rate is modulated with a sinusoidal jitter. The sinusoidal jitter has three parameters, UI_{jitter} (peak-peak), Δf and f_j, as shown in Eq. 3.1. The UI_{jitter} (peak-peak) is the total jitter accumulation in one sinusoidal modulation period. The Δf is the maximum frequency variation in one sinusoidal modulation period. The f_j is the modulation frequency of the sinusoidal jitter.

$$UI_{jitter}\,(peak-peak) = \frac{\Delta f}{f_{j*\pi}} \tag{3.1}$$

Fig. 3.7 shows the sinusoidal jitter tolerance of the ADCDR circuit at 20 Mbps. The proposed reference-less ADCDR circuit only uses the data to perform the clock and data recovery. Thus, the corner frequency is at 1MHz with 0.2UI jitter tolerance.

3.3.3 Error Free Measurement with Frequency Drift

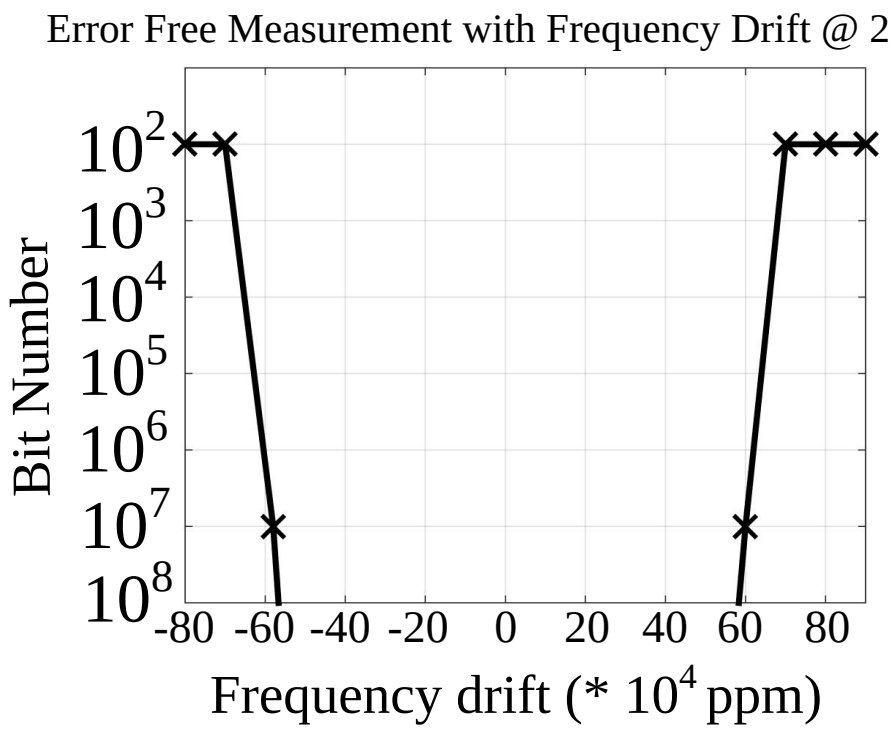


Fig. 3.8: Error-Free measurement with different frequency drift at 20Mbps

Fig. 3.8 shows the error-free measurement with different frequency drift at 20Mbps. The performance of the ADCDR has a BER < 10^{-7} within the range from -600000 ppm to +600000 ppm at 20Mbps. If the frequency is out of the range of the DCO control code, it may cause the bit errors. Because the proposed reference-less ADCDR circuit has the frequency and phase tracking ability, thus, it has a wide range frequency drift tolerance as compared to oversampling-based CDR circuit.

3.3.4 Random Data Eye Diagram

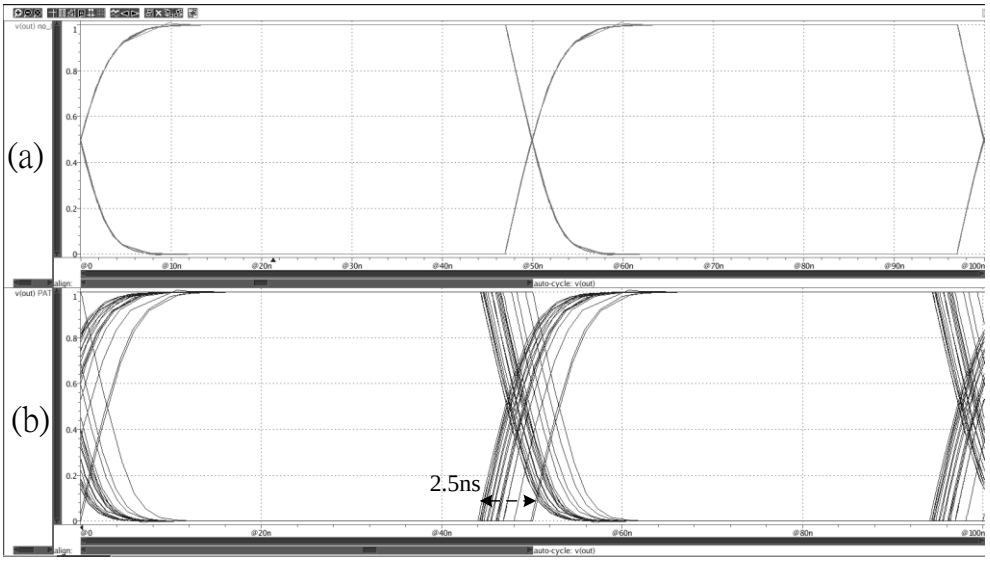


Fig. 3.9: Eye diagram of random data at 20Mbps

(a) No jitter (b) With jitter

Fig. 3.9 shows the eye diagram of the transmitted random data pattern at 20Mbps. We can find that if the data has no jitter effect, the eye is very clear. Oppositely, if the data has jitter effect, the edge of the random data may have some variations.

3.4 Test Chip Summary and Comparison Table

Table 3.2: Chip Summary

Process	90nm CMOS
Operating Range	1 Mb/s ~ 20 Mb/s
Supply Voltage	1.0V
Core Area	0.49 mm^2
Power Consumption	6.0 mW (at 20Mb/s) (w/o AFE circuit)
BER	10^{-8} (at 20 Mb/s)
Energy/bit	0.3 nJ/b (at 20 Mb/s)

The chip summary is shown in Table 3.2. The chip is implemented in TSMC 90nm CMOS process with standard cells and 1.0V power supply. The core area is 0.49 mm^2. The data rate of the proposed WBS transceiver is from 1Mb/s to 20Mb/s. The power consumption is 6.0 mW at 20Mb/s without the AFE circuit. The bit error rate (BER) is less than10^{-8}, and the energy consumption per bit is 0.3nJ/b at 20Mb/s.

Table 3.3: Comparison table

	[11] JSSC'07	[35] JSSC'09	[14] JSSC'12	[13] ISSCC'14	[18] VLSI-DAT'15	[16] JSSC'16	Proposed
Communication Method	Wideband Signaling	FSK	FSK	3-level Walsh Coding	OFDM	BPSK	Wideband Signaling
Process	0.25 μm	0.18 μm	0.18 μm	65 nm	90 nm	65 nm	90 nm
Data Rate	2 Mb/s	60 kb/s ~ 10 Mb/s	1 kb/s ~ 10 Mb/s	60 Mb/s	29.1Mb/s	80 Mb/s	1 Mb/s ~ 20 Mb/s
Modulation	No	Adaptive Frequency Hopping FSK	Double FSK	3-level Walsh Coding	16-QAM OFDM	Binary Phase Shift Keying	Non-Return-to -Zero-Inversed
Supply	1 V	1 V	1 V	1.1 V	0.53 V	1.2 V	1 V
Sensitivity	-36 dBm	-65 dBm	-66 dBm	-58 dBm	N/A	-58 dBm	-18.87dBm
Power Consumption	0.2 mW	3.7 mW	4.4 mW	10.87 mW	9.37mW	6.3 mW	6 mW (w/o AFE circuit)
Area	0.85 mm^2	2.30 mm^2	4.5 mm^2	0.85 mm^2	5.2 mm^2	5.76 mm^2	0.49 mm^2
BER	$1.1*10^{-7}$	10^{-5} (10Mb/s) $<10^{-9}$ (60kb/s)	10^{-5}(10Mb/s) 10^{-12}(10kb/s)	$<10^{-5}$ @ 60Mb/s	N/A	$<10^{-5}$ @ 40Mb/s	$<10^{-8}$ @20Mb/s
Energy/bit	2.5 nJ/b	0.37 nJ/b	0.44 nJ/b	0.18nJ/b	0.32 nJ/b	0.079 nJ/b	0.3nJ/b

Table 3.3 shows the comparison with other BCC design. The chip area of the proposed design has small area. Although [13] and [16] achive high data rate, they still have a high power consumption. Moreover, the proposed design also has higher data rate than [11], [14], and [35].

3.5 Tape-Out Chip

3.5.1 Tape-Out Chip Implementation

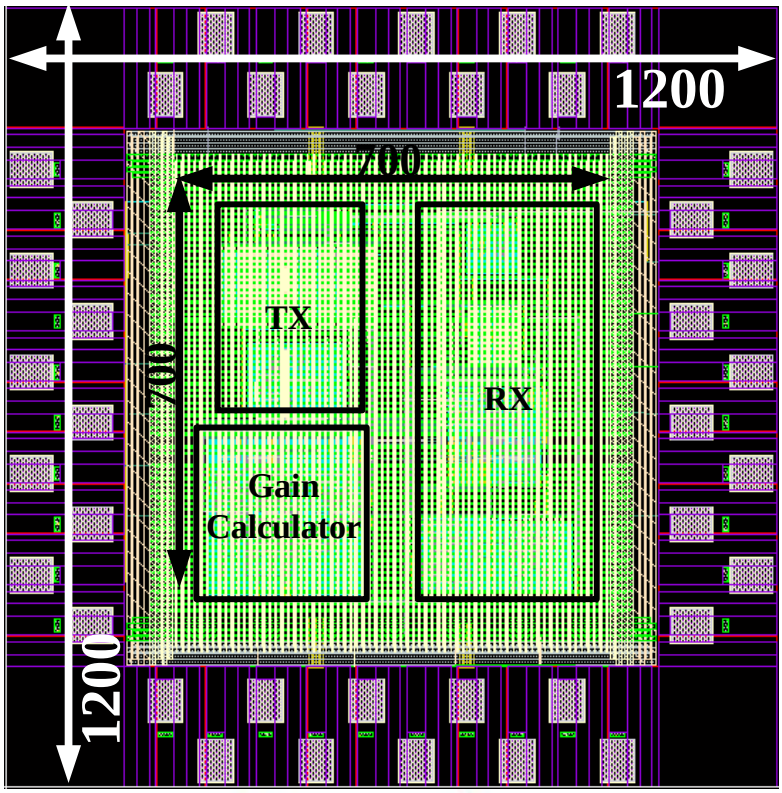


Fig. 3.10: Layout of the tape-out chip

Fig. 3.10 shows the layout of the tape-out chip. The tape-out chip is implemented in TSMC 90nm CMOS process with standard cells and 1.0V power supply. The core size of the tape-out chip is $700 \times 700 \mu m^2$.The chip size including I/O PADs is $1200 \times 1200 \mu m^2$.

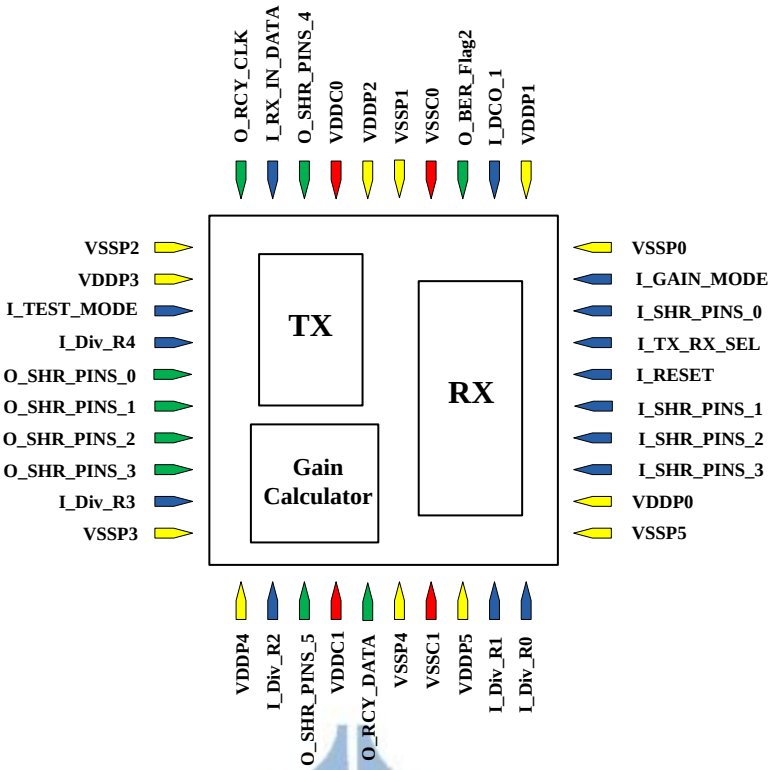


Fig. 3.11: Tape-out chip floorplan and I/O plan

The tape-out chip I/O planning and the floorplanning are shown in Fig. 3.11. There are 15 input pins, 9 output pins, and 16 power pins. The detail I/O description is shown in Table 3.4. If the signal TEST_MODE equal to 0, the signal I_SHR_PINS can only set the DCO_CODE of the TX. When signal TX_RX_SEL equal to 0, the signal SHR_PINS is represented as TX information. Oppositely, the signal SHR_PINS is represented as RX information. If the signal TEST_MODE equal to 1, according to signal TX_RX_SEL, the chip can be TX or RX.

Table 3.4: Tape-out chip I/O description table

Input	Bits	Function
RESET	1	System reset
TX_RX_SEL	1	0: TX 1: RX
GAIN_MODE	1	0: Internal calculated

<table>
<tr><td></td><td></td><td colspan="3">1: External input</td></tr>
<tr><td>TEST_MODE</td><td>1</td><td colspan="3">0: Loopback test
1: TX or RX</td></tr>
<tr><td>RX_IN_DATA</td><td>1</td><td colspan="3">RX input data</td></tr>
<tr><td rowspan="11">I_SHR_PINS</td><td rowspan="11">4</td><td colspan="3">TEST_MODE = 0</td></tr>
<tr><td>Index</td><td colspan="2"></td></tr>
<tr><td>3</td><td colspan="2">DCO_CODE[5]</td></tr>
<tr><td>2</td><td colspan="2">DCO_CODE[4]</td></tr>
<tr><td>1</td><td colspan="2">DCO_CODE[3]</td></tr>
<tr><td>0</td><td colspan="2">DCO_CODE[2]</td></tr>
<tr><td colspan="3">TEST_MODE = 1</td></tr>
<tr><td>Index</td><td>TX</td><td>RX</td></tr>
<tr><td>3</td><td>DCO_CODE[5]</td><td>GAIN[3]</td></tr>
<tr><td>2</td><td>DCO_CODE[4]</td><td>GAIN[2]</td></tr>
<tr><td>1</td><td>DCO_CODE[3]</td><td>GAIN[1]</td></tr>
<tr><td>0</td><td>DCO_CODE[2]</td><td>GAIN[0]</td></tr>
<tr><td>DCO_CODE_1</td><td>1</td><td colspan="3">DCO_CODE[1]</td></tr>
<tr><td>Div_R</td><td>5</td><td colspan="3">Divide Ratio</td></tr>
<tr><td>Output</td><td>Bits</td><td colspan="3">Function</td></tr>
<tr><td>RCY_CLK</td><td>1</td><td colspan="3">CDR circuit recovery clock</td></tr>
<tr><td>RCY_DATA</td><td>1</td><td colspan="3">CDR circuit recovery data</td></tr>
<tr><td rowspan="4">SHR_PINS</td><td rowspan="4">6</td><td>Index</td><td>TX</td><td>RX</td></tr>
<tr><td>5</td><td>TX_DATA</td><td>BER_Flag[1]</td></tr>
<tr><td>4</td><td>TX_CLK</td><td>BER_Flag[0]</td></tr>
<tr><td>3</td><td>TX_STATE[3]</td><td>COMPARE</td></tr>
</table>

		2	TX_STATE[2]	LOCK
		1	TX_STATE[1]	RX_STATE[1]
		0	TX_STATE[0]	RX_STATE[0]
BER_Flag_2	1	BER_Flag[2]		

3.5.2 Simulation Result

Fig. 3.12 to 3.16 show the post layout simulation of the proposed transceiver with PVT variations. After system reset, the TX starts to generate preamble pattern, SFD, and random data. The RX will firstly calculate the GAIN value, and will start frequency and phase acquisition. After the frequency and phase acquisition is complete, the ADCDR will detect the SFD and start random data tracking. At last, the demodulator will demodulate the data and the LFSR checker will check the data.

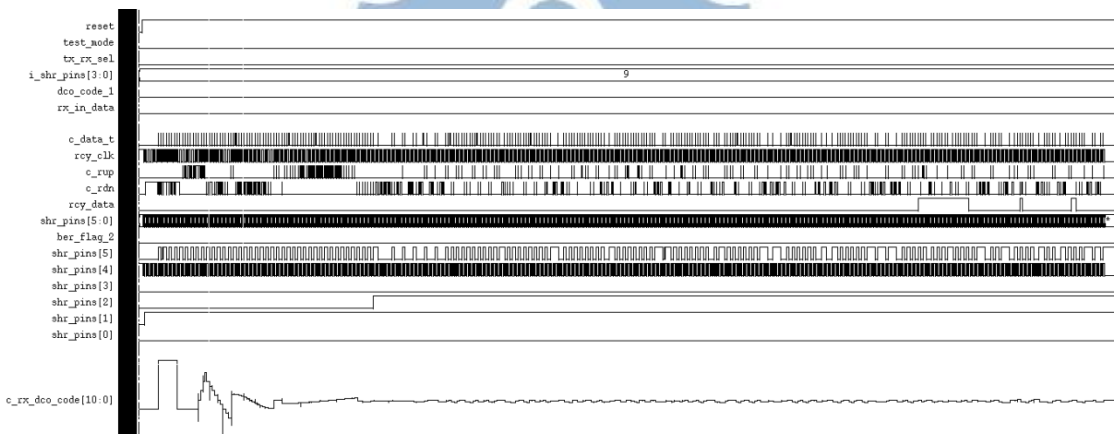


Fig. 3.12: Post-Sim at 1.0V, TT corner, 20Mbps, loopback

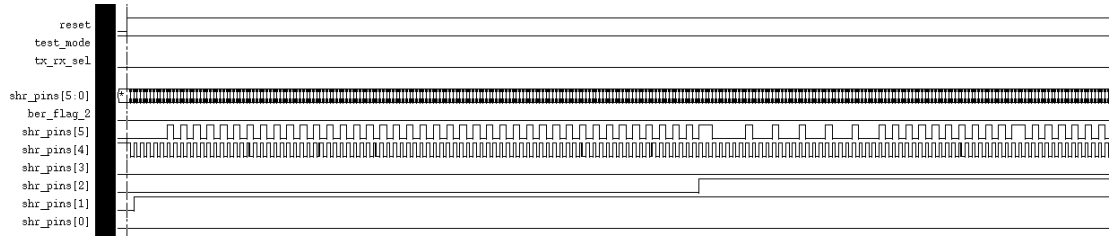


Fig. 3.13: Post-Sim at 1.0V, TT corner, 20Mbps, TX

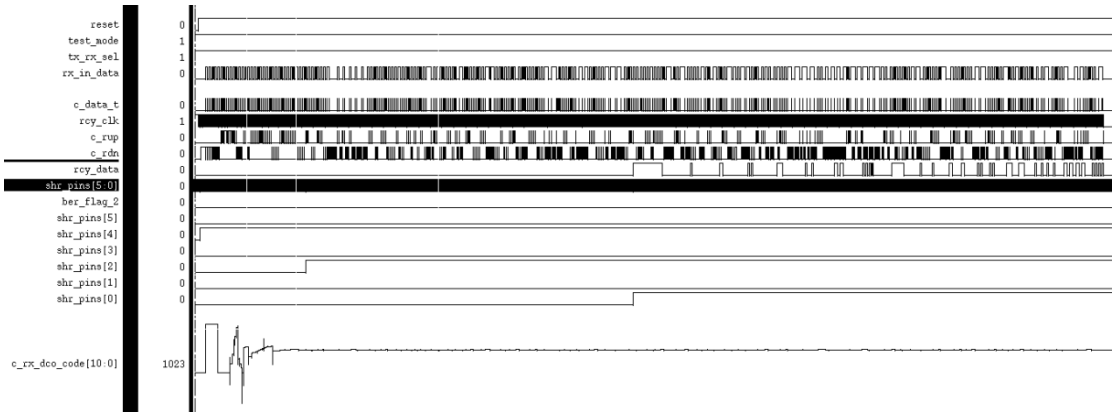


Fig. 3.14: Post-Sim at 1.1V, FF corner, 20Mbps, RX (no data jitter)

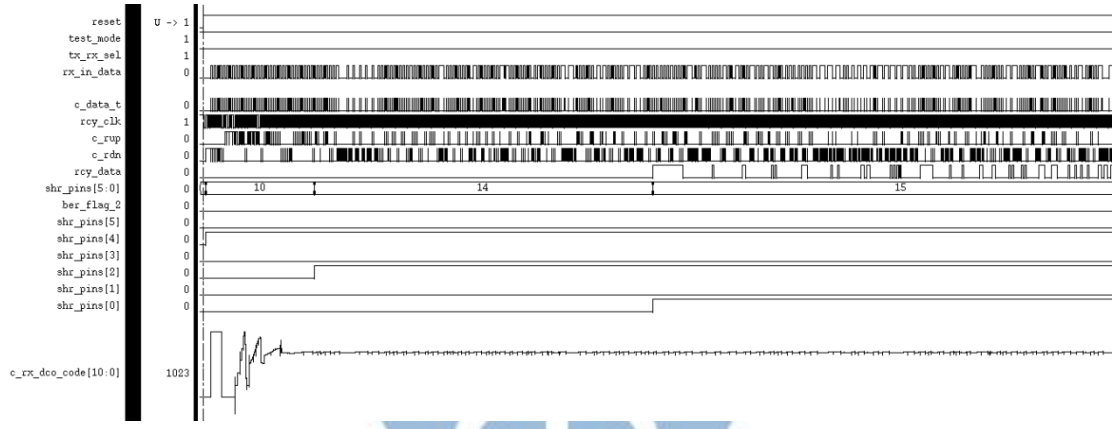


Fig. 3.15: Post-Sim at 1.0V, TT corner, 20Mbps, RX (no data jitter)

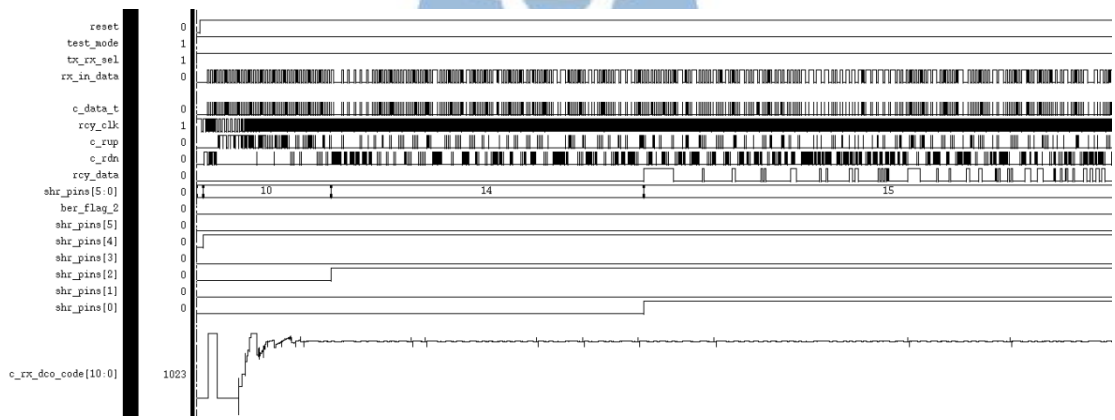


Fig. 3.16: Post-Sim at 0.9V, SS corner, 20Mbps, RX (no data jitter)

Fig. 3.17 shows the post layout simulation of the proposed receiver. The input data is with 25ns Pk-Pk jitter. We can easily find that there is a bit error if the signal COMPARE equals to “1”. We can know that the BER_Flag is equal to 2, according to table 2.2, the BER performance < 10^{-3}.

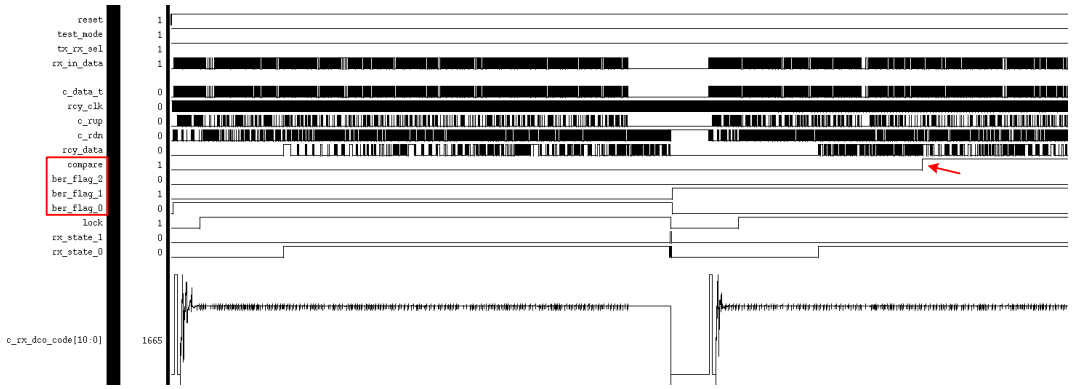


Fig. 3.17: Post-Sim at 1.0V, TT corner, 20Mbps, RX (with 25nsPk-Pk data jitter)

3.5.3 Tape-Out Chip Summary

Table 3.5: Tape-Out Chip Summary

Process	90nm CMOS
Operating Range	1 Mb/s ~ 20 Mb/s
Supply Voltage	1.0V
Core Area	0.49 mm^2
Power Consumption	5.5 mW (at 20Mb/s) (w/o AFE circuit)
BER	10^{-8} (at 20 Mb/s)
Energy/bit	0.275 nJ/b (at 20 Mb/s)

The tape-out chip summary is shown in Table 3.5. The tape-out chip is implemented in TSMC 90nm CMOS process with standard cells and 1.0V power supply. The core area is 0.49 mm^2. The data rate of the proposed WBS transceiver is from 1Mb/s to 20Mb/s. The power consumption is 5.5 mW at 20Mb/s without the AFE circuit. The bit error rate (BER) is less than10^{-8}, and the energy consumption per bit is 0.275nJ/b at 20Mb/s.

Table 3.6: Comparison table

	[11] JSSC'07	[35] JSSC'09	[14] JSSC'12	[13] ISSCC'14	[18] VLSI-DAT'15	[16] JSSC'16	Proposed
Communication Method	Wideband Signaling	FSK	FSK	3-level Walsh Coding	OFDM	BPSK	Wideband Signaling
Process	0.25 μm	0.18 μm	0.18 μm	65 nm	90 nm	65 nm	90 nm
Data Rate	2 Mb/s	60 kb/s ~ 10 Mb/s	1 kb/s ~ 10 Mb/s	60 Mb/s	29.1Mb/s	80 Mb/s	1 Mb/s ~ 20 Mb/s
Modulation	No	Adaptive Frequency Hopping FSK	Double FSK	3-level Walsh Coding	16-QAM OFDM	Binary Phase Shift Keying	Non-Return-to -Zero-Inversed
Supply	1 V	1 V	1 V	1.1 V	0.53 V	1.2 V	1 V
Sensitivity	-36 dBm	-65 dBm	-66 dBm	-58 dBm	N/A	-58 dBm	-18.87dBm
Power Consumption	0.2 mW	3.7 mW	4.4 mW	10.87 mW	9.37mW	6.3 mW	5.5 mW (w/o AFE circuit)
Area	0.85 mm^2	2.30 mm^2	4.5 mm^2	0.85 mm^2	5.2 mm^2	5.76 mm^2	0.49 mm^2
BER	$1.1*10^{-7}$	10^{-5} (10Mb/s) $<10^{-9}$ (60kb/s)	10^{-5}(10Mb/s) 10^{-12}(10kb/s)	$<10^{-5}$ @ 60Mb/s	N/A	$<10^{-5}$ @ 40Mb/s	$<10^{-8}$ @20Mb/s
Energy/bit	2.5 nJ/b	0.37 nJ/b	0.44 nJ/b	0.18nJ/b	0.32 nJ/b	0.079 nJ/b	0.275nJ/b

Table 3.3 shows the comparison with other BCC design. The chip area of the proposed design has small area. Although [13] and [16] achive high data rate, they still have a high power consumption. Moreover, the proposed design also has higher data rate than [11], [14], and [35].

Chapter 4

Conclusion and Future Works

4.1 Conclusion

In this thesis, a WBS transceiver is proposed. In transmitter part, the data can generate by the LFSR circuit or external input. The data are modulated by the NRZI encoder and the bit stuffer to increase the data transitions. Moreover, the data are transmitted in the packet format. In receiver part, a reference-less all-digital clock and data recovery (ADCDR) is proposed. The proposed PFD and the phase compensation approach can enhance the frequency and phase tracking ability. During the preamble pattern, the ADCDR controller uses binary search to perform frequency and phase acquisition. After phase and frequency is complete, the ADCDR controller detects the SFD and start random data tracking. In random data tracking, the proposed PFD will detect the phase error between data and recovery clock. The PFD generates different phase error value according to the magnitude of the phase error. Thus, the ADCDR controller can fast compensate for the phase error by the proposed design.

Due to the PVT variations, the DCO resolution varies with operating conditions. Therefore, an automatically phase track gain calibration method is proposed to solve the problem. The method uses the ratio between the symbol time and the DCO clock period at the median frequency (R_{mid}) and the maximum frequency (R_{max}) to calculate the gain value. Thus, in different PVT conditions, the gain value will be calibrated automatically.

The test chip is implemented in TSMC 90nm process with standard cells. The core area is 0.49 mm^2 and the power consumption is 5.5mW at 20Mbps.

4.2 Future Works

In our design, the ADCDR controller is in the DCO clock domain. Thus, the ADCDR controller works at high frequency. For example, at 20Mbps, the ADCDR controller runs at 320MHz. It causes the proposed design has relatively high power consumption. If the ADCDR controller can be changed to the reference clock (data) domain, the ADCDR can work at lower frequency. Then, the power consumption of the ADCDR can be further reduced.

The method that used to change the clock domain of the ADCDR controller is shown in Fig. 4.1. The FCLK will sample and quantize the RUP or RDN signal. The signals UP_CNT and DN_CNT are the quantized value. We can use a register (UP_Reg/DN_Reg) to store the quantized value. Then, in next RCY_CLK rising edge, by restoring the UP_Reg or DN_Reg, the ADCDR controller can get the previous quantized value. Therefore, the ADCDR controller can move to RCY_CLK domain.

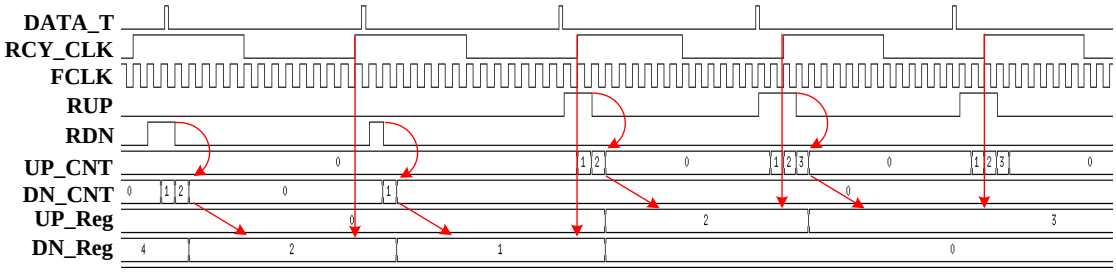


Fig. 4.1: ADCDR controller change clock domain illustration

In this thesis, the AFE circuit is not included in the test chip. We want to integrate the proposed transceiver and the AFE circuit into a single chip. Thus, the transceiver can perform in a single chip without external AFE board.

Finally, in order to improve the BER performance, the error correction mechanism must be adopted. Thus, the bit error in the recovery data can be corrected, and improve the raw BER.

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