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資訊工程研究所碩士論文

建構於可程式邏輯板之人體通道傳輸收發器設計

An FPGA-based Transceiver for Human Body Channel Communication Applications

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An FPGA-based Transceiver for Human Body Channel Communication Applications 建構於可程式邏輯板之人體通道傳輸收發器設計

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摘要

現今可攜帶式的醫療裝置隨著人口老化的情況加劇而有了快速的發展，一般而言，像是藍芽或紅外線此類無線傳輸的方式是透過無線射頻來傳輸資料，但是這種傳輸方式只能提供低速的資料傳輸，而且通常伴隨著較大的功率消耗。除此之外，如果附近有相近的頻段在使用的話也會影響無線射頻的傳輸。因此，另一種人體區域網路的概念開始被重視，也就是人體通道傳輸，此種傳輸方式是利用人體的皮膚當作傳遞的介質，相較於無線射頻的傳輸方式，這種方式傳輸更加穩定而且功率消耗也比較低，同時對於環境周遭的干擾比較無感。

在本篇論文中，我們先探討了人體通道傳輸的特性，為了要設計出合適的人體通道送收器，我們做了很多的人體量測，根據不同頻率以及傳輸距離的測量結果建立了人體通道模型。另一方面，當訊號經過人體後會產生衰減的情況，因此我們設計了一張 AFE PCB 板子來處理這個問題，利用前端的放大電路來放大衰減後的訊號，再使用 Schmitt trigger 來將訊號切回原來的方波。

在我們提出的人體通道送收器的架構中，主要包含了一個傳送器、一個人體通道、一個 AFE PCB 板子以及一個接收器。為了將人體通道送收器實現在 FPGA 的平台上，傳送器和接收器的電路都會燒錄到 FPGA 中。在傳送端的部分，外部的訊號會先透過 UART 介面傳送到 FPGA 中，接著訊號再經過 NRZI 編碼後，以封包的格式一個一個傳出。在接收端的部分，經過人體後衰減的信號會使用 AFE PCB 板子來還原。之後接收器再回復成原本的資料以及時脈，最後用 UART 介面將資料回傳給電腦。總結來看，我們成功的將人體通道傳收器實現在 FPGA 的平台上，並且可以順利的進行資料傳輸。

關鍵字:人體通道傳輸、人體通道特性、可程式邏輯板、通用非同步收發傳輸器

Abstract

Nowadays, portable healthcare devices are developed rapidly because of the aging of population. In general, wireless communications based on radio frequency (RF) transmit data through the air like Bluetooth and ZigBee. However, this type can only transmit the data in a low data rate and consume relatively high power. In addition, RF transmission is sensitive to the interferences in nearby environment. Consequently, another type of BAN is suggested. Body channel communication (BCC) uses the human body skin as a transmission medium. Compared to the RF transmission, it is more stable and less power attenuation. Moreover, it is less insensitive to the interferences in surrounding environment.

In this thesis, the body channel characteristics are first discussed. We do lots of measurements to realize the characteristics of the HBC and develop a proper BCC transceiver. Thus, the human body channel model can be built up according to a variety of measurements with different transmission frequencies and distances. However, human body transmission would attenuate and add interferences to the transmitted signal. Therefore, an AFE PCB board which consists of a voltage gain amplifier (VGA) and a Schmitt trigger is used to amplify and recover the attenuated signal from human body back to ordinary square waveform.

In our proposed BCC design, the transceiver is mainly composed of a transmitter, a human body, an AFE PCB board and a receiver. Both the transmitter and the receiver are downloaded to the FPGAs such that we can accomplish the BCC transceiver in the FPGA platform. In the transmitter part, the external signal will be first transmitted into the FPGA board via UART. Subsequently, the signal is encoded

as NRZI signal and then outputs in the packet format. In the receiver part, the attenuated signal from human body is recovered by the AFE PCB board. Later, the receiver recovers the clock signal and data. In the end, the data are sent to the computer via UART. In conclusion, we successfully implement the BCC transceiver on the FPGA platform which can provide a reliable data transmission.

Keywords : BCC, FPGA, UART, Human Body Channel Characteristics

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Chapter 1 Introduction

1.1 An Overview of Human Body Communication

As the growing demand for mobile devices and wearable devices, the requirements to power efficiency and reliable transmission become more important now. Recently, a new type of communication protocol called body area network (BAN) was appeared which was standardized in IEEE 802.15.6 [22]. The task group 6 of IEEE 802.15.6 is formed to deal with specific needs of body area networks. It defines a network access protocol that supports three physical layers. BAN is one of the physical layers that is an emerging technology. BAN can combine health care and consumer electronic applications around the human body. By continuously connecting and sharing the information of mobile devices, it allows convenient usages and application services.

Body channel Communication (BCC) [23] uses the human body as the transmission medium to transmit the electric signals. The idea of this technique is to use electric field rather than electromagnetic wave between the transmitter and receiver as shown in Fig. 1.1. In addition to the BCC technology, there are several RF-based technologies that can be used to communicate in a short distance. Bluetooth is one of a short-range, high data rate communication way. It enables point-to-point connection between devices and is widely used in mobile products.

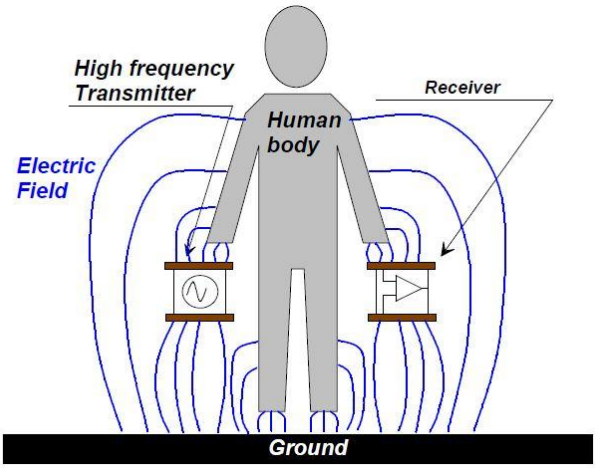


Fig. 1.1: Principle of near-field intra-body communication [1]

Zigbee is a low data rate communication which is usually adopted in monitoring and controlling applications. The frequency range of BCC is much lower than typically considered for RF devices. The RF devices usually use 2.4GHz and 5GHz frequency bands. Frequency below 100MHz is of interest for BCC. At frequencies above 100MHz, the carrier wavelength approaches the length of the human body. Consequently, the human body will act as an antenna [24] and the communication is no longer limited to the human body. Also, the radio wave-based methods are susceptible to interferences and can not connect between many computers without decreasing speed. Besides, the unique features of intrabody communication are that the data can be exchanged by unconscious actions such as touching or stepping. In addition, data transmission through human body can provide secure transmission without intercepting by hackers. Compared to RF transmission, it is more stable and has less power attenuation. Moreover, wire-line connections are impractical for BAN because wires are so easy to be tangled. Thus, BCC is prepared for short-range wireless communication.

Despite benefits of body channel communication, there are some issues should

be taken into account. If someone wants to enable reliable wireless communication between portable devices in close proximity to the human body, the body influence on the propagation of transmitted signal must be considered. Moreover, transmission distance, signal frequency have a great impact on body channel communication. With a long-term research on BCC, there are varieties of body channel communication applications [5-6] such as secure systems, medical information systems, production management systems and payment systems. As shown in Fig. 1.2, some promising applications like ticket gate for the train station that allows passengers to pass efficiently. Furthermore, a medical information system can allow a doctor to gather information from body sensors with a simple touch.

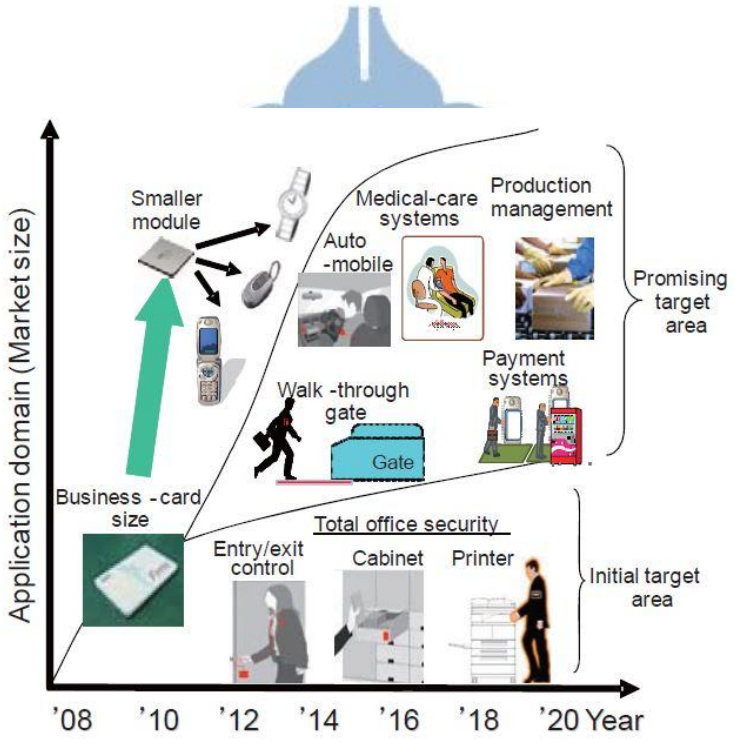


Fig. 1.2: Applications and future directions of BCC [2]

1.2 Body Channel Communication Transceivers

1.2.1 Wide-Band Signaling BCC Transceiver

A system is featured for wideband if the frequency bandwidth exceeds the coherence bandwidth of the channel. In contrast, the bandwidth of narrowband does not exceed the coherence bandwidth of the channel. A wideband transceiver [19] is introduced in this section. Rather than use a 50Ω as an input resistance for the RX, the transceiver applies high resistance to allow RX to sense the signals within 1 to 30MHz band in order to avoid the FM band. Moreover, a novel correlation-based RX is used to get rid of the attenuated signal. The architecture of the transceiver is shown in Fig. 1.3. A Manchester encoding is applied in the TX such that at least one voltage transition exists in each bit time. The electrodes are shorted for a while per bit period and the state of DC level of the amplifier is revived. The input resistance is very high and the input signal is enlarged for the rest of period. This method overcomes low-frequency interferences. To attenuate the high-frequency interferences, the bandwidth of the LNA is limited to 30MHz. Nevertheless, the maximum data rate of this transmitter is 8.5Mb/s that is not enough for the multimedia transmission.

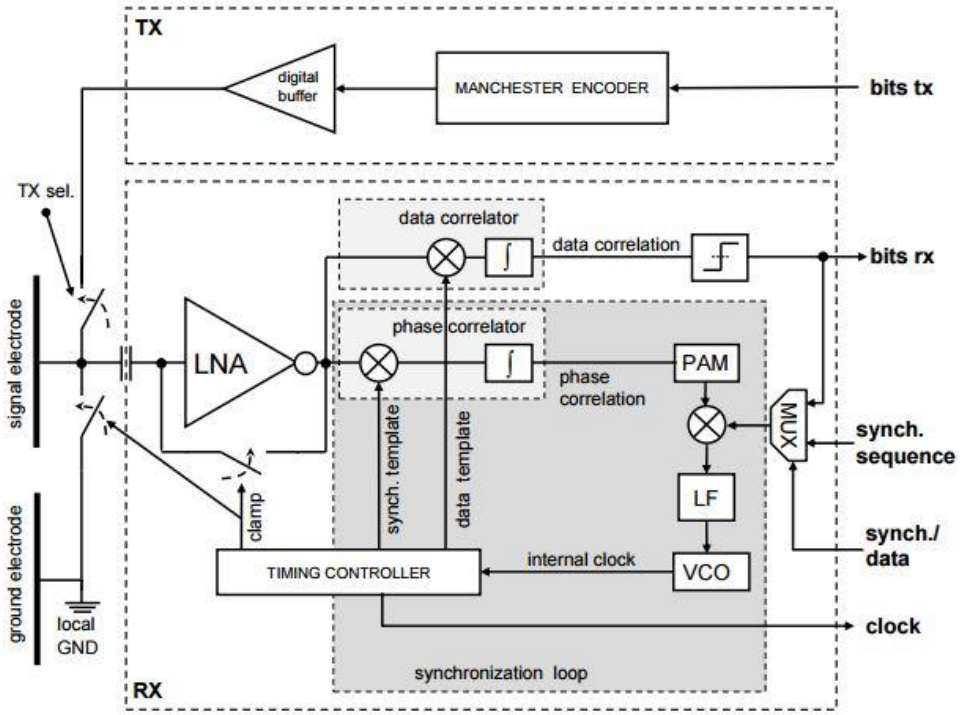


Fig. 1.3: Architecture of transceiver for body channel communication [19]

A WBS transceiver which has high data rate, great jitter tolerance and low power consumption is proposed in [20]. The transceiver applies spread spectrum clock generator (SSCG) in order to reduce the effect of EMI. Besides, the NRZI encoder encodes the data with more data transition so as to recover the data correctly in clock data recovery (CDR). In this receiver, it adopts the 7X oversampling CDR architecture with a voting mechanism.

Fig. 1.4 shows the architecture of the WBS transceiver [20]. The transmitter consists of a SSCG, a linear feedback shift register (LFSR) and a non-return to zero inverted (NRZI) Encoder. The source clock can be either external clock or the spread spectrum clock signal (SSCG_CLK) to trigger the LFSR circuit. Similarly, the transmitted data can be either external data or TX_DATA. Subsequently, the TX_DATA is encoded by the NRZI encoder. Before transmitted into human body, the

bit stuffer performs bit stuffing to limit the maximum value of continuous identical digits (CID) to 5 bits. In the receiver part, the WBS receiver is composed of an analog front-end (AFE) circuit and a CDR circuit. The signal from the human body is amplified by AFE circuit and recovered back to the digital waveforms. In the end, the CDR circuit outputs the data clock (RCLK) and data (RX_DATA).

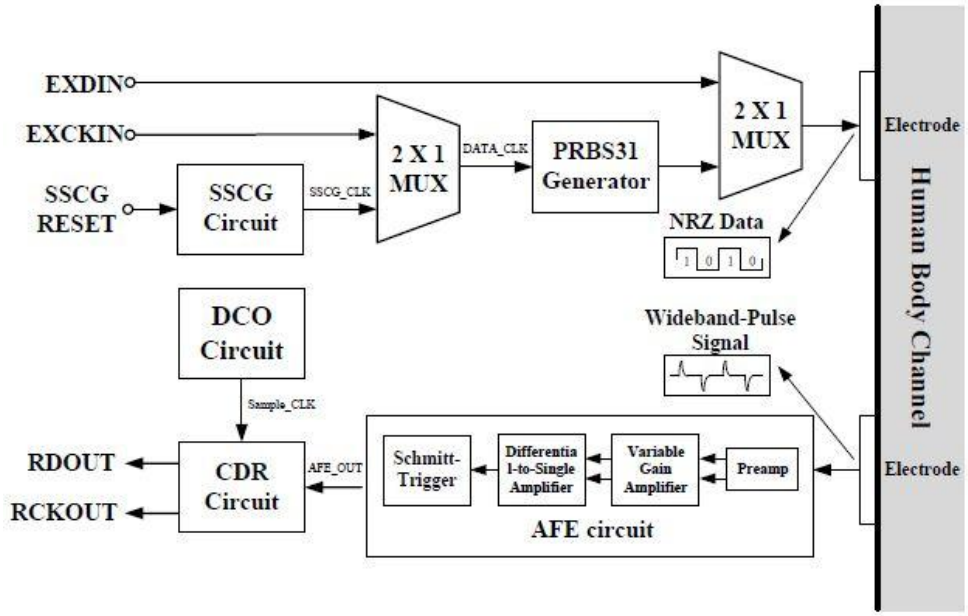


Fig. 1.4: The WBS transceiver and the CDR circuit [20]

Fig. 1.5 shows the illustration of another BCC receiver [21] and the time and frequency domain of signals. A two or three-level transmitted NRZ signal is sent and is received by an electrode of RX. The differentiator outputs the pulses (VDIFF) according to the amplitude of high or low data transition in order to generate the 80MHz frequency in the received signal. Subsequently, a squarer circuit converts the pulses to a single polarity (VSQ). These pulses are sent into an injection-locked ring oscillator (ILO) and output a signal at 160MHz. The signal is re-timed and transmitted to the analog front-end and the demodulator circuit as well as to the digital baseband to recover the data. Therefore, the CRC architecture and injection-locking scheme

remove the need for a PLL and a reference signal. However, the supply voltage is 1.2 V which is higher than other BCC transceivers in 65nm CMOS process.

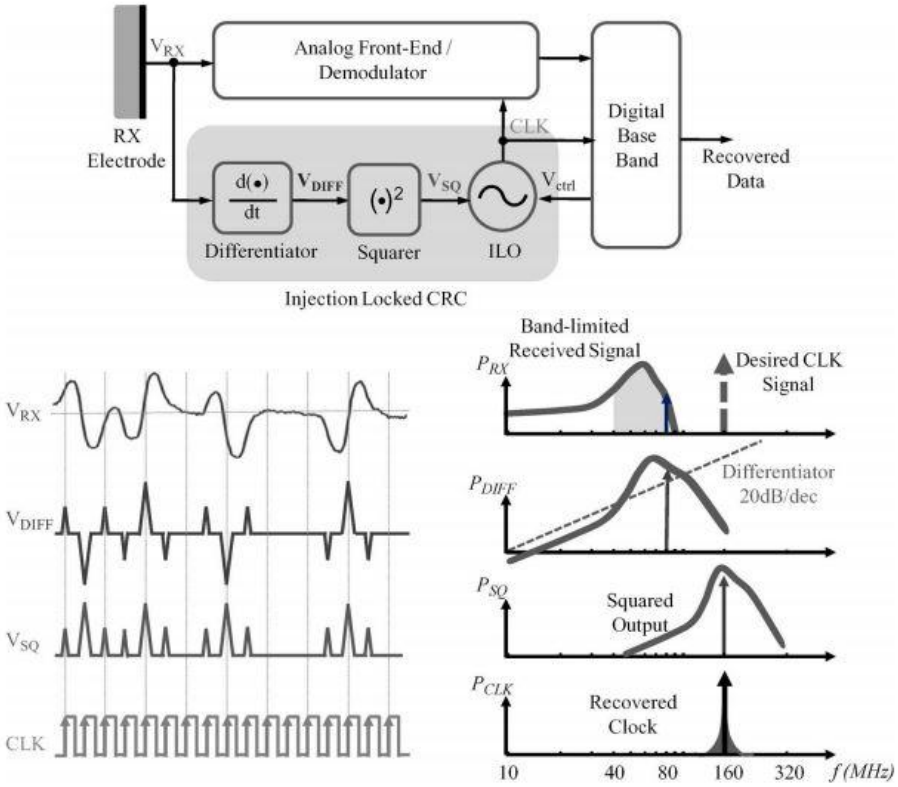


Fig. 1.5: Architecture of body channel receiver with time and frequency domain [21]

1.2.2 Frequency-Shift Keying BCC Transceiver

Frequency-shift keying (FSK) is a kind of frequency modulation technique which is often utilized for communication systems like emergency broadcasts. Binary FSK (BFSK) is the simplest modulation from FSK that applies discrete frequencies in binary information transmission. In FSK, “1” is called the mark frequency and “0” is called the space frequency, respectively.

The architecture of the BCC transceiver [13] is a simplification of traditional FSK transceiver with the help of the reuse of phase-locked loop (PLL). The TX applies open-loop direct VCO modulation and the RX utilizes close-loop PLL demodulation. The block diagram of the transceiver is shown in Fig. 1.6 . Firstly, a command is sent from the host which is then received by the sensor node. Once the instruction is received, the sensor node sends the data. To simplify the circuit, different operations are executed with one identical PLL. Generally, FSK demodulation can be achieved by the PLL circuit. The FSK signal is delivered to the phase and frequency detector (PFD). Voltage controlled oscillator (VCO) gets the baseband pulse as soon as the PLL locks. Then, FSK signal is demodulated.

The TX is composed of a PLL, an open loop control (OCL) and an output driver. Two steps will be executed during the transmission. The first operation is close-loop frequency calibration. In this step, signal CP_EN and B1 are set to 0 which leads to the closed loop. A frequency signal is chosen by MUX and later transmitted to the PFD. The calibration of the VCO frequency is performed as long as the PLL locks to F_{cal}. Moreover, the control voltage is always kept in the loop filter. The second operation is open-loop data transmission. In this step, signal CP_EN turns to “1”. Meanwhile, signal B1 turns to ‘1’. As a result, the output frequency of VCO is modulated by Vt2, which is controlled by signal TX_in. Vt2 is set to a constant

voltage V0 if TX_in is “0” while Vt2 is set to another constant voltage V1 if TX_in is “1”. The RX consists of a front-end amplifier (FEA), a PLL-based demodulator and comparator. The FEA enlarges the modulated signal which is then selected by MUX. The signal is demodulated to a baseband voltage after the PLL locks. Later, the demodulated signal is quantized and recovered as signal RX_out. However, 400kbps data rate is not enough for most of the BCC applications.

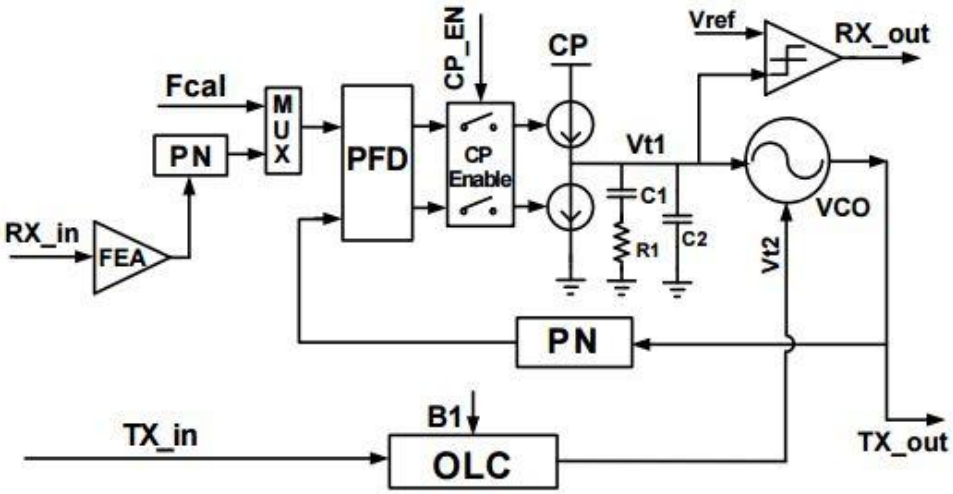


Fig. 1.6: Transceiver architecture of BCC [13]

Low power and low noise are becoming more and more important in recent wearable devices. An ASIC circuit features low frequency, low noise and low power (3Ls) for BAN applications is presented in [14]. The architecture of the proposed design and the relative test bench are depicted in Fig. 1.7. To achieve the purpose of low noise, an analog front-end (AFE) is adopted which contains a low noise preamplifier and a filter. The preamplifier exploits a large PMOSFET pair to make lowering input referred noise. Besides, a 12-bit ADC is employed to digitize the signal. The comparators in the ADC are utilized to decrease the power consumption. Similarly, ARM7TDMI microprocessor is applied to the circuit which is known for its

low power consumption.

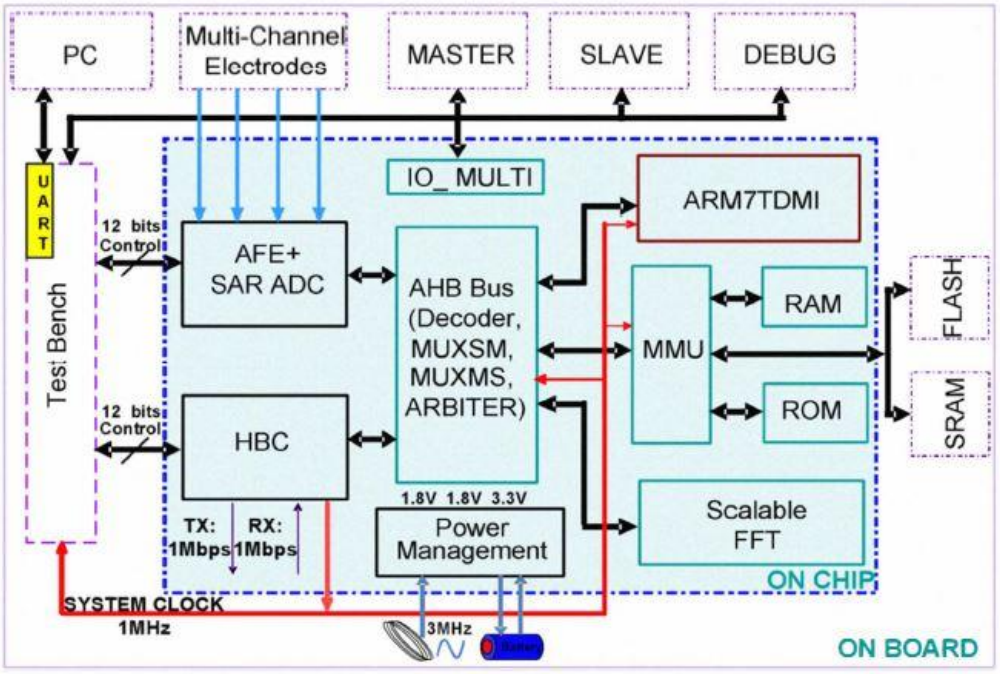


Fig. 1.7 Architecture of the 3Ls ASIC and the FPGA-based test bench [14]

A wake-up receiver which exploits the injection-locking ring oscillator (ILRO) rather than RF amplifier to decrease power consumption is proposed in [15]. The modulated signal is amplified and then demodulated by the PLL-based FSK demodulator with the help of ILRO. In addition, the auto frequency calibrator (AFC) will compensate the frequency error if the temperature variation or leakage current occurs. Fig. 1.8 shows the overall architecture of the ILRO based wake-up receiver [15]. It is made up of a LNA, ILRO, PLL-based demodulator and an 1-bit ADC. The receiver performs in two operation mode. In the wake-up receiver mode (the SW1 is turned on and SW2 is turned off), the signal coming from the electrode is amplified by the LNA and then converted by the ILRO. I_{ref} is the current of ILRO to prevent frequency drift by temperature variation. Later, ILRO outputs the signal that is transmitted to the PLL-based demodulator. There are a PFD, a charge pump, a loop

filter, a VCO and 1-bit ADC in the demodulator. The modulated signal (f_{ILRO}) is demodulated and then quantized by the 1-bit ADC. Finally, the signal is recovered back as RX data. In the auto-frequency calibration mode, the SW2 is turned on and SW1, LNA, VCO and 1-bit ADC are turned off. The frequency (f_{cal}) is transmitted to the PFD so as to calibrate the frequency of the ILRO to get rid of the effect of temperature variation. After the calibration is completed, the SW2 is turned off for the sake of not changing the control voltage of ILRO during wake-up operation. The analog buffer and capacitor are applied to cut down on the voltage variation. Although it performs in low power consumption, the maximum data rate is merely 200 kb/s.

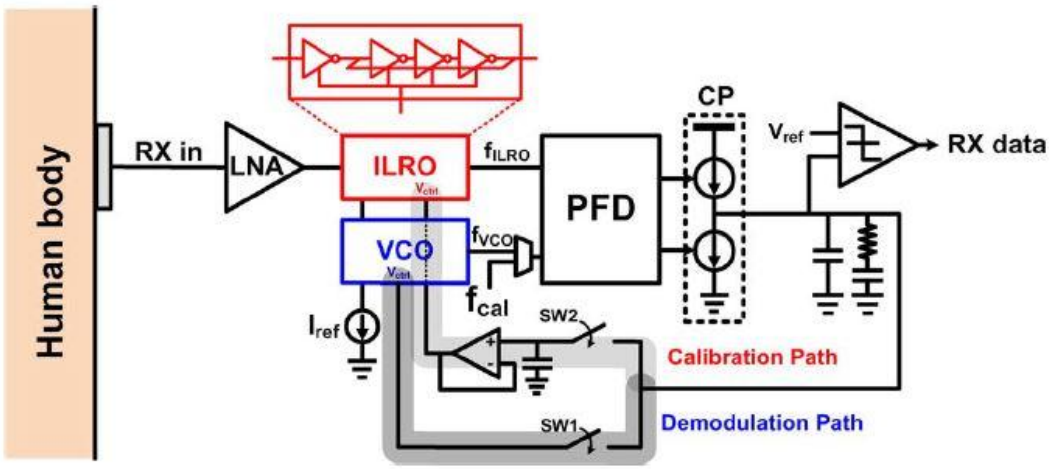


Fig. 1.8: Overall architecture of the proposed ILRO-based wake-up receiver [15]

Fig. 1.9 shows the operation mode of the ILRO-based wake-up receiver [15] in the time domain. The main receiver is turned on while the wake-up receiver is turned off in order to decrease the power consumption. The auto-frequency calibration period is set to 10 second so that the receiver will turn on periodically to calibrate the frequency. The last calibration is done and then all wake-up receivers are turned on to be ready for the incoming command before main receiver turns into the sleep mode.

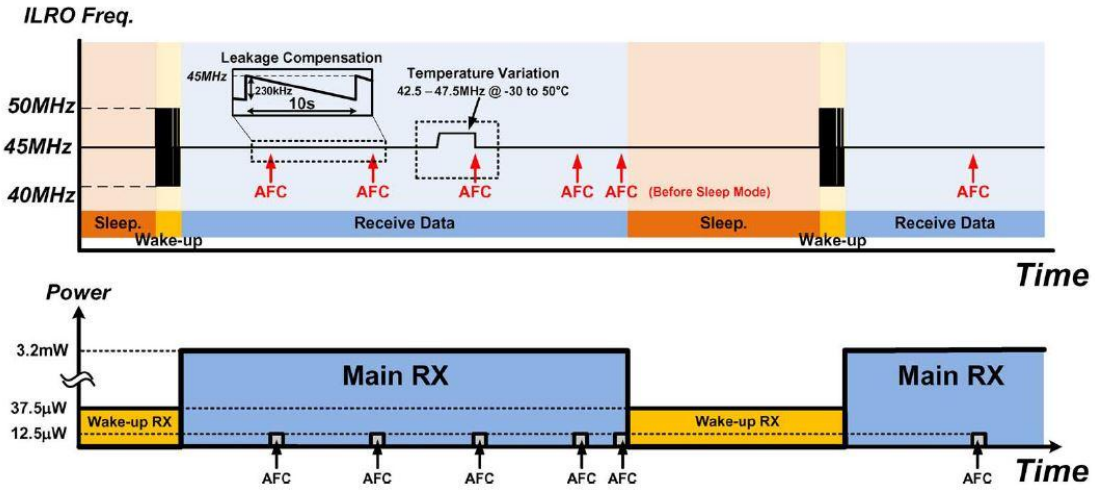


Fig. 1.9: Wake-up mode and frequency calibration mode operation [15]

To deal with the effect of body antenna, the transceiver applies a four channel adaptive frequency hopping (AFH) technique which is performed at 30 to 120MHz band and is proposed in [17]. The transceiver is mainly composed of a direct switching FSK modulator, DLL-based demodulator and an AFH controller. Fig. 1.10 shows the frequency scheme for AFH. First, the frequency band from 30MHz to 120MHz is partitioned into four channels. Initially, four channels are considered to be available. By computing the success ratio of packet transmission, all the channels are monitored repeatedly during the frequency hopping. In the case presented in Fig. 1.10, channel 3 is interfered by another signals. The channel controller is responsible for discarding the channel 3. The remaining available channels are prepared for the next hopping.

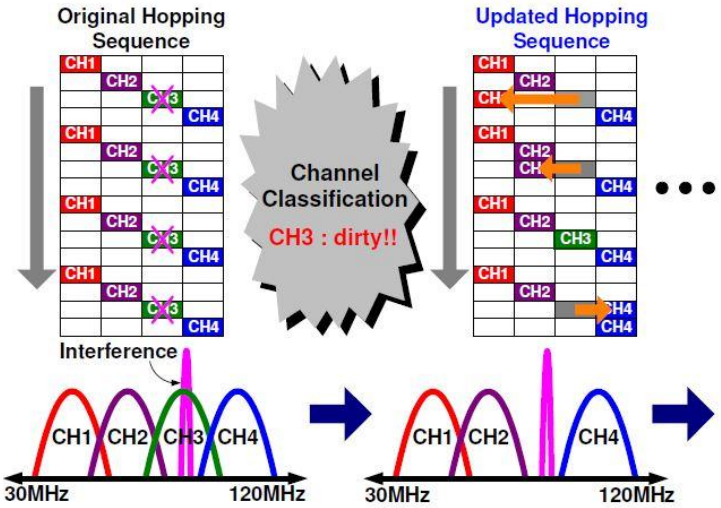


Fig. 1.10: Illustration of adaptive frequency hopping scheme [16]

The architecture of the AFH transceiver is presented in Fig. 1.11 [17]. A medical electrode is attached to the human body for signal transmission. Then, the signal from the external environment is suffered from interferences because of the body antenna effect. After that, the attenuated signal is amplified by the LNA and down-converted by the I/Q mixers. In addition, the limiter is used to digitalize the filtered signal and the DLL-based demodulator is utilized to demodulate the FSK signal. In the transmit path, the signal from the digital baseband is modulated with 10Mb/s FSK and applied to the human skin through the single electrode.

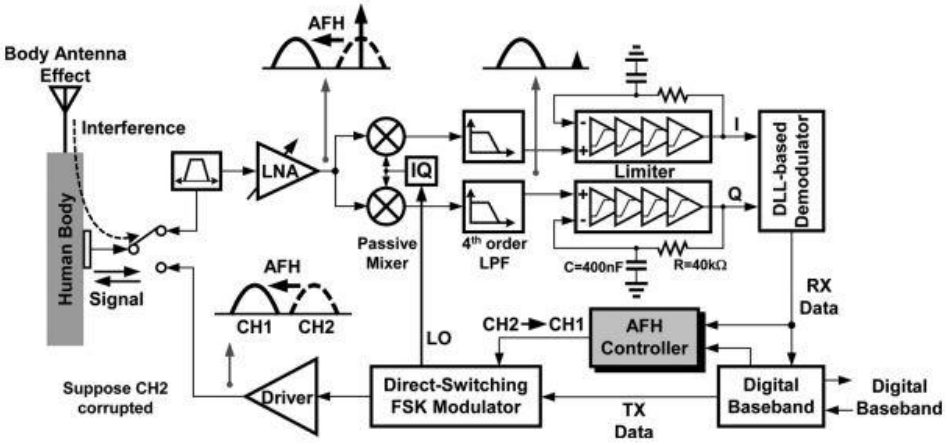


Fig. 1.11: AFH BCC transceiver architecture [17]

Similarly, another BCC transceiver which also applies a variable adaptive frequency hopping is presented in [18]. The transceiver provides both the 30 to 70MHz body channel communication and the 402 to 405MHz medical implant communication service (MICS).

The BCC and MICS circuits are executed simultaneously for low power consumption by sharing front-ends. The front-end circuits contain a cascaded LC tank LNA and a conversion mixer. The regulation of MICS divides the spectrum from 402 to 405MHz into 300kHz subfrequency bands. Any modulation technique is able to be applied in any channel as the technique does not violate the MICS regulation. The listen-before-talk (LBT) protocol is implemented for the ten channels to prevent interferences. The AFH in this work changes the data rate and the channel bandwidth according to interference condition for the sake of maintaining the number of available channels larger than a threshold. The number of hopping channels can be varied from 3 to 20 and the data rate can be varied from 5Mb/s to 500kb/s.

The transceiver architecture is shown in Fig. 1.12. Dual-band operation is done by two paths. The LNA and mixer are shared between the BCC and the MICS to reduce power consumption. The antenna of the MICS is attached to the human body like electrode. The channel bandwidth of the signal varies according to the AFH technique. The frequency of the low-pass filter is programmable for the variable AFH. Besides, the integer PLL outputs the LO signals which are used to the mixer. In order to obtain the BFSK signals in BCC TX, the current of the CCO is adjusted depending on the binary data from the digital circuit. In MICS TX, the 16-bit signal handles the division ratio of the fractional-N PLL. The BFSK signal is determined by changing the code value. Large chip area is the main disadvantage of this design.

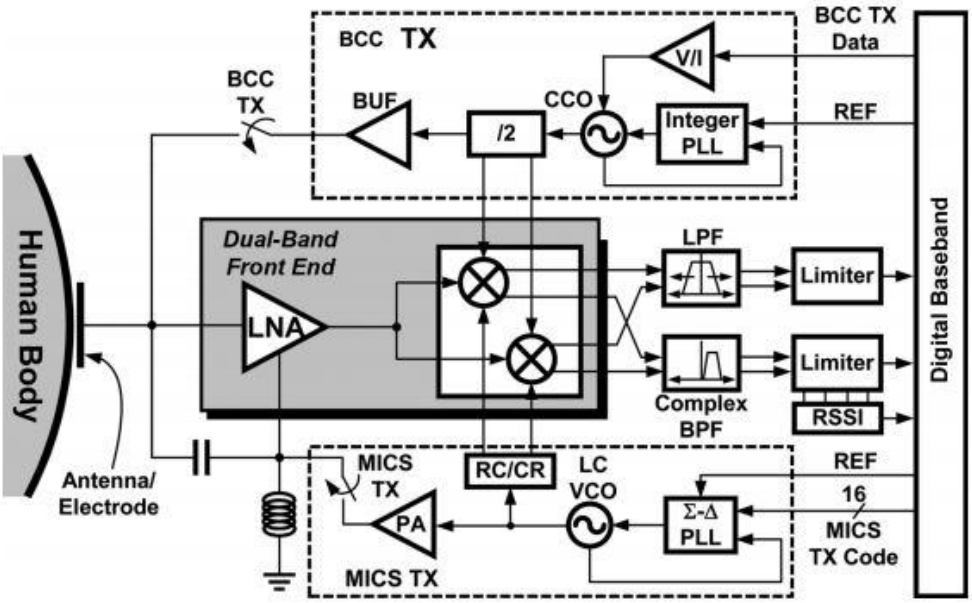


Fig. 1.12: The architecture of the BCC transceiver [18]

1.2.3 Orthogonal Frequency-Division Multiplexing BCC Transceiver

Orthogonal frequency division multiplexing (OFDM) is a modulation technique to digital data on carrier frequencies. OFDM has become a promising scheme for wideband digital communication, which is applied in applications such as television and audio broadcasting. The major benefit of the OFDM against the single-carrier scheme is its ability to deal with the attenuation at high frequencies. In addition, it can be simply implemented to channel conditions without complicated equalization and low sensitivity to timing synchronization errors.

A 16-QAM OFDM is performed in the BCC transceiver [3] to increase the data rate and provide reliability to the transmission. Before the transmission is started, the traditional encoder encodes the data first. According to the channel condition, the modem can select either lower order (QPSK) or higher order (16-QAM) modulation. Later, the signal will be transformed in the form of parallel and make the Fourier transformation. The mechanism is performed and pipelined to reach the goal of timing constraint with the lower supply voltage. Finally, the data will be recovered back to serial. Fig. 1.13 shows the architecture of the OFDM-based BCC transceiver [3]. However, the hardware design is more complex and the FFT occupies large chip area.

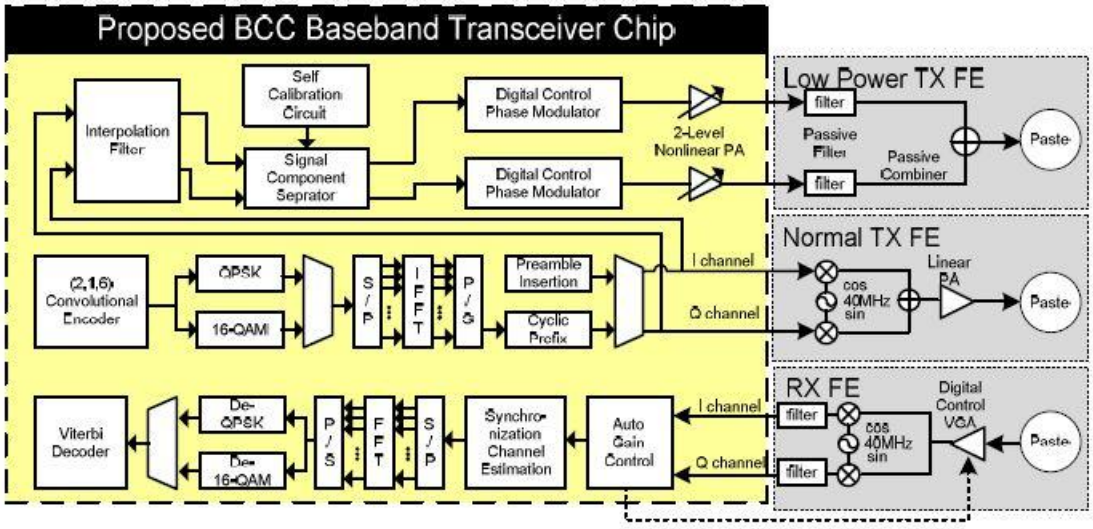


Fig. 1.13: The Proposed OFDM Baseband Transceiver [3]

Despite OFDM-based transceiver has the advantage of high data rate and high spectral efficiency properties, it still derives some drawbacks such as high power consumption and the requirements to the synchronization. The preambles and the cyclic prefix insertions can resolve the demand on the synchronization. On the other hand, high peak to average power ratio and a large number of flip-flops give rise to huge power consumption. Therefore, clock gating and voltage scaling are performed to lower the power consumption.

Another OFDM-based energy-efficient transceiver is presented in [4]. The data is modulated by the OFDM baseband modulator at 10MHz. A linear-phase FIR filter is taken to enlarge the bandwidth of the signal upon 40MHz so as to accomplish the requirement of nonlinear operation. Next, the codewords are determined after the phase calculator computes the required phases and the encoder transfers the phase codewords. In order to seek the mapping parameters for the encoder, a monitor is used to keep track of PVT variations. Then digital-control phase shifters (DCPSs) output phase-modulated signal at the carrier frequency with respect to 40 and 80MHz. Two

digital buffers amplify the two signals before filtering and combining. Fig. 1.14 shows the block diagram of this BCC transceiver [4].

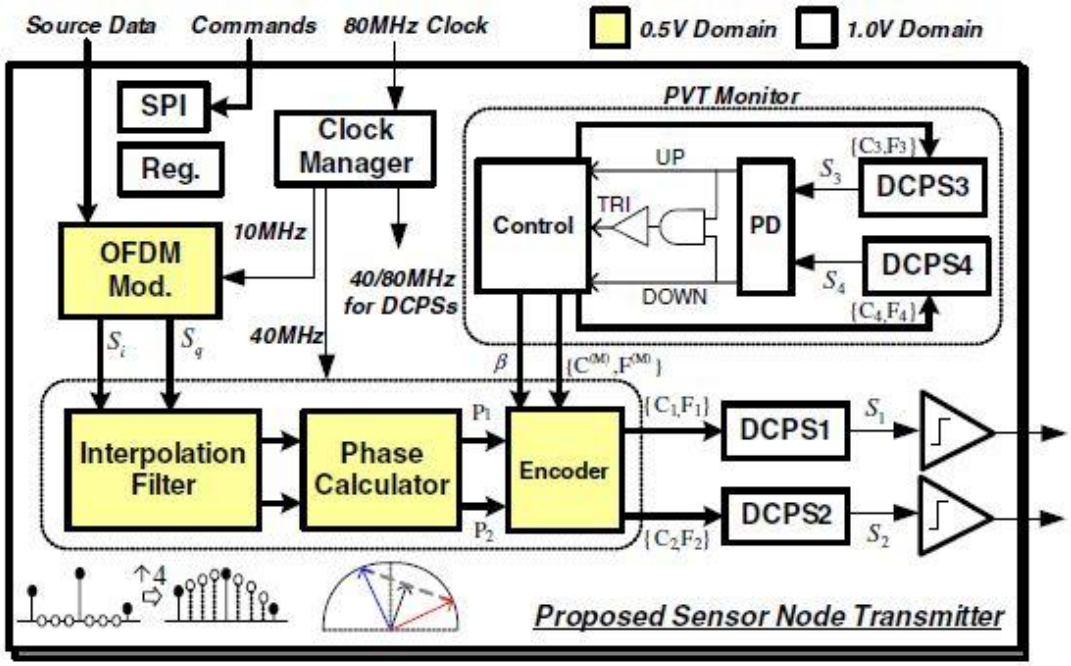


Fig. 1.14: The Chip Block Diagram with Power Domain Partitions [4]

To lower the power consumption, the chip is supplied with two independent supply voltages. Some part of interfaces and controllers are used to communicate with IO pads. The DCPS and the PVT monitor are made to guarantee the accuracy of the circuit. All of them are executed in 1.0V. Besides, the digital signal processing blocks consisting of OFDM modulator, interpolation filter and phase calculator are worked at 0.5V for the purpose of power saving.

1.2.4 Frequency Selective Digital Transmission BCC Transceiver

A BCC transceiver [7] is made for the energy efficiency BCC system with the MAC scheduler and the RSSI channel status monitor. Fig. 1.15 indicates the architecture of HBC transceiver [7]. It makes up of a MAC scheduler, HBC modem and RF transceiver. There are two primary features in the MAC scheduler, which are Duty Cycle Control (DCC) and header generation. The RSSI in the RF module checks the status of the channel in every period, which allows the transmission if a node tries to access the hub. On the basis of the WBAN standard, there are at most 64 nodes allowed to form in a single BAN. To synchronize the sensor nodes and share the accessibility between different nodes, the hub broadcasts a beacon. On the other hand, for the purpose of reducing the area, 11 XNORs and 4 INVs are considered to design the modulator. Maximum likelihood detection (MLD) is applied for Walsh code demodulation such that the modulated data can be mapped into corresponding demodulated Walsh code. In the first place, 16 bits are transmitted into the demodulator and are compared with other 16 candidate codes. The one which presents the most positive comparison result is selected. By this process, the demodulator seeks out the most extremely related 4-bit Walsh code. In addition, the received signal strength indicator (RSSI) allows the MAC scheduler to execute DCC. It constantly monitors the input voltage to determine whether the current body channel is accessible or not. However, this architecture is more complex than other BCC transceivers.

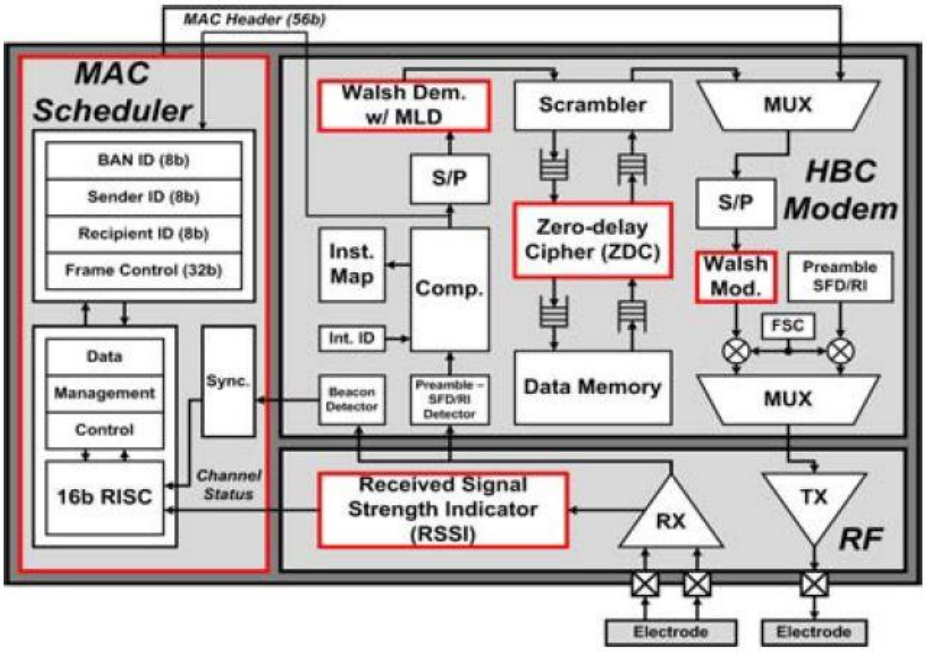


Fig. 1.15: The HBC TRX chip architecture [7]

Nevertheless, a constraint is limited that the maximum data rate of HBC through frequency selective digital transmission (FSDT) is only 1.3125Mbps. To overcome the limitation, a modified FSDT (MFSDT) is proposed in [8]. By adapting the architecture of the FSDT`s transmitter, MFSDT is able to reach a maximum data rate up to 3.9375Mbps. The general FSDT transmitter sends Walsh codes with simply one frequency selective spreader (FS-spreader). In contrast, MFSDT makes use of three FS-spreaders in parallel in order to combine three Walsh codes into one transmitted code to make the data rate three times higher than that of FSDT.

The illustration of the FSDT transmitter is shown in Fig. 1.16 which works at 42MHz clock frequency for a data rate of 1.3125 Mbps. The DIN signal is first transmitted through a serial to parallel converter (S2P) to generate a 4-bit parallel signal. Later, the 4-bit parallel signal is transformed to the corresponding 128-chip Walsh code in FS-spreader to output the DOUT signal.

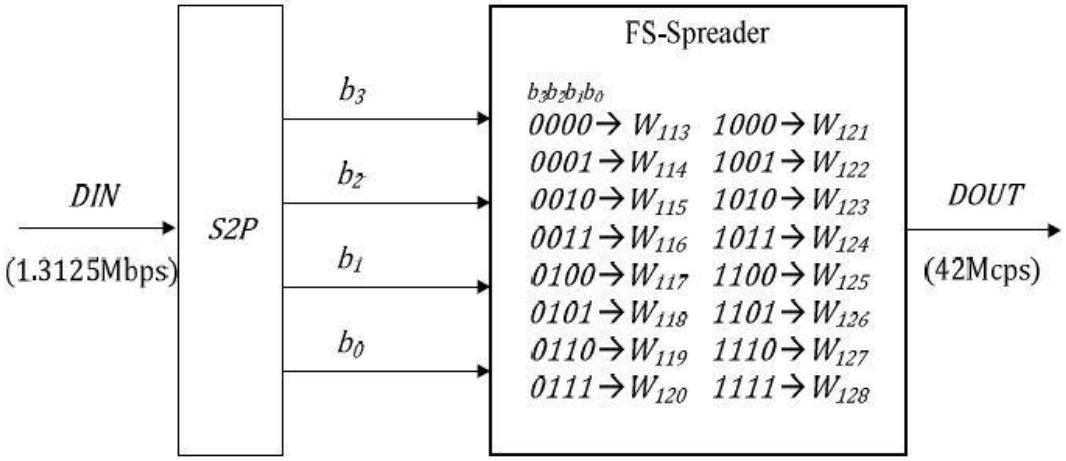


Fig. 1.16: FSDT transmitter implementation for a maximum data rate of 1.3125Mbps [8]

Fig. 1.17 shows the MFSDT transmitter architecture. Compared to the FSDT transmitter, the bit number of the output from S2P and FS-spreader is three times larger than that of FSDT. Moreover, an extra majority selector block is implemented. The MFSDT transmitter achieves a maximum data rate of 3.9375Mbps, which is three times higher than the maximum FSDT data rate of 1.3125Mbps. The 12 bits from S2P are assigned to FS-spreader1, FS-spreader2 and FS-spreader3 respectively. Every spreader includes a 4-bit signal that is mapped to the corresponding Walsh code. $W_{out1,}$ W_{out2} and W_{out3} from the corresponding FS-spreader1, FS-spreader2 and FS-spread3 are merged in the Majority selector according to the following Eq. 1.1:

MDOUT = (W_{out1} and W_{out2}) or (W_{out1} and W_{out3}) or (W_{out2} and W_{out3}) (Eq. 1.1)

On the basis of Eq. 1.1, the majority between a binary 0 or 1 among $W_{out1,}$ W_{out2} and W_{out3} is set as MDOUT. For instance, if W_{out1} = 0, W_{out2} = 0 and W_{out3} = 1, the majority is 0 and MDOUT is set to 0.

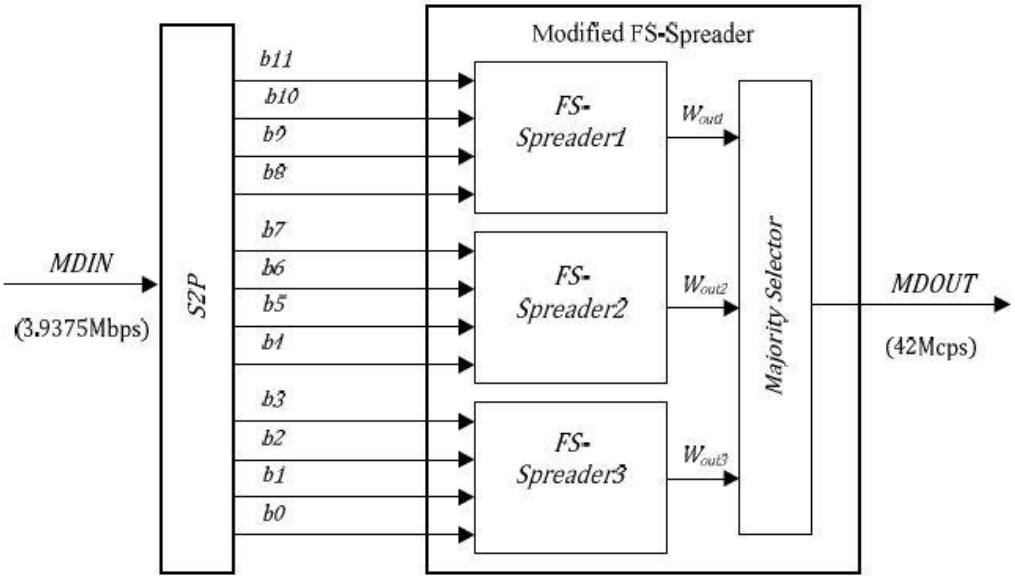


Fig. 1.17: MFSDT transmitter implementation for a maximum data rate of 3.9375Mbps [8]

1.2.5 Phase-Shift Keying BCC Transceiver

Phase-shift keying (PSK) is a kind of modulation which transmits data by adjusting the phase of the reference signal. Some of the digital modulation schemes use different signals to stand for digital data. PSK uses phase which is assigned with a distinct pattern of binary digits. Each pattern of bits forms the symbol that is represented by the particular phase.

Most of the BCC research discussed before utilized simply the frequency band under 100MHz and were only concentrated on the healthcare applications in low data rate or high data rate multimedia entertainments. The channel bandwidth was constrained within 100MHz and the disturbance of FM radio derived from body antenna effect made a serious effect on its performance. Therefore, the BCC transceiver [9] which shows some advantages such as low-energy, dual-wideband and full-duplex is proposed in [9]. First of all, the bandwidth of body channel is increased upon 200MHz and two 40MHz channels are used. One is centered at 40MHz and the other is at 160MHz, which can achieve high-speed requirement for entertainment mode (ET-mode). On the other hand, a RC duplexer is applied to separate each band and carries out the full-duplex operation. In the end, the design can support a maximum data rate of 80Mb/s in ET-mode and provide low power consumption.

Fig. 1.18 shows the block diagram of the BCC transceiver [9] which consists of a full duplex ET-mode transceiver and a super regenerative HC-mode transceiver. The ET-mode transmitter applies a monotonic sinusoidal wave modulation in L-band and can get rid of the harmonics. The dual-band synchronizer uses H-band signal to synchronize L-band signal then the merged data are sent to the human body. The ET-mode receiver applies the BPSK dual-band receiver structure but L-band and H-band share the Q path. No matter which band is in use, the remaining path is turned

off. Both L-band and H-band are combined so as to achieve high data rate in the burst mode. However, the chip area is large and this architecture is also complicated.

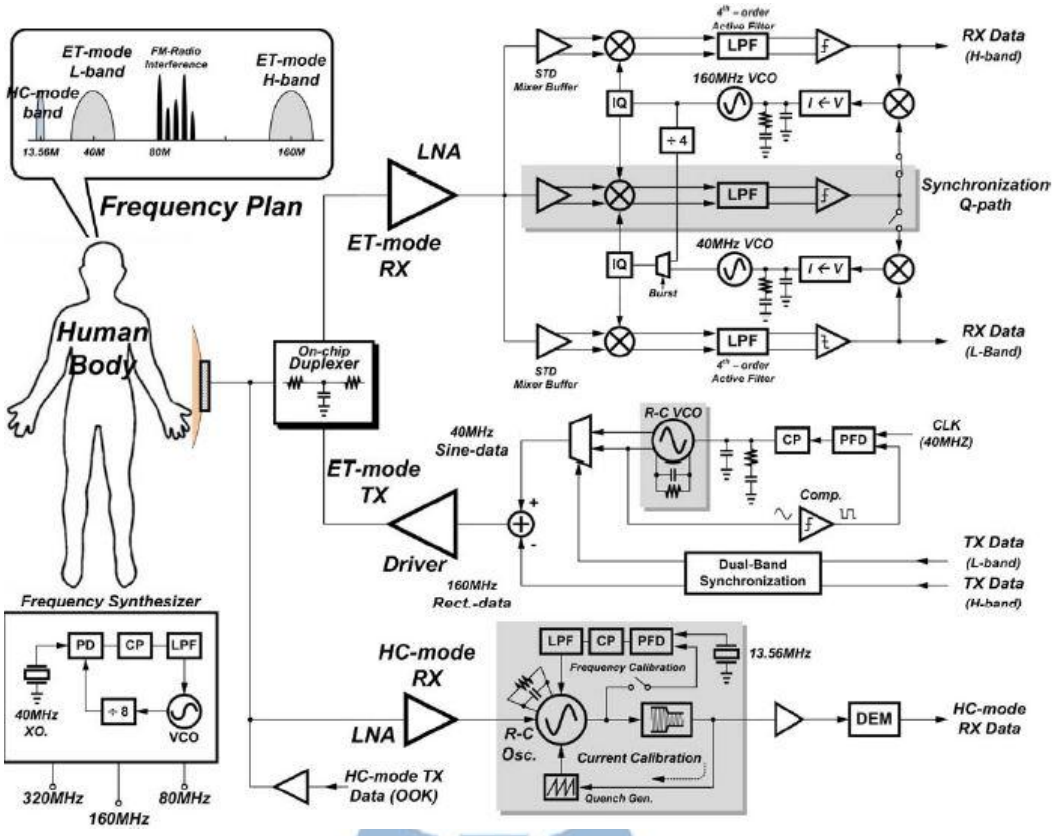


Fig. 1.18: Overall architecture of the BCC transceiver [9]

A QPSK modulated design of galvanic coupling IBC is presented in [10]. In fact, there are two coupling methods for IBC, capacitive coupling and galvanic coupling. In galvanic coupling, the current is coupled into the human body with corresponding electrodes of the transmitter and the receiver. The galvanic coupling performs greater quality of transmission than capacitive coupling. Therefore, it is indicated that galvanic coupling IBC can provide great effects on healthcare devices. The hardware design is accomplished in FPGA devices. The verification of timing constraint and function is done with ModelSim and Quartus II.

A simplified block diagram of the QPSK modulator is illustrated in Fig. 1.19.

QPSK is a general digital modulation scheme in which the phase of the sinusoidal carrier signal is varied in accordance with the value of the symbol to be transmitted. In the QPSK modulator [10], a sequence of data is assigned to a different stream. On the basis of regulation, odd-bit-stream is for I channel and even-bit-stream is for Q channel with the help of Serial-to-Parallel Converter (SPC). The filter filters the two separated data into bipolar NRZ rectangular pulse signals. The signals of both I channel and Q channel are then modulated by carriers. As the result, an adder integrates two signals together to output the desirable QPSK signal. Nevertheless, the data rate is about 100kbps which is not sufficient to support high speed data transmission.

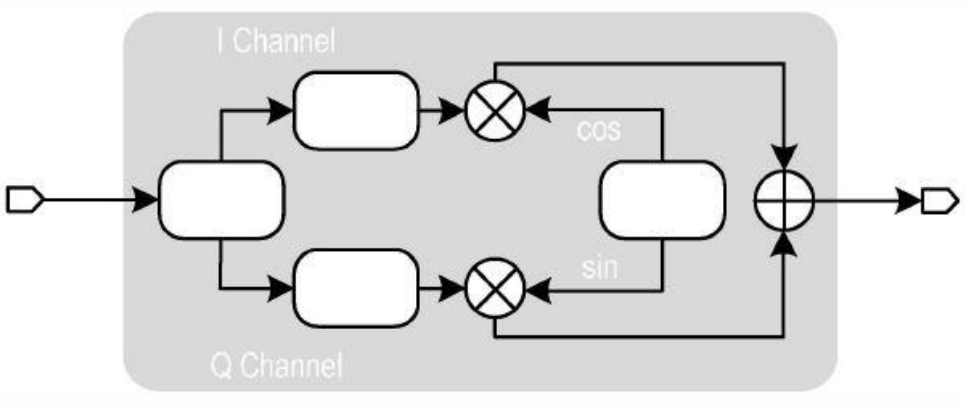
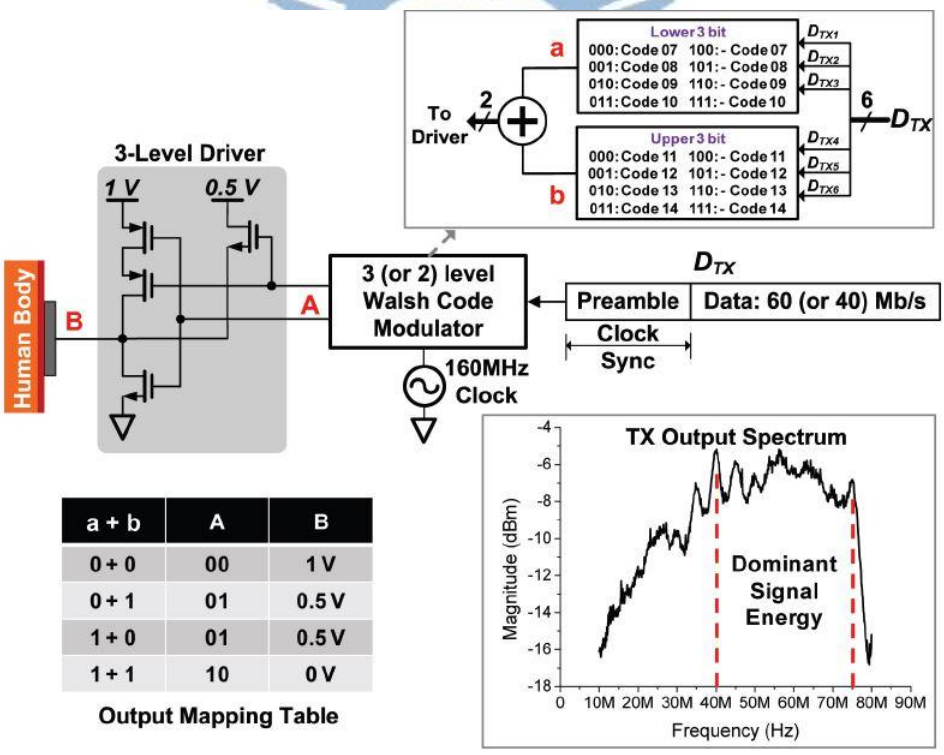


Fig. 1.19: The simplified block diagram of QPSK modulator unit [10]

1.2.6 Walsh Code BCC Transceiver

Many BCC transceivers are utilized in biomedical applications and usually provide a data rate below 10Mb/s. However, it is helpless in multimedia signal transmission for mobile devices due to the low data rate. Therefore, a high speed BCC transceiver features not only high data rate but also low power consumption, which can achieve a data rate up to 60Mb/s is presented in [11]. Fig. 1.20 shows the architecture of the transmitter which exploits three-level Walsh code signaling to increase the data rate and provide less energy consumption. In addition, the transceiver can also be used in two-level Walsh code signaling to deal with interferences in surrounding environment such as FM radio signals. However, the value of SNR is required as high as 18dB which is tough to be realized in the real environment.

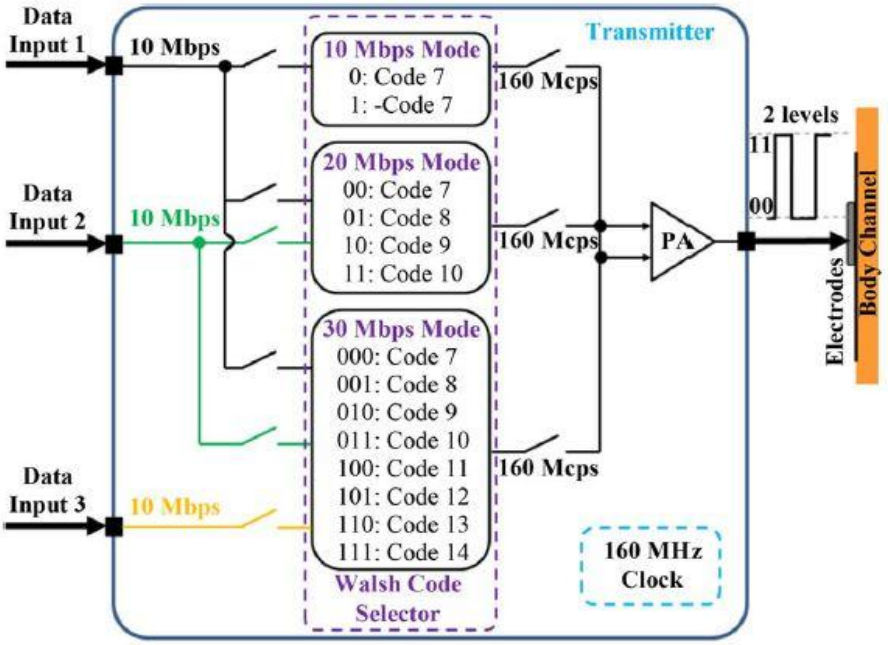


a + b	A	B
0 + 0	00	1 V
0 + 1	01	0.5 V
1 + 0	01	0.5 V
1 + 1	10	0 V

Output Mapping Table

Fig. 1.20: TX structure including the Walsh-code modulator, 3-Level driver and TX output spectrum [11]

In [12], the data is spread with 16-bit Walsh codes before transmitting through a driver. The TX can only utilize Walsh code 7 to 14 because of the limited bandwidth of body channel. In normal operation mode, the TX operates at 160MHz and can provide a data rate of 10, 20 and 30Mb/s. Due to the limitation of the usable Walsh code, the maximum data rate is about to 30Mb/s. For the data rate of 10Mb/s, only one Walsh code is needed. For example, "1" is a stand for Walsh code 7. As for data rates of 20 and 30Mb/s, all Walsh codes are applied to represent multiple data bits. The regulation is shown as Fig. 1.21.

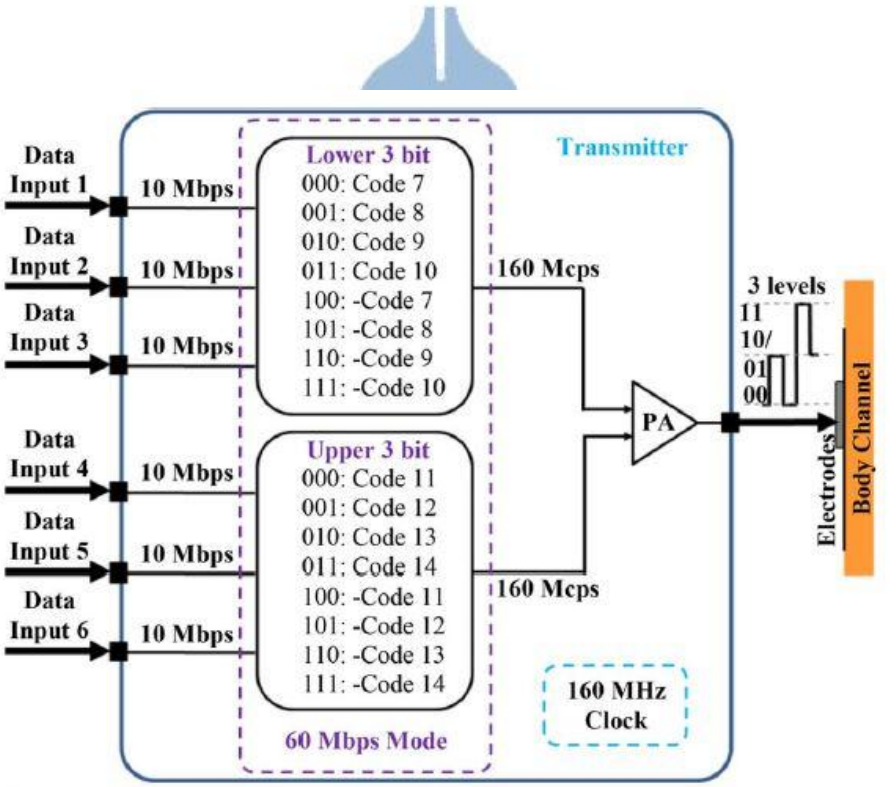


Bits/Symbol	Max Data Rate (Mbps)	Number of Walsh Code Required
1	10	1
2	20	4
3	30	8

Fig. 1.21: The illustration of normal operation mode [12]

High data rate mode is another operation mode in the design [12]. Multiple codes can be stacked on top of one another at the transmitter since the codes are orthogonal. In other words, an amplitude modulated signal can be caused by summing two or

more codes. The technique of stacking codes leads to the higher data rate. The operating demonstration of high data rate mode is illustrated in Fig. 1.22. In the high data rate mode, the system is enabled to support 60Mb/s at 160MHz operating clock. The lower three bits are mapped into code 7 to code 10 while the upper three bits are mapped into code 11 to code 14. Before transmitting into the human body, a power amplifier (PA) is adopted to form a three-level signal. If the input of PA is “00”, it is presented as a low state. In contrast, if the input of PA is “11”, it is presented as a high state. The middle level is formed with the PA input of “01” or “10”. Overall, all of them output three-level signals at the output of the PA. The supply voltage is 1.1V which is higher than other BCC transceivers in 65nm CMOS process.



Bits/ Symbol	Max Data Rate (Mbps)	Amplitude level	Number of Walsh Code Required
3	60	3	8 + 8 inverse

Fig. 1.22: The illustration of high data rate mode [12]

1.3 FPGA-based Body Channel Communication Transceivers

Some BCC transceivers are implemented on FPGA platform. A intrabody communication (IBC) based transceiver is proposed in [5]. The contribution of the work is focused on providing high speed, long distance transmission and synchronization technique.

First of all, two FPGAs are used in the prototype. One acts as the transmitter to store and transmit the audio signal. The other one is used as an IBC receiver for the sake of controlling audio player. The block diagram of the IBC transceiver is shown in Fig. 1.23. The audio signal is transmitted and then stored in the memory of the transmitter. Channel coding module is performed to raise the reliability of the transmission. After some processing of digital blocks, the data are sent into the human body. At the receiver part, the signal is directly recovered by the binary signal recovery and blind oversampling CDR. Finally, the audio signal is transmitted to the chip for music playing.

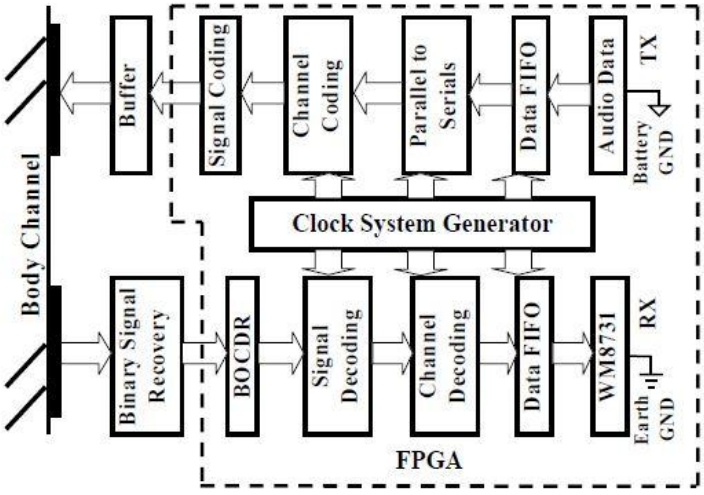


Fig. 1.23: Block diagram of the FPGA IBC audio player [5]

The measurement setup is shown in Fig. 1.24. Due to the requirement of ground isolation, the transmitter is powered by a battery. Touch the corresponding electrodes with two hands to build up the connection. After that, the audio signal is sent and decoded by the chip which is built in the FPGA. The music is played as soon as the receiver detects the audio signal.

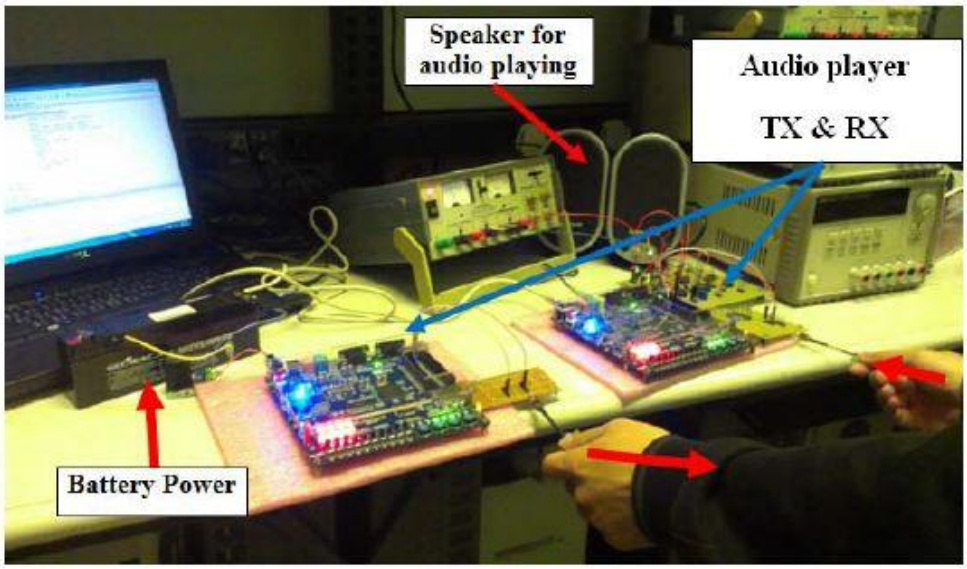


Fig. 1.24: Measurement setup of FPGA IBC audio player [5]

Hearing aids usually make use of RF techniques for the needs of communication even though they consume the relatively high power. A low power BCC communication system for binaural hearing aids is proposed in [6]. Fig. 1.25 shows the top-level block diagram of the binaural communication system [6]. There are three layers in the proposed design which consist of the PHY, media access control (MAC) and the upper layer. The physical link is generated by the PHY layer for data transmission via the skin. MAC deals with data processing and packs the data into frames and then sends to PHY. The upper layer is adopted to contact between the communication module and the controller in the platform.

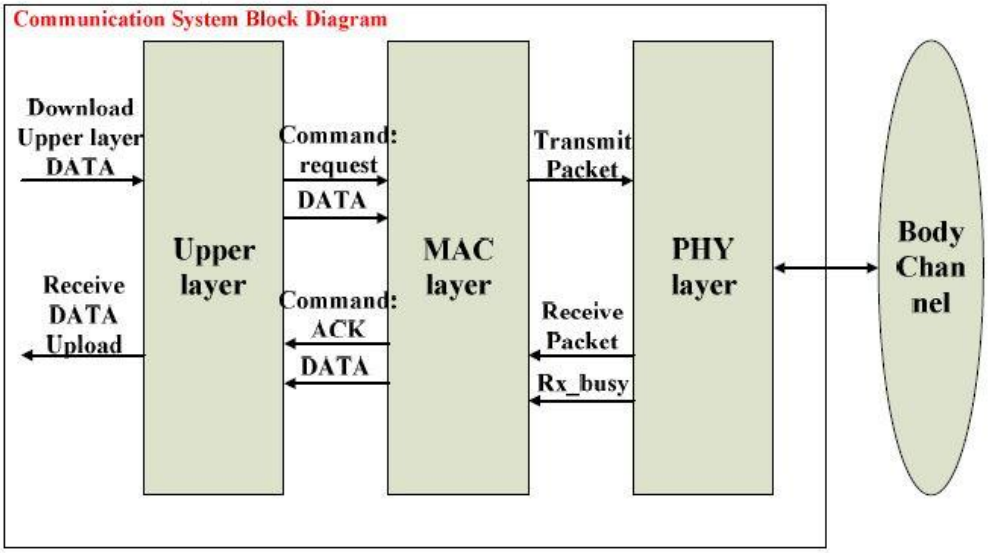


Fig. 1.25 Binaural communication system overview [6]

The circuit design of MAC consists some functional blocks. The TX controller is used to upload and download the data. The RX controller is in charge of de-packing the received frames. Moreover, TX FIFO block stores the data waiting to be sent to PHY while RX FIFO stores the data waiting to be sent to the Upper layer. The compression compresses the voice data to reduce the payload. A prototype is described as Fig. 1.26 to verify the proposed design. The prototype is applied on arms rather than heads because the discrete components are not sensitive as expected. There are two FPGAs as well as analog front-end (AFE) is set up. The audio signal is transmitted from a notebook to a FPGA board. Later the data are sent to the AFE board. With the help of the skin channel, the transmitted signal will be received by the AFE and recovered to be played with speakers.

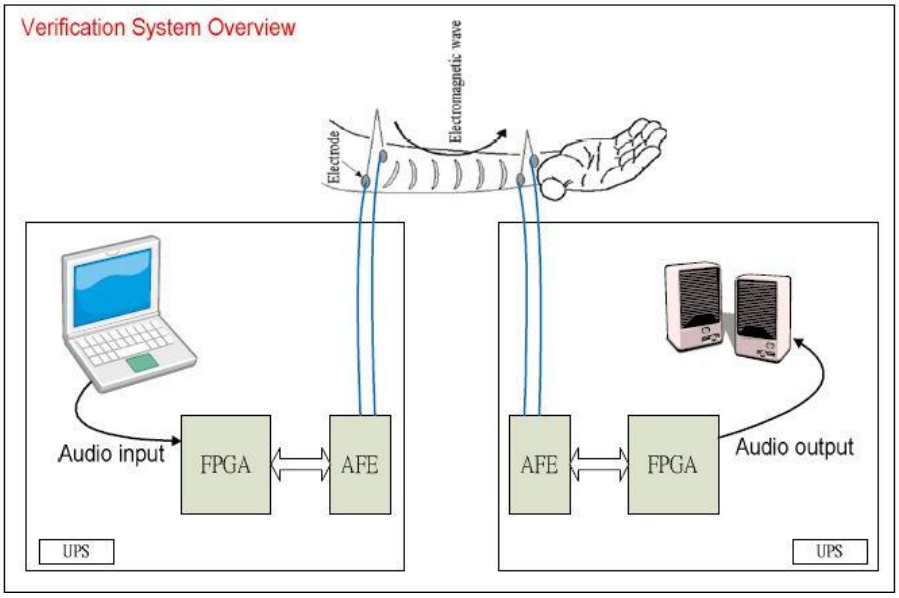


Fig. 1.26 Overview of the verification system [6]

1.4 Motivation

In the paper survey, the biomedical signal transmission in body channel can be performed in a low data rate while a high data rate is essential for multimedia transmission. We can also observe that both frequency and distance play a significant role in body channel communication. Thus, we need to raise the data rate to support multimedia application. In addition, the value of energy per bit can be lower if the data rate increases. On the other hand, body channel communication applications are featured for low power and low noise to provide reliable transmission and long operating time. Therefore, we are eager to develop a platform for body channel communication applications, which is composed of an analog front-end PCB board, two Xilinx Virtex-7 FPGAs (VC707), two personal computers and two circular medical electrodes. The proposed transceiver can support high speed and long distance transmission.

The multimedia signals such as image or audio are first transmitted into VC707 which are located in the transmitter part and stored in the block memory. Once the multimedia data transmission is completed, the user is able to switch on the dip switch. If the dip switch is on, the data stored in block memory would be transmitted to the human body with the help of a single electrode after a sequence of processing and encoding. Due to the effect of body antenna, the transmitted signal through human body will be attenuated. In the receiver part, the AFE board receives the signal from the human body and later amplified by the VGA. Before the AFE board outputs the signal to VC707 which is located in the receiver part, a Schmitt Trigger is performed to recover the signal back to digital waveform. Finally, the BCC receiver in VC707 decodes the data and output the original multimedia data.

In conclusion in this thesis, we design a FPGA-based transceiver which provided long transmission distance and high data rate. In addition, the transceiver is integrated with FPGAs and body sensor equipment to realize body channel communication.

Chapter 2

Experimental Characterization of Body Channel Communication

2.1 Former Research for Body Channel Characteristics

The most important thing to design a body channel communication transceiver is to understand the body channel characteristics. The following works will introduce body channel characteristics. Moreover, a variety of factors such as transmission distance, signal frequency, different human body and motion action would lead to interferences to the HBC. As a result, there are some issues should be taken into consideration before designing the proposed design.

A distributed RC model is generated to observe the properties of the body channel communication in [25]. Fig. 2.1 presents a near-field coupling model of the human body, which is composed of three partitions. The biggest column is considered as the human body and both height and diameter are 140 cm and 30 cm respectively. The remaining two columns are seen as two arms whose diameter and length are 10 cm and 60 cm, respectively. All of the three columns are made up of 10 cm unit blocks. The coupling capacitance (C_C) of the unit block is calculated by

approximating the unit block as the part of a conductive sphere in [25]. A model of the human body can be established by cascading the RC blocks to form the three columns.

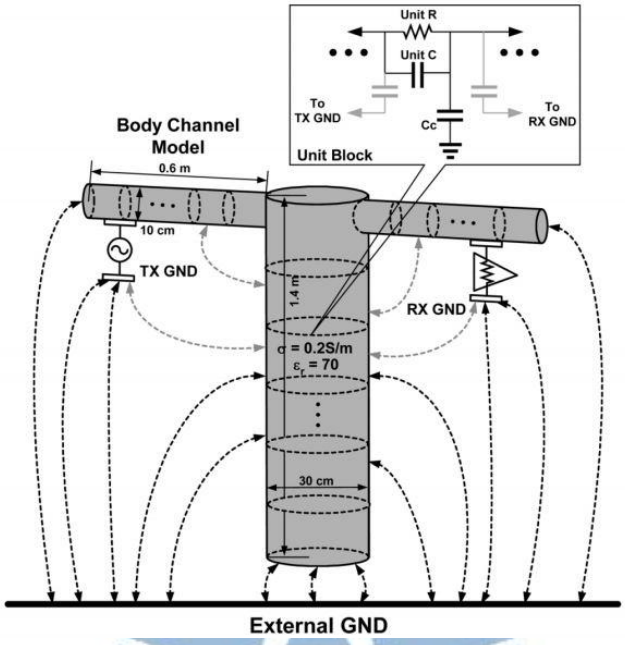


Fig. 2.1: The circuit model of the body channel [25]

Appling high frequency for the body channel communication to derive from better data rate is trivial. However, the variation of the electric field makes human body spread electromagnetic radiation to the environment. The human body acts as an antenna spreading the signal out of the body especially at the high frequencies [32-33]. In order to figure out the ideal frequency range for the body channel communication and least interferences to the RF devices, the measurement of E-field strength is carried out in [24-25]. According to [24-25], the E-field strength raises with the transmitting frequency. Moreover, the radiation range of the transmitted signal is unpredictable.

Generally, both transmitting frequency and distance are the most significant factors to be considered. The high data rate can support multimedia applications while

long distance can provide more flexible communication. As presented in [26], [29], [31] and [35], they analyze the characteristic of the body channel communication at different transmission distance. The transmitting frequency ranges from 1MHz to 100MHz. Fig. 2.2 depicts the attenuation result of body channel.

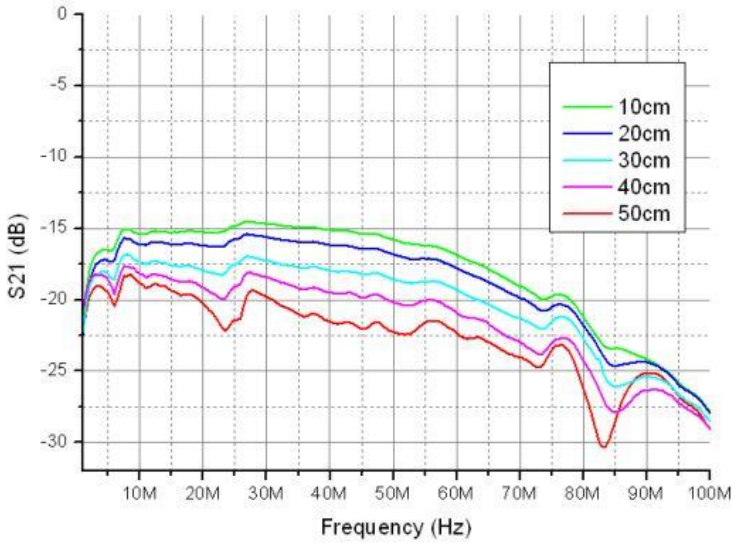


Fig. 2.2: Attenuation curves of body channel with HBC [26]

Due to the measurement results, we can easily observe that the signal power declines as the increase of transmitting frequency. Besides, the longer transmission distance leads to more attenuation to the signal power. From the curved shape of the figure, the band-pass property is shown in body channel communication. The results in the frequency domain are similar to other research. The electrodes also influence the results and the effect with different electrodes will be discussed later.

Body motion is another effect of body channel communication. Fig. 2.3 shows a statistical figure response for the still and motion scenarios when the RX electrode is placed at left arm. In motion scenario shown in Fig. 2.3, the person is walking from 0 to 40s. During 40 and 60s, the person is reading a newspaper; from 60 to 100s, the person is running. We can discover that the signal power has little variations in the

still scenario. On the other hand, different actions cause obvious variation of signal power in motion scenario. With the investigation, we believe that the BCC is almost insensitive to body motions.

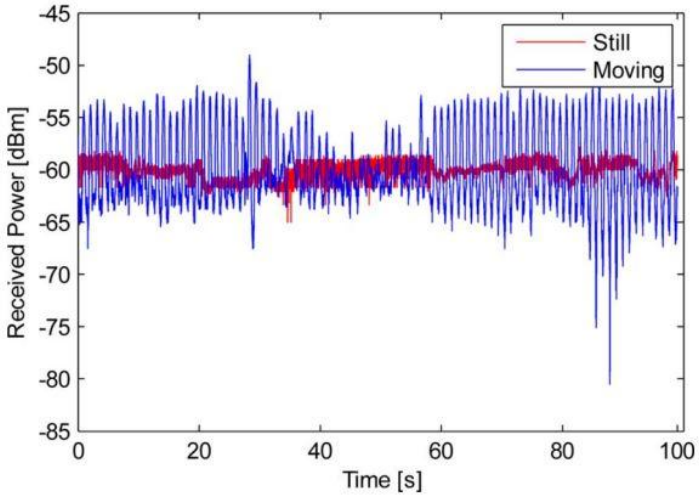


Fig. 2.3: Measurement for still and motion scenarios at RX [27]

Similarly, Fig. 2.4 shows the measurement results of different static motion. The sitting and standing conditions are considered in this measurement. The tendency is no doubt that the signal power decreases as the increase of transmitting frequency. In addition, both sitting and standing conditions achieve a similar result. In summary, we can make a conclusion that body motion is insensitive for HBC.

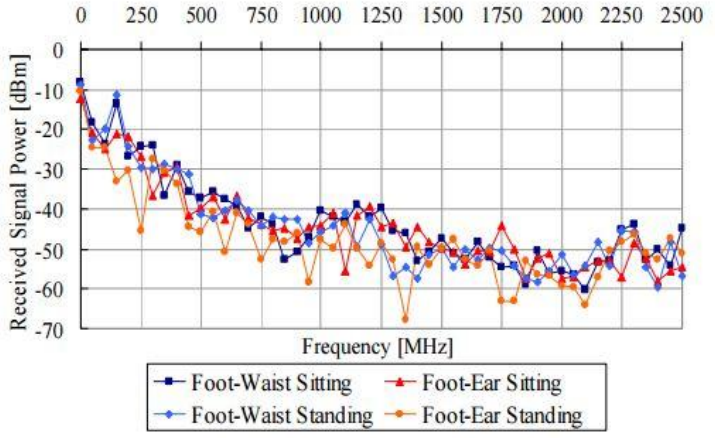


Fig. 2.4: Average received signal power of sitting and standing [28]

To determine whether the electrode material would affect the result of BCC measurement, two kinds of electrodes which mentioned in [29] are used in measurement. The first type is an Ag/AgCl ECG electrode whose area is 1.5 x 1.8 cm^2. The other one is a copper PCB electrode whose area is 2 x 2 cm^2. In both cases, three measurements are performed with a transmission distance of 15cm. Each measurement lasts for 5 minutes for each electrode type. The result is presented in Fig. 2.5.

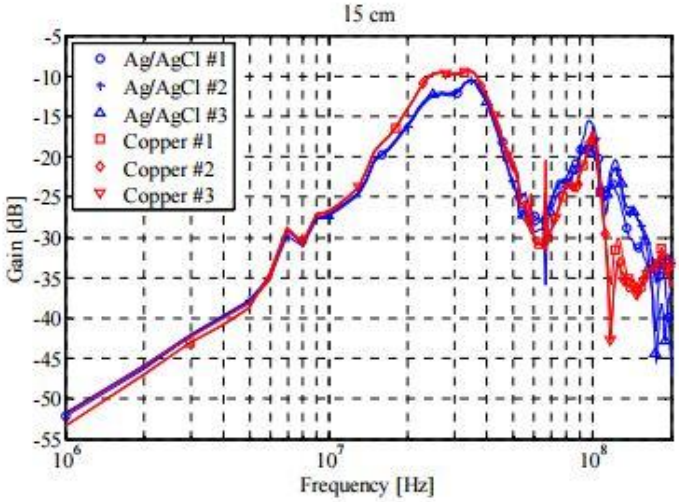


Fig. 2.5: Measurement results for copper(red) and Ag/AgCl(blue) electrode material [29]

Obviously, the difference between the identical material of BCC electrode can be ignored. For different electrode type, there is no significant variation in the band-pass profile and peak frequency. According to the measurement result, the performance of the copper electrodes is merely better than Ag/AgCl electrodes.

There are lots of biomedical characteristics which are the response for the different human body [34]. To figure out the impact on the channel for the different human body, an experience is performed in two subjects with transmission distance of

30 cm [29]. Fig. 2.6 shows the measurement results of different subjects. Each subject is measured three times. We can observe that the two subjects present the similar tendency in the frequency domain. Although the signal power can be distinguished at a higher frequency, the applications of BCC are not essential for such a high frequency. In the summary, the difference between subjects is small and band-pass profile and peak frequency did not change.

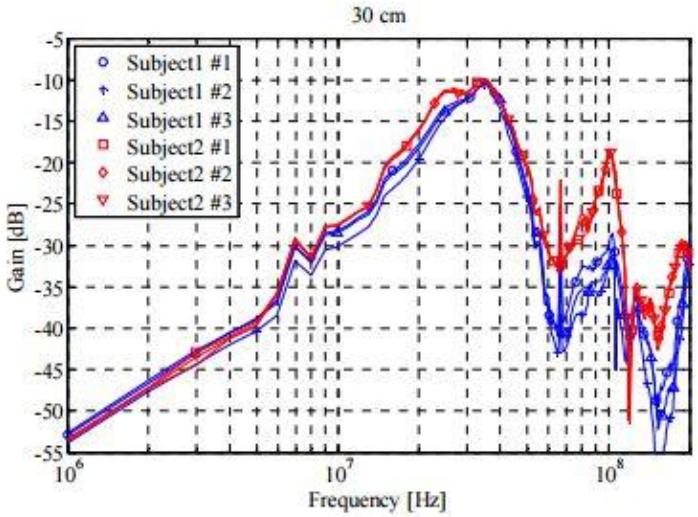


Fig. 2.6: Measurement results for different subjects [29]

One of the advantages of BCC is that the communication range is limited to the body region. A measurement is performed to measure the effect of body separation and propagation loss [30]. The distance from the arm to the couplers is changed while the distance between two couplers is always 11 cm. The maximum difference of propagation loss is appeared between the cases of the arm touching both couplers and no arm present. An increase in loss of 7-14dB and 14-22 dB are derived when the arm is placed 1 and 2 cm from the couplers respectively. If the arm is located 4 cm from the couplers, the propagation loss is exactly the same as the case with no body near the couplers. The measurement result is shown in Fig. 2.7.

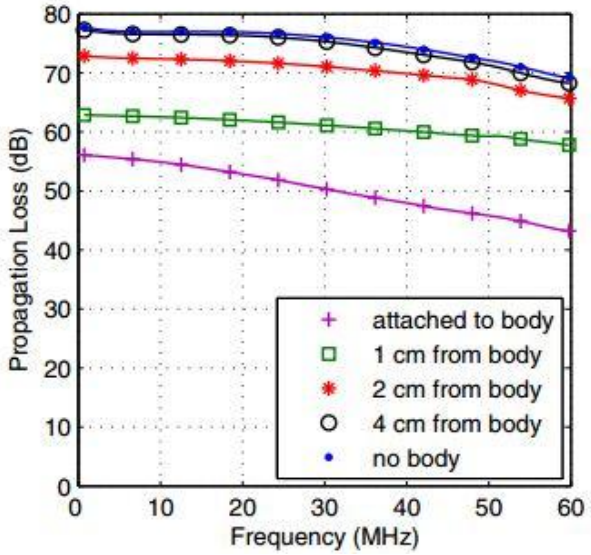


Fig. 2.7: Influence of body-coupler separation on the propagation loss [30]

2.2 Measurement Environment

Before designing a suitable circuit for body channel communication, we measure the characterization of human body communication. Fig. 2.8 shows the measurement setup.

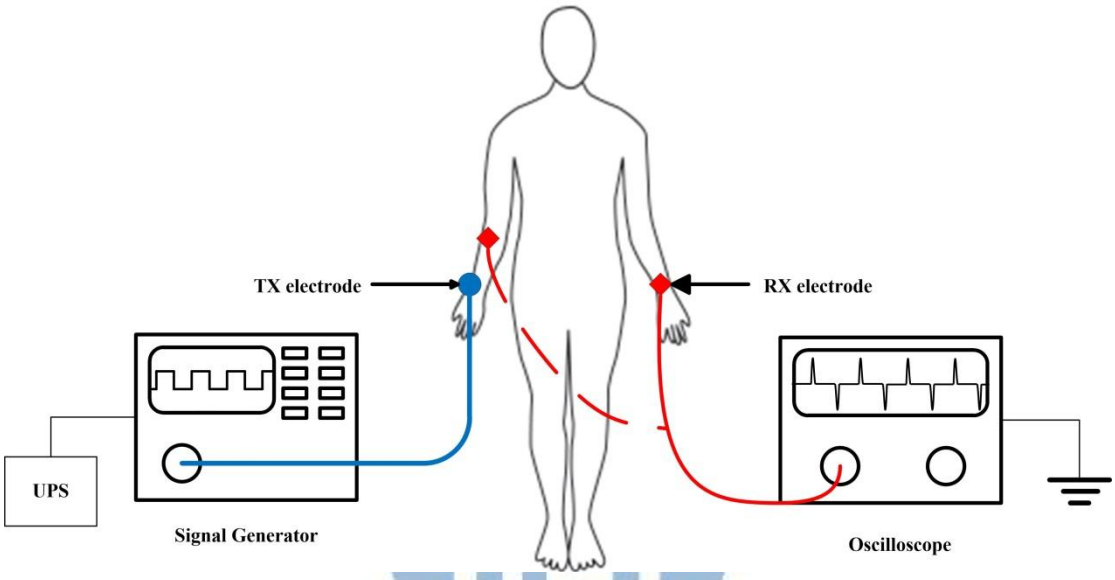


Fig. 2.8: The measurement setup for HBC

The arrangement for HBC measurement is composed of a UPS, a signal generator, a pair of electrodes and cables and an oscilloscope. As illustrated in Fig. 2.8, the signal generator generates a square waveform from 1MHz to 80MHz and the transmission distance between TX and RX is 10, 40 and 140 cm. With the help of a SMA cable and a single electrode (marked as blue), the signal can be directly transmitted into the human body. In the receiver part, the attenuated signal from the human body is passed through a SMA cable and a single electrode (marked as red) and received by an oscilloscope to analyze the result. It is worth mentioning that the return path is formed by air-coupling across the human body in order to correctly measure the HBC characteristics. Therefore, we adopt a UPS to supply the power of

the signal generator. The SMA cables and medical electrodes are presented in Fig. 2.9. A single electrode is applied in TX and RX whose diameter is about 1 cm. The measurement takes place in the laboratory at NCTU Si2 Group. In addition, the test person sits on the chair with his hands placed on the table parallel. The medical electrode is attached to the human skin and connected by a SMA cable in both TX and RX. Each measurement lasts for a while in order to sample sufficient data points. To reduce the effect of the length of the SMA cable to the measurement, a 75cm SMA cable is chosen.

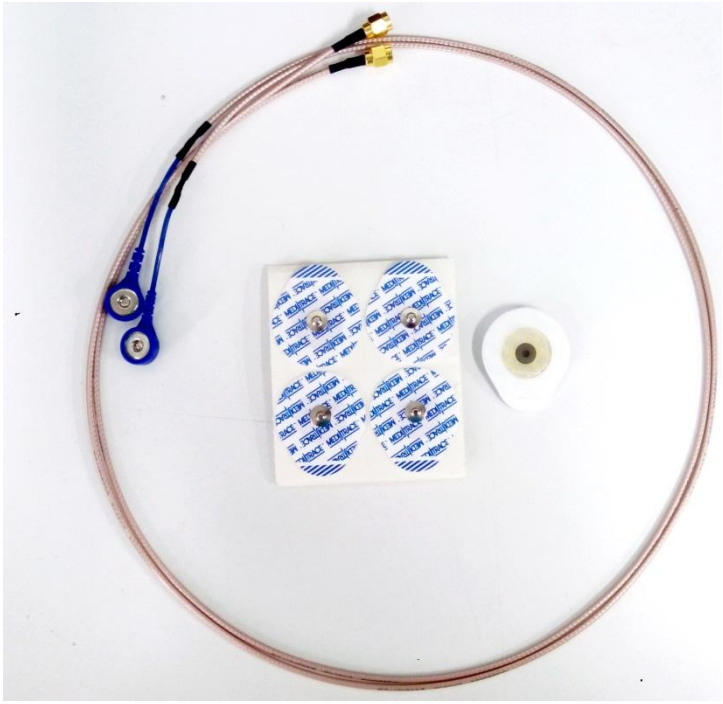


Fig. 2.9: Medical electrodes and SMA cables

Fig. 2.10 shows the illustration of our measurement. As discussed above, a battery-power signal generator transmits square waveform into the human body. The output signal from human body will be amplified and recovered by AFE board which will be introduced in section 2.3 in detail. Finally, the recovered signal is sent to an

oscilloscope to check whether the received signal is recovered correctly according to the original transmitted signal in TX.

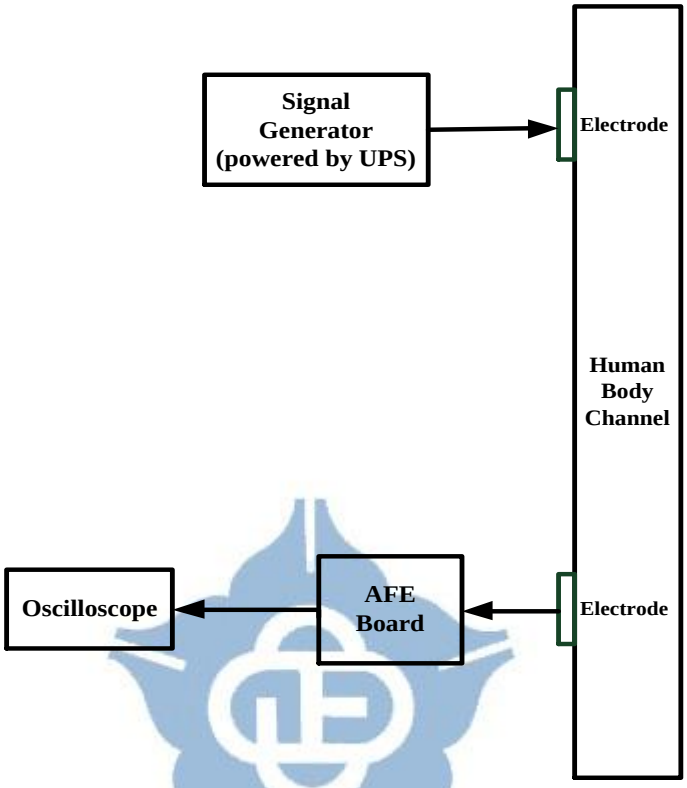


Fig. 2.10: The illustration of the measurement

2.3 Components and Measurements of AFE Board

Generally, the received signal through the human body channel will be attenuated. Hence, it is essential to deal with the issue. We come up with an idea to process the attenuated signal with the analog front-end (AFE) PCB board which is shown in Fig. 2.11. The proposed AFE board mainly contains a voltage gain amplifier (VGA) [36], a Schmitt trigger [37] and a 9.0 V rechargeable battery with power management circuits.

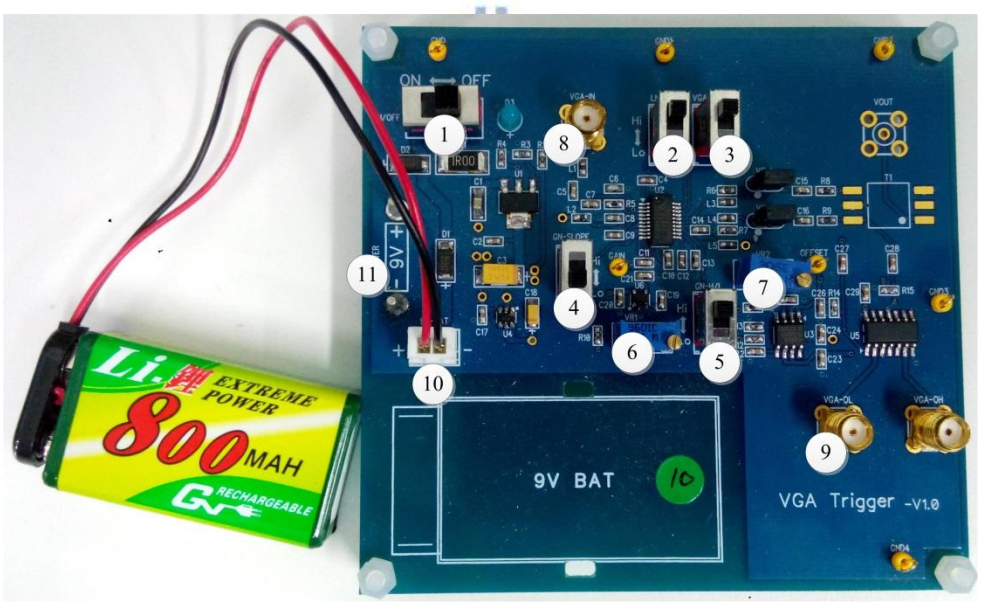


Fig. 2.11: The AFE board and a rechargeable battery

Next, each component on the AFE board will be introduced in detail. Number 1 is a switch which is used to turn on/off the power of AFE board. As shown in Fig. 2.11, number 2 and number 3 are switches to turn on/off for the LNA and the VGA respectively. Number 4 is utilized to determine the gain according to the variable

resistor (number 6). The gain increases with the variable resistor if the state of number 4 is Hi while the gain decreases with the variable resistor if the state is Lo. Number 5 is used to control either a high gain or a low gain of the VGA is chosen. Both Number 6 and Number 7 are variable resistors which can control VGA gain and DC offset of the output signal, respectively. The VGA gain ranges from 0 to 1.0 V and the voltage range of offset is from 0 to 1.5V. A VGA amplifies the attenuated signal (number 8). In addition, a Schmitt trigger is applied for level shifting the signal after amplified by the VGA so as to recover back to a digital signal. The voltage range of the DC offset adjustment is to determine the scope for DC level shifting. Then the signal is transmitted to an oscilloscope through number 9. The AFE board can be powered by a 9.0 V rechargeable battery connected to number 10. Instead of using a 9.0 V rechargeable battery, number 14 is for 9.0 V for external power supply input. The complete AFE board component descriptions are shown in table 2.1

Table 2.1: AFE board component descriptions

Number	Component Name	Component Description
1	ON/OFF	System power switch (5V)
2	LNA-EN	Hi: Enables the LNA
3	VGA-EN	Hi: Enables the VGA
4	GN-SLOPE	Hi: Gain increases with VR1 Lo: Gain decreases with VR1
5	GN-H/L	Hi: High gain Lo: Low gain
6	VR1	3296W-103-ND Potentiometer (10K)
7	VR2	3296W-103-ND Potentiometer (10K)
8	VGA-IN	SMA connector (input)

9	VGA-OUT	SMA connector (output)
10	9V-BAT	9.0 V battery connector
11	POWER	Power supply pin

The block diagram and the operation of the AFE board are depicted in Fig. 2.12. The transmitted signal (AFE_IN) from the human body is reduced to about 272.52 mV peak-to-peak which is a shark-fin-like signal. To amplify the attenuated signal, the VGA (AD8331) is used to enlarge the amplitude of the attenuated signal to about 2 V. In the AFE board, the upper and the lower threshold voltage of the Schmitt trigger is fixed. In order to recover the amplified signal (VGA_OUT) back to the square waveform, a DC level shifting circuit and the Schmitt trigger (MC74HC14A) is utilized for DC level shifting the signal and outputs AFE_OUT.

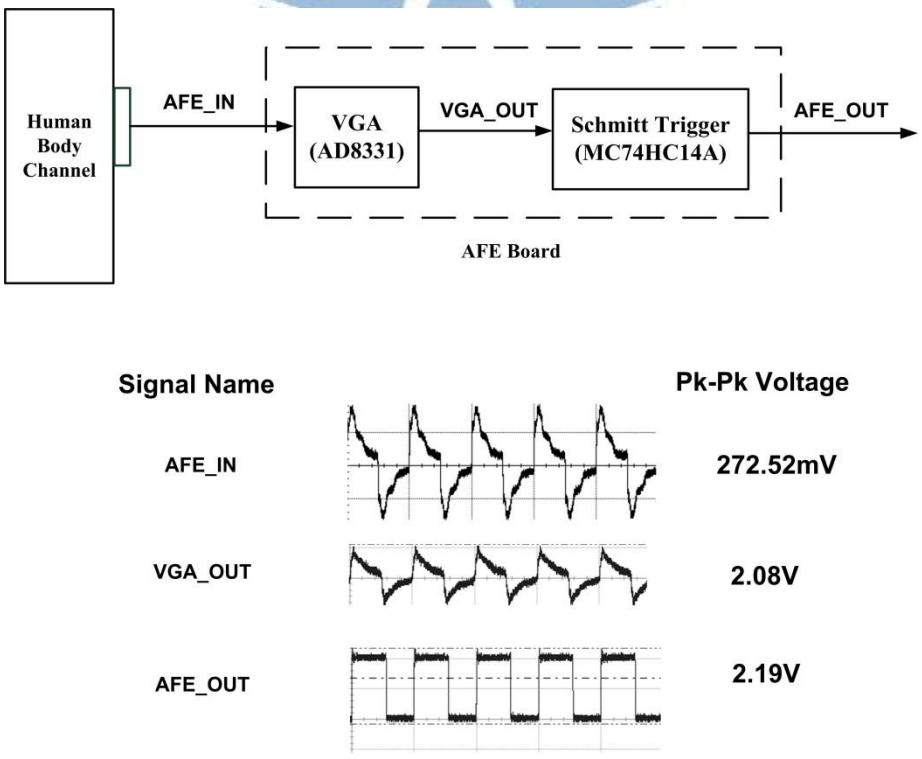


Fig. 2.12: The block diagram and the operation of the AFE board

As mentioned before, the signal power varies according to different transmission distance and frequencies. In order to overcome the case, we test different VGA gain and offset gain values in 10 cm and 140 cm distance. Table 2.2 summarizes the measurement results of the recovered signal of the AFE board from 1MHz to 40MHz.

Table 2.2: Summary of the AFE measurement results [39]

<table>
<tr><th></th><th>Frequency</th><th>Input voltage</th><th>Gain Value (0~1.0 V)</th><th>Offset Value (0~1.5 V)</th><th>Recovered Peak-to-Peak Voltage</th></tr>
<tr><td rowspan="5">10 cm</td><td>1 MHz</td><td rowspan="10">1.0 Vpp</td><td rowspan="5">0.65 V
(27.5 dB)</td><td rowspan="5">0.7 V</td><td>2.05 V</td></tr>
<tr><td>10 MHz</td><td>2.06 V</td></tr>
<tr><td>20 MHz</td><td>2.05 V</td></tr>
<tr><td>30 MHz</td><td>2.00 V</td></tr>
<tr><td>40 MHz</td><td>1.83 V</td></tr>
<tr><td rowspan="5">140 cm</td><td>1 MHz</td><td rowspan="5">1.0 V
(43.0 dB)</td><td rowspan="4">0.96 V</td><td>2.03 V</td></tr>
<tr><td>10 MHz</td><td>2.04 V</td></tr>
<tr><td>20 MHz</td><td>2.08 V</td></tr>
<tr><td>30 MHz</td><td>2.04 V</td></tr>
<tr><td>40 MHz</td><td>1.36 V</td><td>1.62 V</td></tr>
</table>

It is essential to consider the impact of jitter in human body communication for the sake of creating the human body channel model for designing a BCC transceiver. Table 2.3 presents the measurement results of jitter of the recovered signal from 1MHz to 40 MHz. Period jitter peak-to-peak is classified as Unit Intervals. Therefore, one UI of jitter is as same as the symbol time rather than the data rate. The maximum P_K-P_K jitter can be up to 28% UI. According to measurement results, the receiver

should have large jitter tolerance.

Table 2.3: Summary of the jitter measurement results [39]

Distance	**Frequency**	**Input Voltage**	**Period**	**Period Jitter Peak-to-Peak**	**Period Jitter RMS**	**Cycle-to-Cycle Jitter RMS**
10 cm	1 MHz	1.0 Vpp	999.99 ns	3.9 ns (3.9% UI)	471.7 ps (0.05% UI)	849.92 ps (0.08% UI)
	10 MHz		99.99 ns	3.65 ns (3.65% UI)	271.3 ps (0.27% UI)	465.09 ps (0.47% UI)
	20 MHz		49.99 ns	3.05 ns (6.01% UI)	314.4 ps (0.63% UI)	485.63 ps (0.97% UI)
	30 MHz		33.33 ns	1.5 ns (4.50% UI)	160.1 ps (0.48% UI)	295.92 ps (0.89% UI)
	40 MHz		25.01 ns	2.6 ns (10.39% UI)	155.6 ps (0.62% UI)	845.55 ps (3.38% UI)
140 cm	1 MHz		999.88 ns	43.5 ns (4.35% UI)	3.5 ns (0.35% UI)	5.63 ns (0.56% UI)
	10 MHz		99.96 ns	10 ns (10% UI)	1.1 ns (1.1% UI)	1.78 ns (1.78% UI)
	20 MHz		49.99 ns	3.4 ns (6.8% UI)	253.6 ps (0.5% UI)	467.95 ps (0.94% UI)
	30 MHz		33.35 ns	1.72 ns (5.15% UI)	219 ps (0.66% UI)	2.13 ns (6.39% UI)
	40 MHz		25.42 ns	7.1 ns (27.93% UI)	643 ps (2.53% UI)	4.33 ns (17% UI)

2.4 Measurement Results of Human Body Experiments

We have done several measurements to understand the characteristics of BCC. In addition, the results of our measurements give the contribution to building up the human model. Fig. 2.13 presents the measured signal power in the RX electrode with different distance in the frequency domain. Before transmitted into the human body, the amplitude of the signal from the signal generator is set to 1.0 Vpp. According to the figure, we can observe that three curves show the similar tendency which is no difference as described in former research. As the frequency grows, the power attenuation becomes more serious. At identical frequency, the signal power of transmitted signal degrades when the transmission distance is longer. The worst case of signal power is about to -26 dBm at 80MHz and 140 cm. The impedance of test person is considered as 50Ω who is in 166 cm tall and 60 kg weight. Due to the analysis of our measurement, we can examine whether the proposed AFE board is able to recover the attenuated signal.

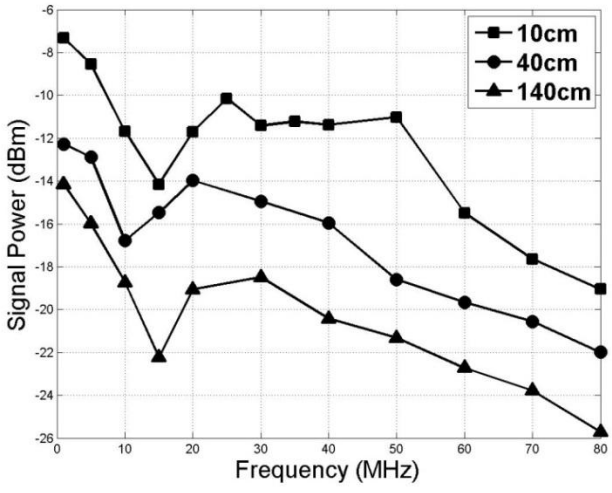


Fig. 2.13: Measurement at 10/40/140 cm

To verify the influence of body channel of different test bodies, we performed the measurement in three subjects. The subjects have different height and weight. Fig. 2.14 presents the result for the three human bodies with 10 cm transmission distance between TX and RX. We notice that the difference in attenuation between the three subjects is not evident. The maximum difference of signal power is about to 7 dBm at 20 MHz between Human #2 and Human #3. However, the difference is tiny and can be neglected. Also, the figure shows the similar property in the frequency domain that the three curves are non-linearity.

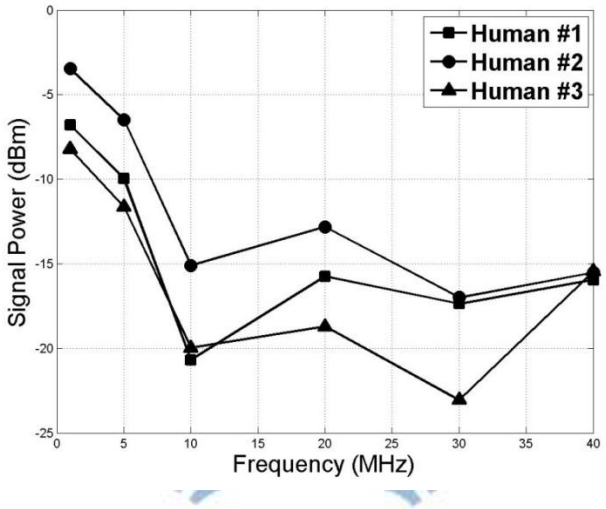


Fig. 2.14: Frequency domain measurements with three subjects in 10 cm

Fig. 2.15 shows the result for the three human bodies with 140 cm transmission distance between TX and RX. The maximum difference of signal power is about to 10 dBm at 20 MHz between Human #2 and Human #3. Despite different transmission distances, Both Fig. 2.14 and Fig. 2.15 demonstrate an alike trend for signal power in the frequency domain.

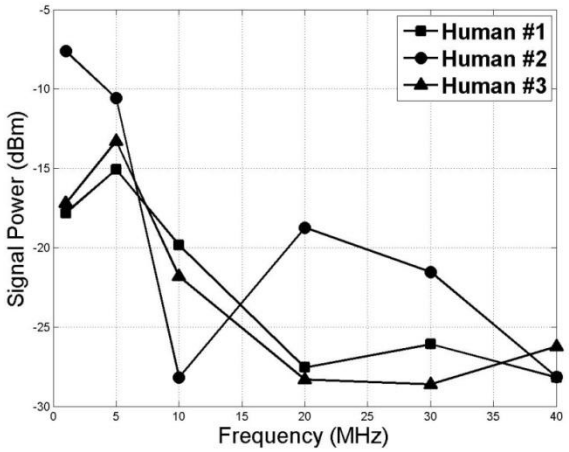


Fig. 2.15: Frequency domain measurements with three subjects in 140 cm

We measure the effect of the human body for the still and motion scenarios. In the still scenario, the test subject sits on the chair with his hands placed on the table. As for moving scenario, the test subject sits on the chair with his hands swinging regularly. The medical electrodes are attached on the left hand and right hand with 10 cm and 140 cm distance at 1MHz and 40MHz. Table. 2.4 summarize the period jitter RMS of the received signal for still and moving scenarios. As shown in the table, we can observe that human body communication is nearly insensitive to the motion of the human body which is the conclusion mentioned in [27].

Table 2.4: Summary of the HBC motion measurement results

		RX Period Jitter RMS	
Distance	**Frequency**	**Still**	**Moving**
10 cm	1 MHz	1.7 (ns)	1.1 (ns)
	40 MHz	734.2 (ps)	667.1 (ps)
140 cm	1 MHz	4.3 (ns)	3.2 (ns)
	40 MHz	472 (ps)	515.7 (ps)

Fig. 2.16: The adopted wireless intercom

As discussed in [38], an experiment is done to measure the effect of interference to body channel communication in the nearby environment. Similarly, we apply a wireless intercom to radiate a signal to measure whether human body channel is sensitive to the interference in the nearby environment. Table 2.5 shows the summary of the effect of interferences from wireless intercom to human body communication. According to the measured period jitter RMS of the received signal, the wireless intercom causes a little interference to the human body channel communication. Fig. 2.16 shows the adopted wireless intercom.

Table 2.5: Summary of the interferences from the wireless intercom to human body communication

		RX Period Jitter RMS	
Distance	**Frequency**	**W/O Interference**	**With Interference**
10 cm	1 MHz	3.21 (ns)	2.71 (ns)
	40 MHz	456.2 (ps)	510.3 (ps)
140 cm	1 MHz	2.51 (ns)	1.87 (ns)
	40 MHz	287.8 (ps)	347.4 (ps)

2.5 Summary

In this chapter, we first study associated research for body channel characteristics. To support the conclusion derived from former research, we have measured some kinds of cases in different situations. As a result, all the measurement results show the similar characteristics compared to former research. Subsequently, an AFE board is designed to overcome the interference and build up human body model. In order to guarantee the AFE board is available, a measurement is taken to estimate the performance. Eventually, we come up with a proposed BCC transceiver according to the measurement results.

Chapter 3

The Proposed BCC Transceiver Based on FPGA Evaluation Boards

3.1 Architecture Overview

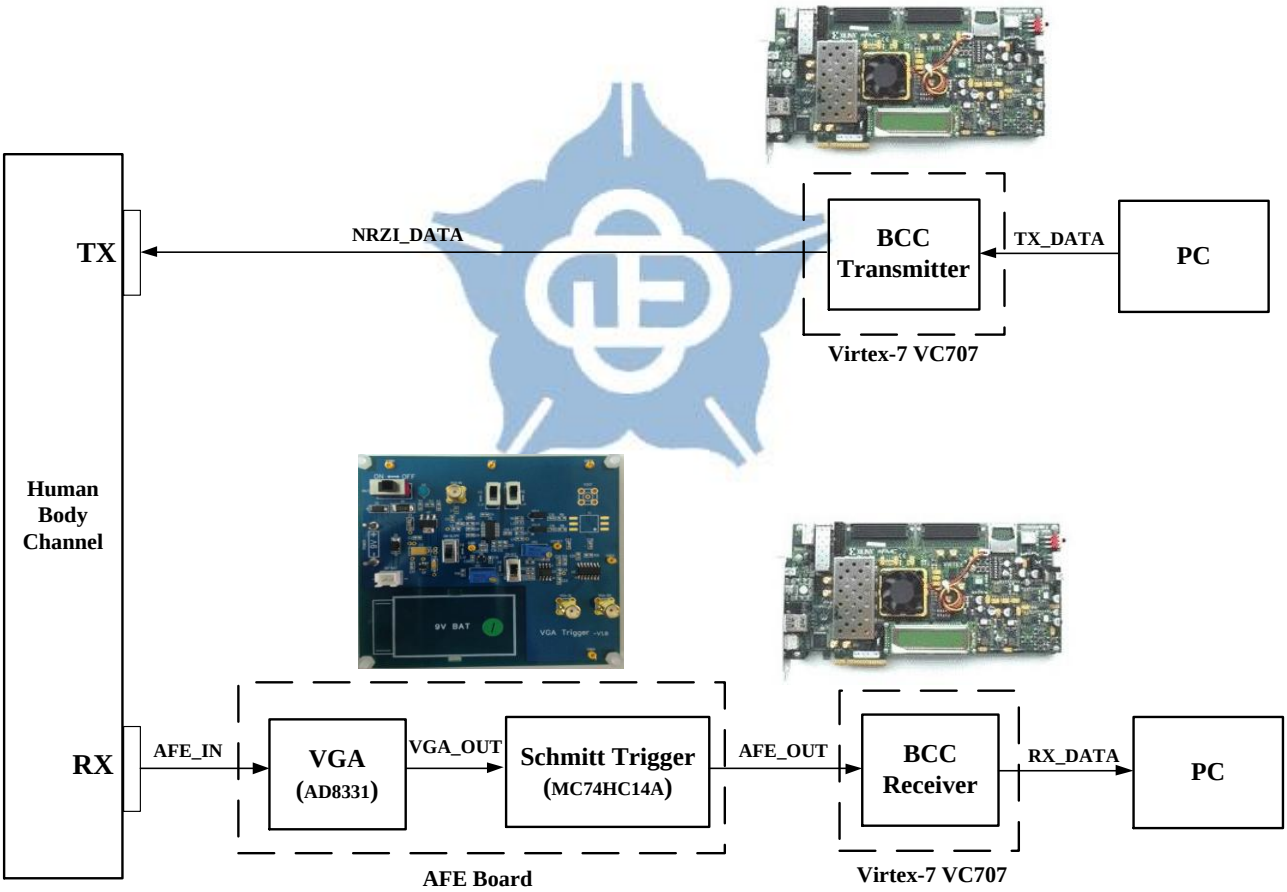


Fig. 3.1: Overview of the proposed FPGA-based BCC transceiver

Fig. 3.1 presents the proposed architecture of the FPGA-based BCC transceiver.

The transceiver mainly consists of four parts including a transmitter, a human body,

an AFE board and a receiver. The BCC transmitter is composed of a preambler, a linear feedback shift register (LFSR), a non-return-to-zero-inverted (NRZI) encoder, two multiplexers, a block memory, an UART and a bit stuffer. All of them are downloaded to Virtex-7 VC707 evaluation board (EVB). Later, the output signal (NRZI_DATA) from BCC transmitter is transmitted into the human body with a medical electrode and a SMA cable. In the receiver part, the AFE board receives the attenuated signal (AFE_IN) from the human body. The VGA first amplifies the attenuated signal to around 2.0 Vpp and then recovered them back to digital signals by a Schmitt trigger and a DC level shifting circuit. The BCC receiver is composed of an 8X oversampling sampler, a vote integrator, a bit unstuffer, a NRZI decoder, a RX controller, a block memory, an UART, a demultiplexer and a LFSR checker. Similarly, all of them are downloaded to Virtex-7 VC707 EVB. The BCC receiver derives the signal (AFE_OUT) and outputs the data (RX_DATA) after a series of processes.

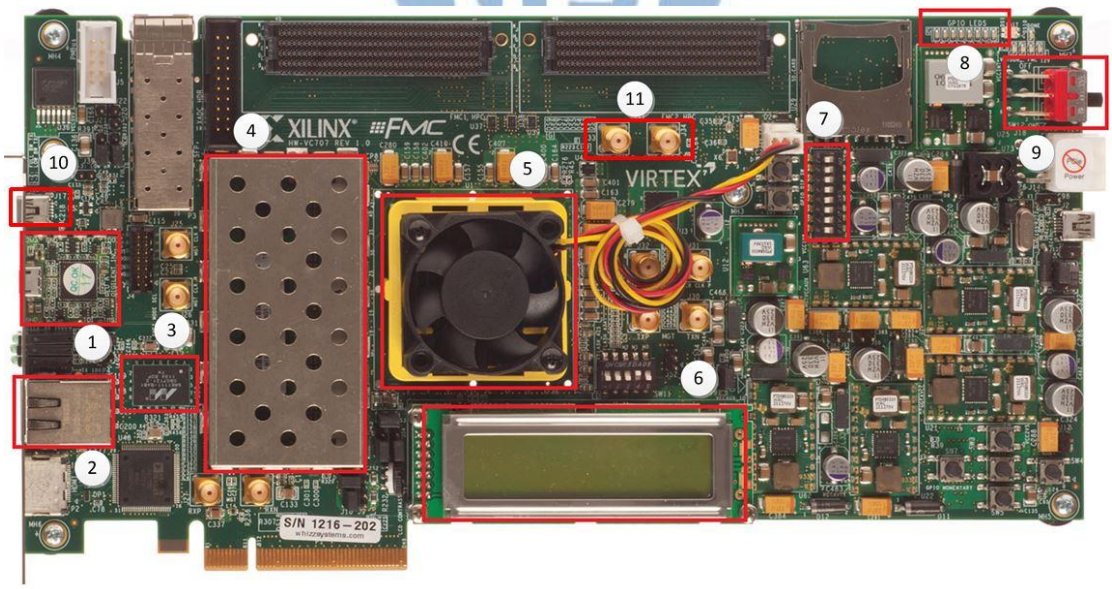


Fig. 3.2: Overview of the Virtex-7 VC707 [40]

Fig. 3.2 shows the overview of the Virtex-7 VC707 [40]. Number 1 is JTAG

interface which is used to make a connection between the computer and the VC707. Number 2 and number 3 are Ethernet RJ-45 port and Ethernet physical layer IC. Number 4 is a 1GB DDR3 memory which provides synchronous dynamic access memory for storing data. Number 5 is a FPGA with a cooling fan and number 6 is a LCD display. Number 7 are the user dip switches. Number 8 are the LEDs and number 9 is a power switch. Number 10 is an USB to Universal Asynchronous Receiver/Transmitter (UART) interface. The image or audio data can be transmitted from the computer to VC707 through UART port. Number 11 are the user SMA ports. Table 3.1 lists the marked components of VC707 in Fig. 3.2 :

Table 3.1: VC707 EVB component description

Locations	Component Description
1	USB JTAG interface
2	Network cable port
3	10/100/1000 Mb/s Ethernet PHY
4	DDR3 SODIMM memory (1 GB)
5	Virtex-7 FPGA with cooling fan
6	LCD character display
7	User DIP Switch
8	User LEDs
9	Power on/off switch
10	USB to UART bridge
11	User SMAs

We develop both BCC transmitter and receiver in Xilinx ISE which provides IPs

such as blocking memory for easy storage. Moreover, the user constraint file (.ucf) is for pin assignments and user constraints. After mapping and routing of the proposed BCC transceiver, ISE finally generates a bit file which is able to be downloaded to VC707 through the JTAG. Since it is not easy to track the operation of the FPGA in VC707, we apply Chipscope for easy observation and trace the specified signals.

3.2 Wideband Signaling BCC Transmitter

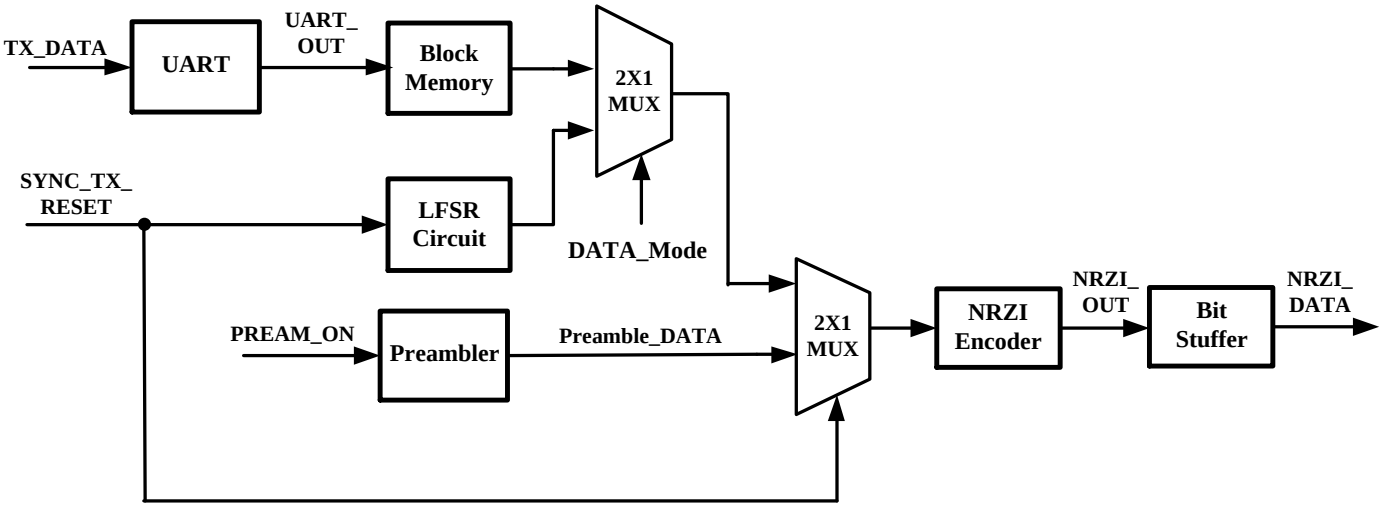


Fig. 3.3: Architecture of the wideband signaling transmitter

Fig. 3.3 shows the block diagram of the proposed BCC transmitter. The system clock is provided by the VC707. The preambler generates both the preamble data and the start frame delimiter (SFD) for synchronization. The LFSR circuit outputs random pattern with every 2^{20} -1 bits repetition which is composed of twenty registers and a XOR gate after receiving a synchronized signal (SYNC_TX_RESET). Both BCC transmitter and receiver have the same LFSR circuit so that bit error rate measurement can operate in an easy way. In addition, external data (TX_DATA) is transmitted from the computer to the UART block and then stored in the block memory [42]. The two multiplexers are used for data selection. Either external data (TX_DATA) or LFSR pattern is determined by DATA_Mode. Subsequently, the chosen data are encoded by the NRZI encoder. When the input data is "0", the NRZI encoder will reverse the output signal (NRZI_OUT). If the input data is "1", the NRZI encoder will remain the output signal. Because of jitter accumulation and the duty-cycle distortion, fewer data

transitions will make it difficult to recover the data in the receiver part. Thus, the bit stuffer will insert an extra inverse bit after five continuous identical digits (CIDs) appear so that the maximum CID is limited to 5 .

Fig. 3.4 shows the packet format of the proposed transceiver. In each packet, twelve preamble bits are firstly transmitted for synchronization. Subsequently, eight SFD bits are transmitted followed by 1000 data bits. After the first packet transmission is completed, the second packet is sent to the BCC receiver, and so on.

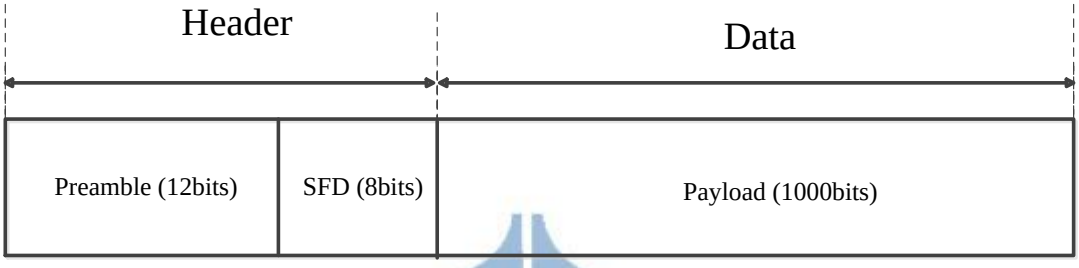


Fig. 3.4: The packet format of the BCC transceiver

UART (Universal Asynchronous Receiver/Transmitter) is one of the wire communication attached to the computers. The data transmitted through UART is one bit at a time. The transmitting speed and data size are not constant. In addition, it is asynchronous for UART since no clock signal is needed to synchronize the data. Therefore, we can set the parameter according to the communication requirement as long as both the transmitter and receiver configure the identical parameter.

Since no clock signal is provided, a ‘start bit’ is first transmitted which leads to the logic “high” down to “low” so that the receiver can wake up for the word followed by the start bit. Each word is composed of eight bits. The receiver samples each bit at the half of the pulse width so as to keep the sampled data correct. If error-checking is necessary, a “parity bit” can be added next to the word. Finally, a “stop bit” is sent to inform that the transmission of the word is finished. Fig. 3.5 depicts the flow of

UART operation.

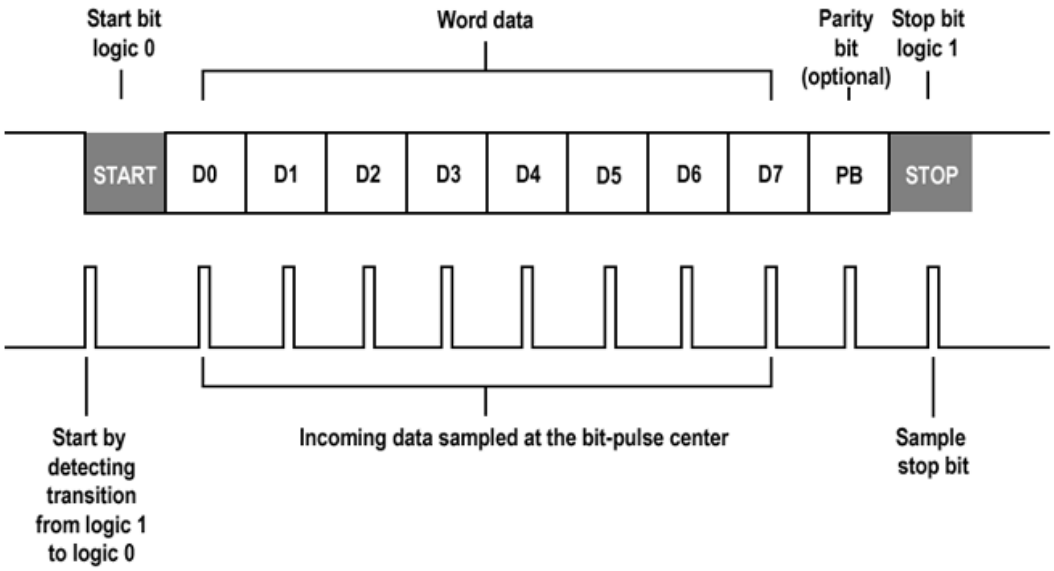


Fig. 3.5: The operation flow of UART [41]

3.3 Oversampling based BCC Receiver

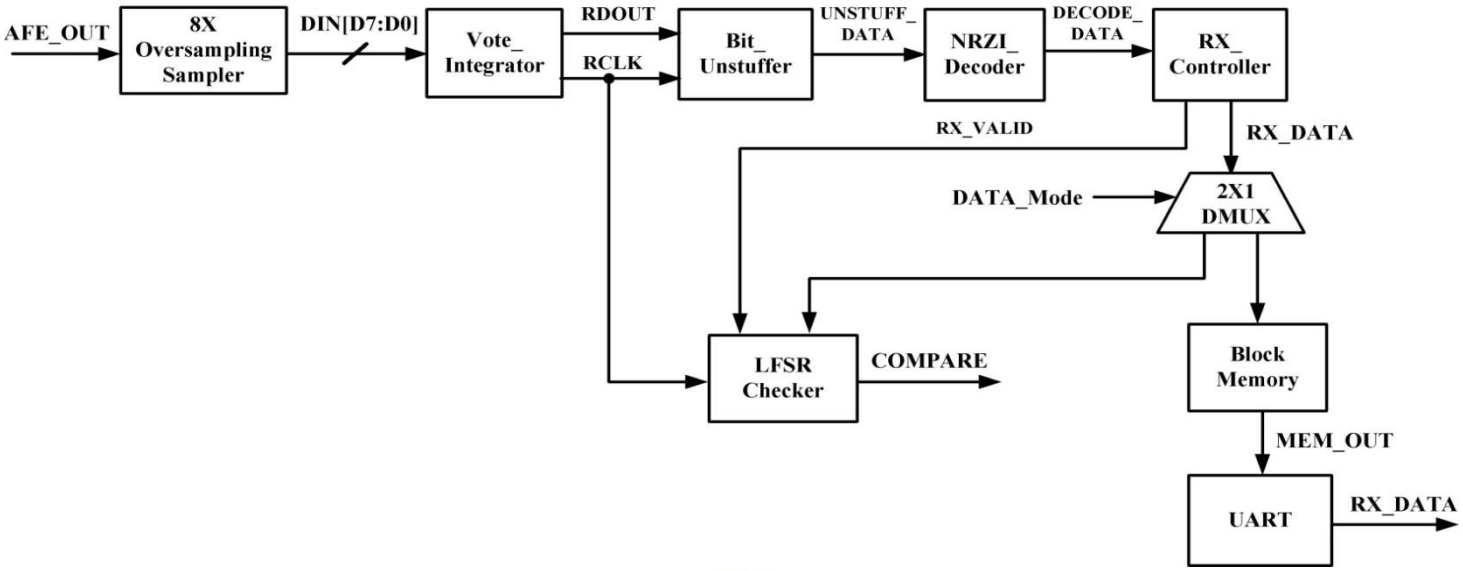


Fig. 3.6: Architecture of the BCC receiver

Fig. 3.6 shows the block diagram of the proposed BCC receiver. After the received signal is amplified and recovered by the VGA and the Schmitt trigger, the output signal (AFE_OUT) from the AFE board is then sent to the BCC receiver. The 8X oversampling sampler samples eight data in one data period and outputs the signal (DIN[D7:D0]) to the vote integrator. In the vote integrator, it operates the vote mechanism to determine the recovered data (RDOUT) and the recovered clock signal (RCLK). Subsequently, the bit unstuffer removes the extra bits added in the bit stuffer in the transmitter part. After the signal (UNSTUFF_DATA) is decoded by NRZI decoder, the output signal (DECODE_DATA) is sent to RX controller. Once the SFD bits are detected by the RX controller, it generates the signal (RX_VALID) to the LFSR checker. The LFSR checker is used for automatic error-free measurement. It creates the same random pattern sequences as in TX for comparing with the recovered data. If the RX_DATA is exactly the same as the random pattern generated in TX, the

output signal (COMPARE) is set to “0“. Otherwise, if the RX_DATA is not as expected, a bit error appears and the output signal is set to “1“. Moreover, if the transmitted data is external data rather than the LFSR pattern, it will be stored in the block memory [42] after bit unstuffing and decoding. Finally, the data (MEM_OUT) are packed and transmitted to the computer via UART.

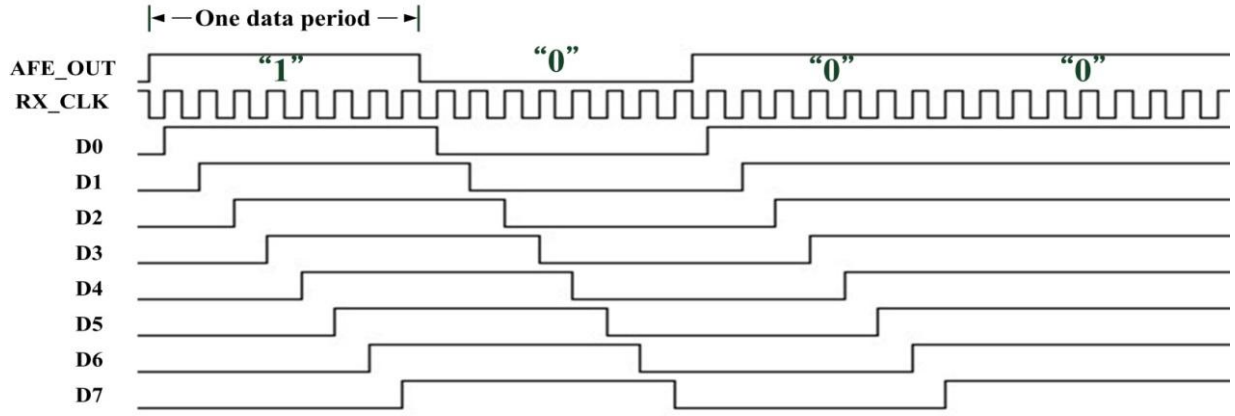


Fig. 3.7: Illustration of the vote mechanism

Fig. 3.7 presents the illustration of the vote mechanism. The 8X oversampling sampler samples eight data in one data period and outputs the signal DIN[D7:D0] to the vote integrator. The vote integrator computes the number of “1” of DIN[D7:D0] in one data period. As shown in Fig. 3.7, one data period consists of eight time slices. In other words, the maximum value of the value_integrator is 64.

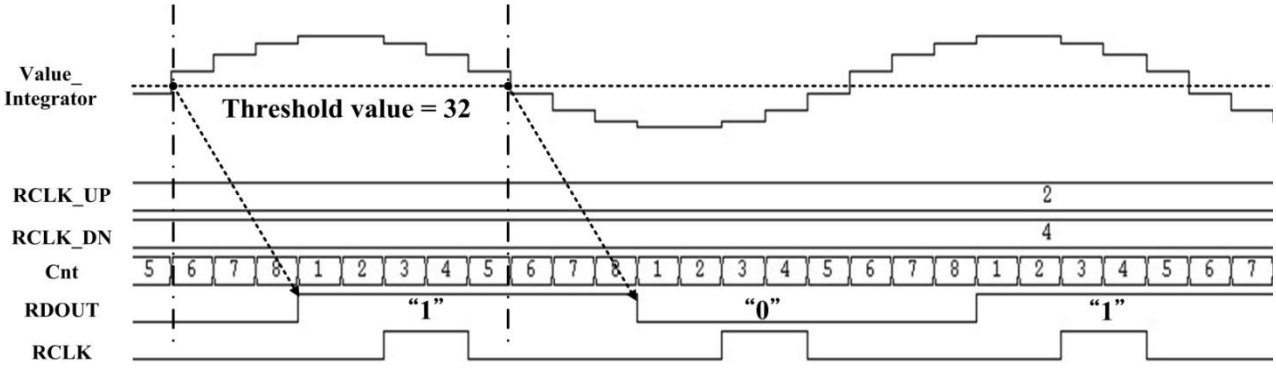


Fig. 3.8: Clock and data recovery from the value of the vote integrator

In order to recover the data and the clock, we set a threshold to the half of the maximum value of Value_Integrator. If the value of Value_Integrator is larger than the threshold, the signal RDOUT is set to “1” which is represented as the recovered data. Oppositely, if the value of Value_Integrator is smaller than the threshold, the signal RDOUT is set to “0”.

Next, let`s take a look at the recovered clock signal named RCLK. As shown in Fig. 3.8, the signals RCLK_UP and RCLK_DN are used to decide when RCLK is going to rise or fall, respectively. The two signals will be updated according to the value of Cnt whenever the Value_Intrgrator has a rise or fall transition against the threshold. For instance, when the value of Value_Integrator is larger than the threshold at the first time, the Cnt value is 6. Then, the RCLK_UP is updated as the result of (6+3) mod 8 and then add 1 while RCLK_DN is updated as the result of (6+5) mod 8 and then add 1. Similarly, when the value of Value_Integrator is smaller than the threshold at the first time, the Cnt value is 6. Thus, the RCLK_UP and RCLK_DN are updated as 2 and 4, respectively.

After the vote integrator refreshes both RCLK_UP and RCLK_DN, RCLK can be determined. If the value of RCLK_UP is as same as Cnt, RCLK is set to “1”. If the value of RCLK_DN is as same as Cnt, RCLK is set to “0”. Generally, RCLK will update in every data period in order to determine the recovered data. Thus, the vote integrator can guarantee the correctness of the recovered data.

3.4 Implement the Proposed BCC Transceiver on the FPGA Platform

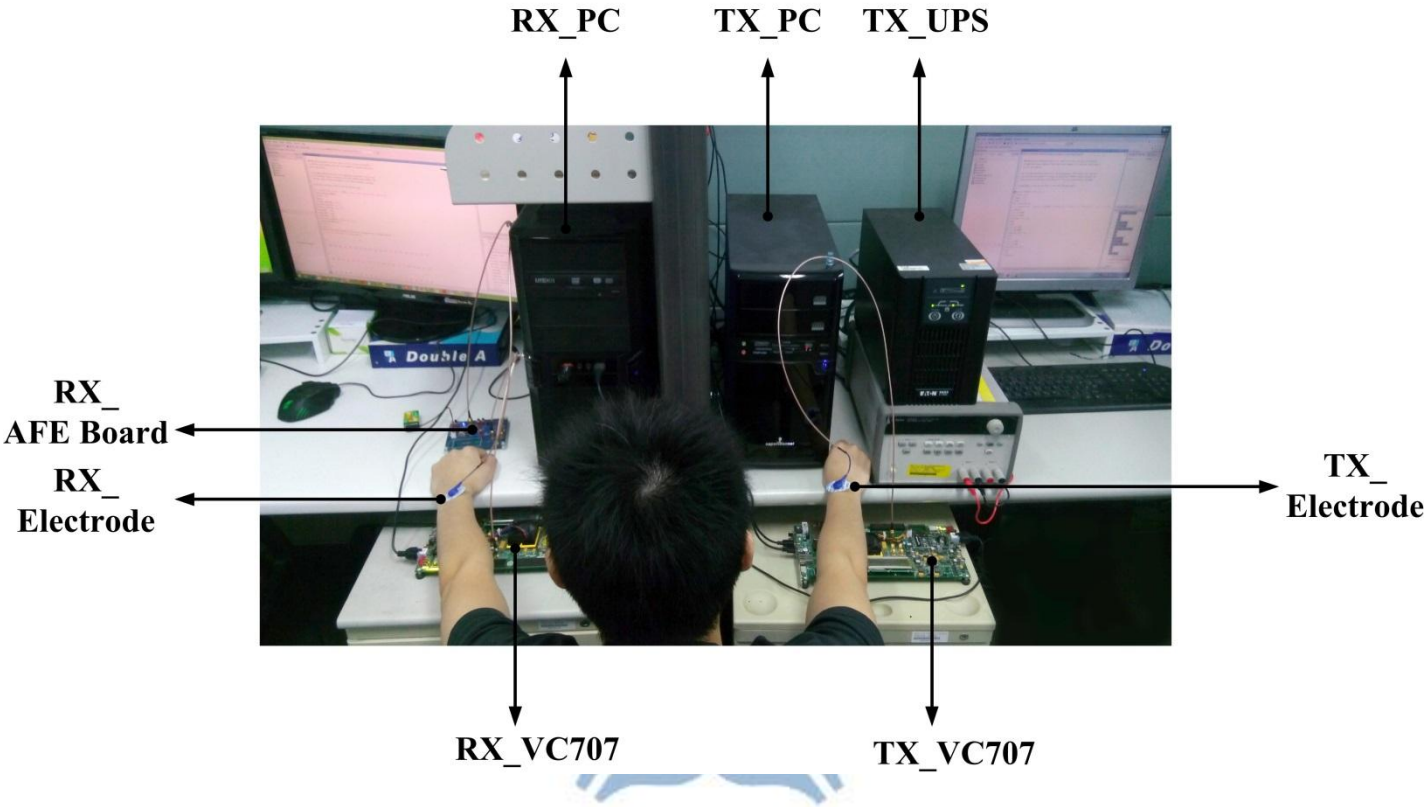


Fig. 3.9: The setup of the BCC implementation

Fig. 3.9 shows the setup of the implementation of the proposed BCC transceiver. The UPS is used to supply the power of the computer as well as the VC707 in the TX part. On the other hand, the AFE board is powered by a 9.0 V rechargeable battery. The connection between the VC707 and the human body is accomplished by the SMA cables and the medical electrodes. We are going to transmit an image from the transmitter to the receiver and finally displayed on the monitor of the computer. Before the BCC transmitter starts to work, we set a serial port in MATLAB to send the image from the computer to the TX_VC707 via UART and then stored in the

block memory. The LED on the TX_VC707 board is not bright until the image had already stored in the memory. As the DIP switch on, the TX_VC707 turns on, the transmission in the BCC transmitter begins. The transmission distance between two medical electrodes is 140 cm. In the receiver part, we had set the proper parameters of VGA gain and DC offset according to previous measurement results to ensure the AFE board is functional. After bit unstuffing and NRZI decoding, the data are stored in the block memory. As soon as the storage is completed, the LED on the RX_VC707 board is light. Consequently, the DIP switch is turned on and the RX_VC707 starts to transmit the data to the computer via UART and shown on the monitor.

Chapter 4

Measurement Results of the BCC Transceiver

4.1 Implementation Information

The implementation components used in VC707 EVB are listed in Table. 4.1. The table summarizes the pin information and gives brief pin descriptions.

Table 4.1: Pin assignment summary

Net Name	I/O	FPGA Pin	Description
BCC Transmitter			
clk_in_p	Input	E19	The VC707 has an oscillator to create 200MHz clock signal pair.
clk_in_n	Input	E18	
RESET	Input	AV40	A button to reset the CPU.
TX_DATA	Input	AU33	An input port for UART.
FIFO_VALID	Input	BA30	A DIP Switch to start the transmission in TX.
NRZI_DATA	Output	AP31	An SMA port for output data.
LED	Output	AR37	A LED for the state of the storage. The LED lights when the image storage is completed and vice versa.

BCC Receiver			
clk_in_p	Input	E19	The VC707 has an oscillator to create 200MHz clock signal pair.
clk_in_n	Input	E18	
RESET	Input	AV40	A button to reset the CPU.
SWITCH	Input	BA30	A DIP Switch to start the transmission from RX to PC.
AFE_OUT	Input	AN31	An SMA port for the data from the AFE board
RX_DATA	Output	AU36	An output port for UART.
LED	Output	AR37	A LED for the state of the storage. The LED lights when the image storage is completed and vice versa.

Table 4.2 shows the hardware resource utilization of the proposed BCC transceiver. In this table, “Slices” are presented as the real blocks rather than “Logic Cells” in the FPGA board. They can be either partially utilized or fully utilized. In addition, “Slice Registers” show the number of flip-flops implemented in slices while “Slice LUTs” indicate the number of lookup tables implemented in slices. Meanwhile, “Occupied Slices” is the number of slices that are at least used in the project. It indicates whether your design can fit the hardware resource requirement. Generally, the design can be mapped successfully without the resource warnings if the “Occupied Slices” is below 90%. As the “Occupied Slices” gets close to 100%, it will spend more time in mapping and make it difficult for meeting the timing requirement. “Number used as Memory” shows the number of the LUT which is used to form the

memory. The “available” column gives total device resources that can be used in the FPGA board. The mapper will determine the number when it packs multiple functions into a slice.

Table 4.2: FPGA utilization summary

Slice Logic Utilization	**Used**	**Available**	**Utilization**
BCC Transmitter			
Number of Slice Registers	1203	607200	1%
Number of Slice LUTs	1164	303600	1%
Number of Occupied Slices	630	75900	1%
Number used as Memory	271	130800	1%
BCC Receiver			
Number of Slice Registers	1647	607200	1%
Number of Slice LUTs	1608	303600	1%
Number of Occupied Slices	835	75900	1%
Number used as Memory	316	130800	1%

4.2 Measurement Results in Different Configuration

We download the bit file of the BCC transmitter and receiver to the corresponding VC707 EVBs. Subsequently, the DIP switch turns on to start the data transmission in TX. The distance between two medical electrodes is 140 cm. In the receiver part, we adopt the Chipscope to observe whether a bit error occurs in the LFSR checker. The signal RX_DATA represents the recovered data while the signal out_data is for the output of the LFSR circuit in the receiver. The signal COMPARE is set to "1" once any bit error exists. As shown in Fig. 4.1, there is no any bit errors after 1.287×10^7 bits are examined in the LFSR checker at 1.56Mbps. Fig. 4.2 shows the measurement result of LFSR random pattern at 600kbps. As shown in Fig. 4.2, there is no any bit errors after 1.158×10^7 bits are examined in the LFSR checker. Due to the air coupling effect, the attenuation would increase extremely if the transmission is at low data rate.

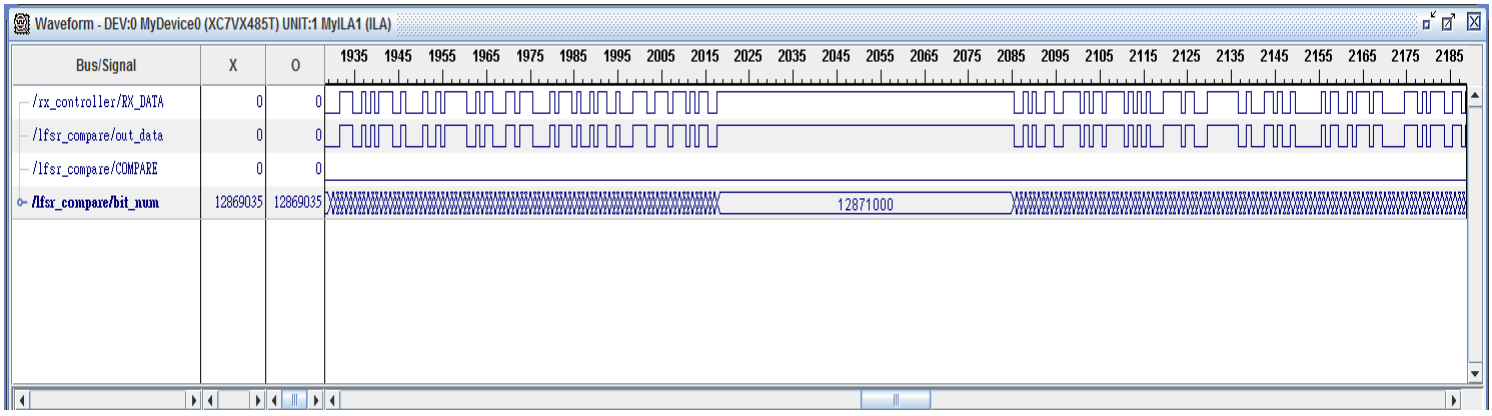


Fig. 4.1: Measurement result with LFSR random pattern at 1.56Mbps

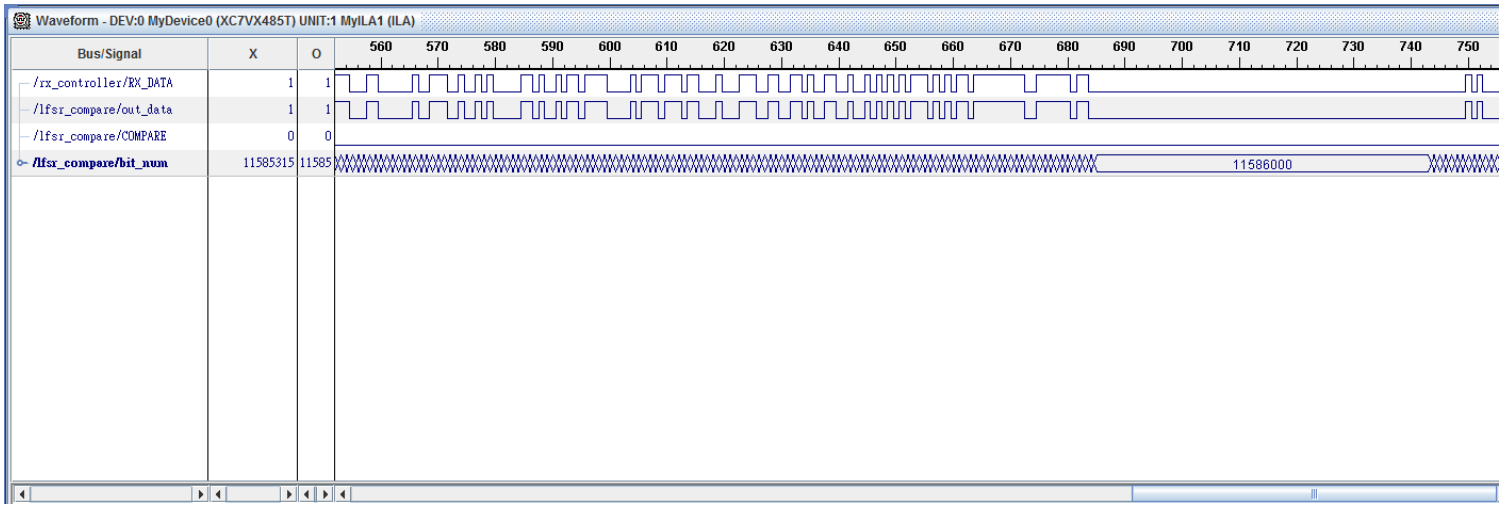


Fig. 4.2: Measurement result with LFSR random pattern at 600kbps

To figure out the limitation of the data rate in the proposed design, we first transmit the LFSR random pattern with two FPGA EVBs and the AFE PCB board. Subsequently, we remove the AFE PCB board and then transmit the data. As shown in Fig. 4.3 and Fig. 4.4, None of them can provide a correct data transmission at 3.12Mbps. On the other hand, we also test different transmission pattern in body channel communication. Fig. 4.5 shows the 01 regular data pattern measurement result. The maximum data rate without any errors is 3.12Mbps and the transmission distance is 140 cm. In addition, we output the 01 regular data and the clock signal from the transmitter to the receiver. The receiver can get the correct data at about 50MHz. Moreover, we modify the oversampling mechanism such as rising the sampling rate and adjusting the calculation of recover clock signal and recover data. Unfortunately, all of the attempts is not beneficial for the data rate.

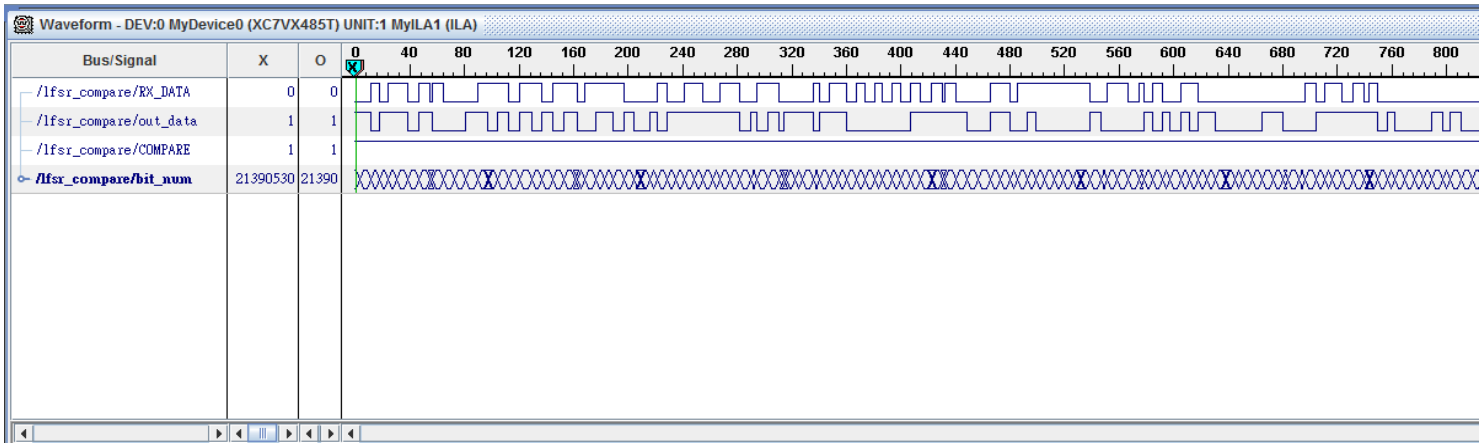


Fig. 4.3: Measurement result with two FPGA EVBs and the AFE board at 3.12Mbps

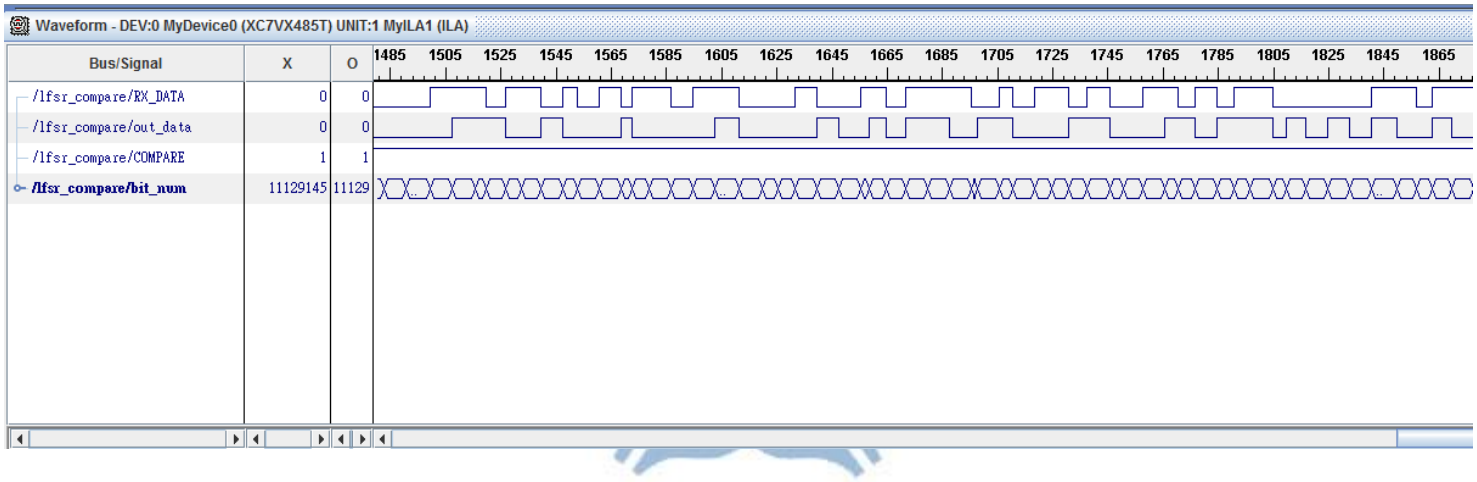


Fig. 4.4: Measurement result with two FPGA EVBs at 3.12Mbps

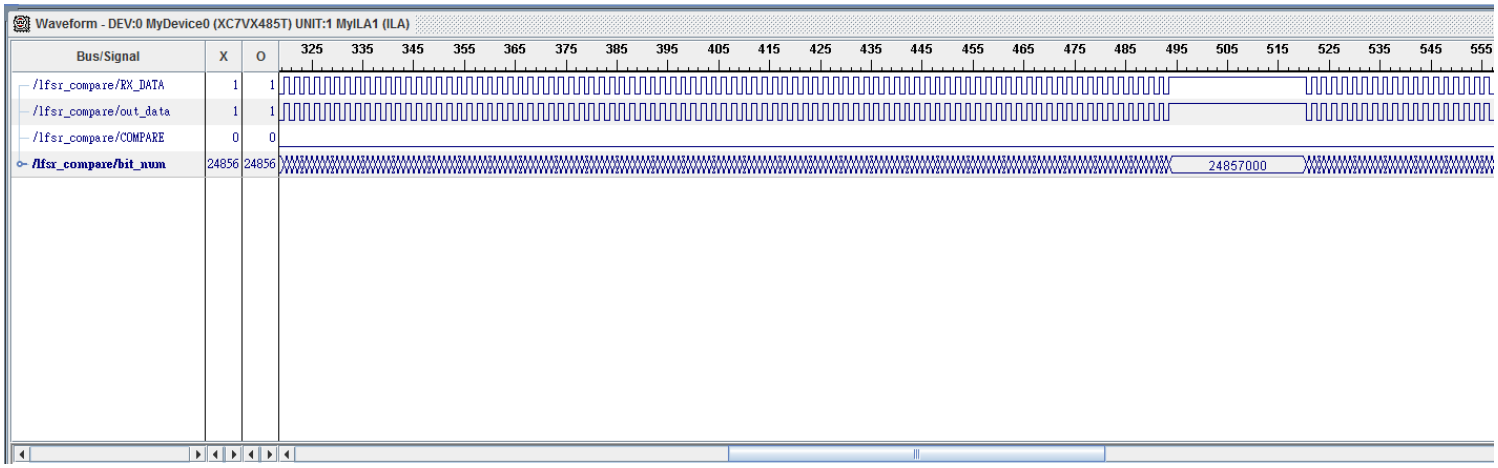


Fig. 4.5: Measurement result with 01 regular pattern at 3.12Mbps

Fig. 4.6 shows an image is transmitted through a human body at 1.56Mbps. The left part shows the original image before transmitted while the right part presents the image recovered by the receiver. The size of the image is 200 × 200 pixel and the bit depth is 24. As seen in Fig.4.6, the received image is as same as the original image. The subject can`t touch any metal-made object during the image transmission in case the data are interfered. Besides, the version of MATLAB must fit the operation system to ensure the image can be received correctly.

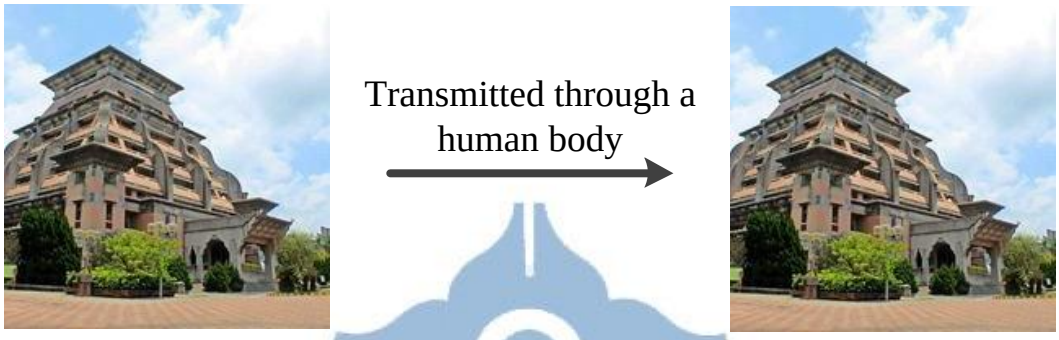


Fig. 4.6: Image transmission result in BCC

4.3 Bit Error Measurement with Frequency Drift

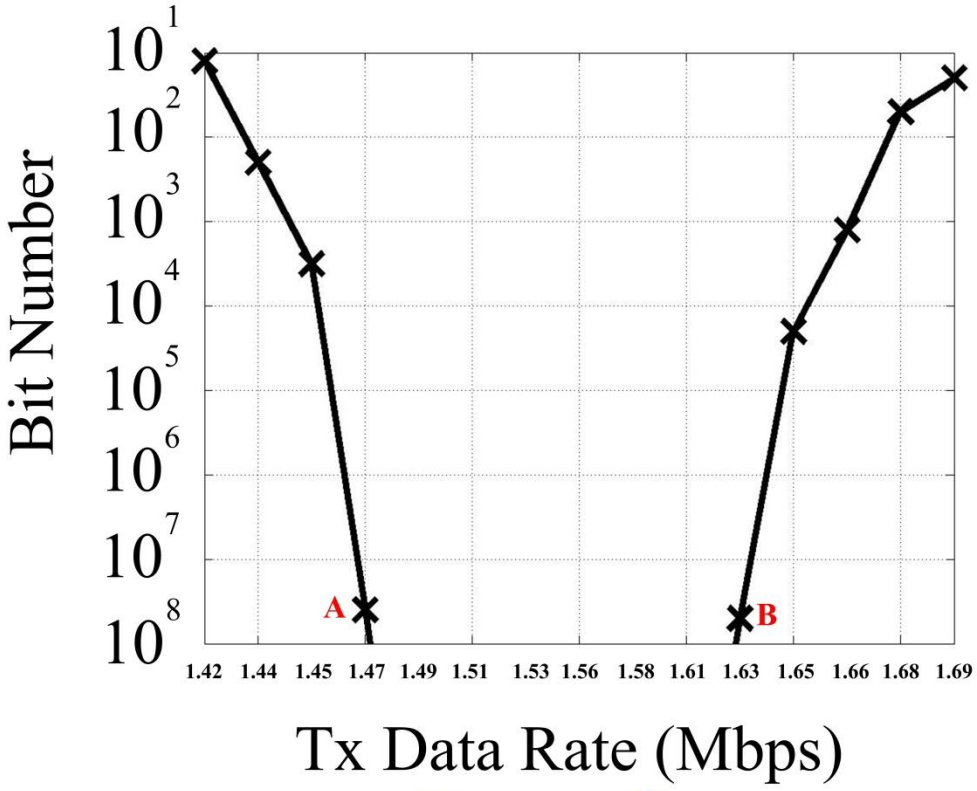


Fig. 4.7: Bit error measurement result with frequency drift

$$\text{Frequency Drift} = \frac{(\text{Drifted Freq}) - (\text{Central Freq})}{(\text{Central Freq})} \times 10^6 \text{ (ppm)} \qquad \text{(Eq. 4.1)}$$

$$\text{A} = \frac{(1.47) - (1.562)}{(1.562)} \times 10^6 = -5.88 \times 10^4 \text{ (ppm)} \qquad \text{(Eq. 4.2)}$$

$$\text{B} = \frac{(1.639) - (1.562)}{(1.562)} \times 10^6 = 4.92 \times 10^4 \text{ (ppm)} \qquad \text{(Eq. 4.3)}$$

Fig. 4.7 shows the bit error measurement result with frequency drift. The operation clock is constant in the receiver part. We adjust the offset frequency in the

transmitter part with respect to the operation clock in the receiver to emulate the frequency drift. The formula for the frequency drift calculation is shown in Eq. 4.1. In Fig. 4.7, the central frequency is 1.562 Mbps and the drifted frequency is determined by changing the operation clock in the transmitter. As shown in Fig. 4.7, the amount of the frequency drift of point A and point B are presented in Eq. 4.2 and Eq. 4.3, respectively. According to the measurement result, the BER is less than 10^{-8} when the frequency drift is from -58000 to 49000 ppm.

4.4 Summary of the Proposed BCC Transceiver

Table 4.3: BCC transceiver summary

Operating Range	600 kbps ~ 1.56 Mbps
Transmission Distance	10 ~ 140 cm
Core Voltage	1.0 V (for FPGA)
Power Consumption	27.5 W (w/o AFE circuit)
AFE Power Consumption	0.486 W
Sensitivity	-18.87 dBm
BER	10^{-8}
Energy/bit	17.884 μJ/b

Table.4.3 shows the summary of the proposed BCC transceiver. The data rate ranges from 600 kbps to 1.56 Mbps and the maximum transmission distance is 140 cm. The core voltage of the FPGA in the VC707 EVB is 1.0 V. The power consumption without AFE board is 27.5 W while the AFE power consumption is 0.486 W. The measurement result of sensitivity is -18.87 dBm. The bit error rate (BER) is less than 10^{-8} and the energy consumption per bit is 17.884 μJ/b at 1.56 Mbps.

Table 4.4: Comparison table

	[17] JSSC'09	[18] JSSC'09	[19] ISSCC' 09	[4] ASSCC'11	[11] ISSCC'14	[9] ISSCC'15	Proposed
Communication Method	FSK	FSK	Wideband Signaling	OFDM	Walsh Coding	Coherent BPSK	Wideband Signaling
Process	0.18µm	0.18µm	0.13µm	90nm	65 nm	65 nm	28 nm
Data Rate	60 kb/s ~ 10 Mb/s	500 kb/s ~5 Mb/s	8.5 Mb/s	14.55Mb/s	60 Mb/s	80 Mb/s	600 kb/s ~1.56 Mb/s
Modulation	Adaptive Frequency Hopping FSK	Binary Frequency Shift Keying	Correlation Direct Digital	Orthogonal frequency division multiplexing	3-level Walsh Coding	Binary Phase Shift Keying	Non-Return to Zero Inverted
Supply	1.0 V	1.8 V	1.2 V	0.5 V	1.1 V	1.2 V	1.0 V
Sensitivity	-65 dBm	-65 dBm	-56dBm	N/A	-58dBm	-58dBm	-18.87 dBm
Power Consumption	3.7mW	10.8 mW	2.75mW	0.67mW	10.87mW	8.9 mW	27.9 W
Area	2.30 mm^2	4.75 mm^2	0.19 mm^2	1.10 mm^2	1.12 mm^2	5.76 mm^2	N/A
BER	10^{-5} (10Mb/s) $<10^{-9}$ (60kb/s)	10^{-6}	$<10^{-3}$	N/A	$<10^{-5}$ @60Mb/s	$<10^{-5}$ @40Mb/s	$<10^{-8}$ @1.56Mb/s
Energy/bit	0.37 nJ/b	2.16nJ/b	0.32nJ/b	0.05nJ/b	0.18 nJ/b	0.079 nJ/b	17.884 µJ/b

The proposed design is implemented in the FPGA platform which can provide a reliable system clock. It is convenient to complete a HBC implementation such as an image transmission with the VC707 EVB and the AFE board. As compared with other BCC transceivers, it can achieve low bit error rate. Moreover, the architecture of the BCC transceiver is simpler than others which can reduce the hardware cost. It is worth mentioning that the BCC transceiver does not actually consume large power because some of the components in the FPGA are not used by the body channel communication. However, these components still cause the power consumption.

Chapter 5

Conclusion and Future Works

5.1 Conclusion

To understand the human body channel characteristics, we perform a lot of measurements to build up the human body channel model. An AFE PCB board is applied to amplify the attenuated signal from the human body and recover data back to the digital waveforms. Both the VGA gain and the DC level shifting in the AFE board can be controlled manually so as to overcome different attenuation in different transmission distance.

In the proposed BCC transceiver, the transmitter can either transmit the external data or generate internal random pattern by the LFSR circuit. Subsequently, the NRZI encoder encodes the data and the bit stuffer performs bit stuffing before the data are transmitted into the human body in the packet format. In the receiver part, the recover data from AFE PCB board are sampled by the 8x oversampling sampler and then outputs the clock signal and the data by the vote integrator. The LFSR checker can verify whether a bit error occurs in the LFSR pattern transmission. If the transmitted data are external data from the transmitter, we can output the data via UART and display on the computer.

Finally, we develop a FPGA-based BCC transceiver and implement on the FPGA platform. The proposed BCC transceiver can be downloaded to FPGA boards and connect to the AFE PCB board and the human body to complete an image

transmission. Moreover, the VC707 EVBs also contain some communication interfaces such as the SMA port, the UART interface and the JTAG that is flexible for human body channel to communicate with different devices to create the FPGA-based BCC implementation.

5.2 Future Works

As surveyed in the former research, some of the body channel communication applications rely on high transmission rate. Thus, the oversampling mechanism should be either adapted or replaced by other sampling mechanisms to raise the data rate to support the multimedia transmission. Moreover, high data rate transmission is more likely to suffer from bit errors. Therefore, we can apply error correcting to provide reliable and robust transmission quality. In order to achieve low hardware cost and low power consumption, we look forward to integrating all the circuits into a chip because both FPGA boards and AFE PCB board occupies enormous area. In addition, the chip definitely consumes less power than the total power of FPGA boards and AFE PCB board. If we want to apply an ADPLL to replace the FPGA board to generate the system clock, the effect of frequency drift and the calibration circuit should be taken into consideration. In addition, the communication setting among the FPGA board and the chip is an important issue.

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