國 立 中 正 大 學

資訊工程研究所碩士論文

使用標準邏輯元件及相對式參考模型技術設計之靜態電壓壓降偵測器與嵌入式矽振盪器

Design of a Static IR-Drop Monitor and An On-Chip Silicon Oscillator with Cell-Based and Relative Reference Modelling Approaches

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中華民國 一零四 年 七 月

摘要

由於現今的系統晶片整合度日益提高，對於晶片工作時的電力網路中壓降監控的重視度也更勝以往。本論文提出一個根據相對參考模型建立而成的全數位壓降監控器。 在一點 1.1V 電壓校正後，此全數位壓降監控器可以監控晶片的工作電壓，並且將增測到的電壓轉成數位的編碼輸出給後續系統晶片測錯和測試使用。他可以達到 0.027mV 的解析度且最大誤差為 16.4mV 在製程、電壓和溫度飄移之下。

此外，在先前利用相對參考模型建立而成的全數位震盪器也有所改進。改進了先前全數位震盪器中費時的邏輯閘選擇的過程，改以兩個可調整式的震盪器取代。利用控制兩個震盪器的控制碼來得到期望中溫度和電壓對應延遲比例的趨勢線。以上兩個研究皆是建構於相對參考模型並且在 90 奈米製程技術實現。

關鍵字：全數位，抗製成電壓溫度飄移，常態電壓監控，震盪器。

Abstract

Due to the high level integration of the system-on-a-chip (SoC), it becomes more and more important to monitor the IR drop of the power network during chip operation. In this thesis, an all-digital on-chip voltage sensor which uses a relative reference modeling (RRM) is presented. After one-point calibration at 1.1V, the proposed all-digital voltage sensor can monitor the operating voltage of the chip and outputs digital codes for SoC chip debugging and testing. It achieves a 0.027mV resolution and has a maximum error 16.4mV with process, voltage, and temperature (PVT) variations.

In addition, the prior work of the on-chip oscillator with RRM is improved. The timing consuming cell selection flow in prior on-chip oscillator design can be reduced by two digital controllable oscillators. The control codes of the two DCOs are adjusted to achieve the desired trend lines of delay ratio versus temperature and voltage curve. As a result, the frequency error of the on-chip oscillator can be reduced. Both the proposed relative reference modeling based static IR-drop monitor on-chip silicon oscillator are implemented in 90nm CMOS process.

Keyword: all-digital, static IR-drop monitor, oscillator, tolerance PVT variations

Acknowledgments

Content

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Static and Dynamic IR Drop Analysis in SOC Design Verification and Testing

The process technology has enhanced rapidly and the number of devices on a chip has grown aggressively and it causes SoC has many challenges than before. According to Moore's law shown in Fig. 1.1. The numbers of transistors in a chip will double every two years, and the integration level of the system-on-a-chip (SoC) also becomes higher than before.

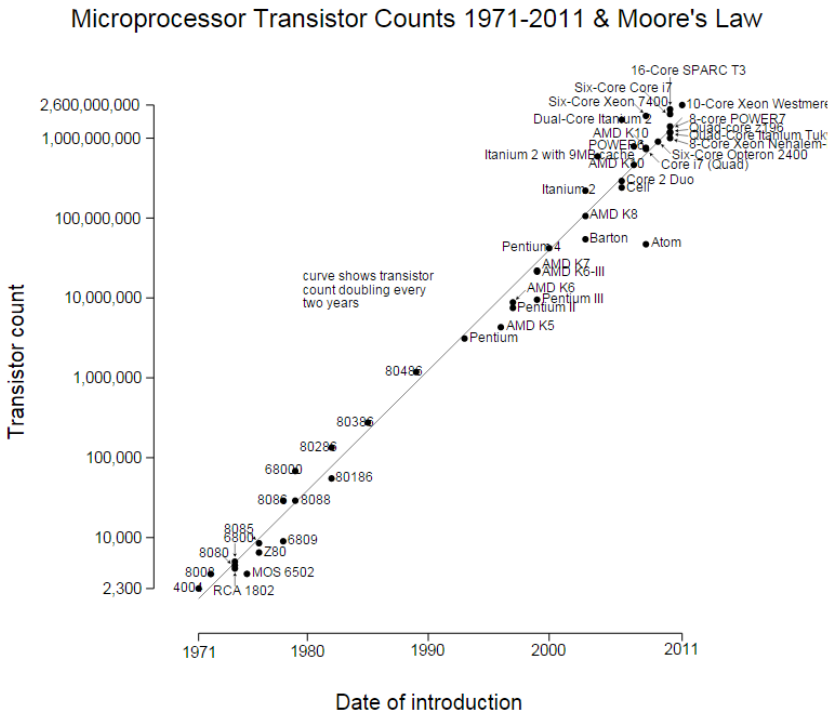

Fig. 1.1 CPU transistor counts against fates of introduction

1.1.1 Current Challenges in Semiconductor Industry

One of the main challenges in semiconductor industry is the variability in devices and circuit parameters which will harm the performance and the energy efficiency of the circuit. Parameters are separated into two groups such as static and dynamic behaviors due to their temporal features. The static parameter variation is produced during manufacturing process and is known as process variation. Although the static parameter may change from die to die, but it is static after fabrication. The dynamic parameter variation happens when the chip is operating including working conditions and surrounding environment. Dynamic parameter variations includes supply voltage drop which known as voltage variation, temperature gradient which known as temperature variation, and transistor aging effects [18]. The random variations, process, voltage and temperature (PVT) are major challenges to the high performance SoC.

Fig. 1.2 presents the distributions of frequency and standby leakage current of the microprocessors within a wafer where every spot refer to a different chip. The spread in frequency and leakage distributions is caused by variations in transistor parameters and it results in about 20 times of variations in leakage current and 30% variation in chip frequency. The most concern groups are highest frequency chips with large leakage and low frequency with high leakage chips which may affect the yield [19].

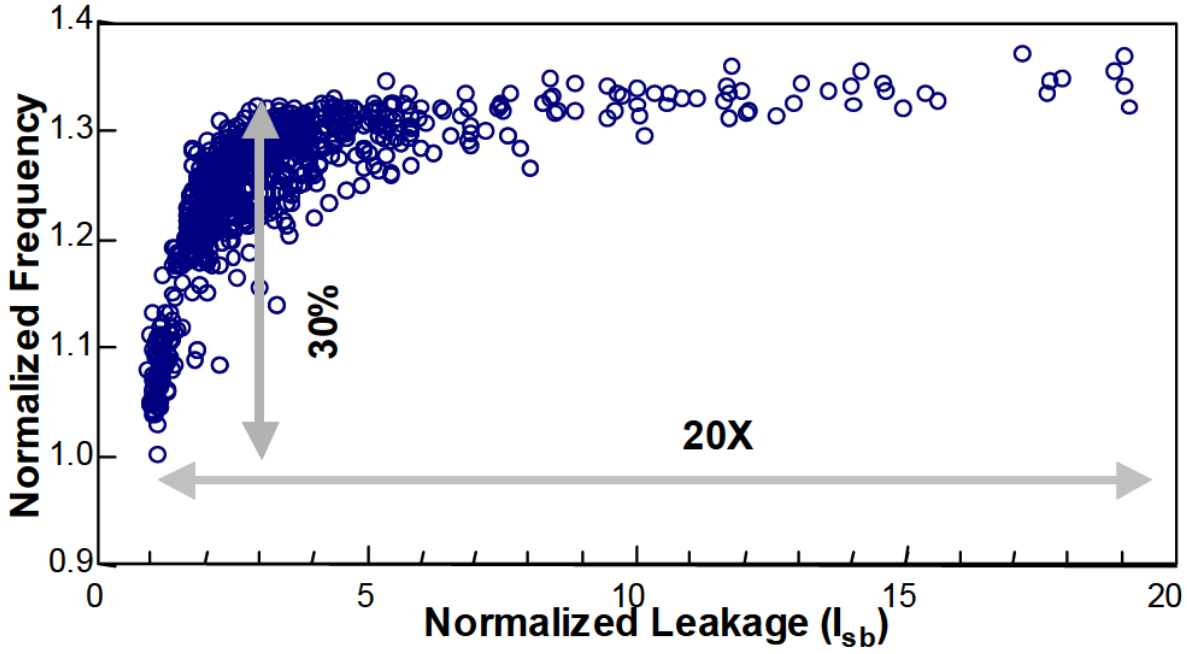

Fig. 1.2 Leakage and frequency variations [19]

The variation in channel length and variations in the threshold voltage cause the spread in standby current. Fig. 1.3 illustrates the die-to-die V_t distribution and its resulting chip I_{sb} variation. The figure of V_t variation is a normal distribution whose 3σ variation is about 30mV in a 180nm CMOS logic technology which causes a significant variation in circuit performance and leakage. The most sever critical paths in a chip may be different from chip to chip. Fig. 1.3also shows the 20 times of I_{sb} variation distribution in detail [19].

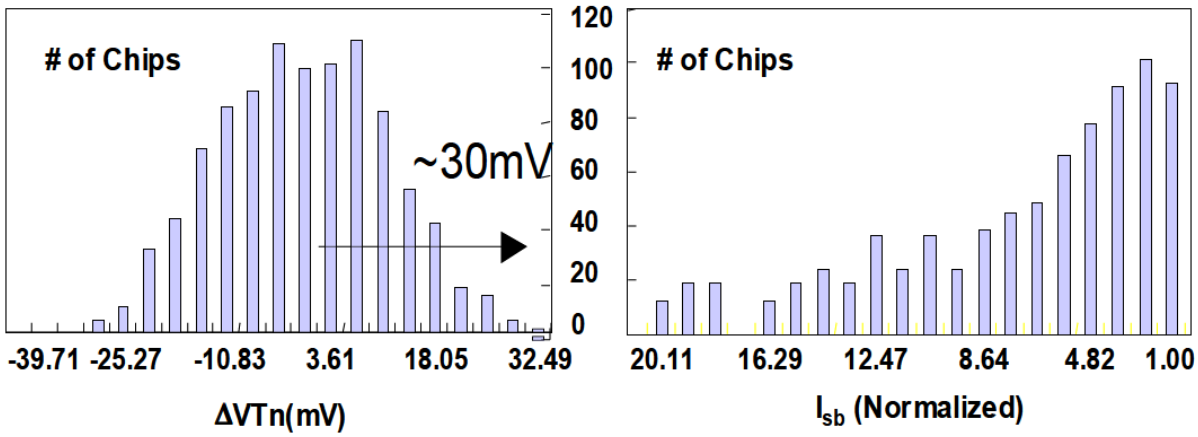

Fig. 1.3 Die-to-die V_t, I_{sb} variation [19]

From above discussion we can clearly understand the process variation within wafer bring significant effect to the performance and stability to microprocessors. In the following section we will head to voltage and temperature variation.

Uneven power dissipation across the die is caused by the variations in switching activity across the die and diversity of the type of logic. This variation results in uneven supply voltage distribution and temperature hot spots, across a die, causing transistor subthreshold leakage variation across the die. Due to the difficulties in scaling threshold voltage (Vt), and to meet the transistor performance goals. Maximum Supply voltage V_{cc} is specified as a reliability

For the target performance, limit for a process and minimum V_{cc} is required. V_{cc} variation inside the max-min window is shown in Fig. 1.4. This figure shows a droop in V_{cc}, which degrades the performance. Packaging and platform technologies do not follow the scaling trends of CMOS process. Therefore, power delivery impedance does not scale with V_{cc} and ΔV_{cc} has become a significant percentage of V_{cc}[19].

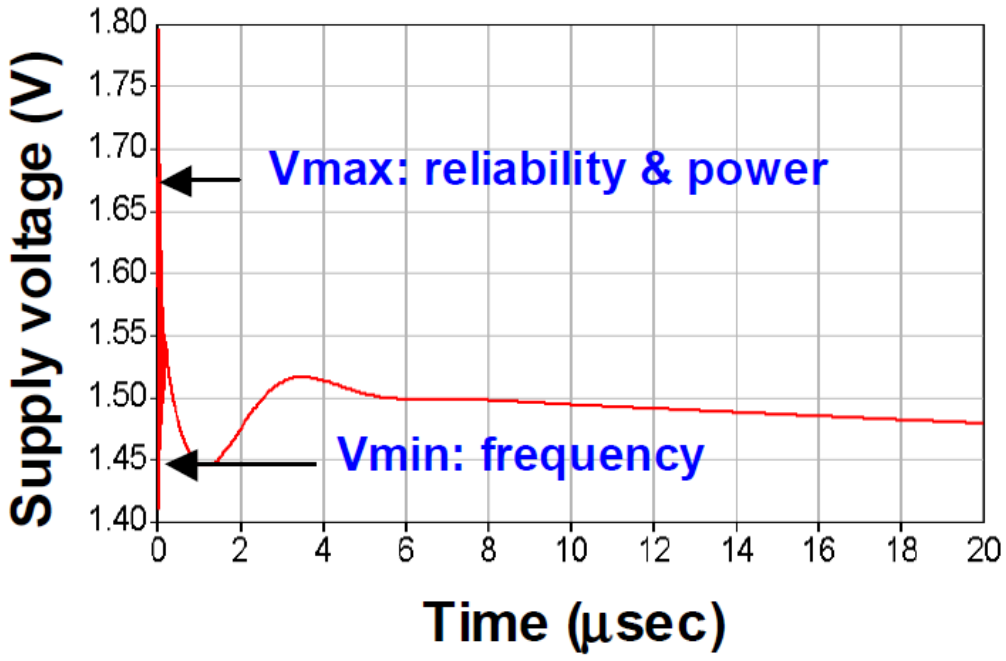

Fig. 1.4 Supply voltage variation [19]

Fig. 1.5 shows the thermal image of a leading microprocessor die with hot spots. The warm colors in the thermal image show the heating locations, and cold colors refer to the cooler part of the die. Within die temperature fluctuations have become major performance and packaging challenge for microprocessors. Both devices and interconnects are effected by temperature that higher temperature will cause performance degradation. Additionally, temperature variations across communicating blocks on the same chip may cause performance mismatched and lead to logic or functional failures [19].

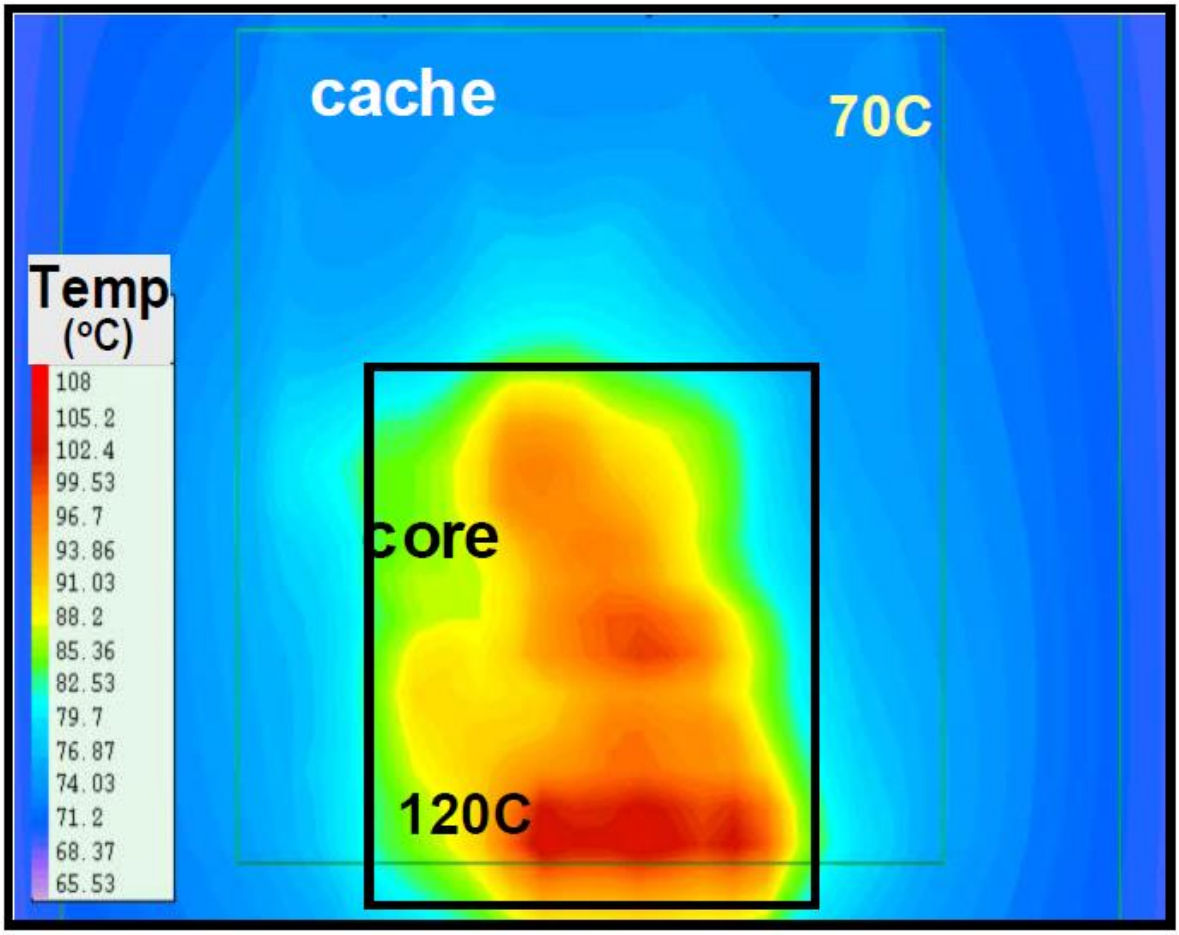

Fig. 1.5 Withing die temperature variation [19]

The demand for low power consumption makes voltage variations being unignorablys. We had discussed the impact of PVT variations on circuits and microprocessors. In the section 1.1.2, we discuss voltage drop and also search for the solutions for PVT variations compensation. Moreover, we will also present possible solutions to reduce or tolerate the parameter variations in high frequency microprocessor design.

1.1.2 How Dynamic and Static Voltage Drop Affect Circuit

Power is defined as the product of voltage (V) and current (I) which shown in Eq. 1.1.

$$P = IV \qquad \text{(Eq. 1.1)}$$

The sources of power dissipation can be classified into three types. Firs type is called dynamic power dissipation which is caused by the circuit activities when the node value changing from 1 to 0 or vice versa at logic gates. The formula for dynamic power consumption is expressed in Eq. 1.2.

$$P_d = CV^2f \qquad \text{(Eq. 1.2)}$$

The second type of power dissipation is short circuit current which is generated during the rise/fall time of the circuit input. The above two types of power dissipations are occurred while the circuit is active. The third type of power dissipation is called static power dissipation which will consume power even when the circuit is stand-by. We can classify above power dissipations into two types, as dynamic power and static power dissipations. The dynamic power consumption happened when the CMOS logic gate drive their outputs to new values. The static power is consumed even when the logic gates are inactive and the output values are not changed. The current flow through the power to the ground rails only happened during active state except leakage current. The circuit generates a resistive path to draw current from the power rails when nodes switching their states which bring the current flow of the design [10].

As process technique advancing aggressively, the operating voltage toward low voltage and reduces the dynamic power dissipation. However, over voltage which is the difference between operating voltage is also reduced of the threshold voltage, and sub-threshold conduction becomes more and more important. Despite that, the above power dissipation can be estimated by Computer-Aided Design (CAD) tools. Voltage fluctuation during work time which known as voltage drop or IR-drop is hard to be predicted by CAD tools since there are too many possible conditions.

The voltage drop occurs due to the suddenly increase of the switching activities in microprocessors, and large current transient in the power rail. Thus, voltage drop contains two parts, DC and AC. The DC part is due to the resistance of the power rail network and when current flows resistance causes voltage. The AC part is generated by the parasite resistance, inductance and capacitance (RLC) response for current change [10]. The voltage drop will increase with the delay of a logic gate. The supply voltage fluctuation is shown in Fig. 1.6. The inductance (L) and capacitance(C) of the package, the socket and the motherboard are the main reason of the noise for mid frequency (1-10 MHz) circuit which spread all across the die [8]. The noise of the low frequency is mastered by L and C of the Voltage Regulator Module (VRM) and the motherboard. Fig. 1.6 shows the factors which influence the voltage noise and worsen the performance of microprocessors.

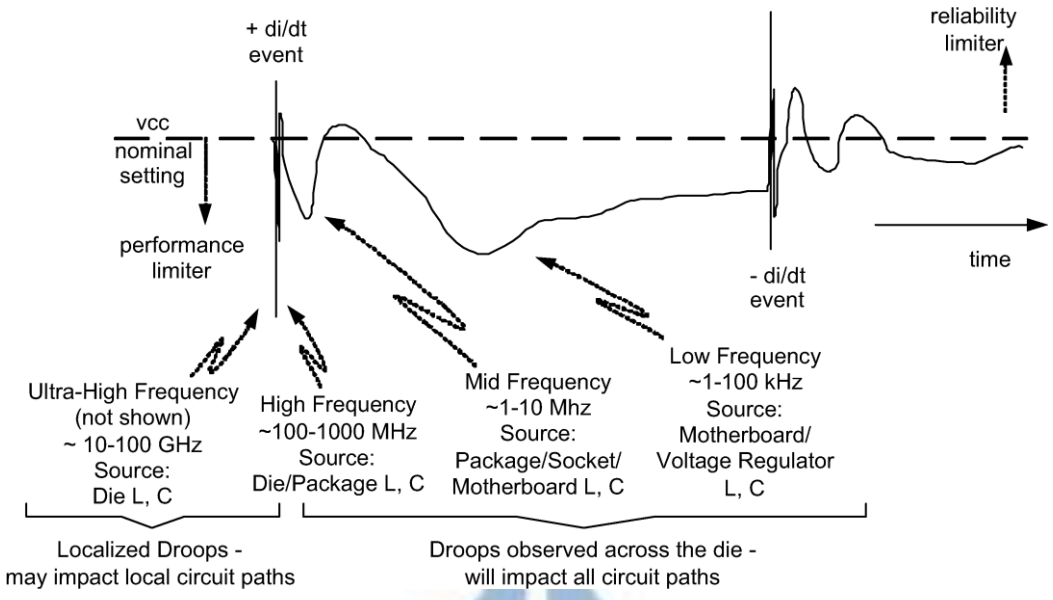

Fig. 1.6 Diverse supply voltage variation in frequency domain [9].

When the on chip voltage varies on a time scale which is comparable to the cycle time of the circuit, and then the switching speed will be affected [15]. Voltage fluctuation may cause the performance of the design unpredictable. The high performance modern microprocessor may cause more severe voltage drop phenomenon due to their higher operating frequency [18]. Fig. 1.7(a) shows the difference before taking supply noise into consideration of an SRAM. The measurement result is different from simulation result. Fig .1.7(b) takes voltage variation into consideration, and the curve of measurement result can close to the simulation results of an SRAM [15].

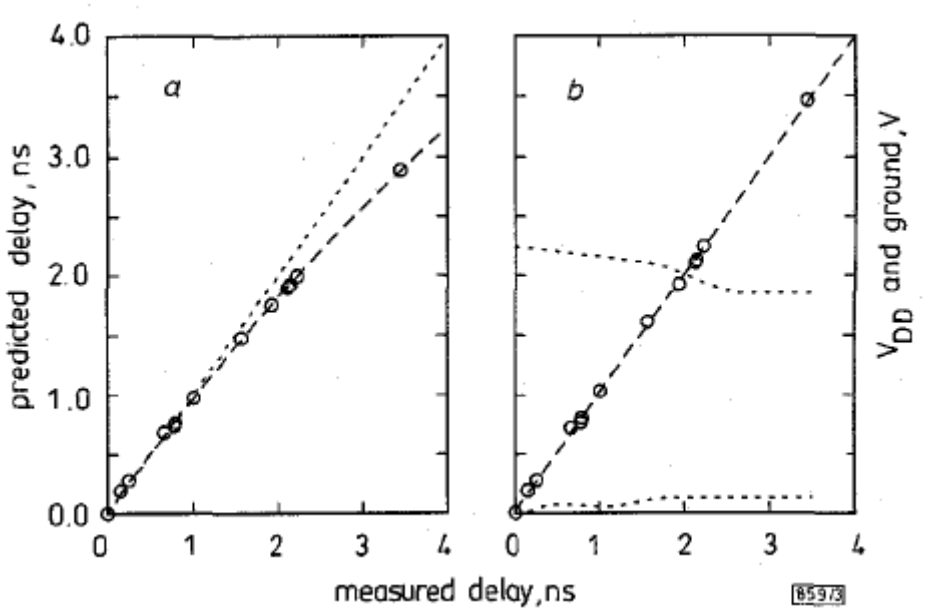

Fig. 1.7 Predicted delays against measured delay in SRAM [15]

As a result, it is essential to monitoring the fluctuation of the voltage and taking it into consideration on circuit design. Furthermore, voltage fluctuation information can provide more important diagnosis information for design when chip is failure, and it also make power efficiency and performance more predictable.

1.2 Survey of Conventional On-Chip Voltage Sensor for IR Drop Monitoring

As discussed in previous sections, voltage fluctuation in microprocessor is unignorably. As a result, plenty of voltage sensors have been proposed.

There are mainly two IR-drop monitoring applications. One is aimed to estimate real-time (dynamic) IR-drop and the other is targeted on long-term (static) IR-drop. Each of them is applied for different fields. Fig. 1.8(a) shows an VDD waveform example and Fig. 1.8(b) shows the example of sampling the VDD waveform with 1 GHz sample rate. From the Fig 1.8(b), we can see that the purpose of real-time IR-drop monitoring is to catch every voltage change versus time. However, most of the circuits have certain voltage-drop tolerant, and a dynamic IR-Drop circuit usually takes a lot of cost and power consumption. Instead, we study in designing a static voltage sensor which can detect the average IR-drop with a simpler architecture with relatively less power consumption and relatively low calibration cost.

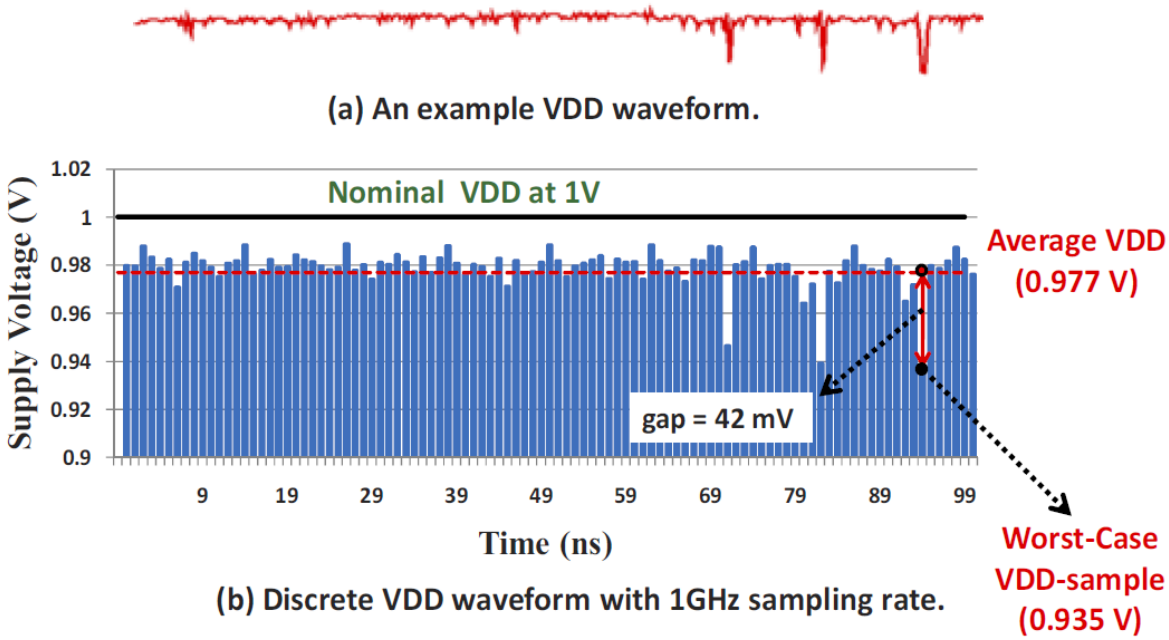

Fig. 1.8 An example VDD waveform and its sampled version at 1 GHz sampling rate [13]

1.2.1 Voltage Sensor for Dynamic IR-Drop Monitoring

The dynamic IR-Drop monitor aims to track the real-time voltage fluctuation. This type of voltage sensors often require high sampling rate to sample the high frequency transients. We will discuss different methods in the following paragraph to get a closer view to the real-time voltage sensor.

In the previous research, an ADC is commonly used to sample the analog voltage into digital codes [20]. However, in this voltage sensor the power consumption is extremely high (49 mW) and the chip area is also large (1.2 mm^2). Furthermore, in this voltage sensor, the sample rate does not reach the required sample rate as GHz. After a year, the related work [31] uses a high speed ADC to perform the measurement on VDD. The power consumption in the voltage sensor is also very could be extremely high (nearly 50 mW), and this could make this direct measurement scheme useless. It is important that an embedded IR-drop

monitor should not consume too much power. Otherwise, the voltage sensor worsens the IR-drop.

In [30], they compare the sampled VDD signal with an external threshold voltage to produce a one-bit result to inform whether there has any abnormal IR-drop. Even though this method provides a high sample rate, it cannot provide the information about the worse IR-drop. Therefore, the decision of picking appropriate operating voltage is difficult.

The logic gates density is high in the modern VLSI circuit. When there are several gates connect to a M2-M3 via and simultaneously switch, the region of a M2-M3 via may cause voltage drop in the power supply which is known as droop [14]. The analog on die droop detector [9] proposes a method which compares the difference between sampled VDD signal and external supplied threshold voltage to generate a one-bit result signal to warn if there existing any IR-drop. The system architecture is shown in Fig. 1.9 which contains three main units including a control unit, a reference unit and a detector module.

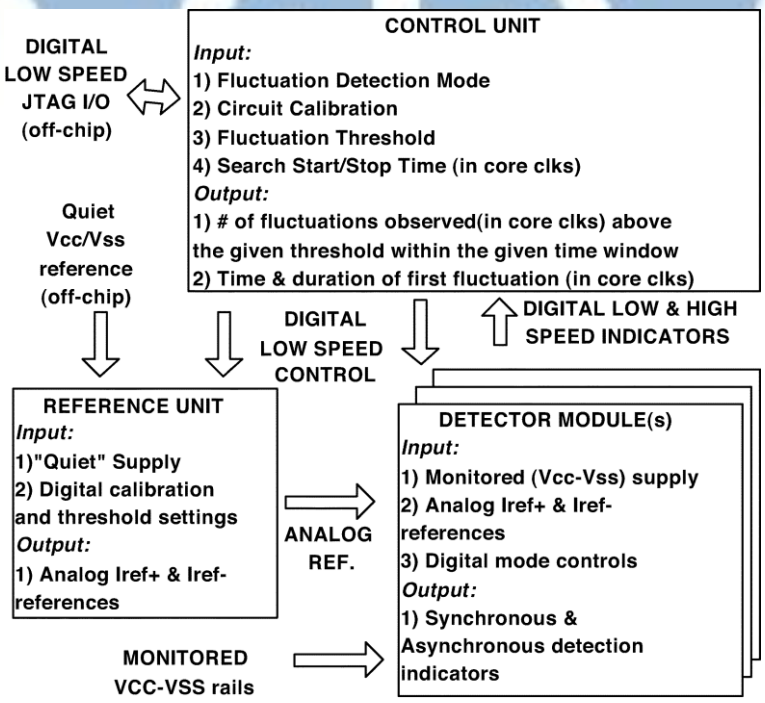

Fig. 1.9 On-die droop detector (ODDD) architecture [9]

The Control Unit is the interfaces to the external world using the standard JTAG port and it implements the following features, negative versus positive overshoot detection, noise level and duration detection settings, start/stop time for the droop search window, PVT calibration for the analog circuits. The reference unit uses a non-noise supply pin to provide a differential analog input to the detector module. The on-die droop detector modules are cloned and placed at different location to compare the monitored local power supply(Vcc-Vss) level with the threshold which is set via I_{ref}^{+}/I_{ref}^{-} pair. The asynchronous results record the change events via the JTAG clock. Then, the second output is synchronized to the core clock for higher time resolution and for improving the capability of event-filtering.This on-die droop detector (ODDD) aims to provide a high sample rate as multigigahertz. However ODDD unable to provide further information about how sever does. Moreover, the decision of appropriate threshold voltage is hard to decide itself [9].

The recent work [13] provides high accuracy and a high sampling rate by adopting the popular method VDD-to-Time-to-Digital Conversion (VTDC) to convert the voltage measurement results into an oscillator period measurement problem. Furthermore, it also using dynamic voltage scaling (DVC) design methodology and assumes the availability of several clean VDD reference voltages (0.8V, 0.9V, 1.0V) as the work proposed in [12]. The proposed system architecture of [13] is shown in Fig. 1.10. This work contains two modes, the calibration mode and the monitoring mode. During the calibration mode, the monitor circuit uses several VDD reference supply voltages (which are assumed to have no IR-drop), to the monitor circuit. 8-bit digital codes are generated for each VDD reference voltage. The relation between the VDD reference voltages and their corresponding output codes are modeled mathematically as a VDD-versus-output-code dictionary. During the monitoring mode, a time-varying VDD signal under monitoring is applied to the monitor circuit for a designated monitoring window. In the sequel, this signal is denoted as VDD-monitored. At

the end of the monitoring window, an 8-bit digital code will be produced, which is correlated to the smallest VDD level (or the worst-case IR-drop) during the monitoring window [13].

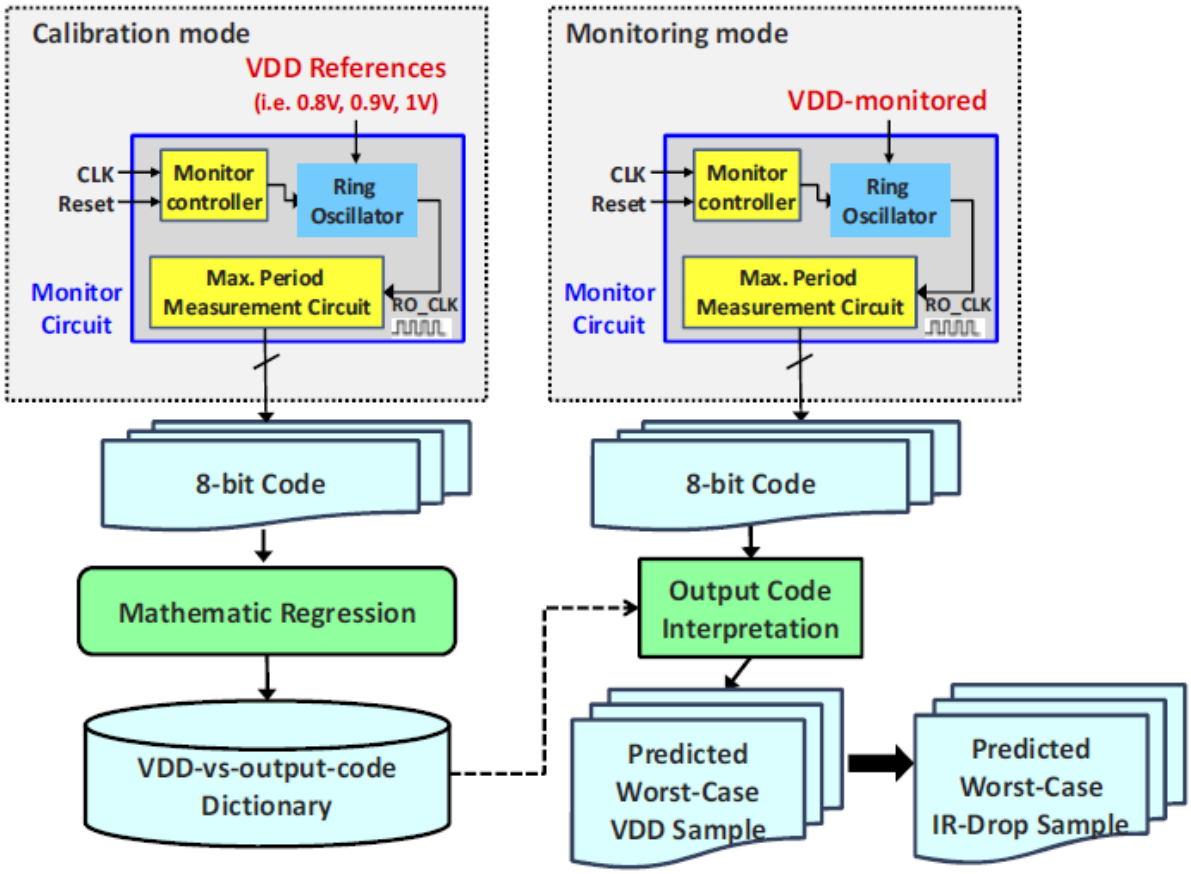

Fig. 1.10 Overview of the worst-case IR-drop monitoring method [13]

Fig. 1.11 shows the operating sequence of the system. First of all, it begins with a calibration session and follows with a sequence of measurement sessions. Each of the measurement session further consists of three intervals which are the monitoring interval, the settling interval and the output interval. During monitoring interval, the monitor circuit continuously receives the IR-drop-bearing oscillation signal which is about 1 ns. Assume that the monitoring interval is set as 1000 ns, then there will be approximately 1000 clock cycles to be examined and the maximum one will be recorded. The settling interval is for computing the output code after the oscillation signal stops and passes the code to the monitor circuit. The period of settling interval depends on the latency for a signal to travel through the monitor circuit which is about 100 ns. Finally, the output interval is the time for the monitor circuit to report the output code before another measurement session start [13].

This voltage sensor does meet its goal to have a high sample rate as 1.193 GHz and high accuracy as the maximum error voltage less than 4.81 mV. However, the voltage sensor [13] needs to execute the calibration process periodically (e.g. every 1ms) for compensation for temperature variations. In addition, in each calibration process, it also requires three input reference voltages (0.8V, 0.9V, and 1.0V) for 2nd-order polynomial regression which makes the voltage sensor [13] not easily applicable for SoC design.

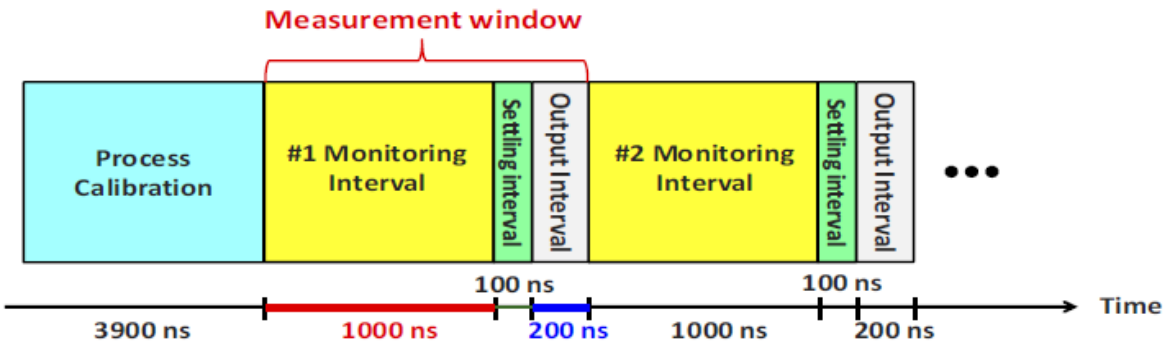

Fig. 1.11 A typical operation sequence [13]

Another similar work proposed in [23] compares the voltage sensor performance between [12] and [23]. It mentions that there are two main drawbacks of using mitigator transistor to provide a current variation of the opposite sign with respect to the one generated by the concurrent activation of the sinking circuit blocks of the system under control. Firstly, adding a mitigator will increase power consumption. Secondly, it needs an external signal to trigger the mitigator before the droop event [23]. To overcome those problems, [12] adding a feedback logic as shown in Fig. 1.12 to control the inducers to allow them flowing the real time droop event and mitigate it. In Fig. 1.12 the gate of an NMOS mitigator and the drop event is controlled by the same voltage. When VDD is normal, M2 conducts a constant current. Otherwise, if the droop event causes VDD lower than the normal condition, the mitigator will become led conductive to reduce the current flow through it. However, this work did not take any PVT variation into consideration.

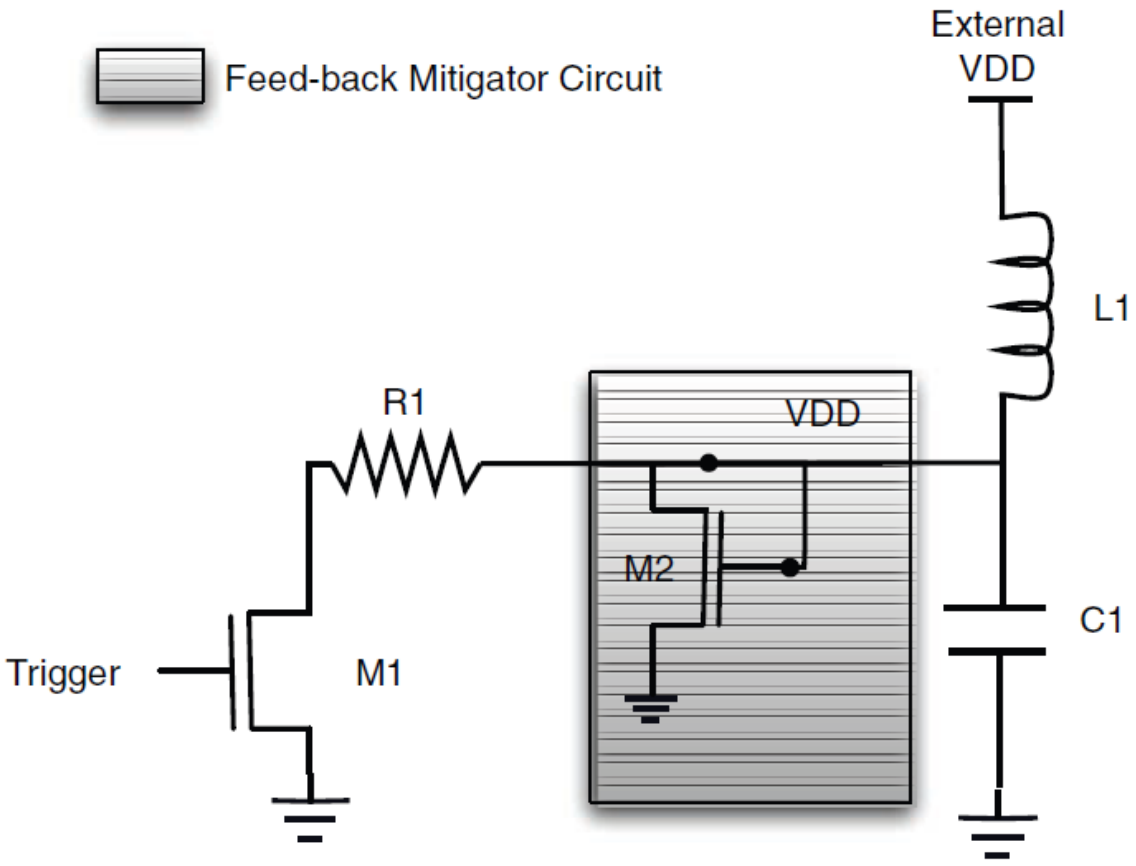

Fig. 1.12 Feedback based droop mitigation [23]

Another monitoring technique proposed in [24] uses the oscillation frequency of a ring oscillator as the metric of effective power supply voltage. Fig. 1.13 shows the measurement circuit called “gated oscillator” which gate the ring oscillator by the transmission gate. The construction of this gated oscillator is built by inverters, and NAND gate and transmission gates from standard cell libraries.

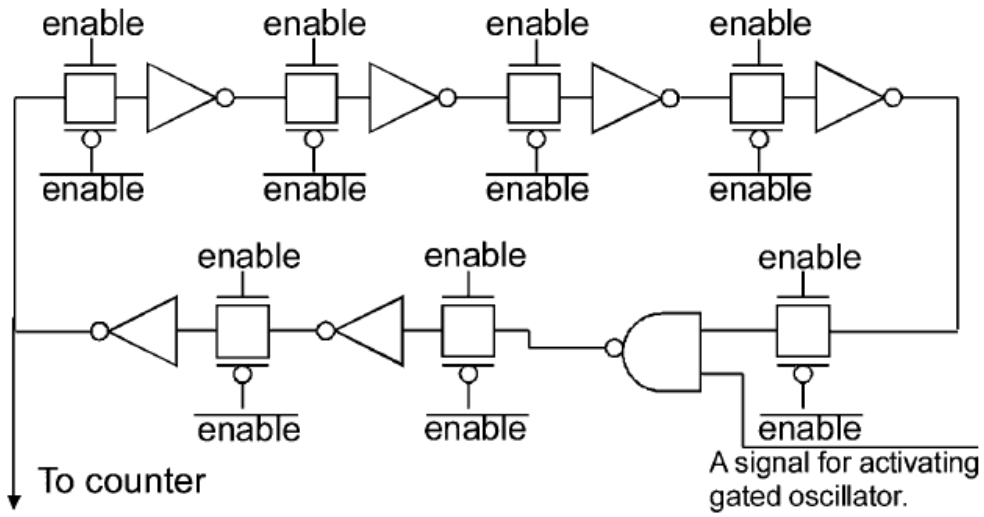

Fig. 1.13 Gated oscillator [24]

The operation of gated oscillator is shown in Fig. 1.14. While enable signal equals 1, the gated oscillator begins to oscillate, and while the enable signal turns to 0, then the oscillation is stopped by the transmission gates. The cycle count of the oscillator is recorded. The supply waveform is sampled while the enable signal is equal to 1. Otherwise, the operation of the gated oscillator is hold.

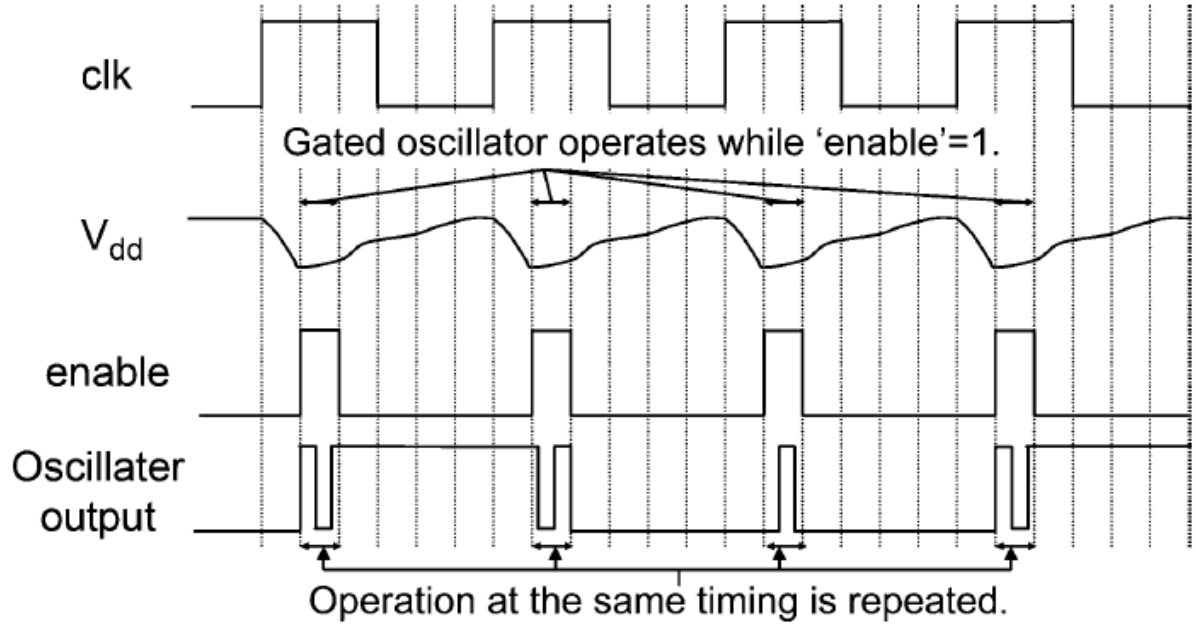

Fig. 1.14 Operation of gated oscillator [24]

The gated oscillator needs a cycle counter to repeatedly obtain the toggle count for accurate measurement. The measured voltage waveform is reproduced at each sample time as shown in Fig. 1.15. The measured voltage is computed from the toggle count and the prepared calibration table. The calibration table describes the relation between the measured voltage value and the toggle count, and this table is constructed by measuring the toggle count without any noise varying the voltage supplied to the proposed circuit. The measured voltage is the average voltage value of the actual waveform during each time slot. As a result, the bandwidth of the voltage sensor depends on the width of the time slot during measurement.

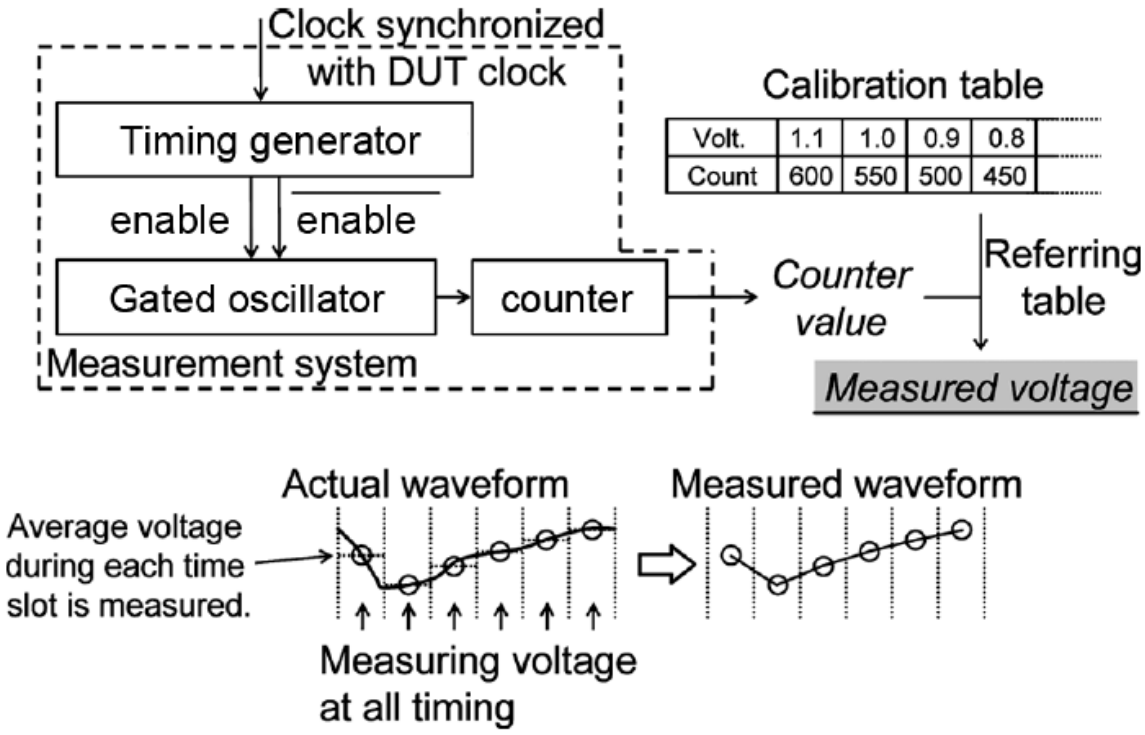

Fig. 1.15 Waveform measurement with gated oscillator [24]

This gated oscillator provides the smallest area to be embedded within the chip. However, the monitor can linearly trace severely limited range of the noise magnitude. The large dynamic range is desirable for chip-wide measurement within all voltage domains of digital and analog circuits.

1.2.2 Voltage Sensor for Static IR Drop Monitoring

The static IR-drop monitor aims to track the average voltage variation in long-term. These types of voltage sensors often require longer periods to catch the long-term voltage transient behavior. We will discuss different methods in the following paragraph to get a closer view to the long-term voltage sensor.

The method proposed in [6] is ambitiously provided a high accuracy, low power and wide voltage range PVT sensor without using voltage/current analog-to-digital

convertor(ADC) or the bandgap reference to avoid high power consumption and large area cost as compared to the voltage sensor with an ADC [20]. The system architecture of this PVT sensor is shown in Fig. 1.16, and it consists of four main blocks, a temperature sensor, a voltage sensor, a voltage reference and a process sensor.

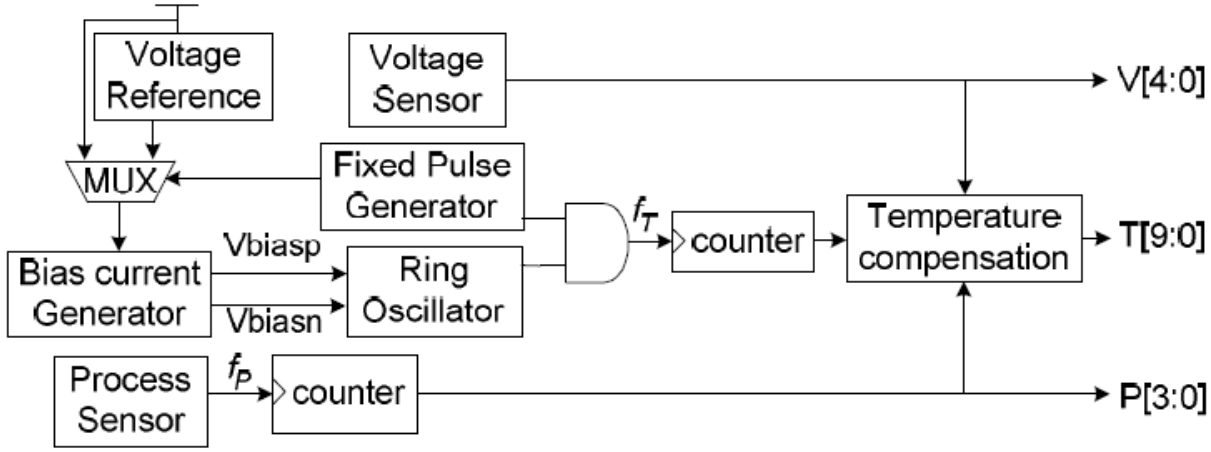

Fig. 1.16 Architecture of the PVT sensor circuit [6]

First of all, the temperature sensor produces proportional frequency (f_T) to measure the temperature. The frequency passes through the counter and generates a corresponding temperature code T [9:0]. However, this T [9:0] digital code contains the effects of the voltage and process variations. As a result, the voltage sensor and process sensor is built to remove the variations of temperature and process. The process sensor designed with zero temperature coefficient (ZTC) characteristics which the ZTC point of NMOS and PMOS are at 0.4V and 0.6 V respectively. The PMOS and NMOS mutual current are compensated at 0.5V to make the result immune to the temperature variation and generate current process information P [3:0] as shown in Fig. 1.17. The counter converts the output frequency (f_p) into 4-bit digital code P [3:0] from SS corner (0100) to FF corner (1111).

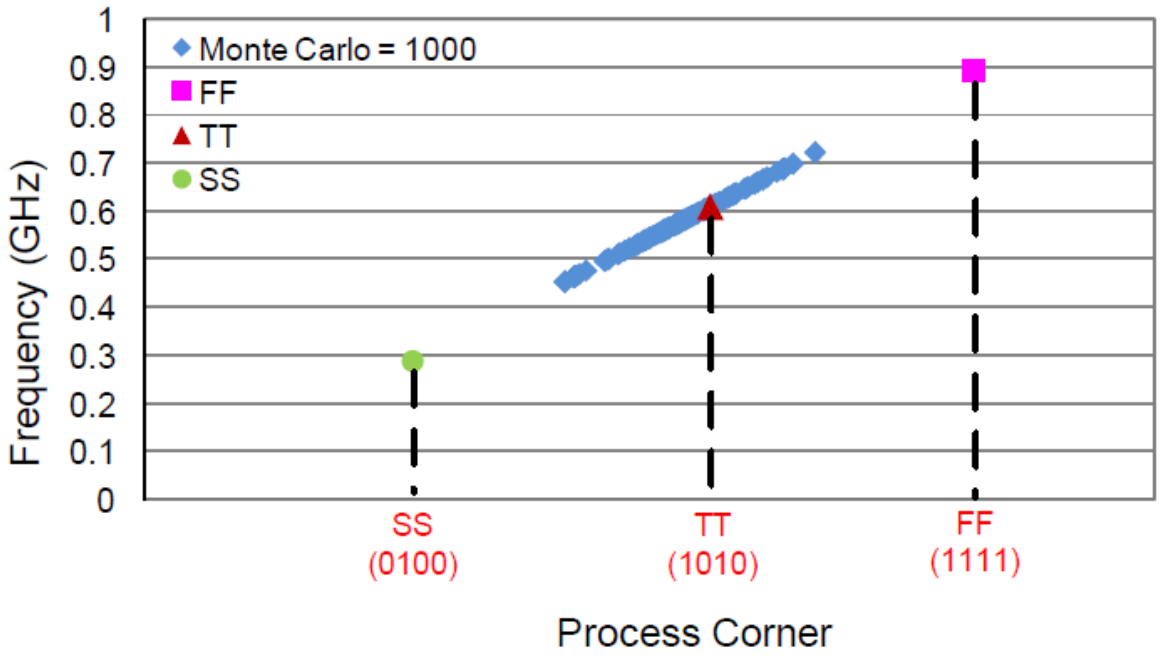

Fig. 1.17 Process sensor simulation results [6]

The voltage sensor used a novel ultra-low voltage to time convertor (ULV^{2}TC) to convert the input analog voltage into time or phase information. It converts input voltage to a 5-bit digital code V [4:0] as shown in Table 1.1 and using the control bit to compensate process variation. TABLE 1 represent the V[4:0] for different voltages, and the quantization step is 50 mV [6].

Table 1.1 Voltage sensor digital code table [6]

Vin	**Digital Code**				
	V[0]	V[1]	V[2]	V[3]	V[4]
0.3V	1	0	0	0	0
0.35V	0	1	0	0	0
0.4V	0	0	1	0	0
0.45V	0	0	0	1	0
0.5V	0	0	0	0	1

However, this work cannot provide precise environmental voltage information and the

0.5 mV resolution of voltage sensor is good enough. Furthermore, it doesn't take account temperature variation effect to voltage sensor which may affect the accuracy of the voltage sensor.

The enhanced work of [13] is proposed in [7] which improves the resolution and is able to work in near subthreshold voltage range. It can easily apply to ultra-low voltage dynamic voltage and frequency scaling (DVFS) platform. Unfortunately, the disadvantages of this work are such as imprecise voltage output and without compensating for temperature variations of the voltage sensor.

The similar work proposed in [12] also aims to measure the magnitude of the voltage droop event. It is assumed to achieve high accuracy IR drop by using the VDD-to-Time-to-Digital conversion (VTDC) method. The voltage sensor [12] requires three different input reference voltages for sensor calibration. Each on-chip voltage sensors are calibrated individually, and the process variation of the voltage sensor is normalized after calibration. However, the error of the voltage sensor will be increased accordingly with temperature variations after chip calibration since the calibration for each voltage sensor is performed once.

The high performance and low power are becoming much higher demand in mobile application system-on-a-chip (SoC). As a result, an on-chip low dropout (LDO) voltage regulator is required. It can supply suitable voltage for each circuit block of the SoC depending on its performance requirements. In addition, it is able to suppress voltage noises generated in the switching DC-DC converter. However, many LDOs are needed in the SoC in order to provide different voltages for the blocks. Hence, reducing the area of the LDOs

is an important challenge. Recently, digitally controlled LDOs are discussed for their low sensitivity to process variations and low voltage operation [3]. The architecture of digitally controlled LDO is shown in Fig. 1.17.

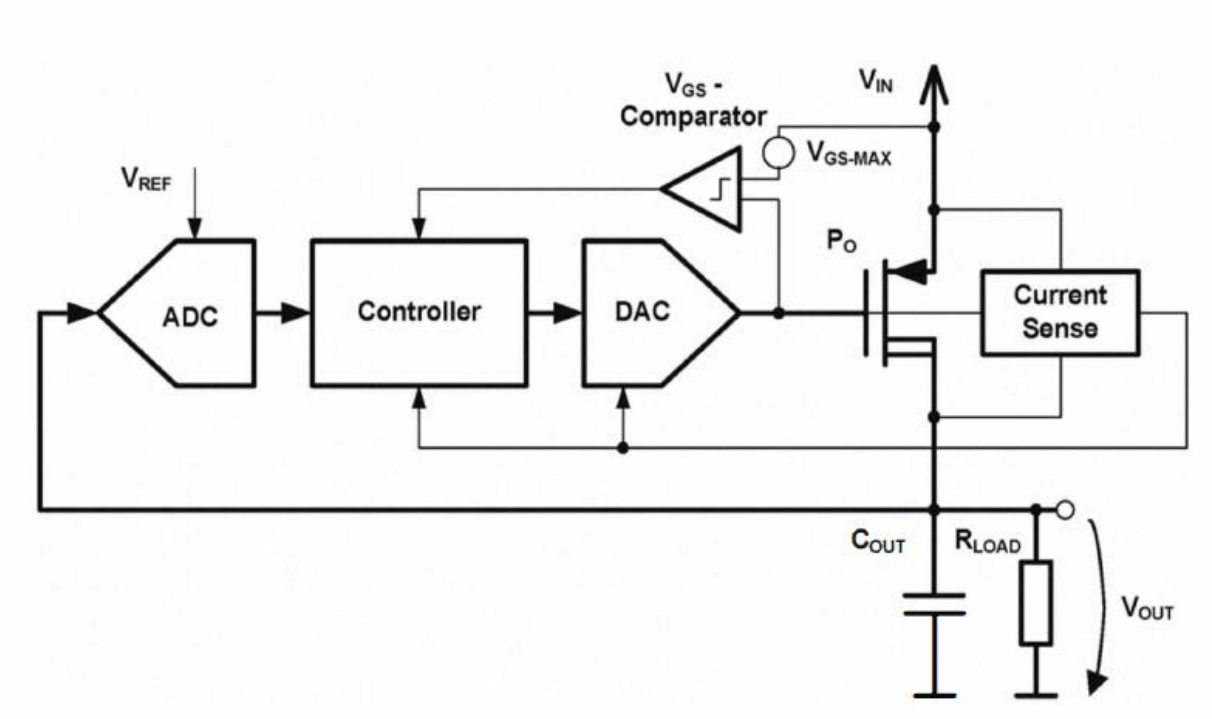

Fig. 1.18 Block diagram of the digitally controlled LDO [3]

This LDO consists of six major components as depicted in Fig. 1.18, which are a PMOS pass transistor P_o, a current sensing circuit, a ADC, a DAC, a digital controller and a gate-source overvoltage comparator. The output voltage is sensed by the ADC. The controller calculates the actuating variable by the digitized output voltage, and then the DAC converts this result into the current to drive the gate of the pass transistor P_o. The drain current of Po generates the output voltage on the R_{LOAD} and the capacitor C_{OUT}.

However, the analog-to-digital converter (ADC) and the digital-to-analog converter (DAC) blocks are analog circuits which need large chip area. Also, digital-control DC-DC converters included an analog-to-digital converter (ADC) is a quite complex analog circuit block. Furthermore, it does not show any technique to take care of the process variation.

In [4] a tunable critical path replica based dynamic variation monitor which is able to capture voltage or frequency fluctuations. However, the drawbacks of the existing on-chip monitors are that the monitors require high area overhead due to the presence of analog blocks or customized operations. The sensors monitor the noise events dynamically at each clock cycle. As a result the worst case scenario is often unseen. Furthermore, the sensors cannot compatible in SoC's architectural.

A digital voltage sensor [1] using the characteristics of FinFET devices including superior ability in controlling leakage and minimizing short channel effects to build the controllable delay element to govern the propagation of the clock input. Fig. 1.19 shows the relationship between the input voltage V_{in} and the propagation delay of the controllable delay element (CDE) in which Vin increases gradually from 0.7 V to 1.1 V by the step of 50 mV. It can be seen that the propagation delay of the CDE is linearly proportional to V_{in} which means that we can control operation of CDE by V_{in}.

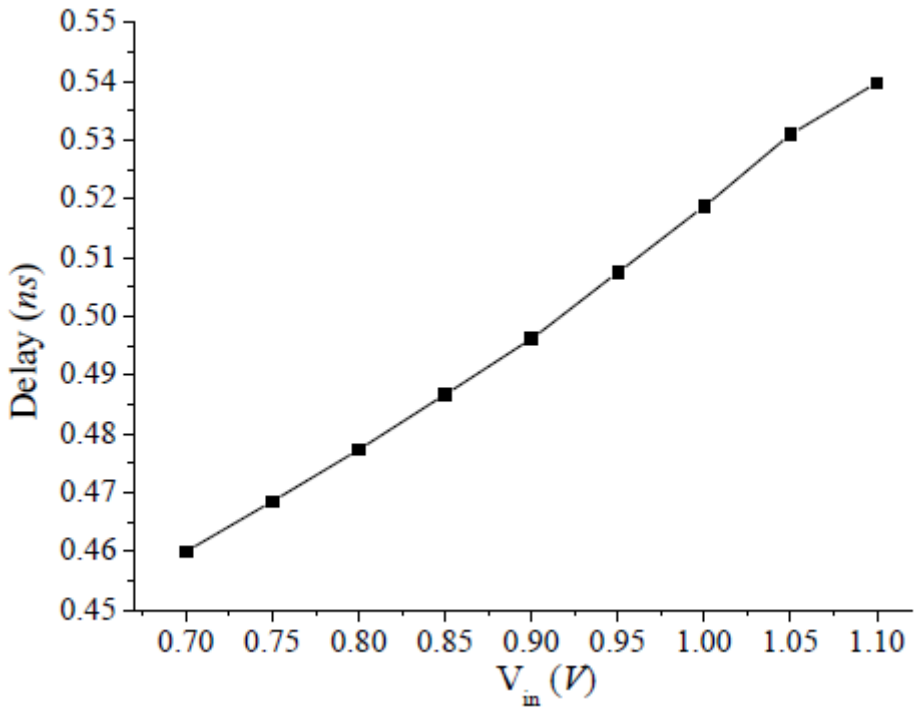

Fig. 1.19 Delay against V_{in} of the controllable delay element (CDE) [1]

The 32 nm FinFET-based voltage sensor is shown in Fig. 1.20 which consists of a controllable delay block, a calibration block, positive-edge flip-flops, and XOR gates [1]. The clock passes through calibration block and be separated by the delay buffers to create the lag between consecutive D input of flip-flops. Simultaneously, controllable delay block is governed by V_{in} to determine shifting delay of the rising edge of the clock to shift the rising edge of the clock into the gap between two adjacent D inputs of the flip-flops. At the Q outputs of the flip-flops, XOR gates are applied to detect the difference between two adjacent Q outputs and make the voltage sensor output only one high value at once. The lookup table for the sensor output is shown in Table 1.2.

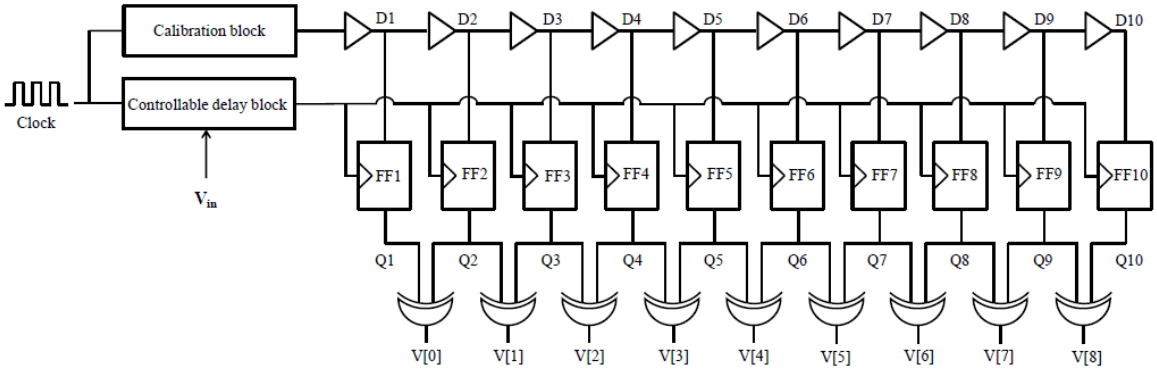

Fig. 1.20 Voltage sensor schematic [1]

Table 1.2 shows the corresponding 9-bit digital codes of the sensor outputs for several values of V_{in}.

Table 1.2 Voltage sensor digital code table [1]

V_{in}	Digital code								
	V[0]	V[1]	V[2]	V[3]	V[4]	V[5]	V[6]	V[7]	V[8]
0.7	1	0	0	0	0	0	0	0	0
0.75	0	1	0	0	0	0	0	0	0
0.8	0	0	1	0	0	0	0	0	0
0.85	0	0	0	1	0	0	0	0	0
0.9	0	0	0	0	1	0	0	0	0
0.95	0	0	0	0	0	1	0	0	0
1.0	0	0	0	0	0	0	1	0	0
1.05	0	0	0	0	0	0	0	1	0
1.1	0	0	0	0	0	0	0	0	1

The waveform of V_{in} and the corresponding V_{out} waveforms are shown in Fig. 1.21, where each value of V_{in} is mapping to a V_{out} value and only one high value is set once.

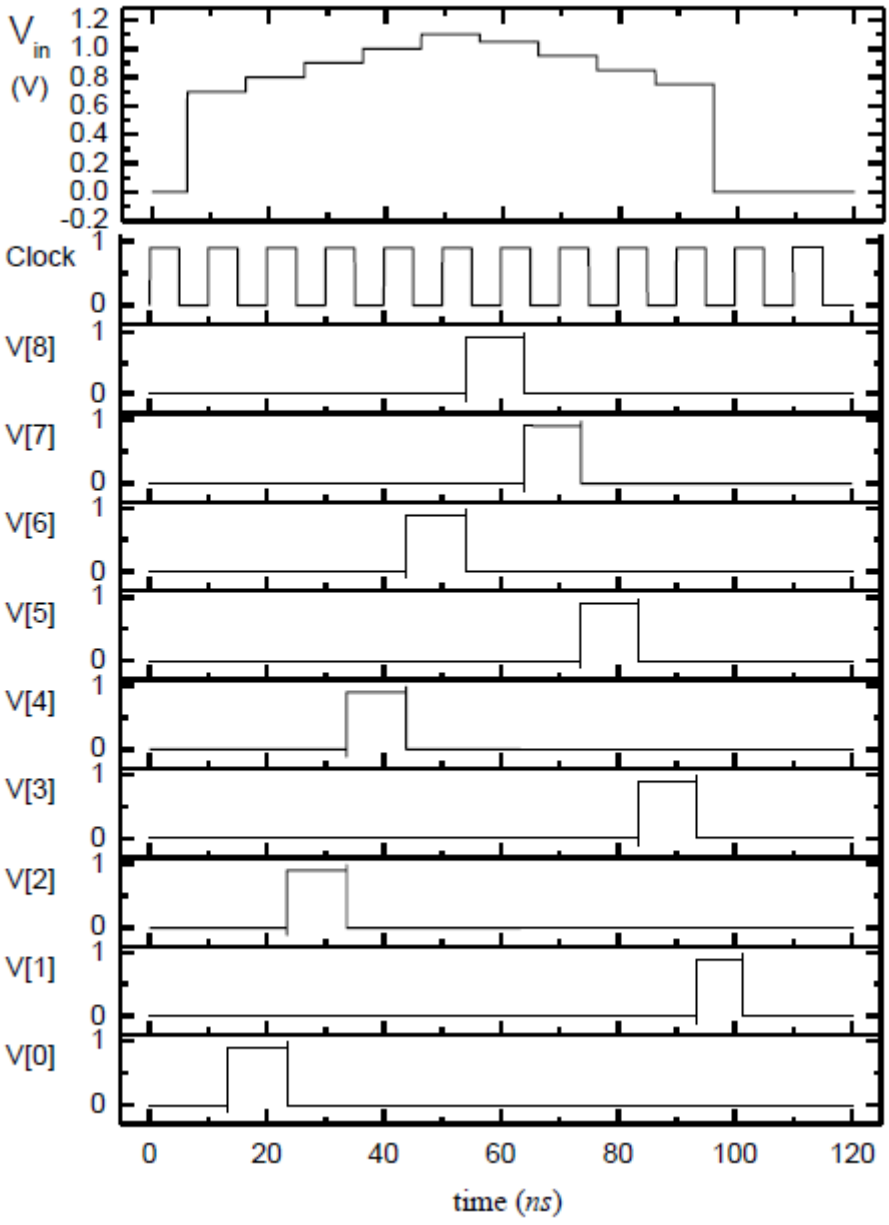

Fig. 1.21 Simulation results of V_{in} and V_{out} [1]

The digital voltage sensor [1] consume low power consumption as 20.6 μW, operate under wide voltage range (i.e., ±22% of the supply voltage), and has a high conversion rate as 100 MHz. However, it cannot give the precise voltage value. Moreover, this method does not take temperature variations into consideration which may make the performance unpredictable under different temperature variations.

1.3 Motivation of Proposed All-Digital Voltage Sensor

In above real-time and static voltage sensors we have discussed in the 1.2.1 and 1.2.2 own their pros and cons. However, we have noticed that most of these works didn't consider the PVT variations which will affect the relationship between the measured voltage values and the output digital codes.

Some designs are analog based approaches. However, due to several advantages of the digital-based design approaches, such as insensitivity to noise, robustness to process variations and work environment, and more design flexibility to other processes. As a result, we propose an all-digital voltage sensor which uses a relative reference modeling (RRM). Furthermore, we want to reduce the calibration cost. In this thesis, we propose an all-digital cell-based voltage sensor with one voltage point calibration and can against PVT variations.

1.7 Thesis Organization

Chapter 1 briefly discuss the challenge we are facing in semiconductor industry nowadays, the effect of static and dynamic IR-drop to circuit performance, we also introduce the pros and cons of published voltage sensors.

The rest of the thesis is organized as follows: Chapter 2 describes the design of the proposed static IR-drop monitor including the method and the simulation result. Chapter 3 introduces the improved work of prior relative reference modeling on-chip silicon oscillator. Finally, in Chapter 4, we make a conclusion of this thesis and describe the further works about several design issues which can be extended in the further.

Chapter 2 Relative Reference Modelling Based Static IR-drop Monitor

2.1 The System Architecture

The system architecture of the proposed relative reference modelling based static IR-drop monitor is as shown in Fig. 2.1. The proposed static IR-drop monitor is composed of a delay ratio estimator (DRE), a temperature sensor, a process sensor and a linear calculator. The delay ratio estimator is built by three ring oscillators, and each of them are combined by different cells which will be detail described in the section 2.2. The DRE generates delay ratio 1 (R1 (P, V, T)) and delay ratio 2 (R2 (P, V, T)) which present the distinct relation between process, temperature, and voltage. The value of delay ratio 1 and delay ratio 2 will be the input of temperature sensor and process sensor. Temperature sensor will use the value of delay ratio 1 to sense the current working temperature range from 0°C to 75°C. Process Sensor will sense the process corner of the chip by the value of delay ratio 2. After temperature sensor generates the temp_code, and the process sensor produces the process_code, the linear calculator uses the temp_code, process_code, R1 and R2 as inputs to calculate the current working voltage.

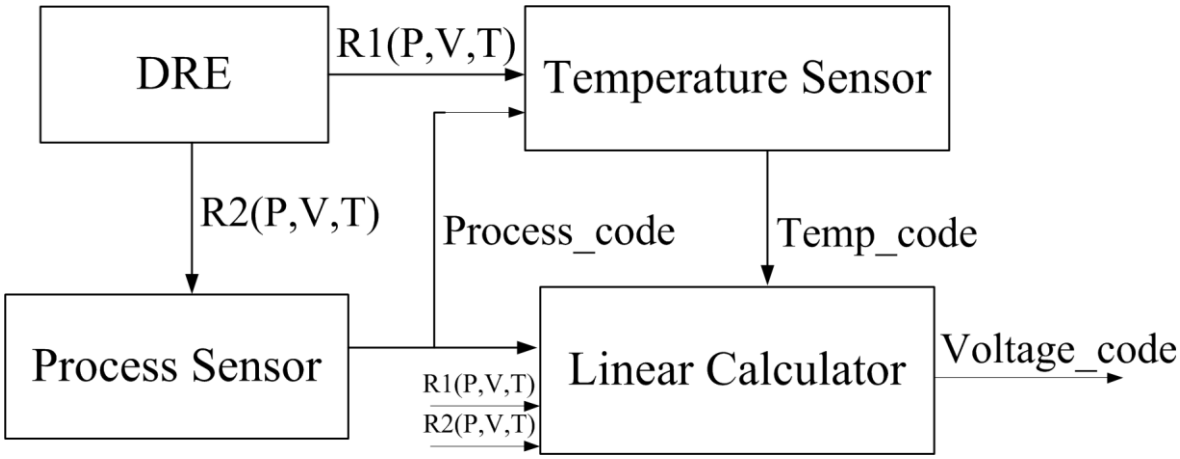

Fig. 2.1 Proposed static IR-drop monitor

We need to perform many SPICE simulations to obtain the delay ratios with PVT variations. In addition, we can change the delay cells in the DRE to obtain the desired delay ratio characteristics.

2.2 Relative Reference Modeling versus Delay Ratio

The proposed static IR-drop monitor adopts relative reference modeling in the circuit. The propagation of logic cells are easily effected by process, voltage and temperature (P, V, T) variation. Our goal is to eliminate the PVT variation from our IR-drop monitor to make it reliable and stable under the operating range. As we know, different cells have different reaction to different process, temperature and voltage. In addition, some are sensitive to certain variation parameter and some are immune to certain variation parameters. As a result, we can use this feature to choose different delay cells from cell-library to build up the delay ratio estimator. One type of cell is adopted as reference delay cell (RDC), another two type of cells is used as compared delay cell 1 (CDC1) and compared delay cell 2 (CDC2). These cells are chosen through the cell selection flow from cell library. The delay ratios of these delay cells are expressed as Eq 2.1 and Eq 2.2

$$\mathrm{R1(P,V,T)} = \frac{D_{CDC1}(P,V,T)}{D_{RDC}(P,V,T)} \qquad \text{(Eq 2.1)}$$

$$\mathrm{R2(P,V,T)} = \frac{D_{CDC2}(P,V,T)}{D_{RDC}(P,V,T)} \qquad \text{(Eq 2.2)}$$

Eq. 2.1 and Eq. 2.2 show the delay relationship between CDC1, CDC2 and RDC, respectively. Under a certain constant temperatures, the R1(P,V,T) will be shown as several approximate straight lines which mean that the delay ratio of CDC1 and RDC is more sensitive to temperature than voltage. On the other hand, the R2(P,V,T) is expressed as several approximate straight lines under certain constant voltages which present the delay ratio of CDC2 and RDC is more sensitive to voltage than temperature. The characteristics of R1(P,V,T) and R2(P,V,T) can be used to determine the working voltage and temperature.

2.3 The Implementation of Static IR-drop Monitor

Fig. 2.1 shows that the proposed IR-drop is composed by four main blocks. The key to the propose design among these block is the DRE which is shown in Fig. 1.34. In section 2.2, we discuss the relative reference modeling approach. Here, we illustrate how our proposed design applies this concept.

Fig. 2.2 shows the simulated R2(P,V,T) curves. The desired R2(P,V,T) characteristic is that the values of R2(P,V,T) at 1.1V are not overlapped in different process corners. Therefore, the simulated values of R2(P, V, T) can be used to identify the process variations of the voltage sensor when the process variation is unknown. For example, after chip fabrication, if we calibrate the chip at 1.1V, and R2(P, V, T)*1024 is 670. Then, the value of R2(P, V, T) is close to the simulated FF process corner. Therefore, the proposed process sensor can determine that the voltage sensor is at FF process corner.

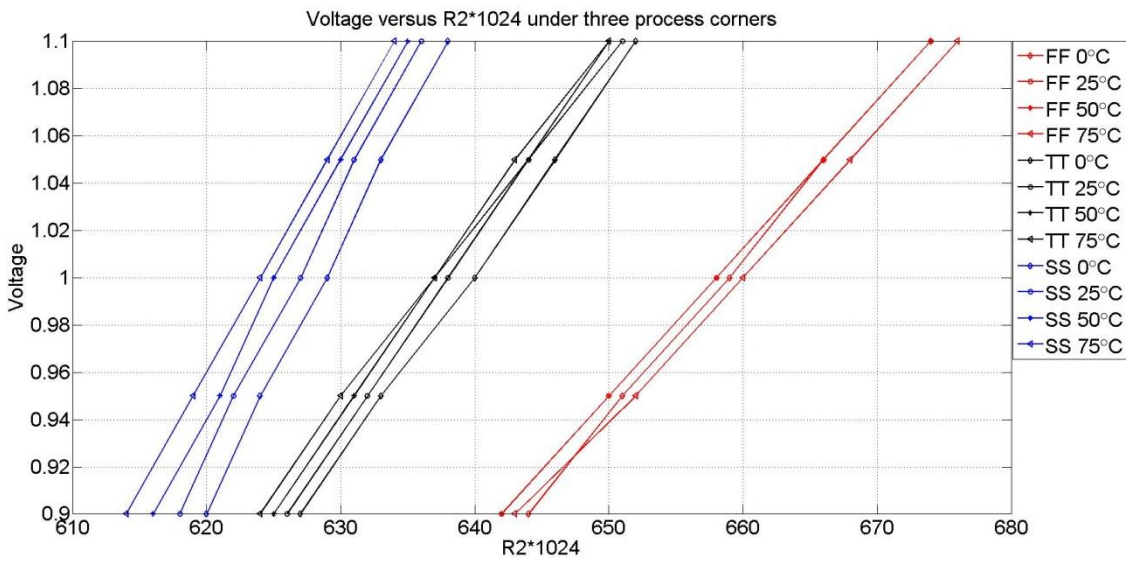

Fig. 2.2 Simulated R2(P,V,T) curves

Fig. 2.3 shows the simulated R1(P,V,T) curves. The desired R1(P,V,T) characteristic is

that at each process corner (TT, SS, FF), the values of R1(P,V,T) at different temperature are not overlapped. Therefore, the simulated values of R1(P, V, T) can be used to identify the temperature variations of the voltage sensor when the temperature variation is unknown. For example, after chip was calibrated at 1.1V, the process corner is known as SS process corner. If R1(P, V, T)*1024 is 1040. Then, the value of R1(P, V, T) is close to the simulated condition at 50°C. Therefore, the proposed temperature sensor can determine that the voltage sensor is at 50°C.

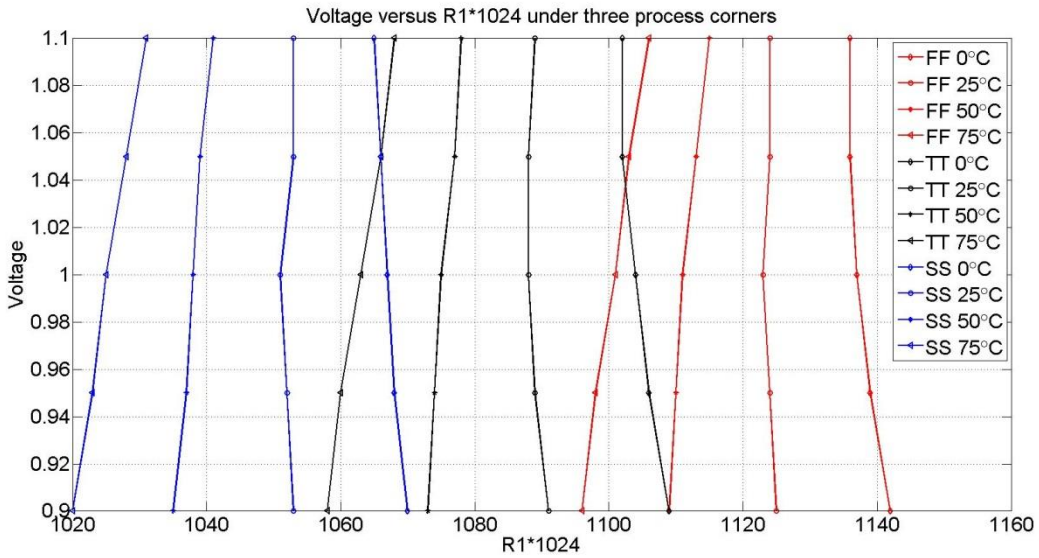

Fig. 2.3 Simulated R1(P,V,T) curves

In the proposed all-digital voltage sensor, the relationship between the measured voltage values and the output digital codes are fixed even with PVT variations. Fig. 2.4 shows the simulated (R1 - R2)/R1 curves. In each process corner, at different temperature, the relationship between (R1 - R2)/R1 and the measured voltage value (i.e. voltage_code) can be approximated as a linear equation. Therefore, the simulated values of (R1 - R2)/R1 can be used to determine slope and intercept of the linear equations to compute the output voltage_code. For example, if the process corner is known as SS process corner, and the voltage sensor is at 50°C, and then the proposed linear calculator can use the suitable linear equation from the simulation results to compute the output voltage_code with the current

value of (R1 - R2)/R1.

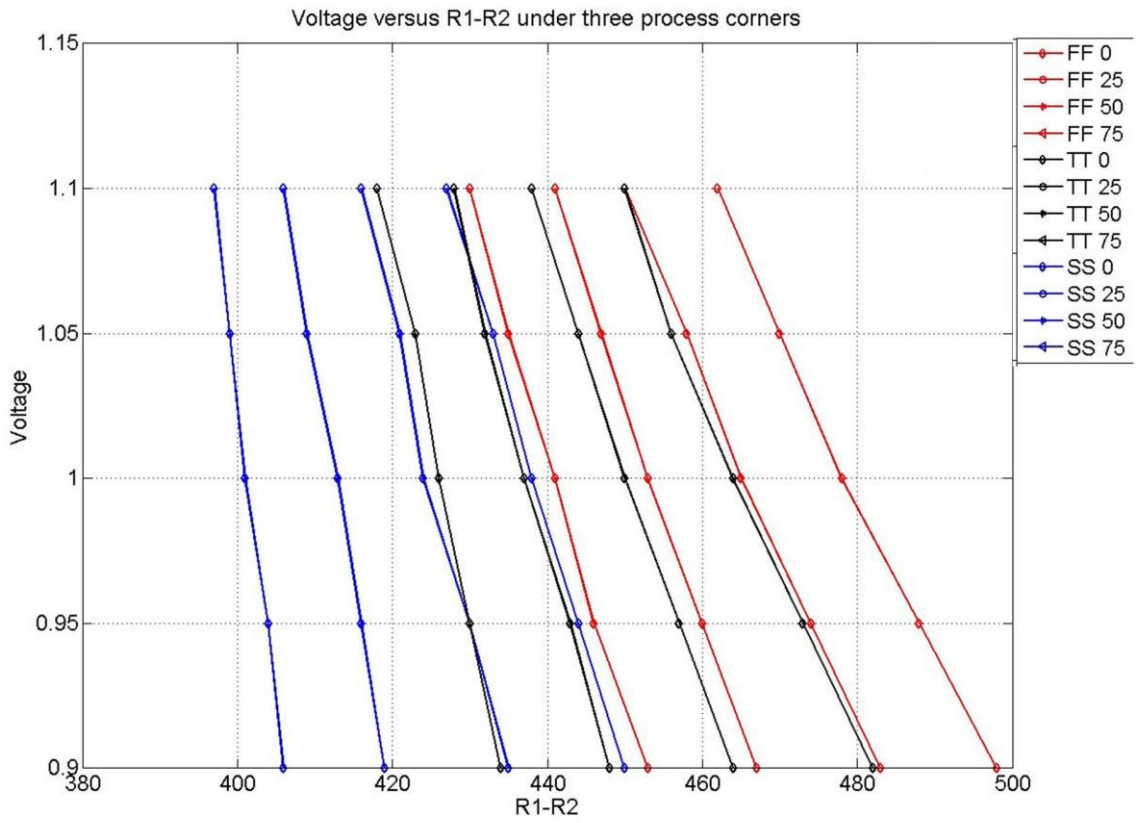

Fig. 2.4 Simulated (R1 - R2)/R1*1024 curves

The operation flow of the proposed all-digital sensor is explained as follows. After chip fabrication, the proposed all-digital voltage sensor needs to be calibrated at 1.1V. During the calibration process, the chip operating temperature is not important, since the proposed process sensor can determine the process corner of the voltage sensor without temperature information as illustrated in Fig. 2.2. When the process_code shown in Fig. 2.1 is determined, the proposed temperature sensor can always determine the chip temperature (temp_code) when the operating voltage ranges within 0.9V to 1.1V as illustrated in Fig. 2.3. Subsequently, the linear calculator of the proposed all-digital voltage sensor will use the value (R1 - R2)/R1 and selects a suitable linear equation to compute the measured voltage value (voltage_code) as illustrated in Fig. 2.4.

The operation flow of the proposed static IR-drop monitor is shown in Fig. 2.5. The first step is to input the external parameter, meanwhile DRE starts to calculate the delay ratios. After DRE calculating R1(P,V,T) and R2(P,V,T). The process sensor and temperature sensor use R1(P,V,T) and R2(P,V,T) to determine the current working temperature and process. By previous steps, we can calculate the current voltage by the Eq 2.3 which is a simple linear operation. The value of slopes and intercepts are from Circuit simulation. When the current voltage is calculated the circuit will output voltage_code, process_code and temp_code. Meanwhile, the circuit will start another cycle when process and temperature condition are changed.

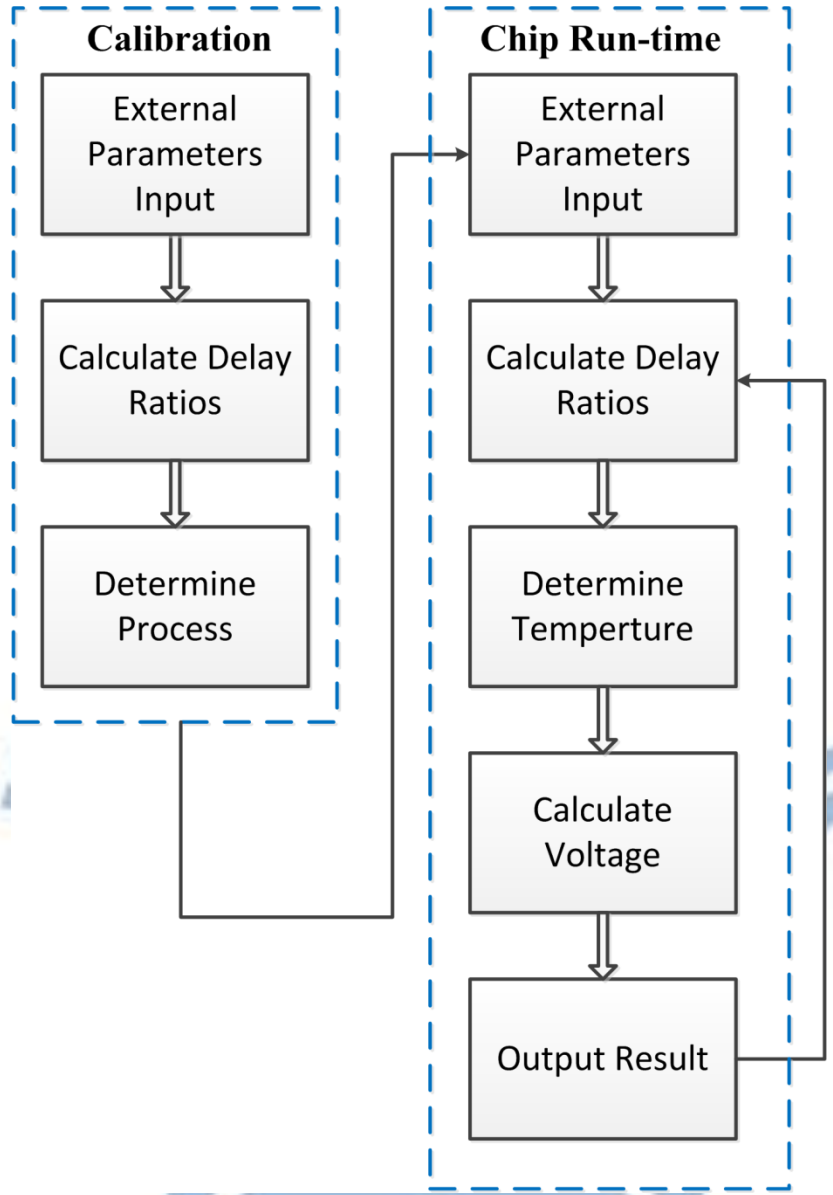

Fig. 2.5 The operation flow of the proposed static IR-drop monitor

The timing diagram of external input values from is shown in Fig. 2.6. When the in_flag trigger a pulse, the coeff will start assign to the parameters from IO pad with ext_clk.

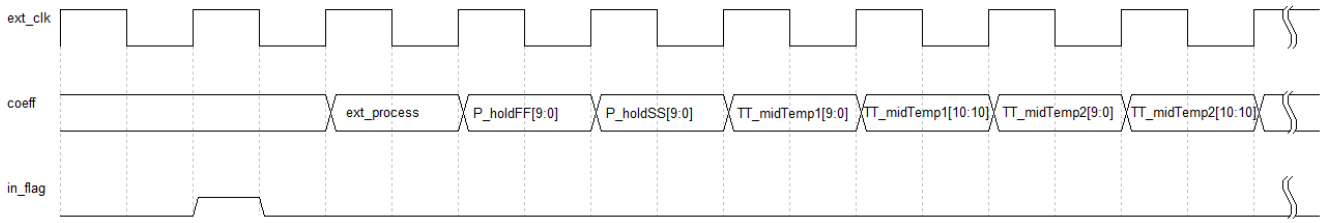

Fig. 2.6 The timing diagram of input external values

Fig. 2.7 presents the timing diagram of the DRE. Three oscillators of the DRE start oscillating together with different frequency. Each of three counters connected with oscillators. When the RRO counter count from 0 to 1023 cycles, the value of CRO1 counter will be R1(P,V,T)$\times$ 1024 and the value of CRO2 counter will be R2(P,V,T) $\times$ 1024 as 1109 and 627 in Fig. 2.7. Once the circuit outputs the value of voltage_out, temp_out and process_code the DRE will restart and recalculate the new R1(P,V,T) and R2(P,V,T).

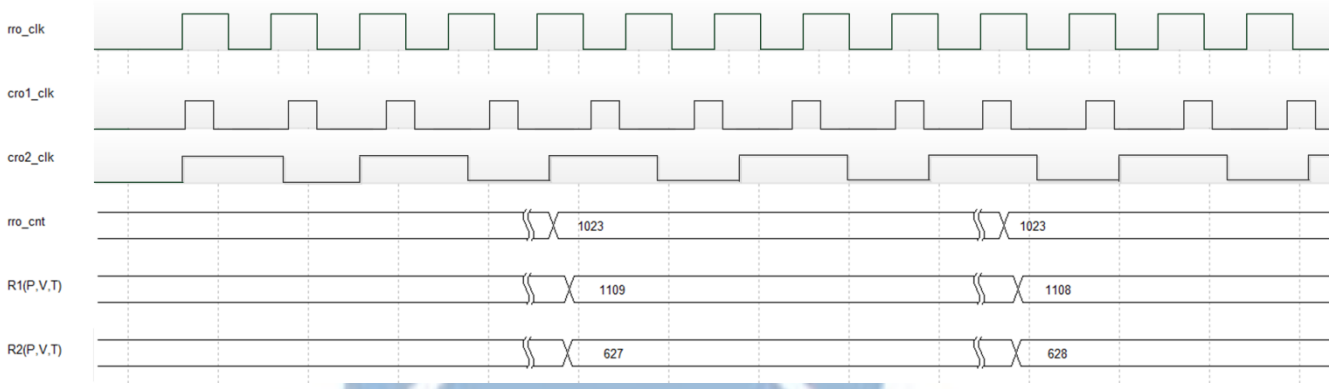

Fig. 2.7 The timing diagram of DRE

Noted that the calculator of $\frac{(R1-R2)}{R1}$ will be one digit after decimal point. As a result, we make $\frac{(R1-R2)}{R1}$ times 1024 to solve the problem of decimal point. Also, to solve the problem of the chosen slope is third digit after decimal point by multiple it by 2^{15} as Eq. 2.3.

$$\text{voltage\_code} = 2^{15} \times (slope \times \frac{R1-R2}{R1} + intercept) \qquad \text{(Eq. 2.3)}$$

The system diagram is shown in Fig. 2.8. After DRE produce R1(P,V,T) and R2(P,V,T).

We can sequentially determine process_code, temp_code and the voltage_code which is computed by Eq. 2.3. After voltage_code is generated, the out_flag raises a pulse to start output detected values through the IO pad and also raises a pulse of reset_flag to reset the circuit for another monitoring cycle. Each of monitoring cycle may not always get the same value, but will be very close if operating conditions are not changed. The detected real voltage will be voltage_code dived by 2^{15}. For example, in Fig. 2.8 we get the voltage_out from first round monitoring where the real voltage value is $\frac{voltage\_out}{2^{15}} = \frac{29456}{2^{15}} \cong 0.898(V)$.

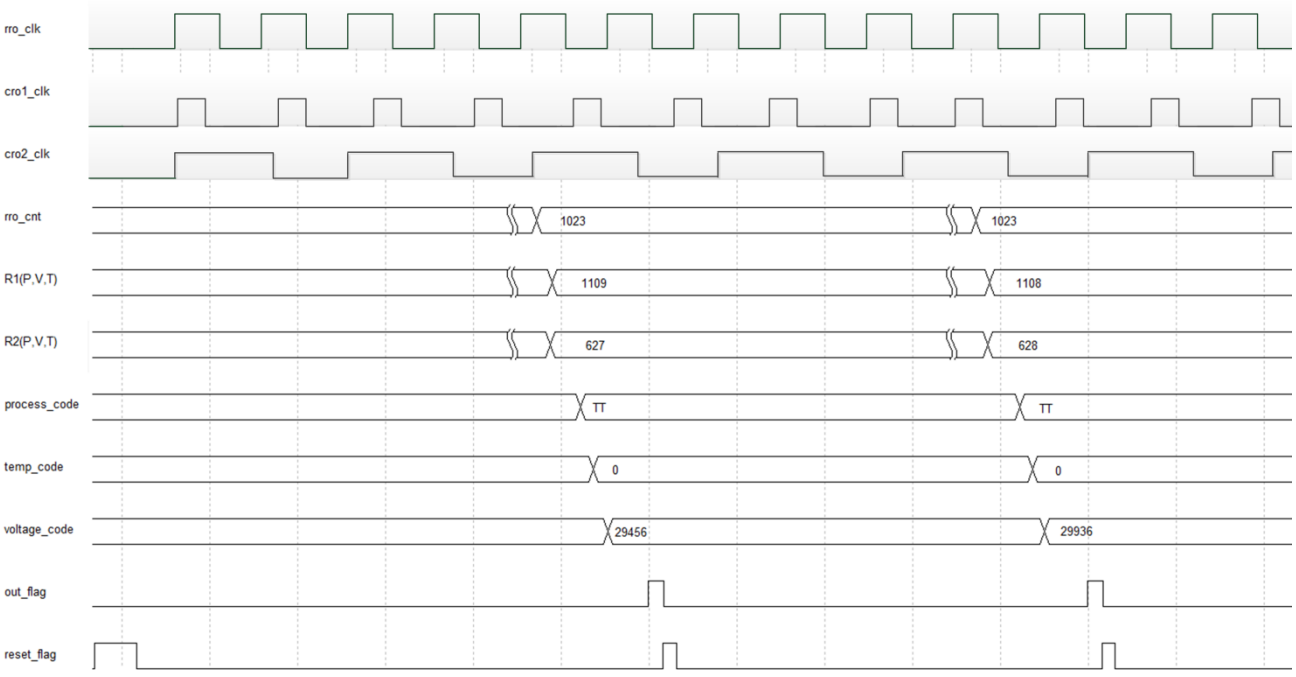

Fig. 2.8 The timing diagram of circuit monitoring

The chip floorplan and IO plan of proposed static IR-drop monitor is shown in Fig. 2.9 and IO pad detail description is in Table 2.3. The number IO pad is one of the main area cost and packaging cost of the chip. During floorplan the number of I/O pin numbers determines whether the chip is a core limit design or a pad limit design. We prefer our design tend to be the core limit design, as a result, we have to limit the number of IO pads.

We use two pair of core power pads and four I/O pad powers pads for the test chip. 10-bit I_COEFF is used for external input when I_IN_FLAG raises a pulse. The external coefficients will be cut into pieces due to I_COEFF only has 10 bit. The output detected values are output through four bit I_OUT after I_OUT_FLAG raise a pulse. Those detected values are also needed to separate into 4 bits data to meet the bit width of I_OUT. I_RESET will reset the circuit. I_EXT_REF_CLK is the clock for external input and I_OUT_CLK is for output.

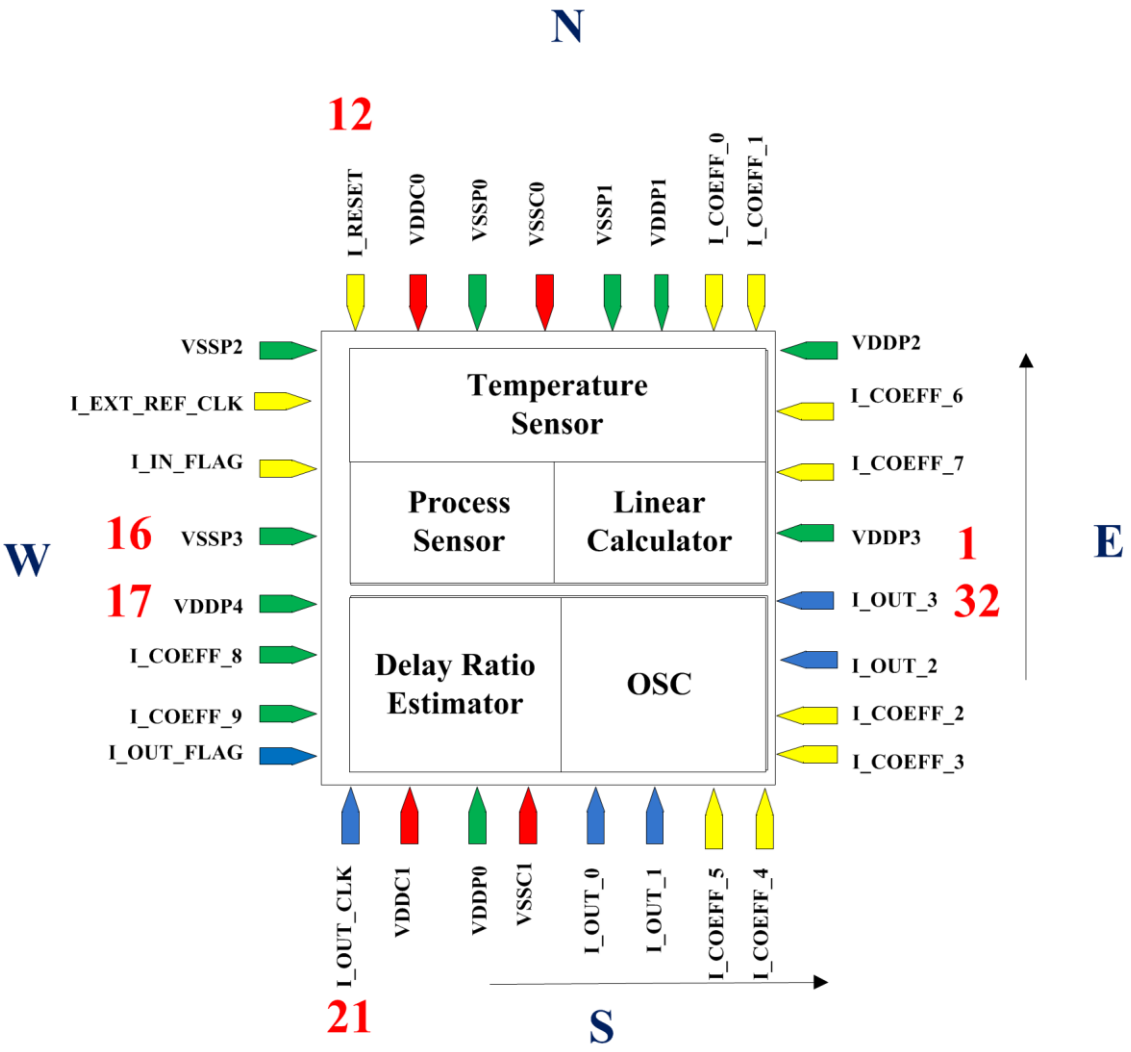

Fig. 2.9 Chip floor plan and IO plan

Table 2.1 The IO pad information of proposed design

Pin Number	Pin Name	Input/Output	Information
1	VDDP3	Input	Pad Power
2	I_COEFF_7	Input	Input coeff[7]
3	I_COEFF_6	Input	Input coeff[6]
4	VDDP2	Input	Pad Power
5	I_COEFF_1	Input	Input coeff[1]

6	I_COEFF_0	Input	Input coeff[0]
7	VDDP1	Input	Pad Power
8	VSSP1	Input	Pad Power
9	VSSC0	Input	Core Power
10	VSSP0	Input	Pad Power
11	VDDC0	Input	Core Power
12	I_RESET	Input	Chip Reset Pin
13	VSSP2	Input	Pad Power
14	I_EXT_REF_CLK	Input	Input external clock
15	I_IN_FLAG	Input	Input data flag
16	VSSP3	Input	Pad Power
17	VDDP4	Input	Change to power on pad
18	I_COEFF_8	Input	Input coeff[8]
19	I_COEFF_9	Input	Input coeff[9]
20	I_OUT_FLAG	Output	Out_flag signal
21	I_OUT_CLK	Output	DCO output clock
22	VDDC1	Input	Core Power
23	VDDP0	Input	Pad Power
24	VSSC1	Input	Core Power
25	I_OUT_0	Output	output value pin[0]
26	I_OUT_1	Output	output value pin[1]
27	I_COEFF_5	Input	Input coeff[5]
28	I_COEFF_4	Input	Input coeff[4]

29	I_COEFF_3	Input	Input coeff[3]
30	I_COEFF_2	Input	Input coeff[2]
31	I_OUT_2	Output	output value pin[2]
32	I_OUT_3	Output	output value pin[3]

2.4 The Simulation Result of Static IR-Drop Monitor

The proposed static IR-drop monitor is implemented in TSMC 90nm CMOS process. The operating voltage ranges from 0.9V to 1.1V, and temperature range is from 0℃ to 75℃. Fig. 2.10 shows the timing diagram of sensor output. The Out_flag raises a pulse, then the Output signal outputs the values of temp_code, process_code and voltage_code in sequential along with ext_clk.

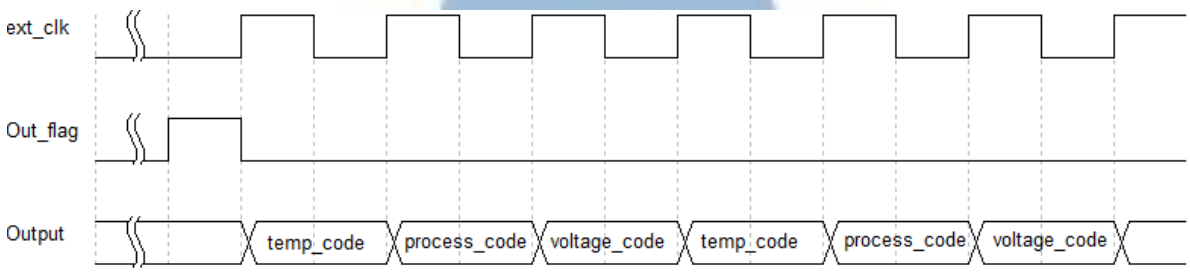

Fig. 2.10 The timing diagram of sensor output process

The proposed static IR-drop monitor achieves a 0.027mV resolution and has a maximum error 16.4mV with process, voltage, and temperature (PVT) variations as shown in Figs. 2.11 and Fig. 2.12. Fig. 2.11 shows the output voltage value versus the ideal voltage value under corner simulations, and we can see that the curve of detected voltage value is close to ideal voltage value as we expected.

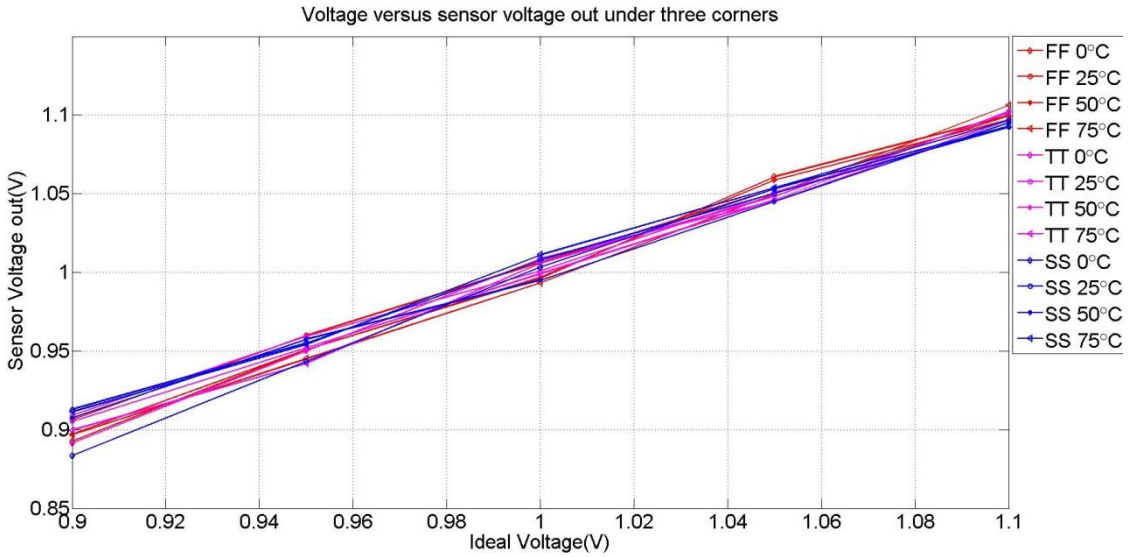

Fig. 2.11 The output of the voltage sensor versus ideal voltage

Voltage error is defined as the sensed voltage value minus ideal voltage value. The voltage error of proposed static IR-drop monitor is shown in Fig. 2.12, where the maximum error voltage is 16.4mV at SS corner and the minimum error voltage is 0.1mV also at SS corner. The average voltage error is 5.1mV.

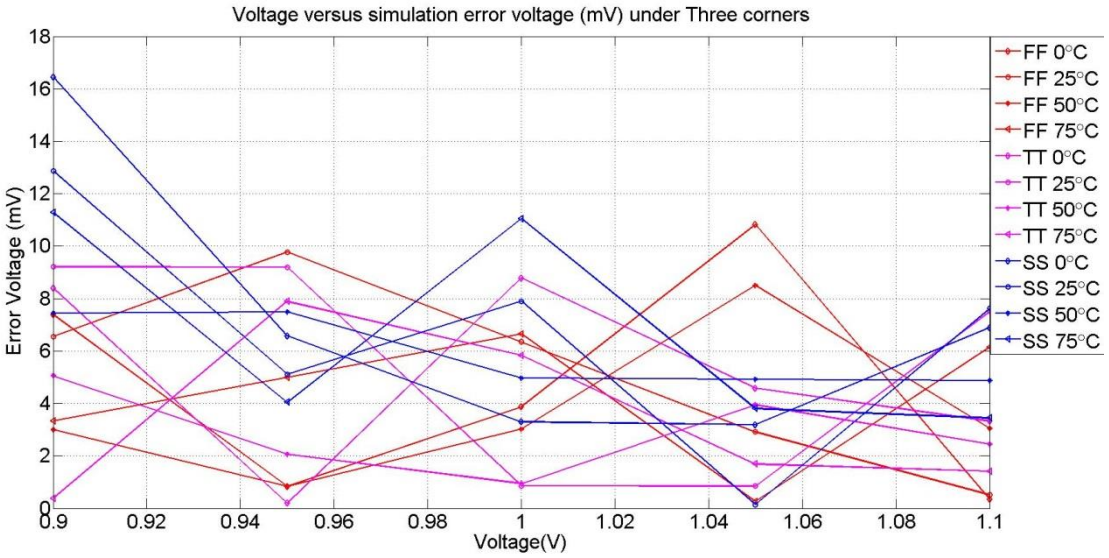

Fig. 2.12 The error of the proposed voltage sensor

We also run the simulations at 15℃, 35℃ and 65℃. The complete simulation results of R2(P,V,T) versus voltage is shown in Fig. 2.13, R1(P,V,T) shown in Fig.2.14 and (R1 - R2)/R1*1024 shown in Fig.2.15.

Although we didn't simulate these temperature values in Fig2.2, the process sensor can still operate correctly according to the simulation curves shown in Fig.2.13.

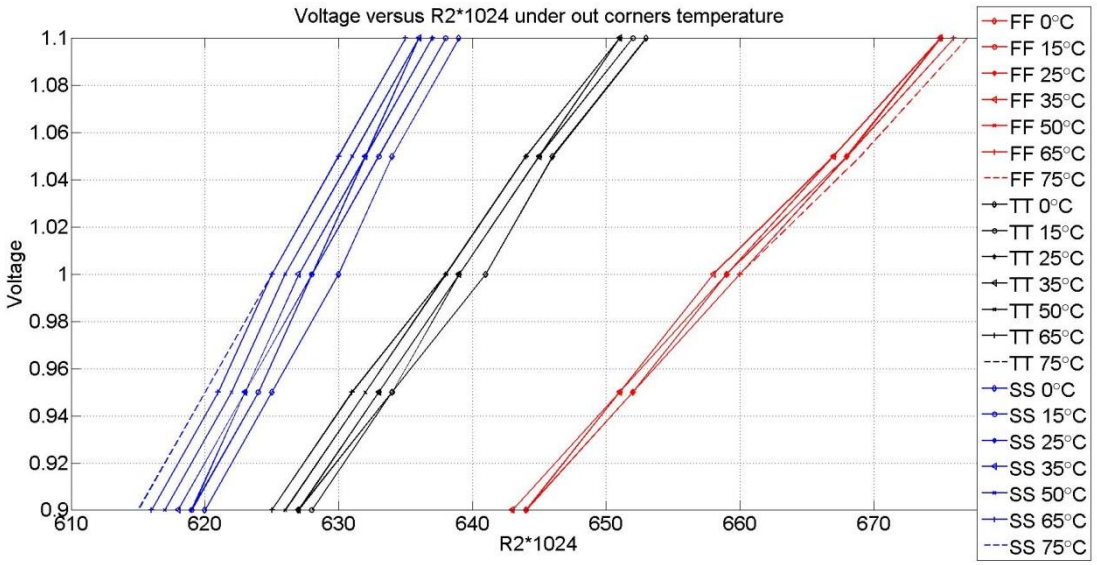

Fig. 2.13 Simulated R2(P,V,T) curves under non-corner temperature

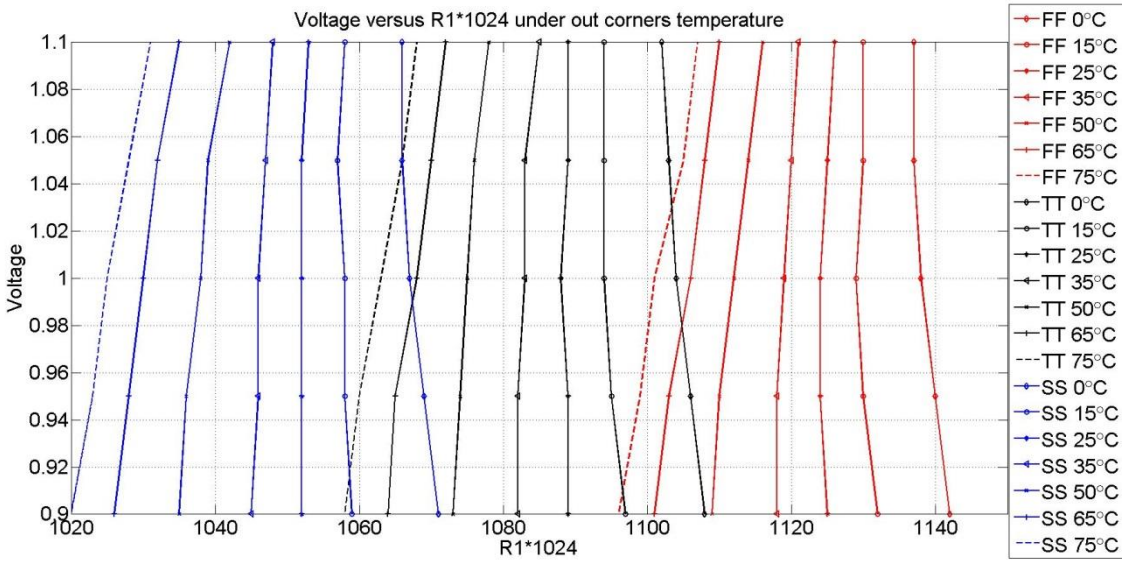

Fig. 2.14 Simulated R1(P,V,T) curves under non-corner temperature

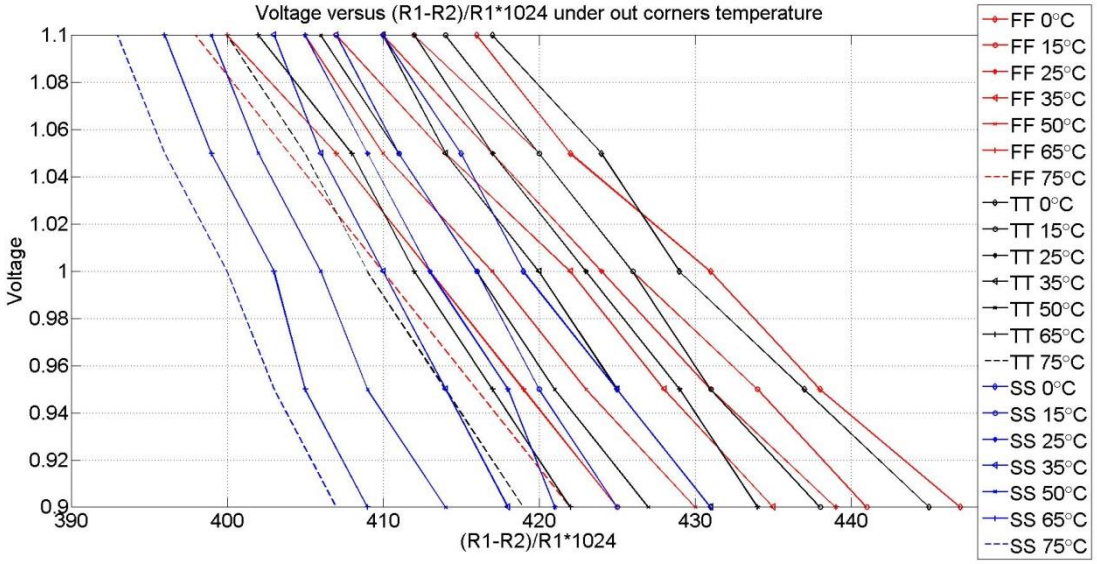

Fig. 2.15 Simulated (R1 - R2)/R1*1024 curves under non-corner temperature

However, since the relationship between (R1 - R2)/R1*1024 and the output voltage code is correlated to the temperature value, the misjudgment of the temperature value increase the maximum error voltage of the proposed all-digital voltage sensor from 16.4mV to 57.2mV.

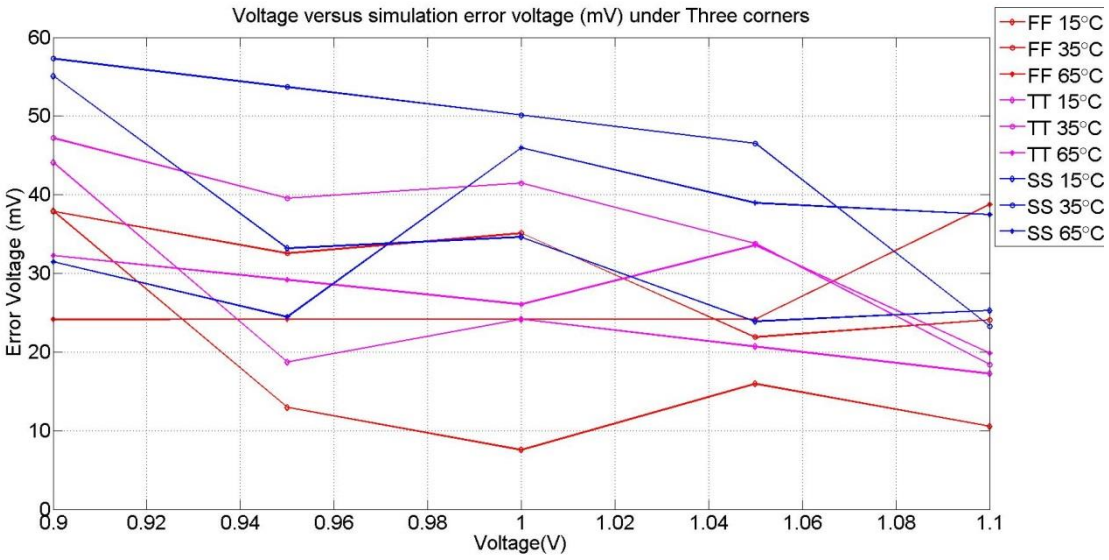

Fig. 2.16 The error of the proposed voltage sensor under non-corner temperature

The layout of proposed static IR-drop monitor is shown in Fig. 2.17 which contained SSC_constrained and SSC_unconstrained two main blocks. We adopt hierarchical

automatic placement and routing to implement our chip. We separate the whole chip into two blocks by whether they are timing constrained or not. If the block mainly contains timing constrained function such as the process sensor, the temperature sensor and the linear calculator, we merge these blocks as SSC_constrained. On the contrary, the non-timing constrained block such as the DRE, we merge the blocks as SSC_unconstrained. The proposed design can operate from 0.90V to 1.10V, and the temperature range from 0℃ to 75℃.The active area of the test chip is 0.063 mm^2. The power consumption of the proposed design is 1.0068mW at 1.0V.

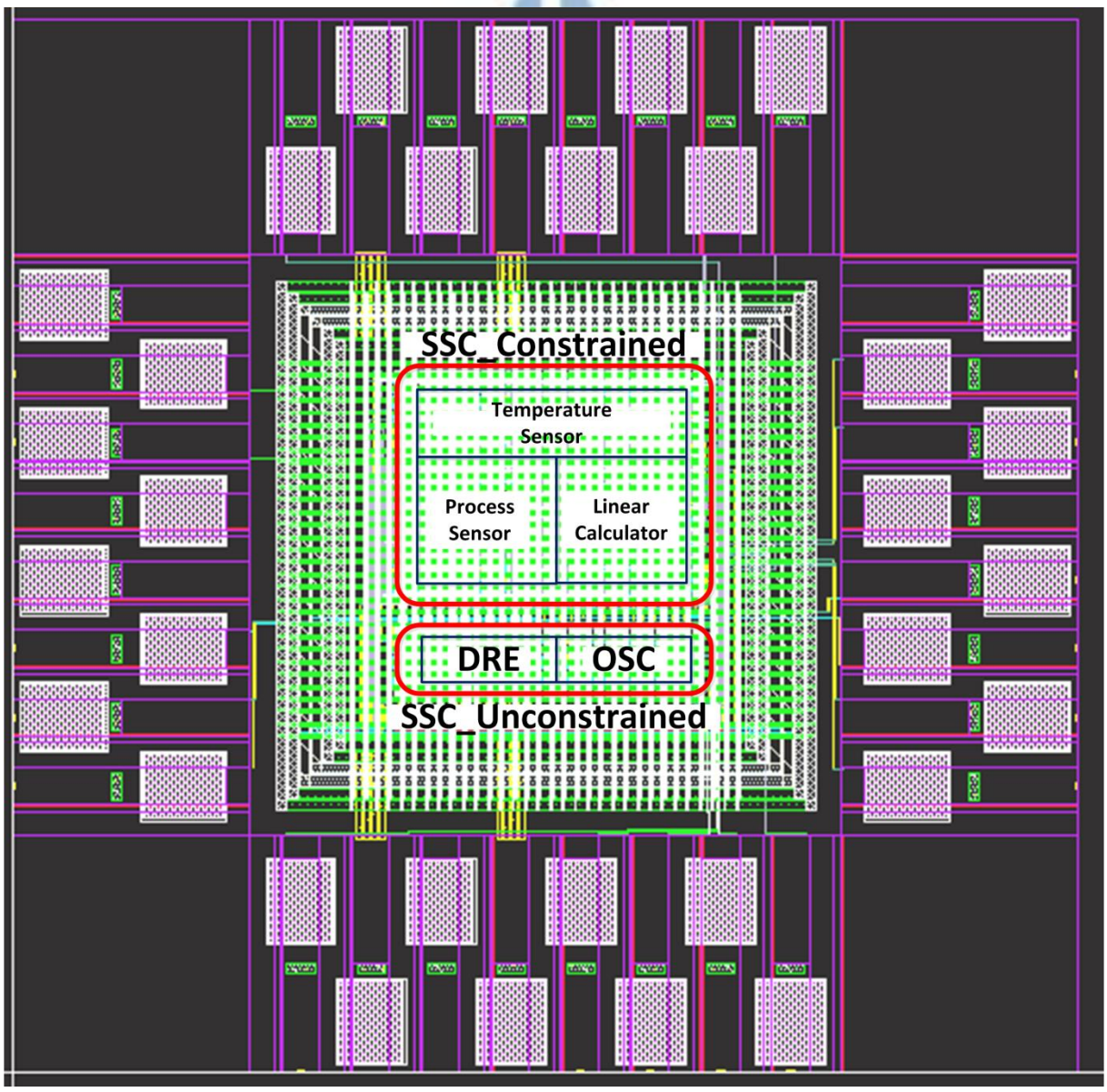

Fig. 2.17 Layout of proposed design

We used a power supply (Agilent E3600), a signal generator (Agilent 81134A), a seeeduino ADK main board, a chip and a test board for chip measurement of the static IR-drop monitor test chip. The power supply provides the Core power and Pad power for the proposed voltage sensor, and the Core power is 0.90V to 1.10V and the Pad power is 3.3V.

The output values of the proposed static IR-drop monitor have too many bits. Therefore, the measurement should take the input and output values from limited I/O pads. We will use the Seeeduino V3.0 to connect with the test board for input external values and samples values output from the test chip. Seeeduino ADK Main Board is an Android Open Accessory Development Kit(ADK), with the general purpose I/O (GPIO) function. The GPIO function can generate digital or analog pluses and provide 3.3V and 5V modes. We can input signal by the test board to our chips by using the GPIO function of the Seeduino. The Seeeduino V3.0 is shown in Fig. 2.18.

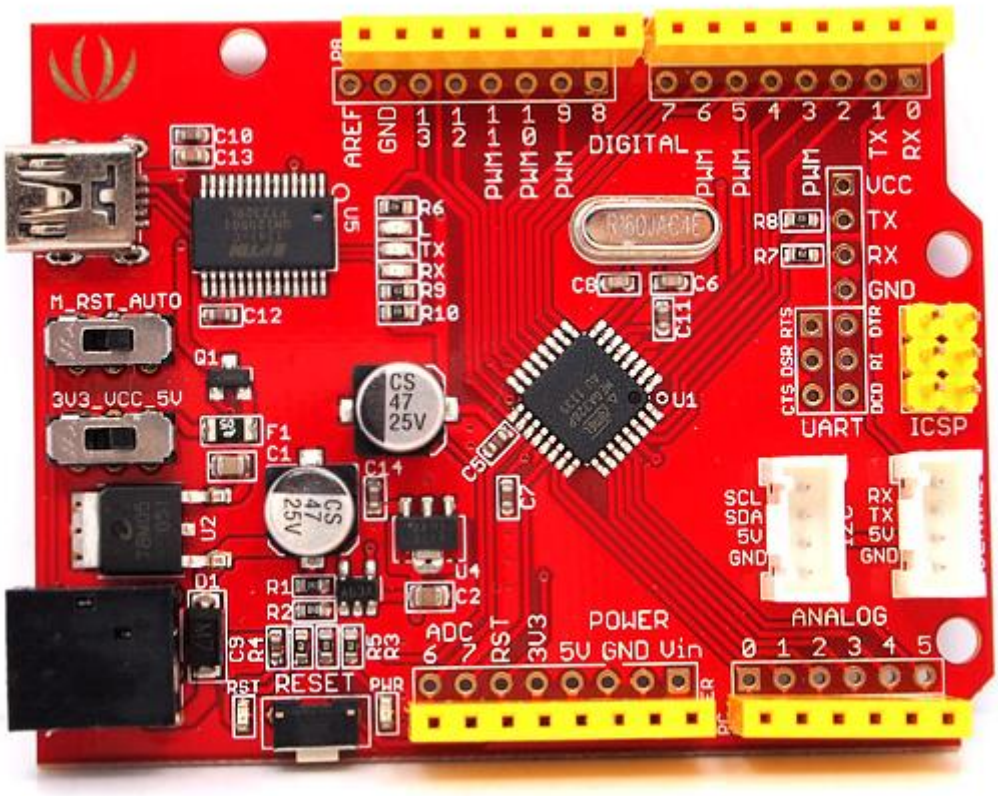

Fig. 2.18 Seeeduino V3.0

The specifications of Seeeduino V3.0 are shown in Table 2.2. Noted that although the clock rate is claim to be 16 MHz. For error prevention concern, the external and output clock of design is aimed to be under 5 MHz by our experience. The input and output values will transmit data via 14 bits of digital IO pins and 8 pins of analog pins.

The application of our design is as shown in Fig. 2.19. We plan to place our static IR-drop monitor in a SoC design. We can place voltage sensor separately around different blocks to monitor the static IR-drop of the chip.

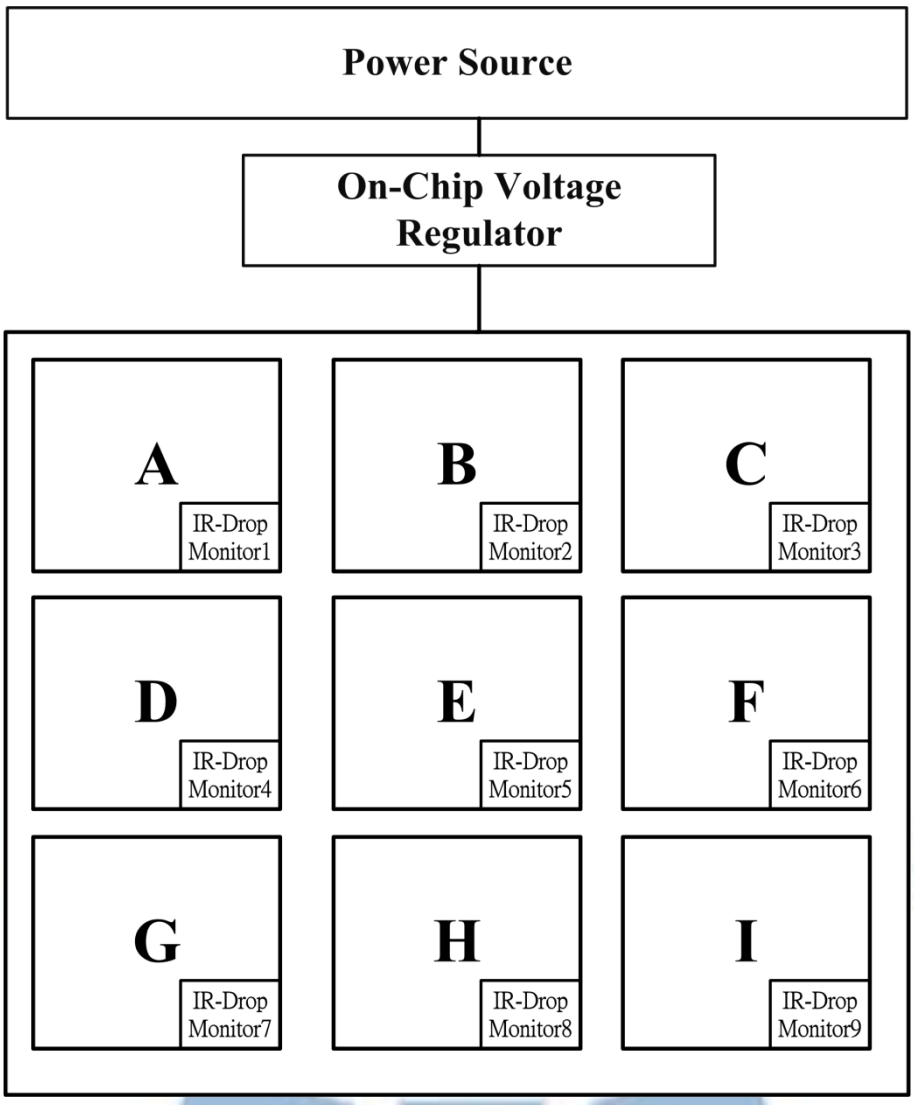

Fig. 2.19 The schematic diagram of application

Table 2.2 The specifications of Seeeduino V3.0

Microcontroller	Atmel ATmega328 (AVR 8-bit) in TQFP-32 package
Board (Boot-loader)	Arduino Duemilanove w/Atmega328
Operating Voltage	5V or 3.3V (choice by slide switch)
Maximum output current of 3V3 port and 5V port	5V port - 500mA, 3V3 port - 800mA(need to be powered by DC jack or Vin)
Maximum output current of digit pins	40mA
miniUSB Input Voltage	5V. Maximum is 5.5V.
DC Jack & Vin Input Voltage	7V to 12V (lower is preferred). Maximum is 20V. If input lower than 7V and switch set to 5V, then VCC at AVR is about 2V below the input.
Digital I/O Pins	14 (of which 6 provide PWM output)
Analog Input Pins	8 (of which 2 are used for I2C communication - PC4 and PC5)
Flash Memory	32 KB
SRAM	2 KB
EEPROM	1 KB
Clock Speed	16 MHz

The table 2.3 shows the comparison table of recent IR-drop monitors. Although [13] shows better error voltage, however it require three clean reference voltage inputs and is not reasonable for real application. The research [28] using voltage to-time-to digital convert technique to convert the ring oscillator period into digital value. The work in [12] using although provide high accuracy result but it also request for three clean reference voltage. In addition, all of these recent works cannot against the variation of PVTs which lowers the accuracy of the performance.

Table 2.3 The comparison table

	This work	[13]	[6]	[28]	[12]	[4]
Type	Voltage sensor	Worst-case IR-drop Monitor	PVT sensor	IR-drop monitor	VBIST	TDC
Technology(nm)	90	90	65	90	65	45
Temp. Range	0 ~ 75	NA	-50 ~ 125	-40~90	NA	30-90
VDD Range	0.9-1.1	0.8-1.0	0.3-1.0	0.9-1.1	0.9-1.1	0.9-1.1
Voltage Error	57.2mV	4.81mV	NA	NA	Within 10% of the actual measure value	27.5mV
Resolution	0.027 mV	3.74mV	50 mV	NA	NA	NA
power(mW)	1.0068@1.0V	1.94@0.8V	0.0037@0.3V	NA	NA	NA
Active area(mm^2)	0.063	0.184	0.1	0.027	NA	NA
Calibration	1 voltage	3 clean voltages	-	3 temperature points and 5 voltage points	3 clean voltages	3 voltages

Chapter 3 Relative Reference Modelling Approached On-Chip Silicon Oscillator

3.1 Reference Clock of Highly Integrated System

Nowadays, there are numerous highly integrated circuit designs have been developed. These complex circuits often require an external quartz crystal oscillator to provide a stable input reference clock to the system for synchronization. Most of the microprocessors, the integrated circuits and the system-on-chip (SoC) require a stable high-speed clock generated by the clock generator. However, the clock generator requires an stable input reference clock.

The quartz crystal is made of silicon and oxygen atoms which chemical name called Silicon Dioxide (SiO2). When the quartz crystal is pressed by a direction of the electric field, the direction of the quartz crystal may be shocked because of the piezoelectric effect.

The quartz crystal characteristics of piezoelectric effect can use the resonance phenomenon to produce precise oscillation frequency which can be used as the reference clock for the clock generator.

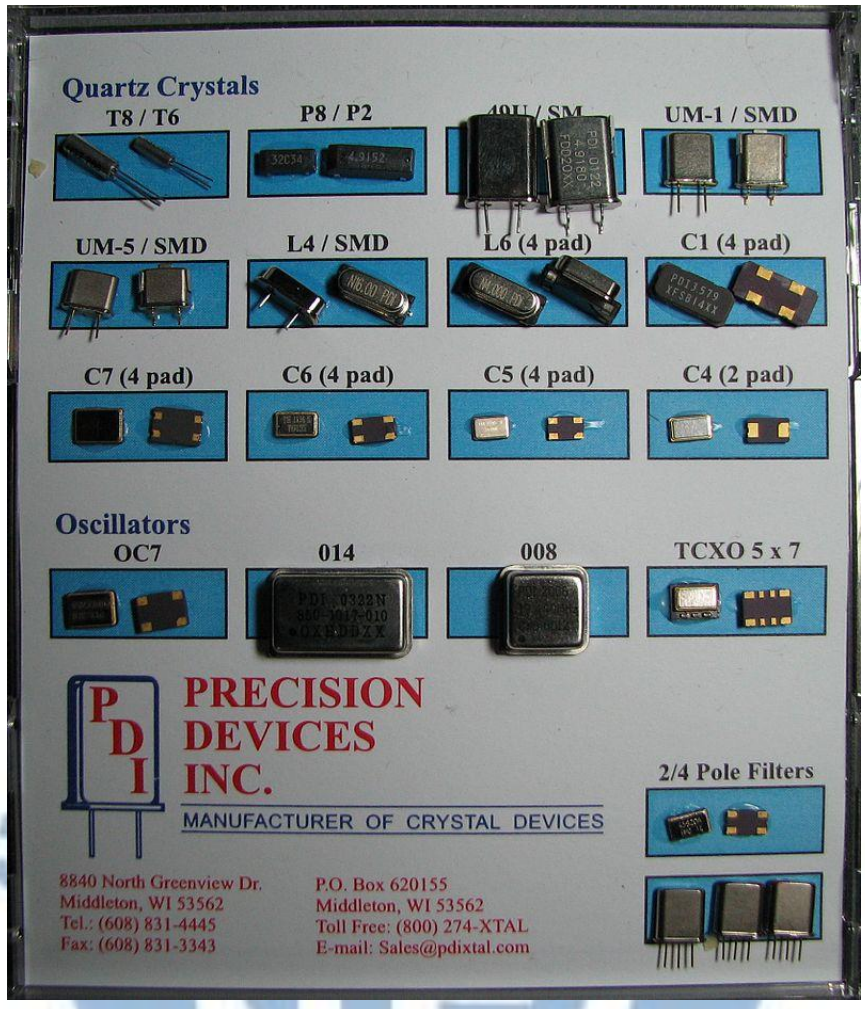

Fig. 3.1: various quartz oscillator.

Fig. 3.1 shows various kinds of quartz crystal oscillators, including the quartz crystal oscillator (XO), Temperature compensated crystal oscillator (TCXO), Oven-controlled crystal oscillator (OCXO) and Voltage-controlled crystal oscillator (VCXO). The quartz oscillators are commonly applied in plenty of products in the current market, such as, motherboards, CPUs, and large-scale medical equipments. These circuits will choose a suitable quartz crystal oscillator according to different applications. For example, integrated circuit or system-on-chip (SoC) often uses the TCXO as oscillator, due to the feature of temperature variation immunity of TCXO. Such circuits do not take price, size, and power consumption as their major consideration. Instead, frequency accuracy is more important than others.

3.2 Survey of Conventional On-Chip Silicon Oscillator

3.2.1 The Band gap Voltage Reference-Based On-Chip Silicon Oscillators

In the prior researches, most of the on-chip silicon oscillators use an external temperature sensor or an input reference voltage [32][33][34][35] to replace the external quartz crystal. These type of circuits, we call them band gap voltage reference-based on-chip silicon oscillators.

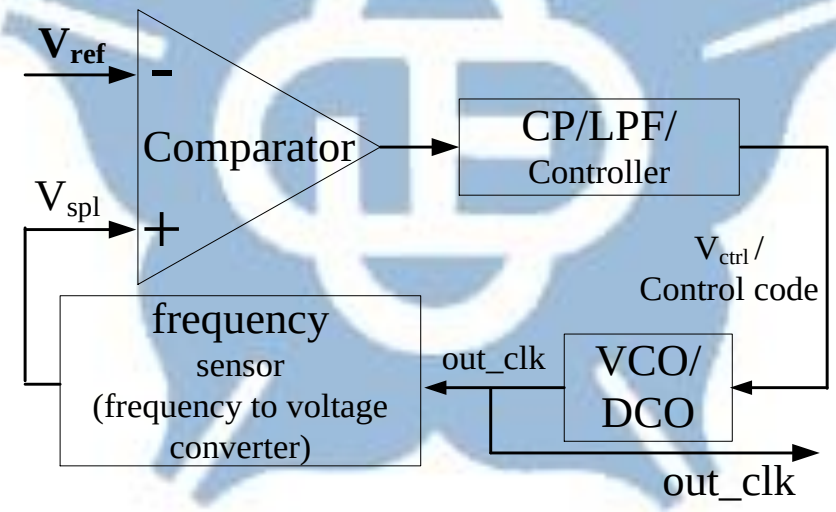

Fig. 3.2: The architecture of the band gap voltage reference-based on-chip silicon

Fig. 3.2 shows the block diagram of a band gap voltage reference-based on-chip silicon oscillator [34] compensation loop. While the circuit applied analog charge pump, it is composed of a comparator, a charge pump (CP), a loop filter (LPF), a frequency sensor and a voltage controlled oscillator (VCO). If the circuit applied a digital approach, it is composed of a comparator, the digital controller, a frequency sensor and a digital controlled

oscillator (DCO). After the VCO/DCO generates the difference frequency (out_clk) by the difference voltage (V_{ctrl}) or the difference digital control code, the frequency sensor detects the VCO/DCO frequency and converted the frequency into the voltage value (V_{spl}).

With an external stable DC voltage reference (V_{ref}), the comparator compares the difference between V_{spl} and V_{ref}. If V_{spl} is smaller than V_{ref}, the circuit will speed up the VCO/DCO by increasing the V_{ctrl} or digital control code. On the other hand, if V_{spl} is larger than V_{ref} the circuit will slow down the VCO/DCO by decreasing the V_{ctrl} or digital control code. During the compensation mechanism, it can against process and temperature variations.

Even though, this circuit does not require a reference clock. However, external reference voltage (V_{ref}) is required to eliminate the process and temperature variations. Moreover, frequency sensor produced some errors while converts frequency into voltage value with PVT variations. Therefore, the frequency error of the band gap reference-based on-chip silicon oscillators is increase with PVT variations.

Fig. 3.3 shows the block diagram of the temperature sensor-based on-chip silicon oscillator [36] compensation loop. It is composed of a temperature sensor, a non-linear mapper, a divider, a phase detector (PD), a loop filter, a digital/voltage controlled oscillator (DCO/VCO) and an electrothermal filter (ETF)[24] oscillator(OSC).

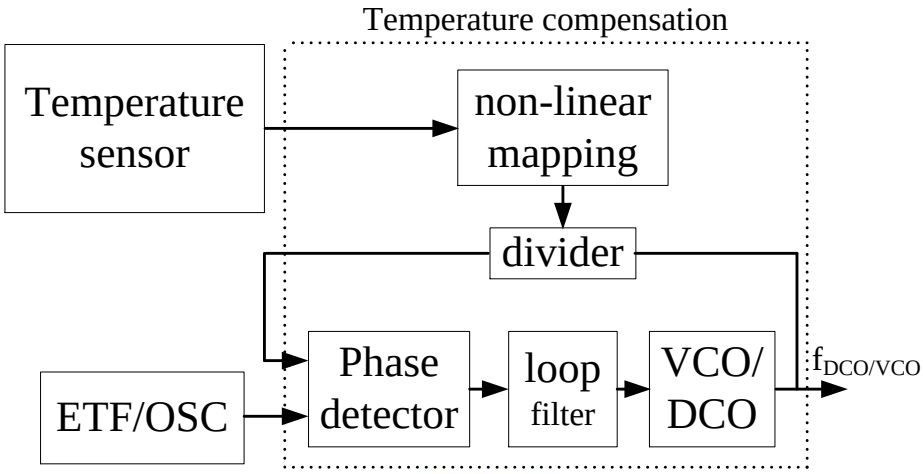

Fig. 3.3: The architecture of the band gap temperature sensor-based on-chip silicon oscillator.

First of all, this circuit uses a temperature sensor to measure the operating temperature and then it uses a non-linear mapping table to change the divider ratio of the PLC. Subsequently, it adopts the phase detector (PD) to compare the phase difference between ETF/OSC and the divided clock to adjust the frequency of the DCO/VCO. The non-linear mapping table can be used to calculate the control code to the frequency divider according to the temperature value. Finally, the control code with temperature variation adjusts the frequency of the DCO/VCO.

A mobility-based frequency reference [36][37] and thermal diffusivity-based frequency reference [38][39] are based on the band gap temperature sensor-based on-chip silicon oscillator. The advantages of these designs are high accuracy, low power, wide temperature range variations and relatively small process variations. However, these designs cannot eliminate voltage variation and they have strongly temperature dependency. As a result, these methods often need accurate temperature sensors to compensate for the output frequency and occupy a large chip area.

3.2.2 The Bias-Based On-Chip Silicon Oscillator

The block diagram of a bias current compensation mechanism frequency-locked loop technique of on-chip silicon oscillator is shown in Fig. 3.4 [40]. It is composed of a current comparator, a VCO, an amplifier (AMP), and a digital-to-analog converter (DAC).

After bias circuit generating a bias current (I_{BIAS}), the AMP amplifies the difference between I_{BIAS} and I_{OUT} as V_{OUT} pass to the VCO. The frequency-to-current converter converts the frequency of f_{OUT} into current I_{OUT}. Above blocks constructed as a feedback loop circuit. The current comparator compares the difference between I_{BIAS} and the output of the converter current I_{OUT} which will adjust the control voltage (V_{OUT}) of the VCO until the I_{OUT} equal to I_{BAS} in this feedback loop.

This type of architecture [40][41][42] are the improved work of the band gap voltage reference-based on-chip silicon oscillator which do not need an external reference voltage as [32][33][34][35]. However, the designs have to face the challenges of circuit accuracy due to the reference bias circuit will be affected by PVT variations and the conversion error in the frequency-to-current converter.

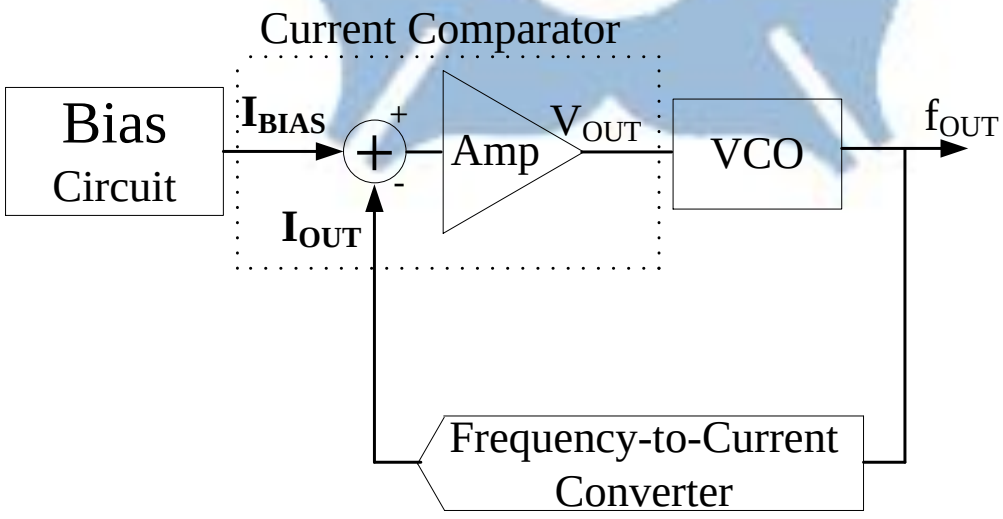

Fig. 3.4: The architecture of the current comparator on-chip silicon oscillator.

Fig. 3.5 shows the block diagram of a two voltages controlled on-chip silicon oscillator [43]. It is composed of a voltage-swing controller, a bias current controller, and a ring voltage controlled oscillator (RVCO).

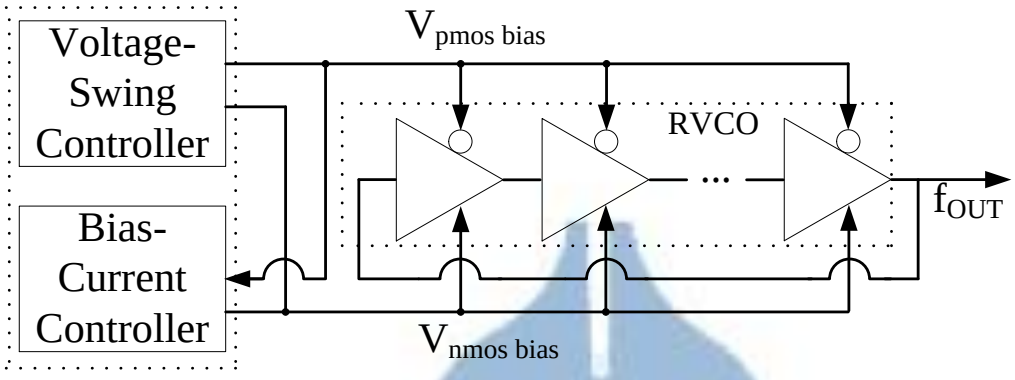

Fig. 3.5: The architecture of the two voltage controlled on-chip silicon oscillator.

This architecture uses on-chip bias-current controller and voltage-swing controller to compensate process and voltage variations of the RVCO frequency.The voltage-swing controller and bias-current controller separately generate different voltage and current for RVCO to control PMOS and NMOS of the RVCO, simultaneously.

Fig. 3.6 shows the simulation results of the voltage-swing controller and the bias-current controller different voltage (V_{swing}) and different current (I_{bias}) to compensate the RVCO [43]. According to Fig. 3.6, the output frequency of the RVCO remains stable with process and voltage variations. However, the voltage-swing controller and the bias-current controller are required to generate the difference voltage to compensate the frequency of the RVCO to overcome the process and voltage variations. In addition, this design method is not suitable to against temperature variations.

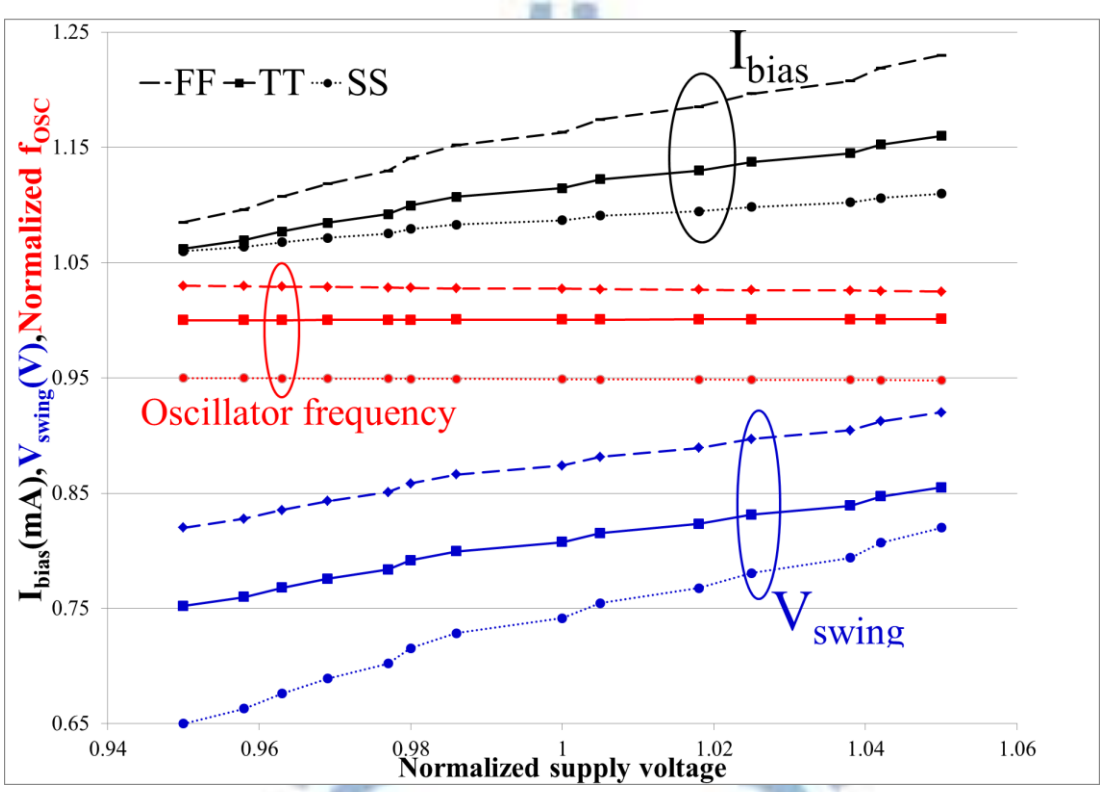

Fig. 3.6: The two voltage controlled on-chip silicon oscillator frequency with process and voltage variation.

3.2.3 Relaxation-Based On-Chip Silicon Oscillator

The relaxation oscillator [44]-[48] is an improved design of the RC-oscillator. The architecture of the conventional RC-oscillator [44] is shown in Fig. 3.7 which is composed of two comparators, a SR latch, some resistors and some capacitors. The conventional RC-oscillator runs through a resistor to charge a capacitor from a current source. In this circuit, the current source I_1 and I_2 have flicker noise, and thus when it uses for a long time, the comparator and other circuit have process, voltage and temperature (PVT) variations and the accuracy of frequency will be degraded.

The relaxation oscillators [44]-[48] aim to reduce the comparator delay time changes (t_d) with PVT variations.

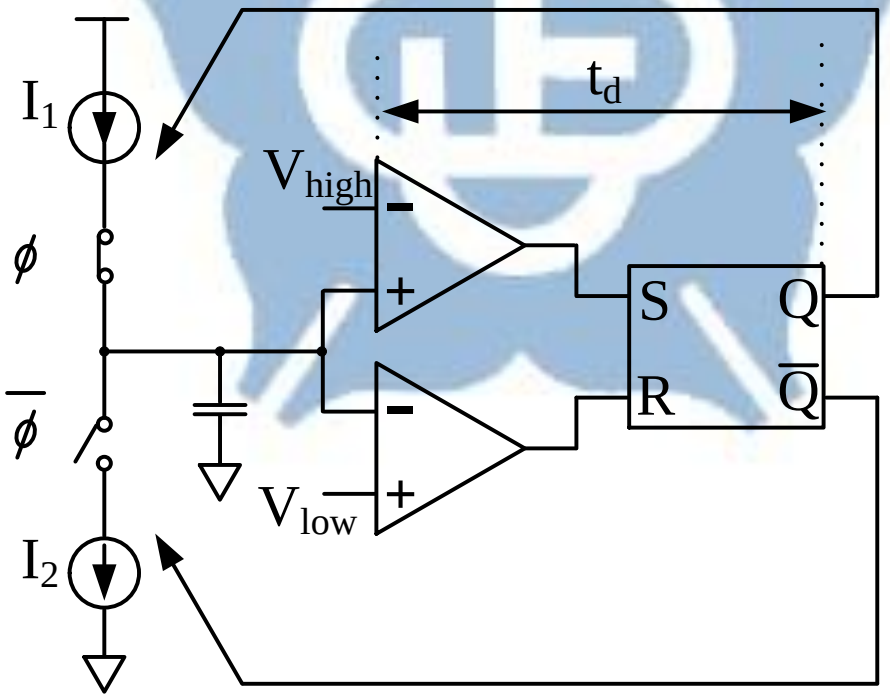

Fig. 3.7: The architecture of conventional RC-oscillator.

Fig. 3.8 shows architecture of the voltage averaging feedback (VAF) relaxation oscillator which is composed of a VAF and a relaxation oscillator [44].

The relaxation oscillators [44][45] with power averaging feedback can tolerate not only temperature but also voltage variations. The voltage reference of resistive divider requires to cancel the temperature dependency which may cause 0.4% frequency error with small voltage variations on the reference voltage (i.e. 2mV) [44]. This shows the sensitivity of the design is to process variations after calibration. Relaxation oscillators [44]-[47][50] need a bias generator to overcome voltage and temperature variations. The disadvantage of these designs is that the bias generator occupies a large chip area.

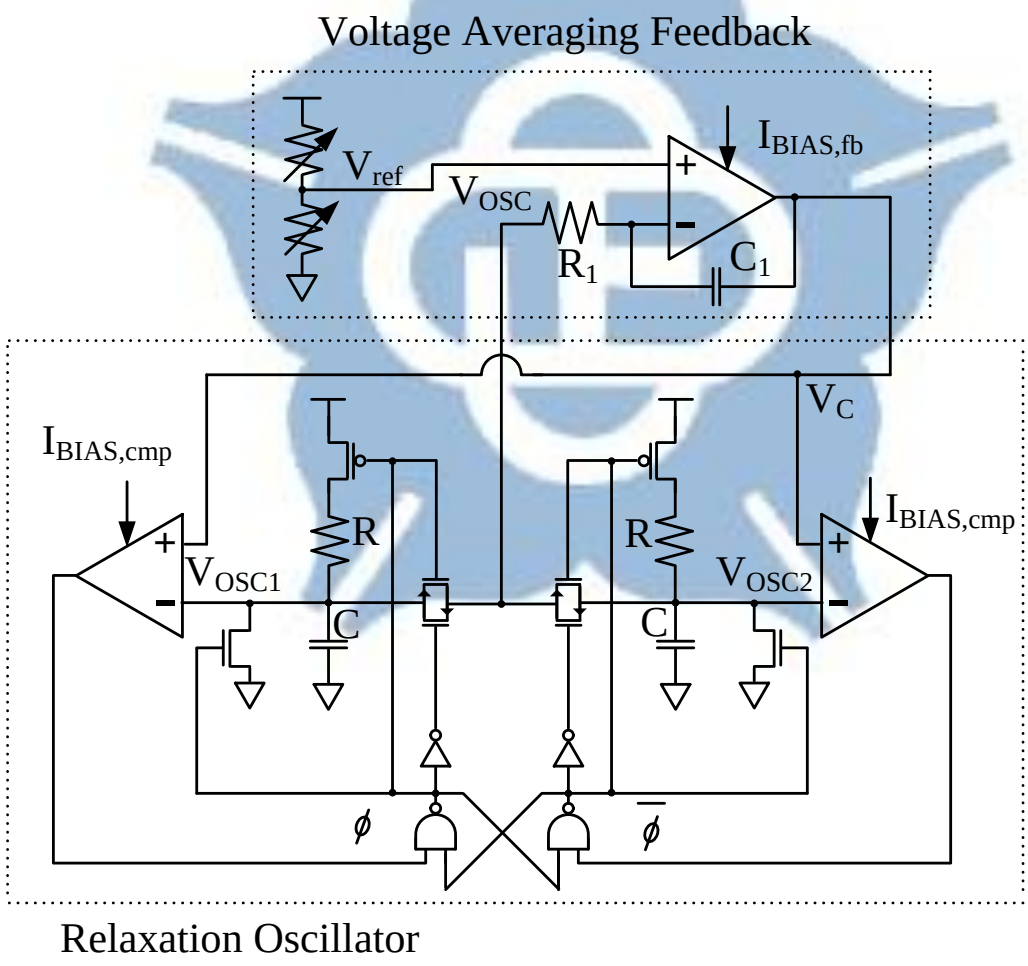

Fig. 3.8: The architecture VAF relaxation-oscillator [44]

3.2.4 The Relative Reference Modeling On-Chip Silicon Oscillator

An all-digital on-chip oscillator with the relative reference modeling (RRM) is proposed in [49]-[53]. The propagation delay time of the logic cells are easily affected by PVT variations. In RRM, they choose two logic cells from the standard cell library, and one uses as a reference delay cell (RDC), and the other cell uses as the compare delay cell (CDC). With PVT variations, delay time of the RDC and the CDC will be both increased and decreased. However, delay time variations in the RDC and the CDC are not the same. In RRM, they define the delay ratio between these logic cells can be expressed as Eq. 3.1.

$$R(P,V,T) = \frac{D_{CDC}(P,V,T)}{D_{RDC}(P,V,T)} \quad \text{(Eq. 3.1)}$$

where $D_{RDC}(P,V,T)$ and $D_{CDC}(P,V,T)$ are delay time of the RDC and CDC, respectively.

The block diagram of the delay ratio estimator (DRE) is shown in Fig. 3.9. In DRE, two logic cells, RDC and CDC are used to create two ring oscillators, the reference ring oscillator (RRO) and the compared ring oscillator (CRO), respectively. The output of the ring oscillator is connected to the counter to record the oscillation cycles of the oscillator. The value of two counters can be used to calculate the delay ratio R(P,V,T) as expressed in Eq. 3.2.

$$R(P,V,T) = \frac{RRO_{CNT}}{CRO_{CNT}} \quad \text{(Eq. 3.2)}$$

where CRO_{CNT} and RRO_{CNT} are the output of the CRO counter and the RRO counter, respectively. The CRO counter will count from 0 to N_{TIME}, and then the two ring oscillators are stopped. The value of N_{TIME} is power of two, thus the delay ratio R(P,V,T) can be

computed without a divider.

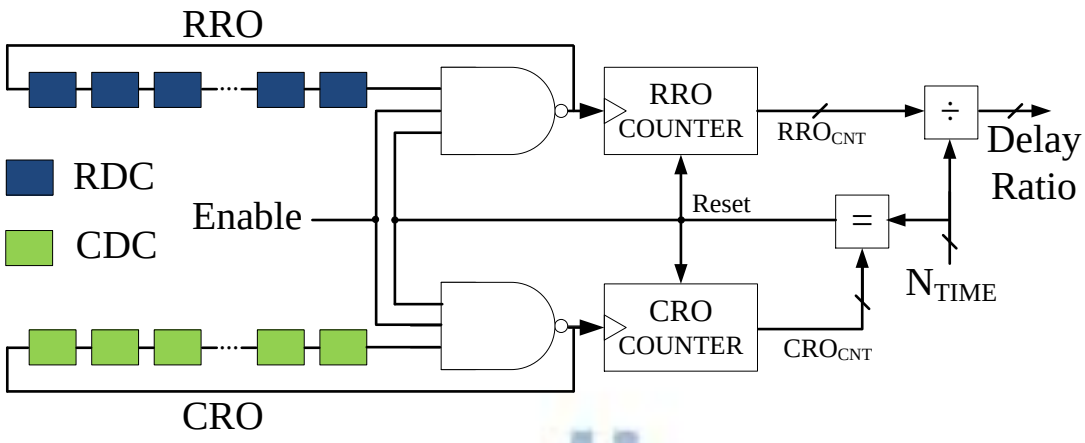

Fig. 3.9: The architecture the delay ratio estimator (DRE).

Fig. 3.10 shows the simulation results of R(P,V,T) and D_{RDC} in typical corner, where D_{RDC} is the period of the reference ring oscillator. The D_{RDC} can be estimated in terms of R(P,V,T) as expressed in Eq. 3.3.

$$D_{RDC}(P,V,T) = coef_0 + coef_1 R(P,V,T) + coef_2 R^2(P,V,T) + \cdots + coef_n R^n(P,V,T) \quad \text{(Eq. 3.3)}$$

where $coef_0$ to $coef_n$ is the coefficients of nth-order curve modeling. In RRM, the high order of curve modeling results in high cost. As a result, they need to trade-off the accuracy and design cost. Finally, they uses a second-order mapper to implement the Eq.3.3.

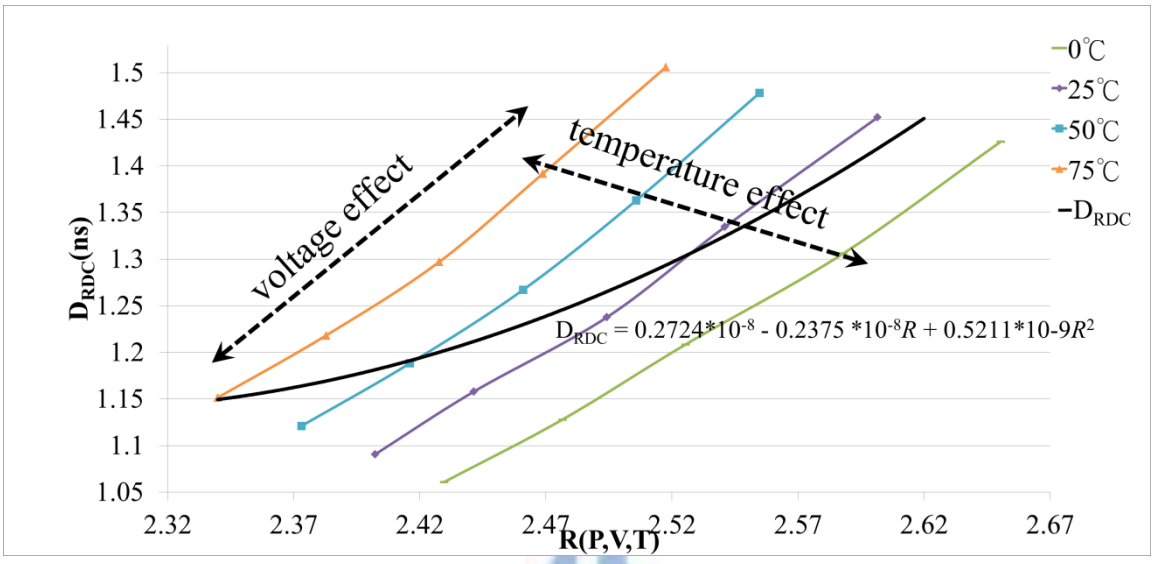

Fig. 3.10: The R(P,V,T), D_{RDC}, and the second-order curve modeling diagram.

Fig. 3.10 shows the system architecture of the RRM. It is composed of a delay ratio estimator (DRE), a mapper and a DCO. The DRE computes the R(P,V,T) at chip run time with voltage and temperature variations. Firstly, the RRM requires multi point calibration. In the calibration mode, the DRE estimates the R(P,V,T) and D_{RDC} at different voltage and temperature. According to R(P,V,T) and D_{RDC} values to build up the second-order curve modeling diagram as shown in Fig 3.11. The mapper is used to to replace the second order equation calculation with a mapping table. Then the mapper outputs control code to the DCO.

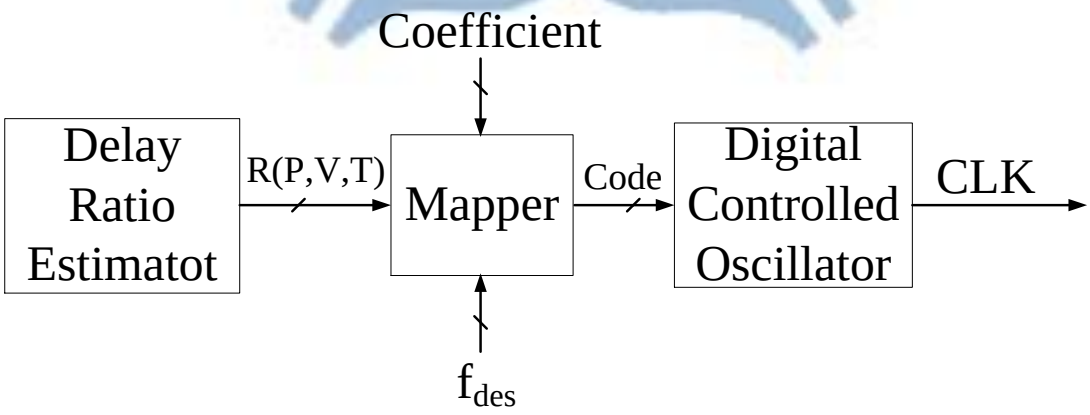

Fig. 3.11: The architecture of the Relative Reference Modeling On-Chip Silicon

Oscillator.

The digital approach of the RRM makes it easy to design the on-chip oscillator. However, a high order polynomial is required to minimize the modeling error, and thus, a mapper is required to reduce the area cost. In addition, in RRM, multi-points calibration is required. The high testing cost make it is not suitable for mass production.

3.2.5 The Prior All-Digital On–Chip Silicon Oscillator

Our proposed all-digital on-chip silicon oscillator is the incremental work of [54]. The propagation delay time of the logic cells are easily affected by process, voltage, and temperature (PVT) variations. The [54] proposed a design which uses the relative modeling to build up the on-chip oscillator. In addition, voltage and temperature classifiers are proposed to reduce the modeling error from temperature and voltage variation to achieve a better accuracy of the output frequency. The system architecture of the all-digital on-chip oscillator is shown in Fig. 3.12. It is composed of a delay ratio estimator, a voltage classifier, a temperature classifier, a linear calculator, and a digitally controlled oscillator (DCO). The DRE estimates the R1(V,T) and the R2(V,T) at chip run time under voltage and temperature variations. This design need to measure the values of R1(V,T), R2(V,T), and $P_{RRO}(V,T)$ with five different voltages (V_1 to V_5) and four different temperatures (T_1 to T_4). Therefore, it needs to measure the values of R1(V,T), R2(V,T), and $P_{RRO}(V,T)$ in totally 20 different (V,T) cases, and $P_{RRO}(V,T)$ means the period of the RRO.

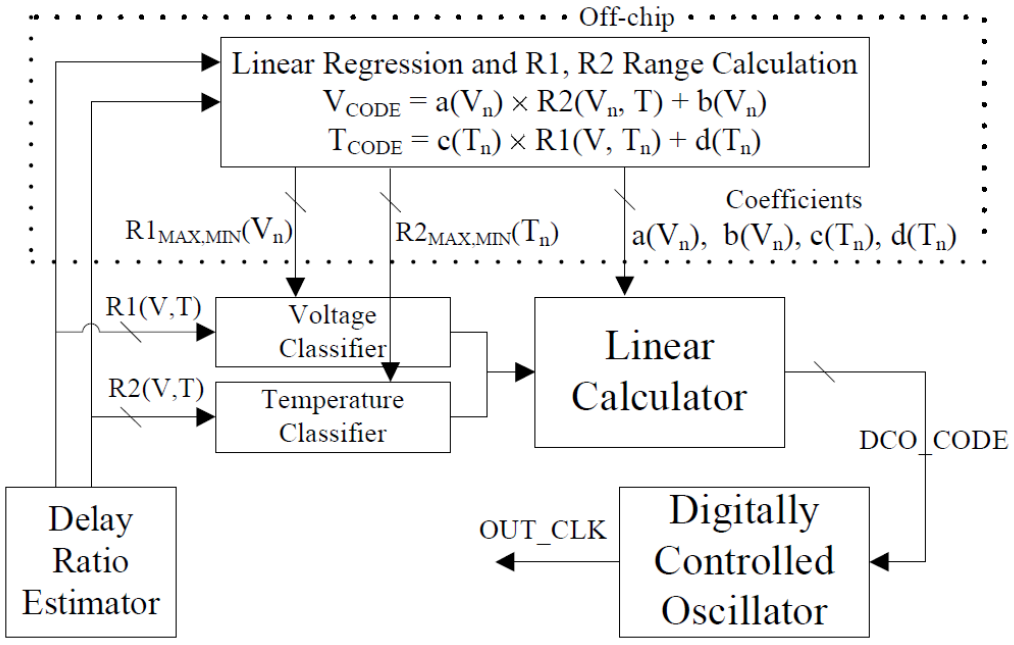

Fig. 3.12 The proposed on-chip oscillator architecture [54]

The block diagram of the delay ratio estimator (DRE) is shown in Fig. 3.13. In DRE, three logic cells, RDC, CDC1, CDC2 are used to create three ring oscillators, the reference ring oscillator (RRO), the compared ring oscillator 1 (CRO1), and the compared ring oscillator 2 (CRO2), respectively. The output of the ring oscillator is connected to the counter to record the oscillation cycles of the oscillator.

The value of these counters can be used to calculate the delay ratio R1(P,V,T) and R2(P,V,T) as follows

$$R1(P,V,T) = \frac{D_{CDC1}(P,V,T)}{D_{RDC}(P,V,T)} \text{(Eq 1.3)}$$

$$R2(P,V,T) = \frac{D_{CDC2}(P,V,T)}{D_{RDC}(P,V,T)} \text{(Eq 1.4)}$$

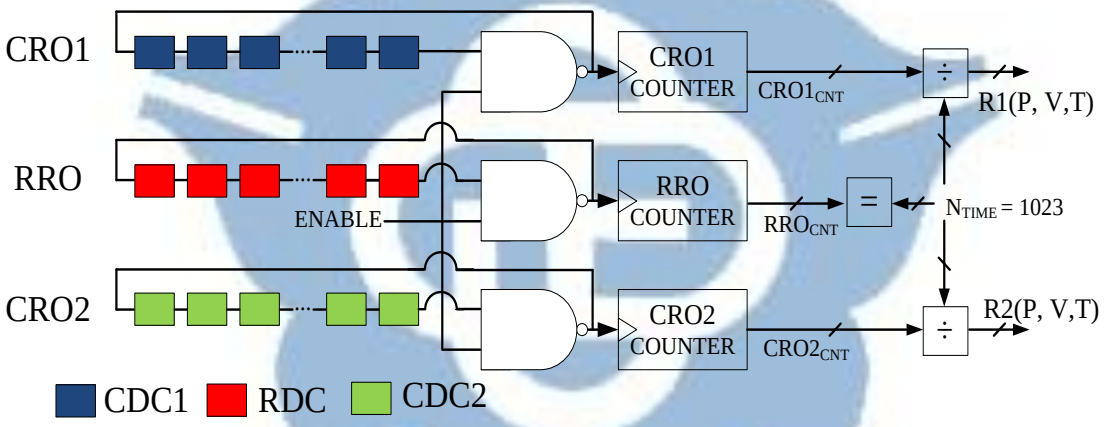

Fig. 3.13 The architecture of delay ratio estimator [54]

Fig. 3.14 shows the cell selection flow chart for RDC, CDC1, and CDC2. At first, any three logic cells are selected from the standard cell library to build up the delay ratio estimator.

Subsequently, we need to perform SPICE simulation of the DRE with PVT variations to obtain delay ratios, R1(P,V,T) and R2(P,V,T). In [54], the voltage varies from V1 to V5 (V1=0.90V, V2=0.95V, V3=1.00V, V4=1.05V, and V5=1.10V), and temperature varies from T1 to T4, (T1=0℃, T2=25℃, T3=50℃, and T4=75℃). In addition, the process variation includes typical process corner (TT), best process corner (FF), and worst process corner (SS). Therefore, it needs to simulate the DRE in totally 60= (3×5×4) different P, V, T combinations.

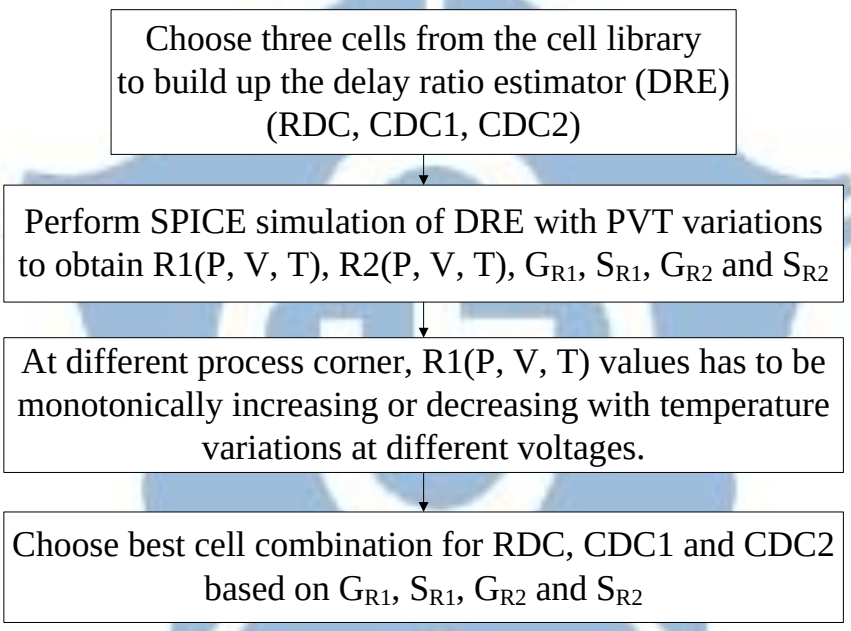

Fig. 3.14 Flow chart of how to choose cells from the cell library [54]

Fig. 3.15 shows the delay ratios R1(V,T) and R2 (V,T) versus the period of the RRO, PRRO(V,T) in typical process corner. In Fig. 3.15(a), with a fixed voltage value, the delay ratio R1 varies with temperature variations. In Fig. 3.15(c), with a fixed temperature value, the delay ratio R2 varies with voltage variations.

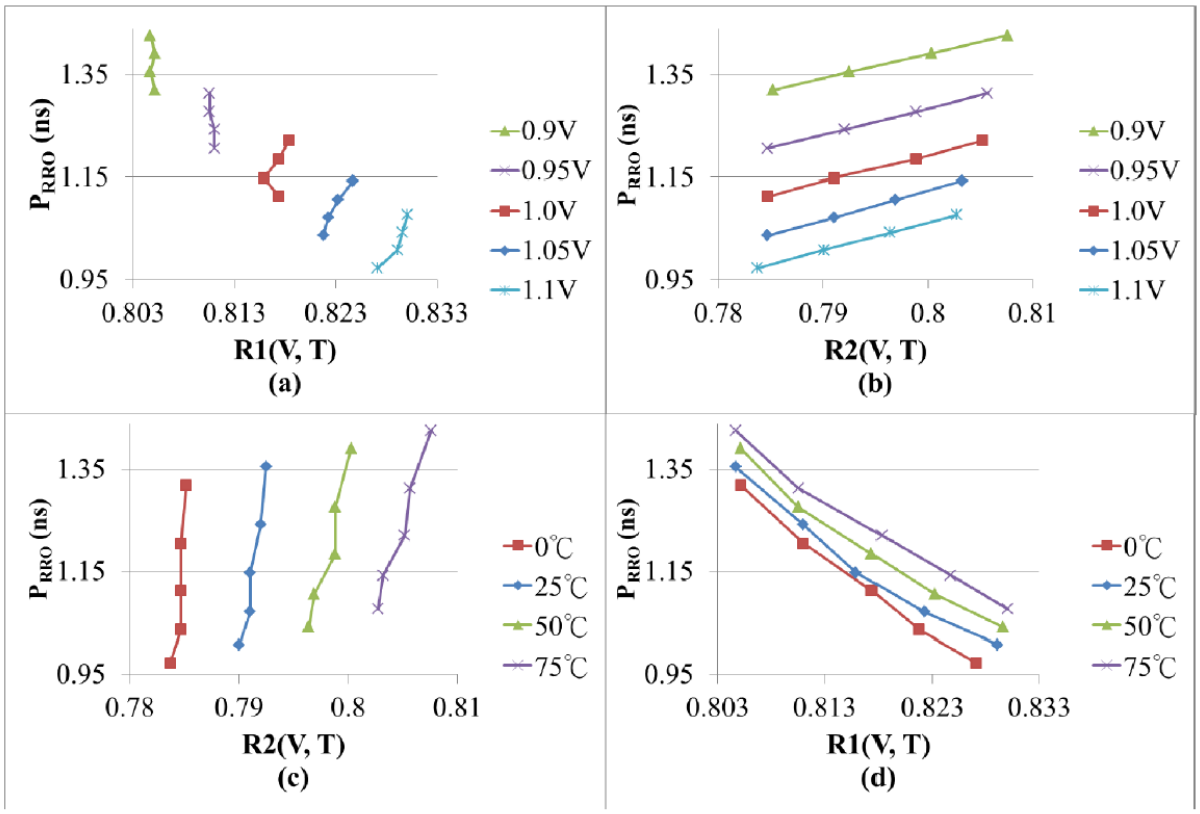

Fig. 3.15 Delay ratios R1 (V, T) and R2 (V, T) versus PRRO (V, T) in typical process corner [54]

This on-chip oscillator with a relative modeling uses a voltage and temperature classifier to roughly estimate the supply voltage and operation temperature at chip run time. The design provides a systematic way to automatically generate the on-chip oscillator with PVT variations tolerance. Thus the design can operate with a low supply voltage, and is very suitable for low-power and low-cost system-on-a-chip application.

3.3 Motivation of Proposed On-Chip Silicon Oscillator

In section 3.2.5 we have discussed the prior design [54]. The advantagess of this work is that it can operate under low voltage with PVT variation tolerance. However, the design flow of choosing DRE cells as shown Fig. 3.14 is too complicated and takes too much effort to find a beast cell combination. As a result, we want to simplify the cells selection procedure of the DRE by using the idea of gated ring oscillator. We assume that tuning the number of open gates in oscillator may have similar result as the cell picking rules in [54].

3.4 The System Architecture

We have done some simulations by connecting different number of CDC cells to see the performance of trend line of voltage versus delay ratio. Furthermore, we define equations to define the performance index includes range and the gradient. We want the trend lines of voltage versus temperature and voltage do not have any overlapped and as straight as possible to avoid wrong decision on decide current voltage and temperature.

$$\text{Range} = \text{Max}(R(Vn+1,Ti)) - \text{Min}(R(Vn-1,Tj)) \quad \text{(Eq. 3.1)}$$

$$\text{Gradient} = |(R(V_{n+1},T_{75}) - R(V_{n+1},T_0))| + |(R(V_n,T75) - R(V_n,T_0))| \quad \text{(Eq. 3.2)}$$

In Eq.3.1 and 3.2 present voltage range from 0.9V to 1.0V and i and j present temperature range from 0℃ to 75℃. In different cell combination, the value of range is larger one is better, and the value of gradient is also smaller one is better. The result of temperature versus delay ratio of is shown in Fig. 3.16. Each lines present voltage from 0.9V to 1.1V under FF, TT and SS corners. Different colors show the different selected

number of the delay cells in the CRO from 1 to 20 and from left to right in Fig. 3.16. When the number of the selected delay cells in the CRO bellows larger, the distance of trend line within the group is wider.

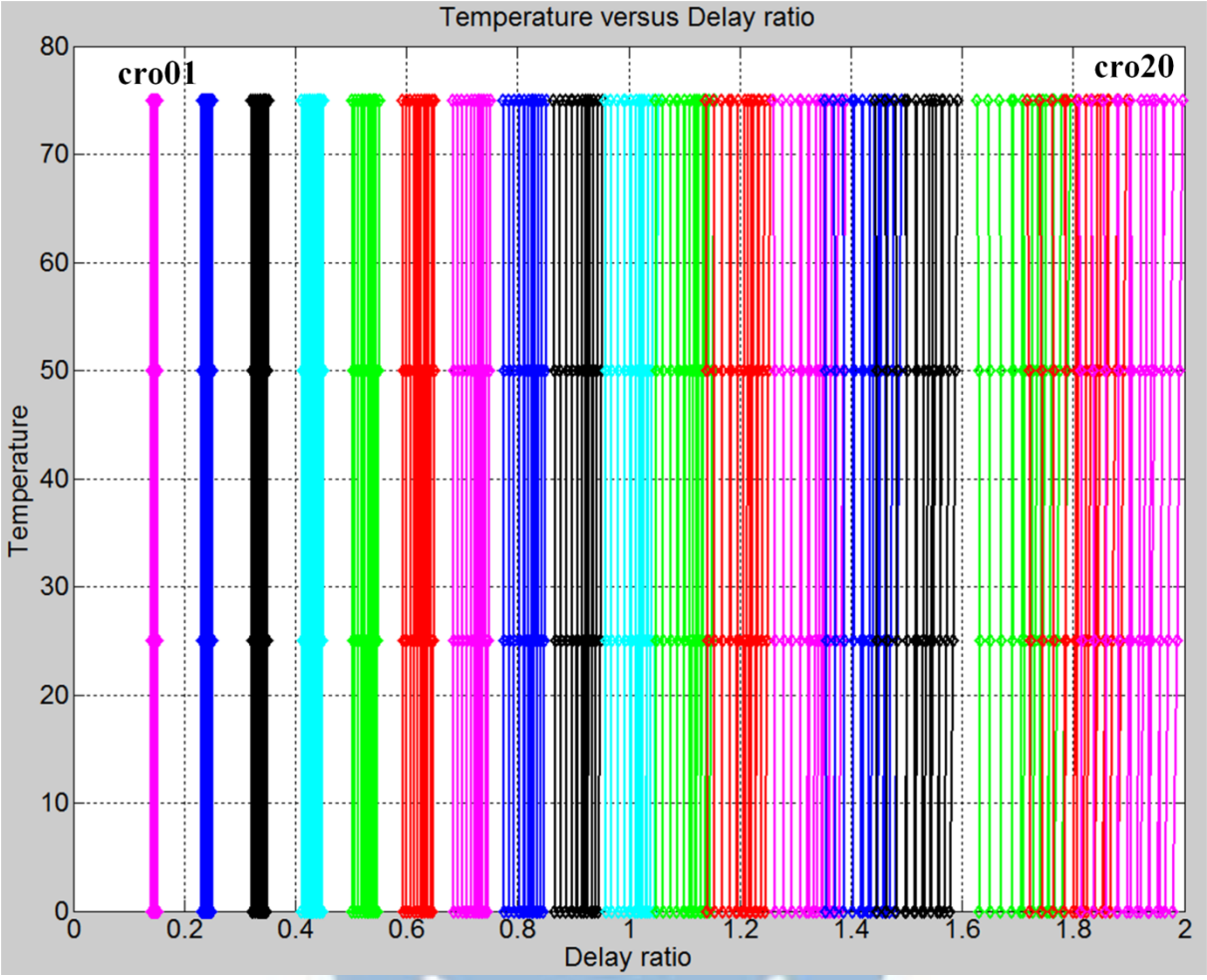

Fig. 3.16 temperature versus delay ratio under different connected number of CDC

Fig .3.17 shows the relation between the gradient and the range of different selected delay cells of CRO. The selected delay cells of the CRO is from 0 to 20 and from the lower left corner to right upper corner under FF, TT and SS corner. We want the wider the range and the smaller the gradient but in Fig. 3.17 we see the trade trade-off between range and gradient.

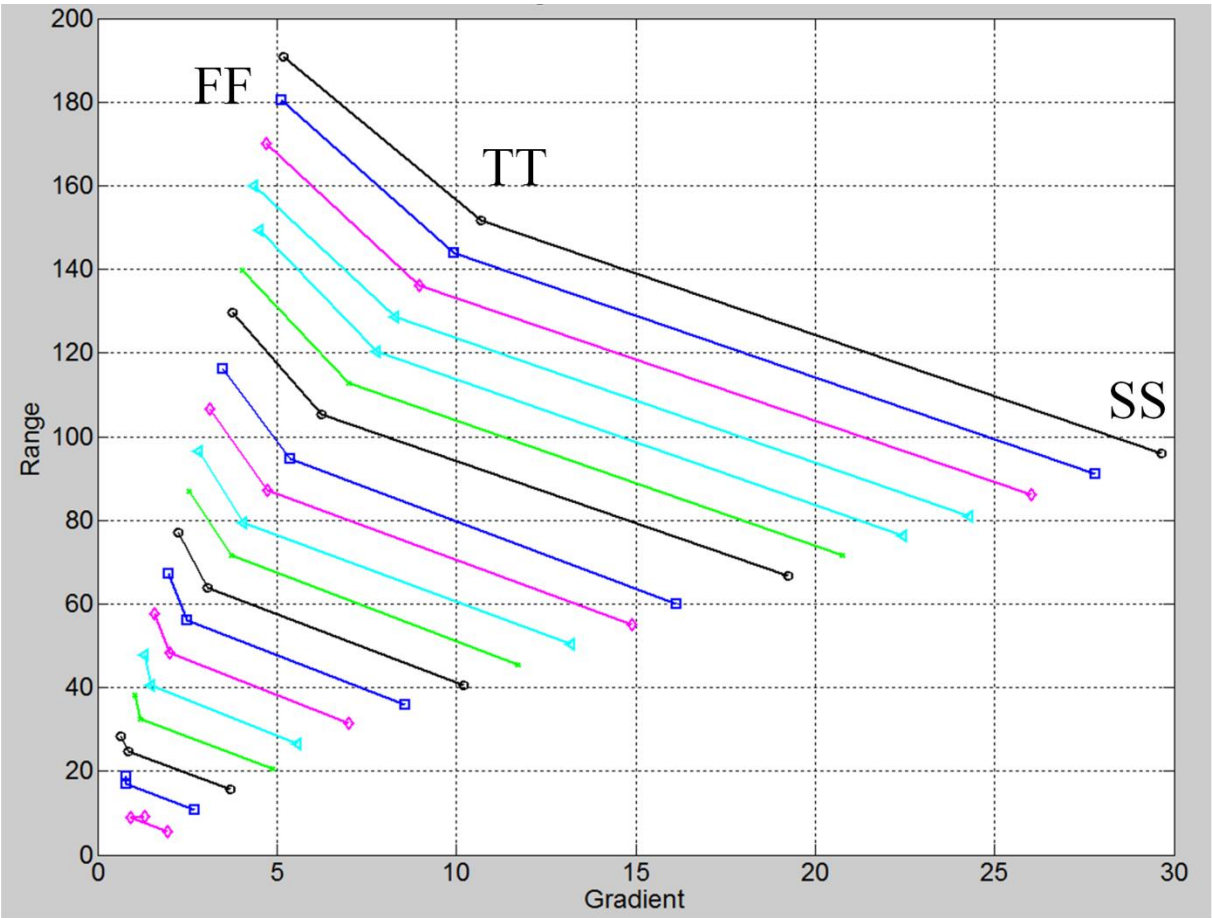

Fig. 3.17 Gradient versus range under different connected number of CDC

From above test, we understand that we may be able to control the delay ratio versus temperature and voltage trend line by choosing different number of delay cells of the CDC. As a result, we replace ring-oscillators in Fig. 1.34 of the DRE unit by three DCOs. The proposed is shown in Fig. 3.18. The gated path oscillator consists of 64 coarse tuning delay cells (CDCs). The resolution of the proposed DCO is two consisted cells gates delay time. In the proposed coarse tuning architecture, the one coarse tuning stage delay is two consisted cells gates delay time. We aimed to use this architecture to see the trend line of voltage versus delay ratio and temperature versus delay ratio will change with the coarse code. Moreover, we expect the trend line will have similar or better performance than prior decision cells.

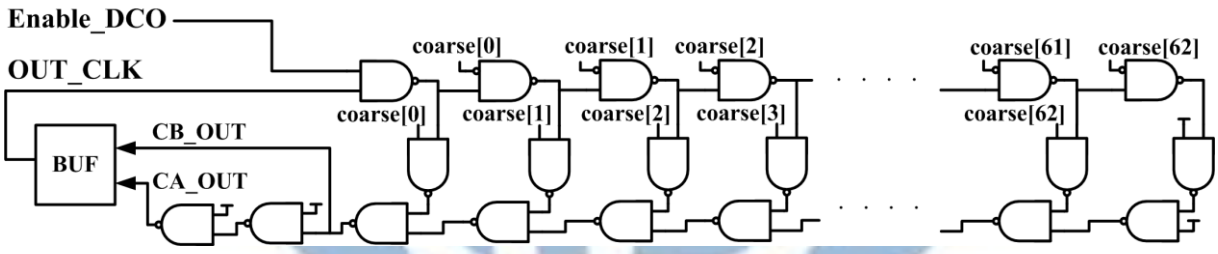

Fig. 3.18 Proposed gated path oscillator

Chapter 4 Conclusion and Future Works

4.1 Conclusion

In this thesis, we use relative reference modelling method to build up the delay ratio estimator. Then the characteristics of the delay ratios can be used to identify the process and temperature variations which apply in design of a static voltage sensor and an on-chip silicon oscillator. The linear calculator of the proposed IR-drop monitor can output an accurate voltage value with PVT variations. The digital controlled oscillator can be controlled by digital control code and output the stable 5 MHz frequency.

Both proposed relative reference modelling designs are implemented with standard cells with the advantages of the digital design approach, such as insensitivity to noise, robustness to process variations and work environment, more design flexibility to other processes, and suitable for SoC design.

4.2 Future Works

In this thesis, there are some weaknesses in our relative reference modeling based IR-drop monitor and relative reference modeling approached on-chip silicon oscillator. The area and power of three ring oscillators affect the IR-drop monitor and on-chip silicon oscillator. In addition, the simulation time of DRE is too long. It takes approximate three days to produce one delay ratio value in circuit simulation. Although we have found methods to accelerate simulation speed, it still needs one day to generate the delay ratio. As a result, we want to improve the architecture of oscillator in DRE to reduce the throughput of the DRE. TDC might be the practicable method to reach the goal through its high resolution and faster calculation speed.

If we can improve the DRE, then the proposed relative reference modeling based voltage sensor and relative reference modeling approached on-chip silicon oscillator will achieve more contribution at sensing environment parameters and also have more real-time estimation ability.

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