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應用於三維晶片時脈同步之全數位延遲
鎖相迴路

An all-digital delay-locked loop for 3D
ICs die-to-die clock synchronization



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摘要

由於成熟的系統晶片(SoC)技術，讓許多模組可以整合至單一晶片中，然而在系統晶片中，存在著許多長距離的繞線，這些長距離繞線會限制系統晶片的可最高工作時脈速度。因此，矽穿孔技術被提出來縮短這些長距離接線。根據莫爾定理，當有愈多的電晶體被整合至單一晶片後，矽穿孔包裝技術在近年來也變得越來越普及與重要。然而，在製造過程中之矽穿孔延遲變異現象有可能會導致系統晶片工作不正常。這是因為使用矽穿孔之三維晶片，上下層晶片互相傳送資料時，矽穿孔延遲變異現象將會對傳送資料能否正常造成影響。對於此問題，將三維晶片中的上下層晶片之時脈相位同步，將能有效簡化三維晶片資料傳輸的問題。

因此，我們提出了兩種全數位延遲鎖相迴路架構，可以有效同步三維晶片之各個晶片間之時脈相位。我們提出之全數位延遲鎖相迴路是由台積電 90 奈米製程之標準元件庫實現，並且具有容忍製程飄移的能力。其中第一種架構可以使用我們所提出的數位可控制變容延遲線來補償矽穿孔延遲變異現象，第二種架構因為使用單一矽穿孔，因此可以直接避免掉矽穿孔延遲變異現象。第一種架構使用雙矽穿孔可以工作的時脈範圍為 300MHz ~ 1GHz，鎖定後最大相位誤差為 21.9ps，第二種單一矽穿孔架構可以工作的時脈範圍為 200MHz ~ 1GHz，鎖定後之最大相位誤差小於 80ps。

關鍵詞：全數位延遲鎖相迴路、矽穿孔、三維積體電路、單一矽穿孔通道，晶片與晶片間之時脈訊號同步。

Abstract

With the advance of system-on-a-chip (SoC) technology, many transistors can be integrated into a single chip. However, in an SoC, there may have many global wires with long distances, and the highest clock speed of a SoC are usually limited by these wires. Therefore, the through silicon via (TSV) technology is proposed to shorten the length of the global wires. Besides, according to the Moore's Law, the (TSV) technology becomes more and more popular in recent years with the increasing of the integrated transistors in a single chip. However, the TSV delay variation phenomenon during manufacturing may cause the SoC systems not work correctly. The TSV delay variation problem affects the data transmission between chips. Therefore, the clock signals between chips need to be phase aligned to simplify the data transmission between chips.

Hence, two all-digital delay-locked loops (ADDLLs) with architectures are proposed in this thesis to synchronize the clock signals between two chips. The proposed ADDLLs are implemented in TSMC 90nm CMOS process with standard cells, and they can tolerate PVT variations. Besides, the first ADDLL architecture with two TSV channels can compensate for the TSV delay variation with the digital controlled varactor-based delay line. The second ADDLL architecture can avoid the TSV delay variation problem with only a single TSV channel. The first ADDLL with two TSVs can operate with the input frequency range from 300MHz to 1GHz, and the maximum phase error is 21.9ps. The second ADDLL with a single TSV can operate with the input frequency range from 200MHz to 1GHz, and the maximum phase error is 80ps.

Index Terms — All-Digital Delay-Locked Loop, Through Silicon Via, 3-D ICs, Single TSV channel, Die-to-die clock synchronization.



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中華民國一零三年七月

寫於國立大學資訊工程所

Contents

Chapter 1	Introduction	1
1.1	Through Silicon Via	1
1.1.1	3-D Network-on-Chip (NoC)	4
1.1.2	Random Access Memory in 3-D ICs	5
1.1.3	3-D ICs Power-Supply Networks	6
1.2	Impact of TSV delay variation	7
1.3	Die-to-Die Clock Synchronization	9
1.3.1	3D-IC Die-to-Die Clock Synchronization	16
1.3.2	Motivation.....	20
1.4	Thesis Organization	21
Chapter 2	3-D ICs clock synchronization with two TSVs	22
2.1	Architecture Overview	22
2.2	The Locking Procedure.....	24
2.3	Circuit Design and Implementation of ADDLL with two TSVs	27
2.3.1	Digitally Controlled Varactor (DCV).....	27
2.3.2	Phase and Frequency Detector (PFD)	29
2.3.3	Digital Controlled Delay Line (DCDL).....	31
2.3.4	FDL.....	33
2.4	Experimental Results	35
2.4.1	Specifications of the ADDLL with two TSVs.....	35
2.4.2	Simulation Results of the ADDLL with two TSVs	36
2.4.3	Comparison Table.....	38
Chapter 3	3-D ICs clock synchronization with a single TSV.....	40
3.1	Architecture Overview	40
3.2	The Locking Procedure.....	42
3.3	Circuit Design and Implementation of ADDLL with a single TSV.....	44
3.3.1	Pulse Generator (PG)	44
3.3.2	TDC-Embedded CDL	46
3.3.3	Phase Detector (PD).....	47
3.4	Experimental Results	49
3.4.1	Test Circuit Implementation.....	49
3.4.2	Specifications	55
3.4.3	Simulation Results.....	58
3.4.4	Phase Error.....	63
3.5	Performance Comparisons	64
3.5.1	Two Proposed ADDLLs	64

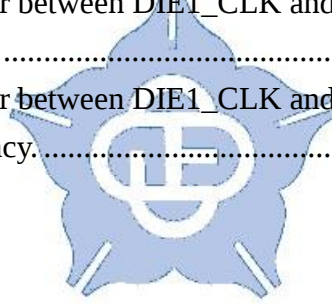
3.5.2	Comparison with prior arts	66
Chapter 4	Conclusion and Future Works	68
4.1	Conclusion	68
4.2	Future Works	69
References		70



List of Figures

Figure 1.1 System on a board (SoB)	1
Figure 1.2 System in a package (SiP).....	2
Figure 1.3 System on A Chip (SoC)	2
Figure 1.4 2D-SoC and 3D-IC.....	3
Figure 1.6 Concept of 3D-DRAM Architecture	5
Figure 1.7 Concept of Clustered and Distributed Topology.....	6
Figure 1.8 TSV resistive-open phenomenon	7
Figure 1.9 Ring-oscillator architecture for TSV delay variation detection	8
Figure 1.10 3D-IC Architecture.....	9
Figure 1.11 3D-IC timing diagram without TSV delay variation	10
Figure 1.12 3D-IC timing diagram with TSV delay variation (clock leads data) ...	11
Figure 1.13 3D-IC timing diagram with TSV delay variation (clock lags data)	11
Figure 1.14 Bidirectional timing diagram with TSV delay variation (clock leads data)	13
Figure 1.15 Bidirectional timing diagram with TSV delay variation (clock lags data)	14
Figure 1.16 Bidirectional timing diagram with clock synchronization.....	15
Figure 1.17 Dual-Locking DLL Architecture.....	17
Figure 1.18 Timing diagram of Dual-Locking DLL	18
Figure 1.19 Dual-Delay-Locked Loop Architecture	19
Figure 2.1 The proposed ADDLL Architecture with two TSVs.....	22
Figure 2.2 Timing diagram of TSV delay variation compensation	24
Figure 2.3 Timing diagram of die-to-die clock synchronization.....	26
Figure 2.4 The proposed DCV-based delay line architecture.....	27
Figure 2.5 The Phase and Frequency Detector.....	29
Figure 2.6 The timing diagram of PFD	30
Figure 2.7 The digital controlled delay line	31
Figure 2.8 The FDL	33
Figure 2.9 Layout of The Proposed ADDLL.....	35
Figure 2.10 Simulation waveform of the proposed ADDLL.....	36
Figure 3.1 The proposed ADDLL architecture with a single TSV	40
Figure 3.2 The timing diagram of locking procedure.....	42
Figure 3.3 The Pulse Generator (PG)	44
Figure 3.4 The timing diagram of PG	45
Figure 3.5 The TDC-Embedded CDL	46
Figure 3.6 The Phase Detector	47

Figure 3.7 The concept of locking window	47
Figure 3.8 The timing diagram of PD	48
Figure 3.9 The test circuit.....	49
Figure 3.10 The DCO	51
Figure 3.11 The Divider	54
Figure 3.12 The layout of the ADDLL with a single TSV	55
Figure 3.13 The layout of the ADDLL with a single TSV	56
Figure 3.14 The post-layout simulation of ADDLL with a single TSV	58
Figure 3.15 The phase error between DIE1_CLK and DIE2_CLK at FF corner with 1GHz operation frequency.....	59
Figure 3.16 The phase error between DIE1_CLK and DIE2_CLK at FF corner with 300MHz operation frequency.	60
Figure 3.17 The phase error between DIE1_CLK and DIE2_CLK at TT corner with 1GHz operation frequency.....	60
Figure 3.18 The phase error between DIE1_CLK and DIE2_CLK at TT corner with 300MHz operation frequency.	61
Figure 3.19 The phase error between DIE1_CLK and DIE2_CLK at SS corner with 1GHz operation frequency.....	61
Figure 3.20 The phase error between DIE1_CLK and DIE2_CLK at SS corner with 300MHz operation frequency.....	62



List of Tables

Table 1.1 PVT conditions in this thesis	21
Table 2.1 The Delay Time of DCV-Based Delay Line	28
Table 2.2 The dead-zone of the proposed PFD	30
Table 2.3 The properties of The Proposed DCDL	32
Table 2.4 Properties of The Proposed FDL	34
Table 2.5 Performance Comparisons.....	38
Table 3.1 Pulse width of The generated pulse	45
Table 3.2 The output frequency range of the slow DCO.....	52
Table 3.3 The output frequency range of the fast DCO.....	53
Table 3.4 I/O pins information of ADDLL with a single TSV	57
Table 3.5 The TSV mirror mismatch.....	63
Table 3.6 The deadzone of the phase detector	63
Table 3.7 Comparison table of ADDLL between a single TSV and two TSVs	65
Table 3.8 Gate count of ADDLL between a single TSV and two TSVs	65
Table 3.9 Performance Comparison with prior arts.....	67
Table 3.10 The power consumption of the DFFs	67

Chapter 1 Introduction

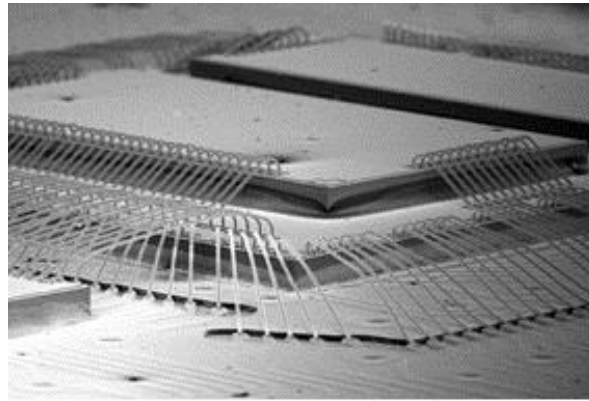
1.1 Through Silicon Via

System on a board (SoB) package technology is widely applied to integrate a system on a printed circuit board (PCB), as shown in Fig. 1.1. The advantage of SoB is low cost. However, the bonding wires and interconnection wires between modules cause RLC parasitic effects. The speed of the integrated system is restricted, and the power consumption due to the extra driving buffers is high. In addition, the volume of the system is very large.



Figure 1.1 System on a board (SoB)

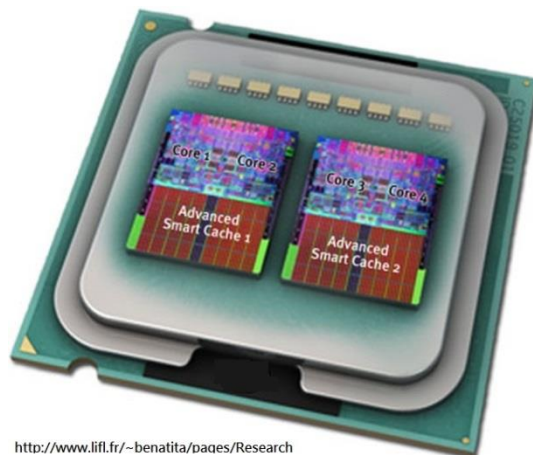
The system in a package (SiP) is to improve the disadvantages of SoB. As shown in Fig. 1.2, the modules are stacked to reduce the length of bonding wire, and the volume of SiP is smaller than the traditional SoB technology. However, the bonding wire is still huge, and has large impact on the speed limitation of modules.



<http://javier.esilicon.com/page/3/>

Figure 1.2 System in a package (SiP)

In order to improve the speed of the system, the system on a chip (SoC) technology is proposed, as shown in Fig. 1.3. The modules are integrated on a single chip, and the bonding wires are eliminated. The RLC effects caused by bonding wires or interconnection wires on PCB can be greatly reduced, and the power consumption also can be reduced due to the elimination of driving buffers. According to Moore's Law, there are a lot of transistors can be integrated in a single chip, and the numbers of transistors are doubled every 18 months. However, Moore's Law seems to achieve a bottleneck in recent years, because the size of the transistor is hardly reduced due to the physical limitations of the transistor.



<http://www.lifl.fr/~benatita/pages/Research>

Figure 1.3 System on A Chip (SoC)

With the skillful SoC technology, more modules can be integrated in a single chip. However, in a SoC, there may have global wires with long distances, and it may limit the highest clock speed of a SoC. Therefore, the through silicon via package technology is proposed to shorten the length of the global wires. Besides, in order to follow the Moore's Law, Through Silicon Via (TSV) [1]-[2] also plays an important role in three-dimensional integrated circuit (3D-IC). As shown in Fig. 1.4, the TSV package technology can connect many two-dimensional integrated circuits (2D-ICs), and the numbers of I/O can be increased. In addition, the delay time of the TSV channel is much smaller than the bonding wires.

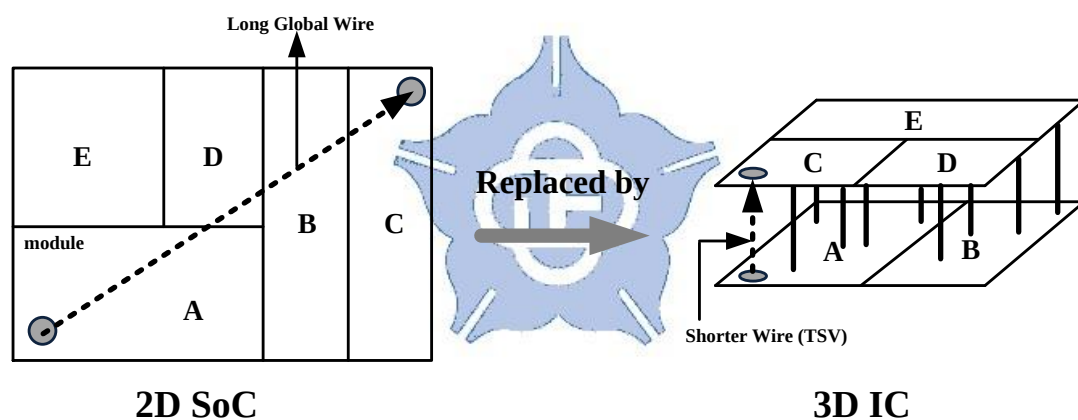


Figure 1.4 2D-SoC and 3D-IC

In summary, the advantages of TSV package are the small wire delay, large numbers of I/O, low power consumption, and high circuit speed, and therefore the TSV technology is popular in recent years. Due to the TSV, the performance of the SoC becomes more powerfully.

1.1.1 3-D Network-on-Chip (NoC)

As shown in Fig. 1.5, TSVs can be applied to the network-on-chip (NoC) to connect multi-processors in 3D-NoC architecture [9]-[18]. In [12], to measure the wire delay impact of the 3D-NoC, the 3D-NoC architectures are proposed to compare the wire delay impact between traditional 2D-NoC and 3D-NoC. However, there are many design challenges for the 3D-ICs such as yield, power density, design flow, design cost, and IC testing. Besides, the thermal problem in 3D-NoC is caused by the traffic block of the network packets. For 3D-NoC traffic block problem, the traffic-balanced topology-aware multiple routing adjustment (TTMRA) [16] is proposed to dynamically adjust the routing path of each packet.

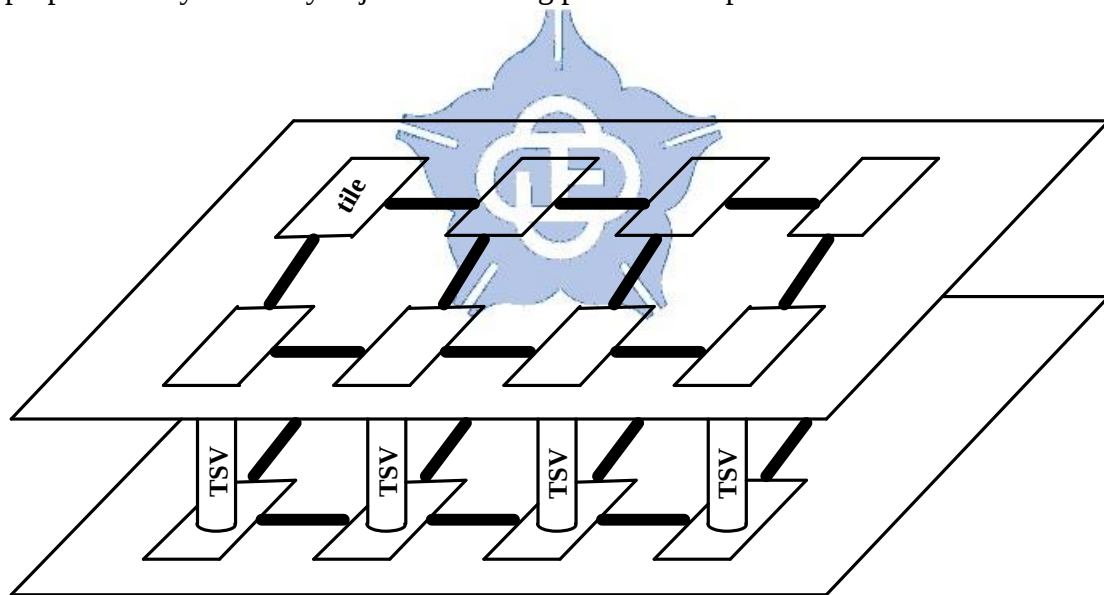


Figure 1.5 Concept of 3D-NoC Architecture

1.1.2 Random Access Memory in 3-D ICs

In [19]-[21], TSV package technology is applied to Random Access Memory (RAM) design. The advantages of TSV technology are performance improvement, power reduction, and increase the chip density. To overcome the I/O speed limitation, several buffered modules are proposed, and many additional chips are added to buffer the data pins. However, the additional chip solutions increase the power consumption, and latency of the operation.

In [19], a Double-Data-Rate (DDR3) DRAM with TSVs is proposed to overcome the limits of conventional DRAMs. It proposes a master and slave architecture to reduce the power consumption as compared to the conventional quad-die packages (QDPs). This architecture also increases the I/O speed of DRAMs and reduces the noise at power lines.

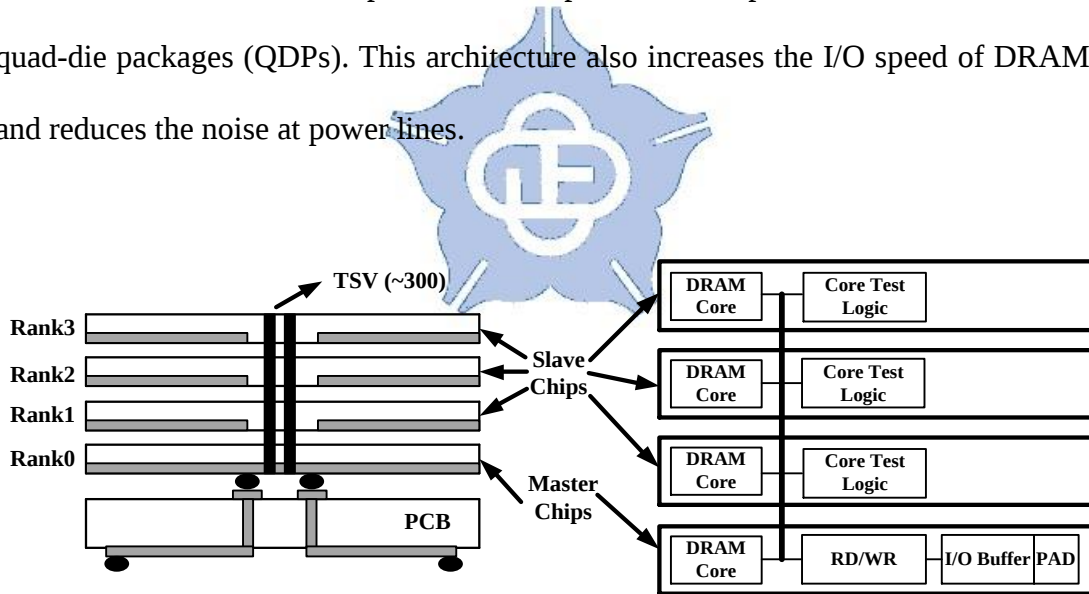


Figure 1.6 Concept of 3D-DRAM Architecture

1.1.3 3-D ICs Power-Supply Networks

IR-drop is the resistive voltage drop in power and ground lines. IR-drop is a design challenge in the advanced CMOS process in addition to leakage power and dynamic power consumption. The distributed TSV topology for 3-D ICs power-supply networks are proposed in [22]-[25].

In [22], the distributed topology power planning is better than traditional 2-D power planning and clustered power planning. The distributed topology power planning is proposed to reduce the IR-drop of 3-D ICs about 21% and also lower the dynamic noise of 3-D ICs about 32% as compared to 2-D ICs. It shows that the distributed topology of 30 stacked tiers can improve nearly 42% lower dynamic noise and 50% lower IR-drop than the clustered power planning topology in 3-D ICs. However, the design challenge for distributed topology power planning is that too many macros or array structure designs are not suited because the small pitch TSVs are required.

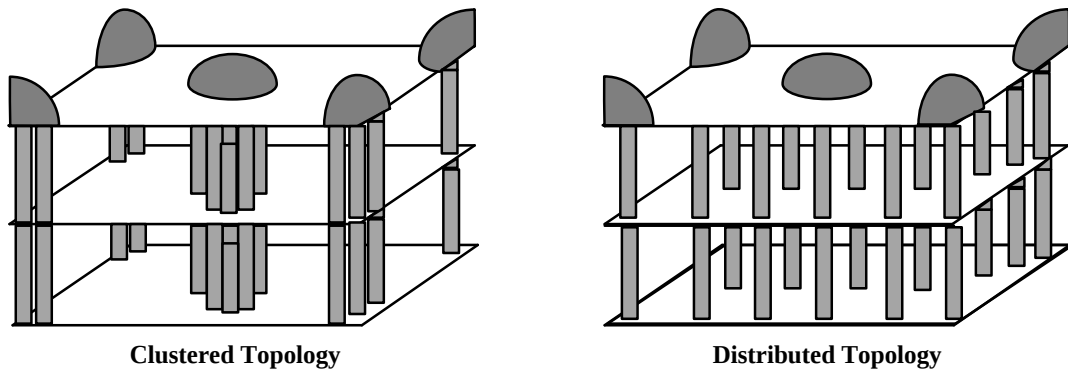
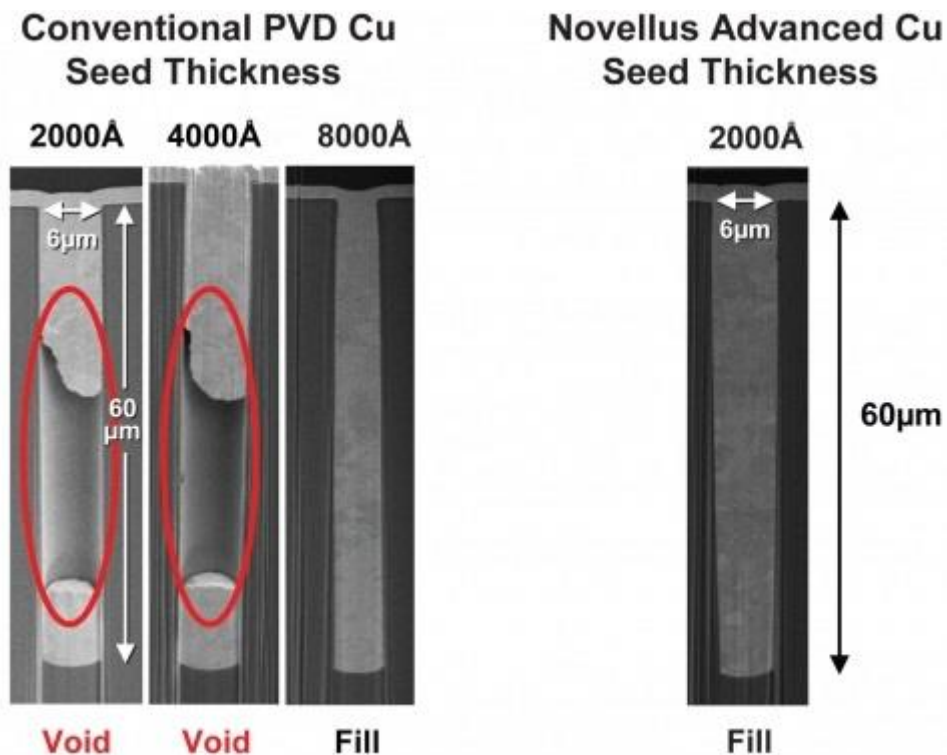


Figure 1.7 Concept of Clustered and Distributed Topology

1.2 Impact of TSV delay variation

As mentioned above, the TSV package technology becomes more and more popular in recent years. However, the cost of the TSV package technology is high, and TSVs may be faulty during manufacturing. Many researches [3]-[8] pay attention to the TSV delay variation problem. In [8], this research focuses on analyzing the impact of TSV open defects. It shows that the resistive-open phenomenon will increase the propagation delay of the TSV. Fig. 1.8 shows the TSV resistive-open phenomenon.



<http://www.newswire.co.kr/newsRead.php?no=463484>

Figure 1.8 TSV resistive-open phenomenon

In [3]-[6], a ring oscillator (RO)-based architecture is proposed to detect the TSV delay variation phenomenon, as shown in Fig. 1.9. In [4], the variable output threshold is proposed. They can detect the parametric delay fault by dynamically switching the inverter driving ability to observe the output frequency of the RO. This research shows that the maximum TSV delay variation between two TSVs can be up to about 500ps. In [3], this research focuses on pre-bond TSV test. It also uses the RO architecture to detect the TSV propagation delay variation with different RC parameters. The proposed pre-bond TSV testing can detect leakage and resistive-open faults during manufacturing test. In accordance with above results, the propagation delay of TSVs varies with process variations.

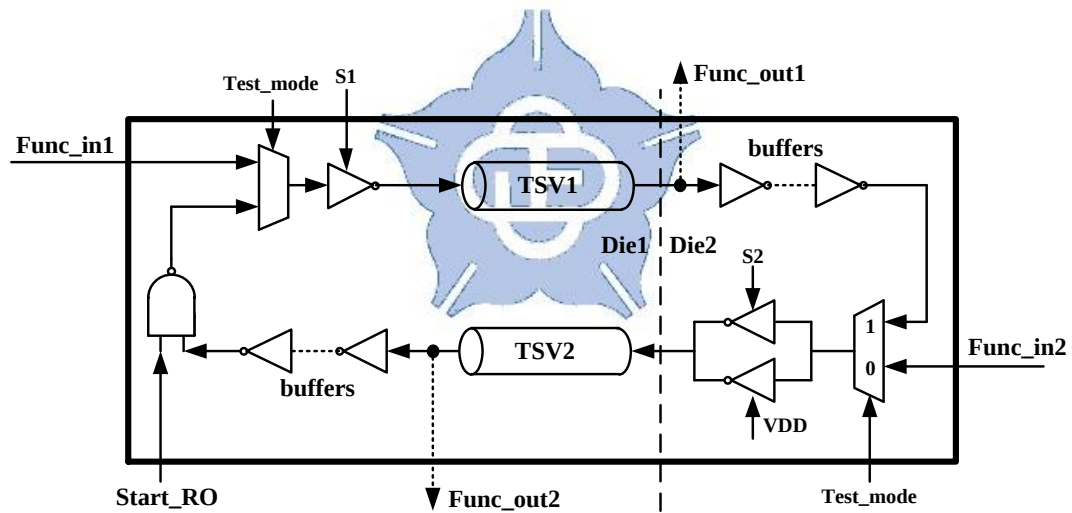


Figure 1.9 Ring-oscillator architecture for TSV delay variation detection

1.3 Die-to-Die Clock Synchronization

In order to explain the impact of the TSV delay variation, a 3D-IC architecture is shown in Fig. 1.10 for illustration. There are two dies connected by many TSVs, and the data signals can transmit between two dies.

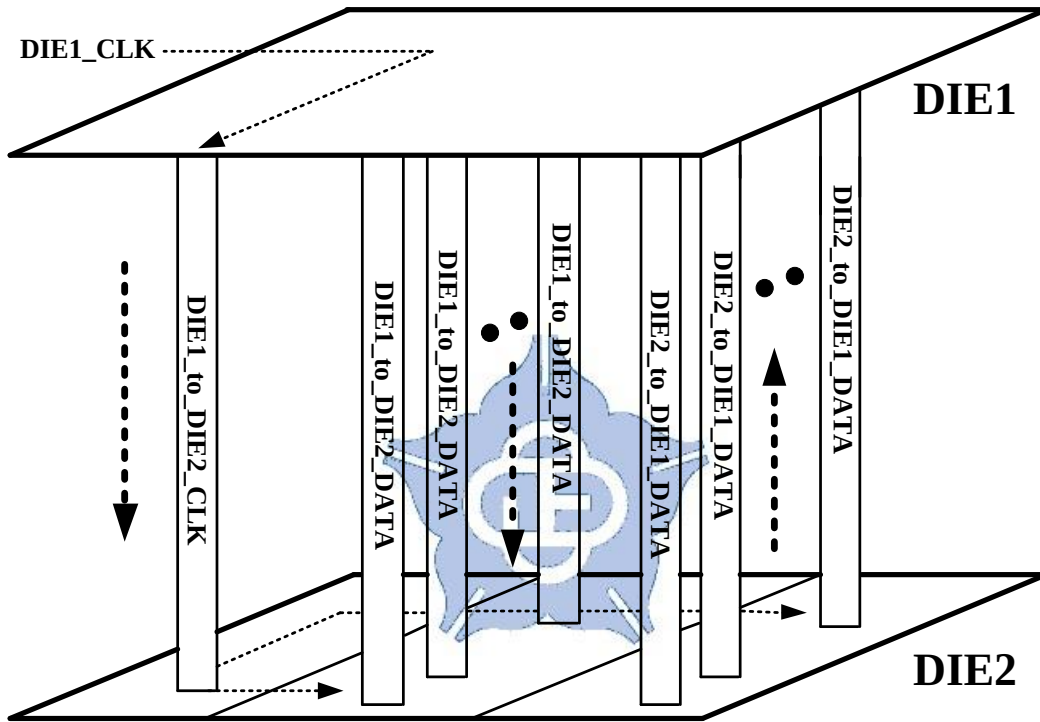


Figure 1.10 3D-IC Architecture

The DIE1_CLK is the global reference clock for the system, and the DIE1_CLK will send to the DIE2 to trigger the circuits on the DIE2. For the ideal situation shown in Fig. 1.11, the TSVs are manufactured without TSV delay variation, and the TSV delays for the clock signal and the data signal are exact the same. For the signal transmission from DIE1 to DIE2, the DIE1-2_DATA signal in DIE2 can be sampled correctly by the negative edge of the DIE1-2_CLK signal. The DIE2_DATA is transmitted back to the DIE1 and denoted as DIE2-1_DATA. Then, the positive edge

of the DIE1_CLK is used to sample the DIE2-1_DATA. Therefore, without TSV delay variation, data can be transmitted between dies correctly.

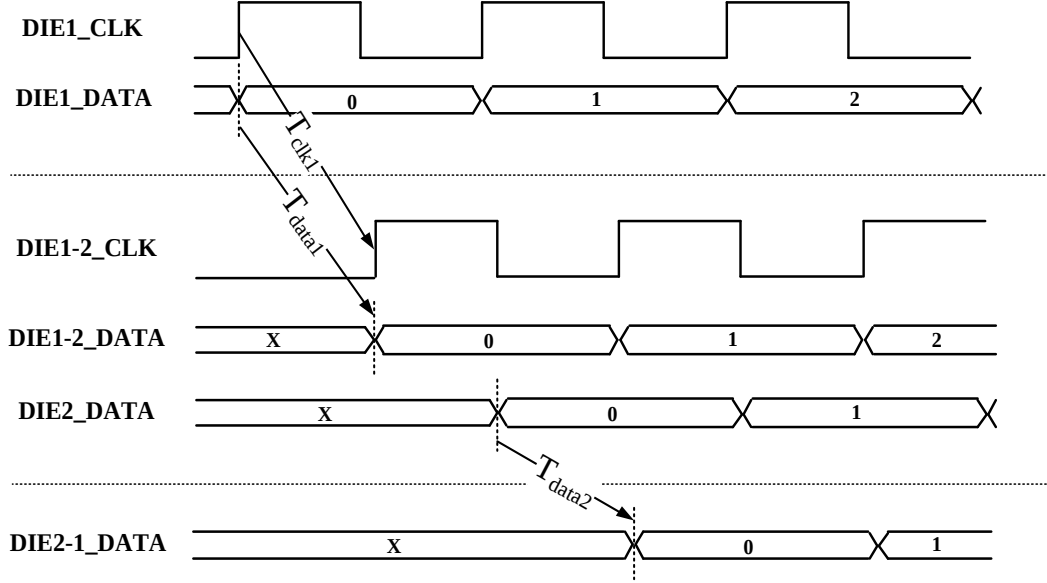


Figure 1.11 3D-IC timing diagram without TSV delay variation

Fig 1.12 shows that the delay time of the clock TSV is shorter than the delay time of the data TSV, and thus, the DIE1-2_CLK leads DIE1-2_DATA. The DIE1-2_CLK can sample the DIE1-2_DATA correctly while Eq. 1.1 is satisfied.

$$T_{hold} < \Delta < T_{cycle} - T_{setup} \quad (\text{Eq. 1.1})$$

where T_{setup} means a small timing margin before the positive edge of the clock signal for the DFFs to sample the data signal, and the data signal must be stable in this timing margin. T_{hold} means a small timing margin after the positive edge of the clock signal for the DFFs to sample the data signal, and the data signal must be stable in this timing margin. T_{cycle} means the clock period of the system clock.

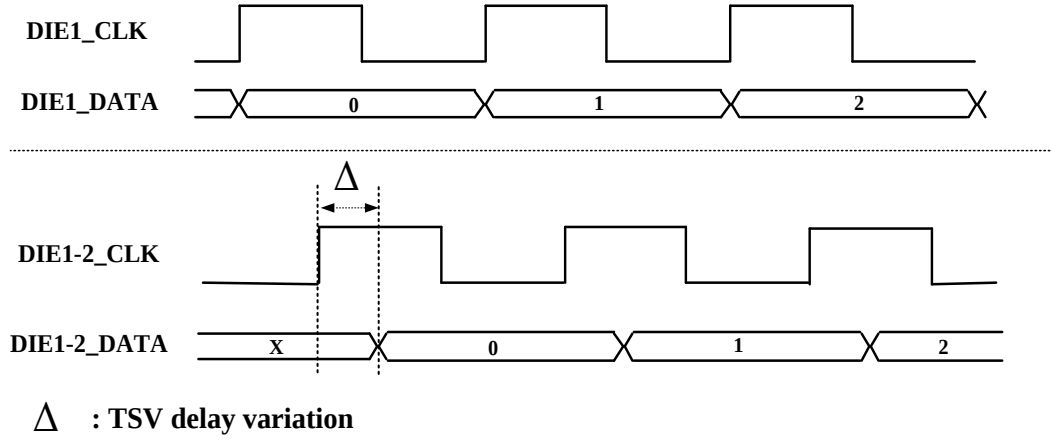


Figure 1.12 3D-IC timing diagram with TSV delay variation (clock leads data)

Fig. 1.13 shows that the delay time of clock TSV is larger than the delay time of data TSV, and thus, the DIE1-2_CLK lags DIE1-2_DATA. The DIE1-2_CLK can sample the DIE1-2_DATA correctly while the Eq. 1.2 is satisfied.

$$T_{setup} < \theta < T_{cycle} - T_{hold} \quad (\text{Eq. 1.2})$$

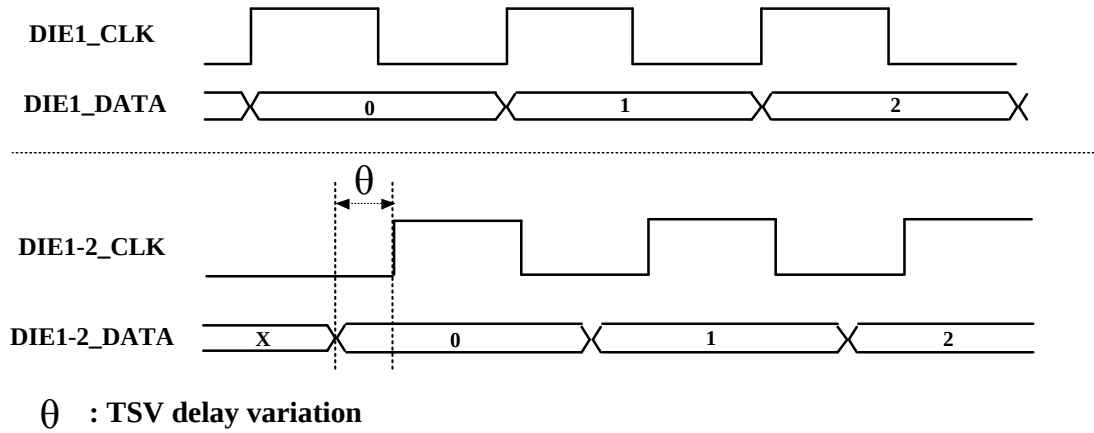


Figure 1.13 3D-IC timing diagram with TSV delay variation (clock lags data)

When there is no delay variations in TSVs, the data can easily transmit between dies, as shown in Fig. 1.11. However, when there has delay variations in TSVs, the Eq.

1.1 and Eq. 1.2 should be satisfied or the data transmission between dies may be failed.

Fig. 1.14 shows that the DIE1_CLK, DIE1_DATA are transmitted from DIE1 to DIE2 and denoted as DIE1-2_CLK and DIE1-2_DATA, respectively. At this moment, the DIE1-2_CLK leads DIE1-2_DATA due to the TSV delay variation phenomenon. The DIE2_DATA will transmit back to DIE1 after the DIE1-2_DATA is sampled by the positive edge of DIE1-2_CLK. In this case, if the DIE2-1_DATA can be sampled by the positive edge of DIE1_CLK successfully, the Eq. 1.3 should be satisfied.

$$T_{hold} < T_{clk1-2} + T_{data2-1} < T_{cycle} - T_{setup} \quad (\text{Eq. 1.3})$$

where T_{clk1-2} means, the delay time while the clock signal transmits from DIE1 to DIE2 and denoted as DIE1_CLK and DIE1-2_CLK. The $T_{data2-1}$ means, the delay time while the data signal transmits from DIE2 to DIE1 and denoted as DIE2_DATA and DIE2-1_DATA, respectively.

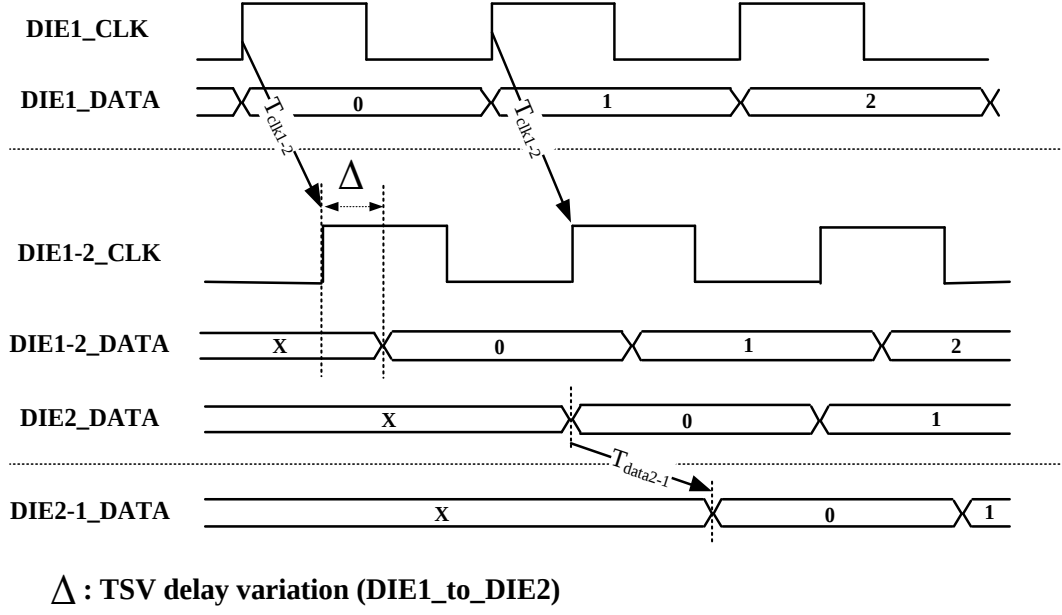


Figure 1.14 Bidirectional timing diagram with TSV delay variation (clock leads data)

Fig. 1.15 shows that the DIE1_CLK, DIE1_DATA are transmitted from DIE1 to DIE2 and denoted as DIE1-2_CLK and DIE1-2_DATA, respectively. At this moment, the DIE1-2_CLK lags DIE1-2_DATA due to the TSV delay variation phenomenon. The DIE2_DATA will transmit back to DIE1 after the DIE1-2_DATA is sampled by the positive edge of DIE1-2_CLK. In this case, if the DIE2-1_DATA can be sampled successfully, the Eq. 1.4 should be satisfied.

If ($T_{clk1-2} + T_{data2-1} < T_{cycle}$)

$$T_{clk1-2} + T_{data2-1} < T_{cycle} - T_{setup} \quad (\text{Eq. 1.4})$$

else,

$$T_{hold} < T_{clk1-2} + T_{data2-1}$$

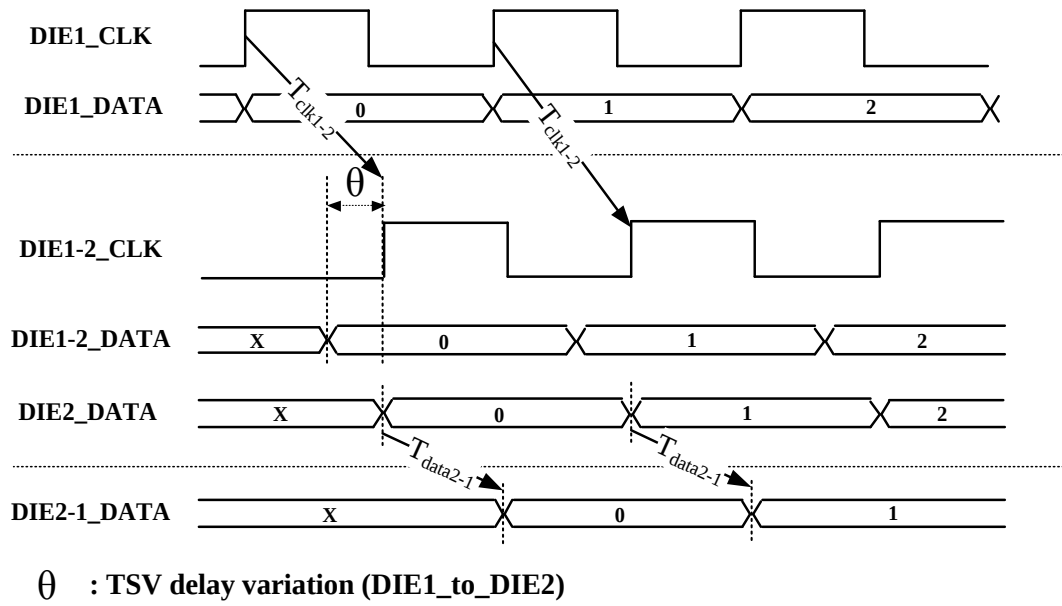


Figure 1.15 Bidirectional timing diagram with TSV delay variation (clock lags data)

In summary, the T_{clk1-2} , $T_{data2-1}$, Δ and θ are unpredictable values because the TSV delay value is decided after manufacturing. In order to simplify the problem in data transmission between dies, the phase between the DIE1_CLK and DIE1-2_CLK should be aligned.

In Fig. 1.16, the data transmission problem is simplified when the phase between DIE1_CLK and DIE1-2_CLK is aligned. The unpredictable values after the manufacturing are simplified to one value. Finally, the data access formula can be simplified, as Eq. 1.5. In addition, Eq. 1.5 is easy to be satisfied.

$$T_{hold} < T_{data2-1} < T_{cycle} - T_{setup} \quad (\text{Eq. 1.5})$$

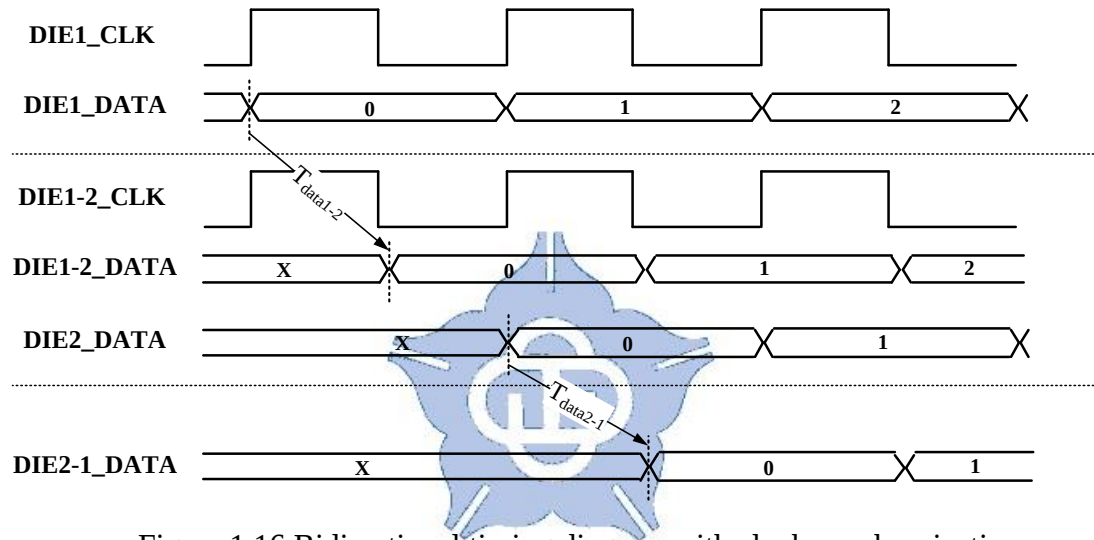
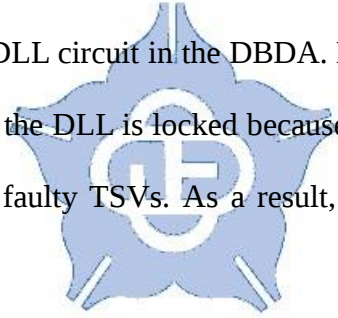


Figure 1.16 Bidirectional timing diagram with clock synchronization

1.3.1 3D-IC Die-to-Die Clock Synchronization

In high-speed SoC design, the clock distribution through clock tree buffers should be carefully planned to eliminate the clock skew between the global clock and the local clocks. Phase-locked loops (PLLs) and delay-locked loops (DLLs) [26]-[29] are widely applied to cancel the clock skew. As mentioned in section 1.3, if the clock phase between two dies are aligned, the data transmission between dies can be simplified.

The 3D-ICs die-to-die clock synchronization between two dies are proposed by [30]-[33]. In order to reduce the data confliction time between the memory outputs of the stacked dies, a DLL-based data self-aligner (DBDA) [30] is proposed. A replica TSV delay is needed for the DLL circuit in the DBDA. However, the DBDA may still have a large phase error after the DLL is locked because the unpredictable TSV delay variations may occur due to faulty TSVs. As a result, the replica TSV delay is not reliable.



A dual-locking DLL [31] is proposed for 3-D ICs die-to-die synchronization, as shown in Fig. 1.17. This architecture needs two loops to finish die-to-die clock synchronization. The first loop path is from Die1_clk, DCDL, TSV1, divider (Div), buffer (B2), TSV2, buffer(B2) to PD (Phase Detector). The θ is defined as the total delay of a divider (Div), a TSV2, and two buffers (B2). When the first loop is locked, the Die1_clk and the fb are phase aligned. That means, the Φ_1 plus the delay time of θ can be phase aligned with Die1_clk, as shown in Fig. 1.18. The second loop path is from Die1_clk, divider (Div), buffer (B1), TSV2, buffer (B1) to PD, and thus, the Φ_1 signal sends to the 2-Phase DCDL to generate the Die2_clk signal and the out signal. That means, the Die1_clk plus the delay time of θ can be phase aligned with the out signal. The 2-Phase DCDL is divided into two same delay lines, and it can generate

two phases (Die2_clk and out). The Die1_clk plus θ equals to the $\Phi1$ plus double θ , and the double θ is generated by 2-Phase DCDL. After the second loop is locked, the Die1_clk and the Die2_clk are phase aligned, as shown in Fig. 1.18.

The phase error caused by the delay mismatch between the real TSV and the replica TSV delay [30] will not occur in [31] because the delay of TSVs does not need to be mirrored in the dual-locking DLL. However, the dual-locking DLL needs to keep fine-tuning the two DLL loops in an interleaved manner to maintain the phase alignment between the clock signals in multiple layers. To perform fine-tuning in two DLLs, the dual-locking DLL needs to regularly change the direction of the forward path and the feedback path, and it may cause a large phase error during maintaining mode.

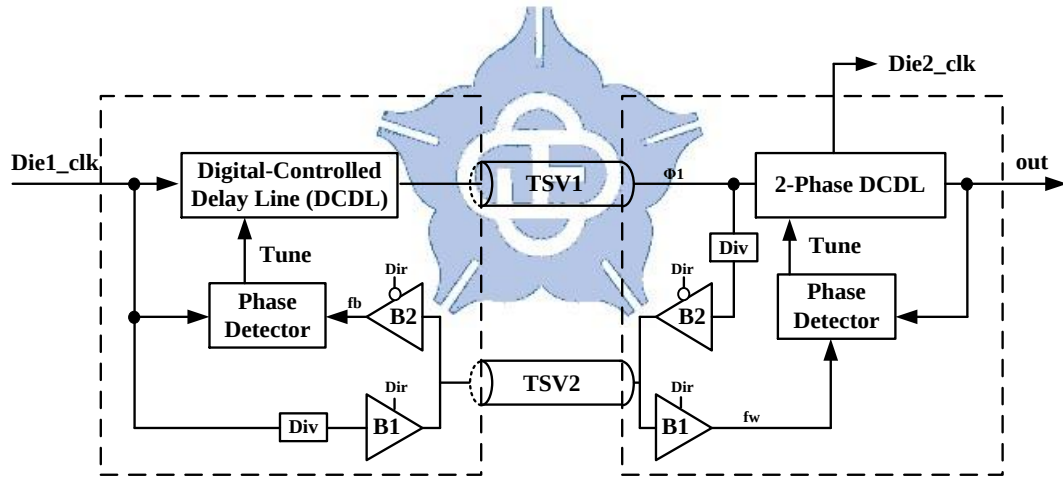


Figure 1.17 Dual-Locking DLL Architecture

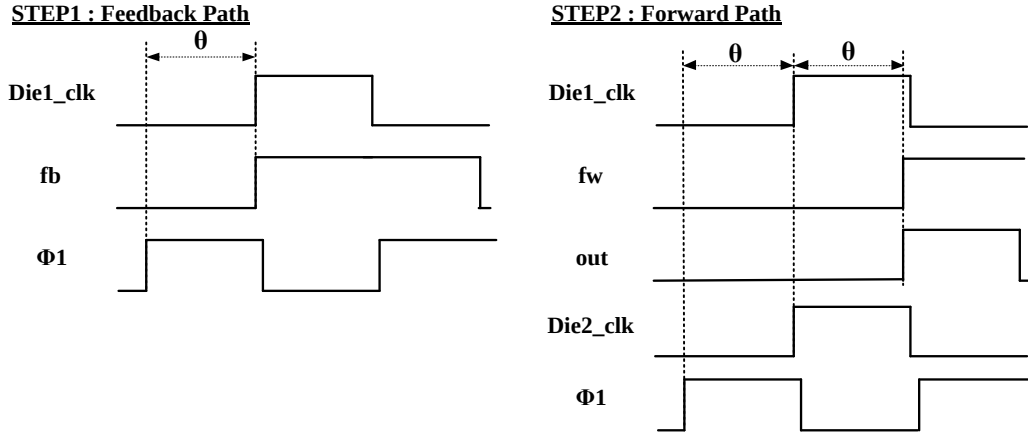


Figure 1.18 Timing diagram of Dual-Locking DLL

A dual-delay-locked loop (D-DLL) [32] is proposed for 3D-IC die-to-die clock deskew circuit applications, as shown in Fig. 1.19. This architecture also needs two loops to finish die-to-die clock synchronization. The first loop path is from $Die1_clk$, TSV1, $VCDL_2$, Buffer, BB, TSV2, BB, $VCDL_1$ to PD, and the second loop path is from $Die2_clk$, BB, TSV2, BB, $VCDL_1$, $VCDL_1$, BB, TSV2, BB to PD. The locking formula is shown in Eq. 1.6, and the total delay of upper path is equal to half of N times $Die1_clk$ period.

Two analog charge-pump-based DLLs are proposed in this design. However, a special bidirectional buffer (BB) is needed to simultaneous transmit signals between two directions on a single TSV. Furthermore, two DLLs are working at the same time, and it increases the design complexity of the D-DLL. In advanced CMOS process, the large voltage control gain problem with a low supply voltage and the leakage current problem of the MOS transistor should be overcome in design of the voltage controlled delay line for operation for the wide frequency range. The above problems will be the design challenges of the D-DLL circuit.

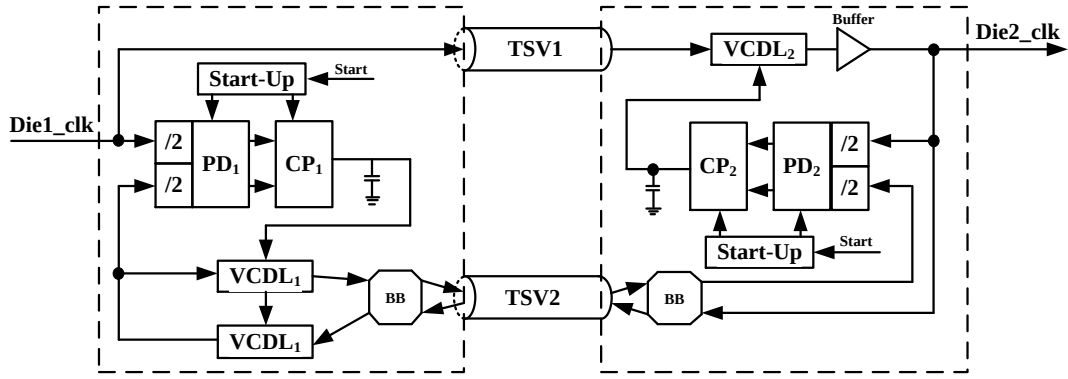


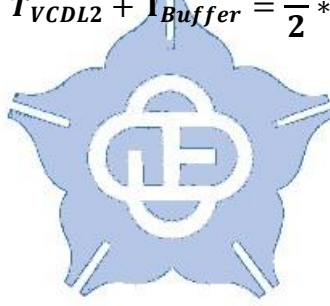
Figure 1.19 Dual-Delay-Locked Loop Architecture

$$T_{loop1} = T_{TSV1} + T_{VCDL2} + T_{Buffer} + T_{BB} + T_{TSV2} + T_{BB} + T_{VCDL1} \quad (\text{Eq. 1.6})$$

$$T_{loop2} = 2T_{BB} + 2T_{TSV2} + 2T_{BB} + 2T_{VCDL1}$$

$$T_{loop1} = T_{loop2} = NT_{Die1_clk}$$

$$T_{TSV1} + T_{VCDL2} + T_{Buffer} = \frac{N}{2} * T_{Die1_clk}$$



1.3.2 Motivation

In recent years, the clock distribution problem and the clock skew problem are the design challenges for the high-speed SoC designs because clock skew may cause operation failure of the system. Besides, the high density transistor designs are implemented by 3-D package technology and face the design challenges of the clock distribution.

For the 3D-IC die-to-die clock synchronization application, DBDA architecture [30] does not consider the TSV delay variation phenomenon. If the TSV delay variation occurs, the phase error between two clock signals may be relatively large. Besides the TSV variation phenomenon, we found that all of the prior architectures require two TSV channels. Therefore, we propose a DLL architecture with a single TSV to eliminate the TSV delay variation. In addition, the cost of TSV manufacturing can be decreased.



1.4 Thesis Organization

Table 1.1 lists the PVT conditions used in the following chapters. The rest of thesis is organized as follows: Chapter 2 depicts the system architecture of the proposed ADDLL with two TSV channels, the locking procedure, and simulation results. Chapter 3 describes the system architecture of the proposed ADDLL with a single TSV channel, the locking procedure, experimental results, and the chip planning of the test chip. Besides, we also list a comparison table to compare the proposed ADDLL with prior arts. At the end of the thesis, we make a conclusion and discuss the future works.

Table 1.1 PVT conditions in this thesis

Corner	Nominal Supply Voltage (V)	Temperature (°C)
FF	1.1	0
TT	1.0	25
SS	0.9	125

Chapter 2 3-D ICs clock

synchronization with two TSVs

2.1 Architecture Overview

Fig. 2.1 shows the proposed ADDLL for 3-D ICs die-to-die clock synchronization with two TSVs. The ADDLL is composed of two digital controlled delay lines (DCDL_A and DCDL_B), two ADDLL controllers (CTRL_A and CTRL_B), two digital controlled varactor-based delay lines (DCV_A and DCV_B), two phase detectors (PD_A and PD_B), two frequency-divided-by-2 circuits, and six tri-state buffers (buf_A to buf_F).

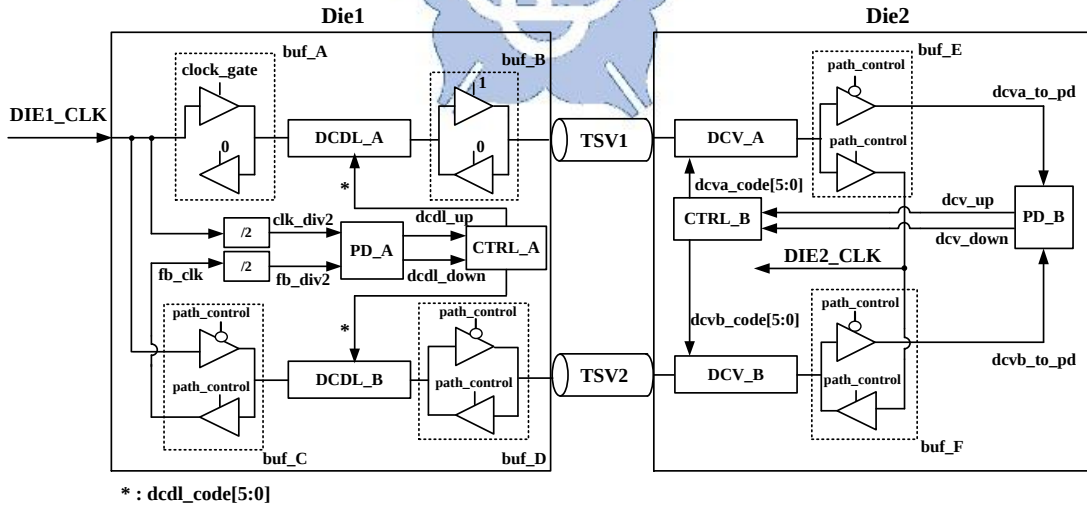


Figure 2.1 The proposed ADDLL Architecture with two TSVs

There are three steps in the proposed ADDLL to achieve die-to-die clock synchronization. **First**, when the ADDLL is reset, the path_control signal is set to zero, and DCDL_A, DCDL_B, DCV_A, and DCV_B are set to provide a minimum

delay time. In the upper delay path, the DIE1_CLK signal passes through buf_A, DCDL_A, buf_B, TSV1, DCV_A, and buf_E to the phase detector B (PD_B) denoted as dcva_to_pd. Similarly, in the lower delay path, the DIE1_CLK signal passes through buf_C, DCDL_B, buf_D, TSV2, DCV_B, and buf_F to the PD_B denoted as dcvb_to_pd. In the proposed ADDLL, six tri-state buffers (buf_A to buf_F) are designed with same tri-state buffers, and the delay time of the DCDL_A is the same as the DCDL_B. Therefore, the phase error between dcva_to_pd signal and dcvb_to_pd signal comes from the delay variations between TSV1 and TSV2.

Second, after TSVs delay variations are compensated, the clock_gate signal is set to zero for three consecutive clock cycles to stop the DIE1_CLK signal propagating to the upper delay path. The clock-gating is performed to recognize the first positive edge transition of the fb_clk signal for the next locking procedure.

Third, after clock-gating is performed, the path_control signal and clock_gate signal are pulled high, and the DIE1_CLK signal passes through buf_A, DCDL_A, buf_B, TSV1, DCV_A, buf_E, buf_F, DCV_B, TSV2, buf_D, DCDL_B, buf_C, and a frequency-divided-by-2 circuit to the phase detector A (PD_A) denoted as fb_div2. In addition, the DIE1_CLK signal is divided by 2 and sent to the PD_A denoted as clk_div2. The PD_A detects the phase relationship between the clk_div2 signal and fb_div2 signal, and it outputs dcdl_up signal and dcdl_down signal to the CTRL_A. The CTRL_A outputs the delay line control code (dcdl_code[10:0]) for adjusting the delay time of the DCDL_A and the DCDL_B.

2.2 The Locking Procedure

Fig. 2.2 shows the timing diagram of TSV delay variations compensation. In Fig. 2.2, dcva_to_pd signal leads dcvb_to_pd signal, and thus, the PD_B generates dcv_up signal to the CTRL_B to increase the delay time of the DCV_A. After two times polarity change of the PD_B from dcv_up to dcv_down or dcv_down to dcv_up, the dcv_lock signal is pulled high to stop tuning the control code of the DCV_A and the DCV_B. Then, the phase error between dcva_to_pd signal and dcvb_to_pd signal are eliminated which means the delay variation between TSV1 and TSV2 is compensated.

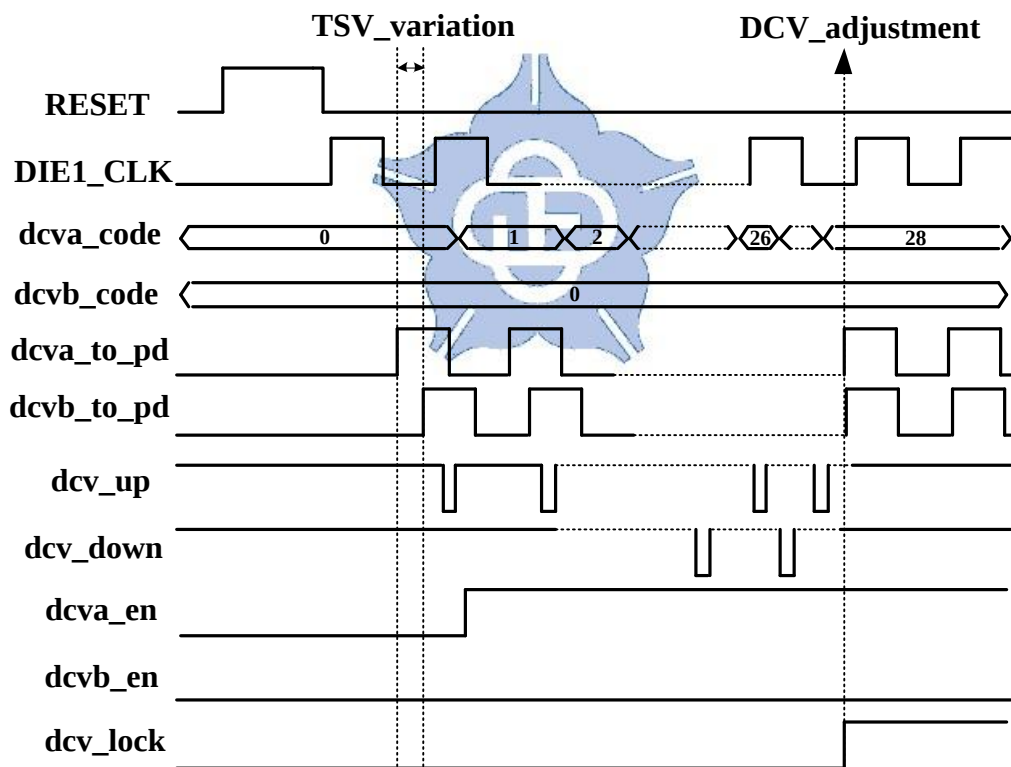


Figure 2.2 Timing diagram of TSV delay variation compensation

Fig. 2.3 shows the timing diagram of die-to-die clock synchronization. After clock_gate signal is pulled high, the CTRL_A starts to align the phase of clk_div2 signal and fb_div2 signal. Because the DCDL_A and DCDL_B are set to a minimum delay time in the beginning, the fb_div2 signal will lead to the clk_div2 signal. The CTRL_A will keep increasing the delay time of the DCDL_A and DCDL_B until the polarity of the PD_A changes from dcdl_down to dcdl_up. The lock condition of the ADDLL can be expressed as Eq. 2.1. Since the total delay in the upper delay path will be equal to the lower delay path, and thus, after the ADDLL is locked, the total delay time in the upper path will be equal to $N \cdot T_{DIE1_CLK}$ which means the phase error between the DIE1_CLK signal and DIE_2 signal is cancelled.

$$\begin{aligned}
 &T_{buf_A} + T_{DCDL_A} + T_{buf_B} + T_{TSV1} + T_{DCV_A} + T_{buf_E} + T_{buf_F} \quad \text{(Eq. 2.1)} \\
 &+ T_{DCV_B} + T_{TSV2} + T_{buf_D} + T_{DCDL_B} + T_{buf_C} = 2N * T_{DIE1_CLK} \\
 &2 * (T_{buf_A} + T_{DCDL_A} + T_{buf_B} + T_{TSV1} + T_{DCV_A} + T_{buf_E}) = 2N * T_{DIE1_CLK}
 \end{aligned}$$

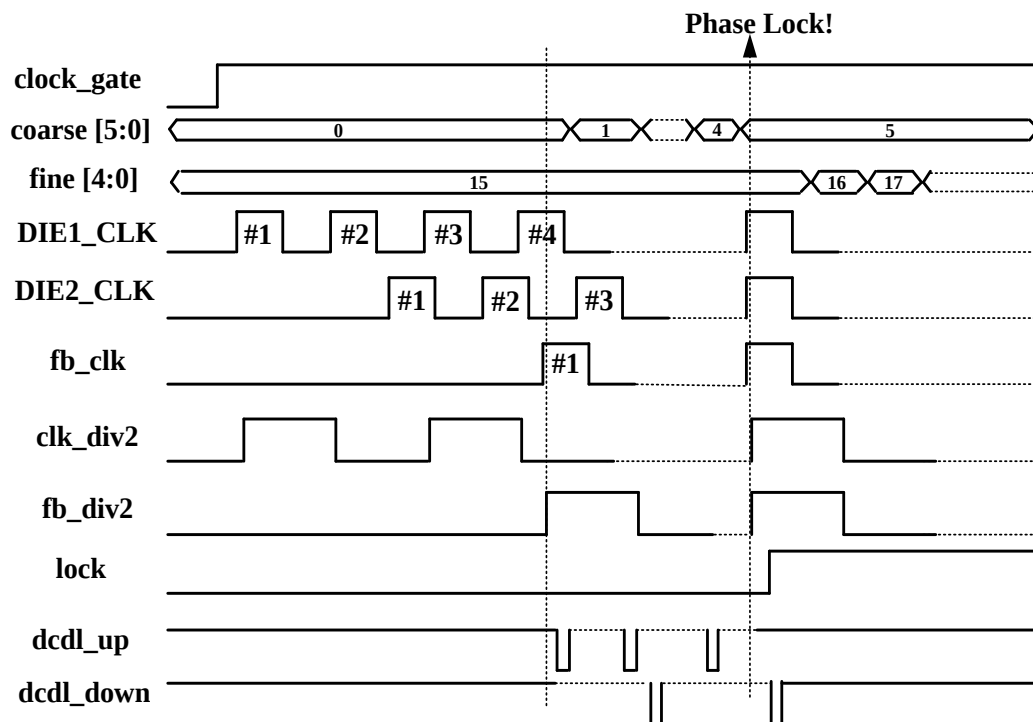
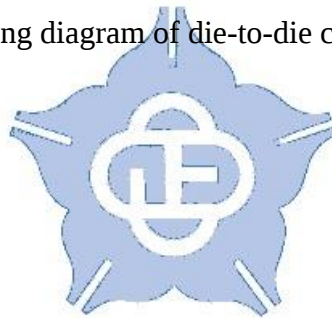


Figure 2.3 Timing diagram of die-to-die clock synchronization



2.3 Circuit Design and Implementation of ADDLL with two TSVs

2.3.1 Digitally Controlled Varactor (DCV)

Fig. 2.4 shows the proposed digital controlled varactor (DCV)-based delay line architecture. It is composed of a bypass inverter chain and a DCV delay line. There are 63 NAND gates used as digital controlled varactors to provide a fine resolution delay line. The DCV_A and DCV_B are used to compensate for the delay variations between two TSVs. The dcv_en signal is used to control the bypass inverter chain to provide a longer propagation delay time in best case PVT conditions. When the operation condition is at worst case PVT condition, the dcv_en is set to 0 to reduce the overall delay time of the DCV-based delay-line.

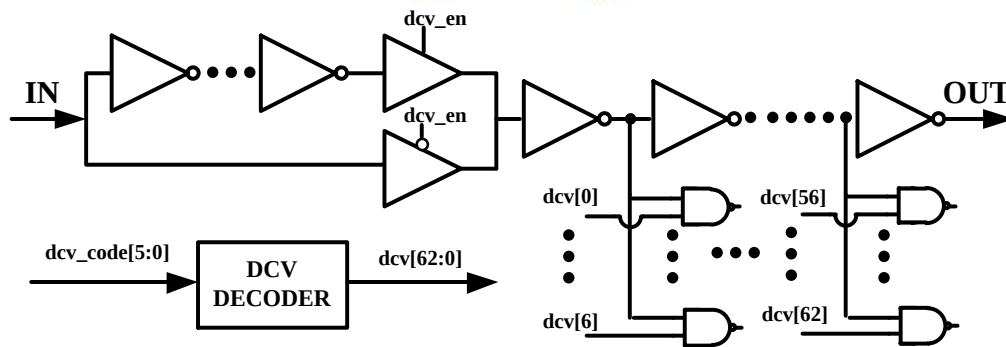


Figure 2.4 The proposed DCV-based delay line architecture

Table 2.1 shows the simulation delay time of the DCV-based delay line (DCV_A and DCV_B) with PVT variations. The worst resolution of the DCV-based delay line is 8.4ps for accurate compensation for the TSV delay variations.

Table 2.1 The Delay Time of DCV-Based Delay Line

	FF	TT	SS
Intrinsic Delay	496ps	676ps	1046ps
Maximum Delay	762ps	1024ps	1585ps



2.3.2 Phase and Frequency Detector (PFD)

In order to align the input clock and the feedback clock, we use a bang-bang phase and frequency detector (PFD). The short high pulses (QU and QD) are generated by the DFFs triggered by CLK_IN and CLK_FB. Subsequently, the NAND gates and digital pulse amplifier (DPA) can determine whether the CLK_IN is leading or lagging the CLK_FB. However, the pulse width of OUTU and OUTD is too narrow to trigger the DFFs of the digital controller. Therefore, we use a digital pulse amplifier to widen the pulse width of OUTU and OUTD. The digital pulse amplifier is composed of many series connected AND gates and a buffer, as shown in Fig. 2.5.

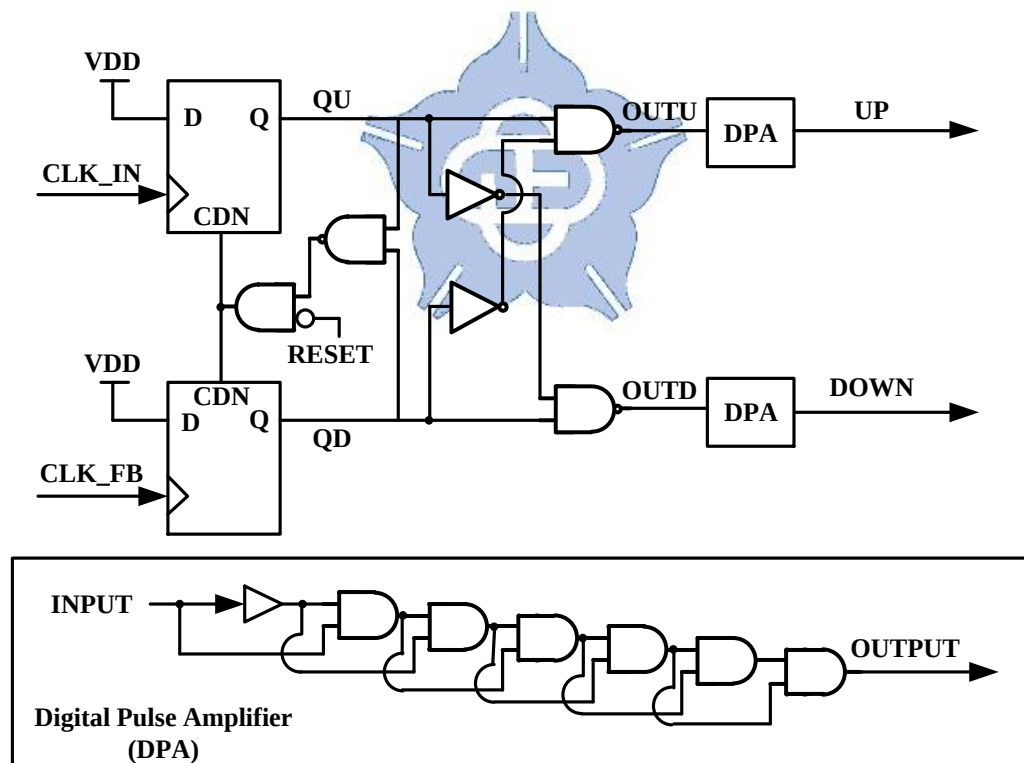


Figure 2.5 The Phase and Frequency Detector

The tiny dead-zone is the advantage of the proposed PFD, and thus, the phase error between CLK_IN and CLK_FB can be controlled in a small value. The dead-zone is whether the PFD can determine the phase error.

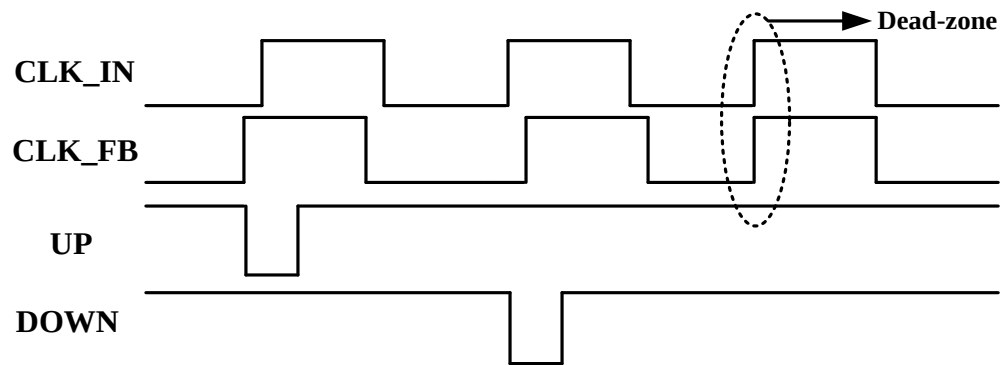


Figure 2.6 The timing diagram of PFD

Table 2.2 shows the dead-zone of the proposed PFD with PVT variations. It shows that the proposed PFD can correctly operate at 1.0V in three different process corners.

Table 2.2 The dead-zone of the proposed PFD

	Dead-Zone (ps)
PVT	1.0V
FF	13
TT	18
SS	29

2.3.3 Digital Controlled Delay Line (DCDL)

Fig. 2.7 shows the digital controlled delay line (DCDL), and it is composed of 63 lattice delay units (LDU), a fine-tuning delay line (FDL), and a delay line decoder. The resolution of a coarse-tuning is two NAND gates, and the dummy NAND gates are used to balance the capacitance loading of every NAND gates. The 11-bit control code can be encoded as 63-bit coarse-tuning code and 31-bit fine-tuning code to control CDL and FDL.

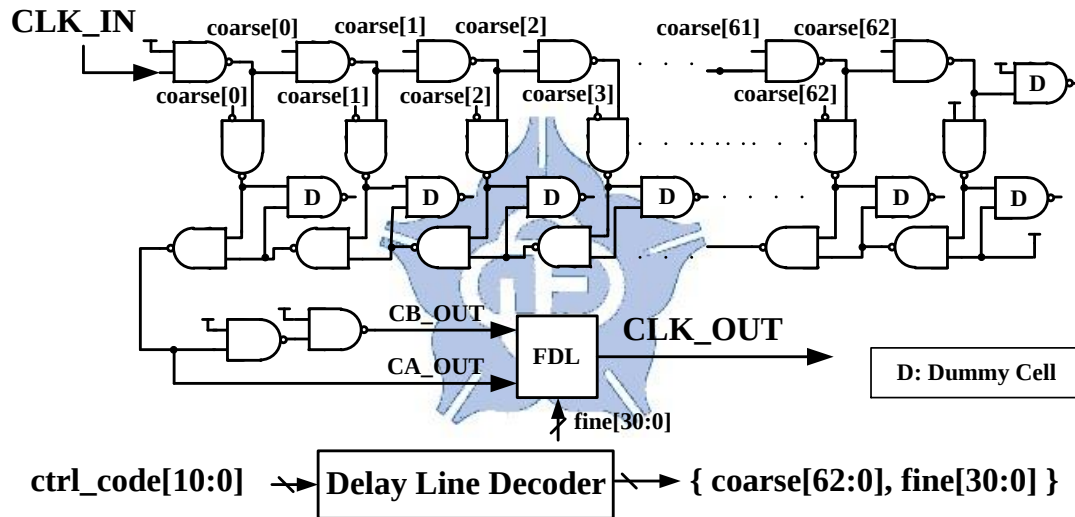


Figure 2.7 The digital controlled delay line

Table 2.3 illustrates the properties of the proposed DCDL with process variations. The proposed DCDL can provide an enough delay time to finish the locking procedure of ADDLL. With a two-stage delay tuning architecture, the proposed DCDL can provide a wide coarse-tuning delay time and has a high resolution fine-tuning resolution.

Table 2.3 The properties of The Proposed DCDL

	1.0V		
PVT	Max Delay (ps)	Intrinsic Delay (ps)	Resolution (ps)
FF	3324	248	48
TT	4227	315	62
SS	5863	433	86



2.3.4 FDL

Traditional fine-tuning delay line (FDL) in a two-stage coarse-fine delay line architecture should overlap fine-tuning range by more than one coarse-tuning resolution about 20% to 30% with PVT variations. This requirement not only increases the chip area but also results in a large cycle-to-cycle jitter when the coarse-tuning control code is switching. Therefore, we use an interpolator architecture to guarantee that the delay controllable range of the FDL can overlap one coarse-tuning resolution with PVT variations.

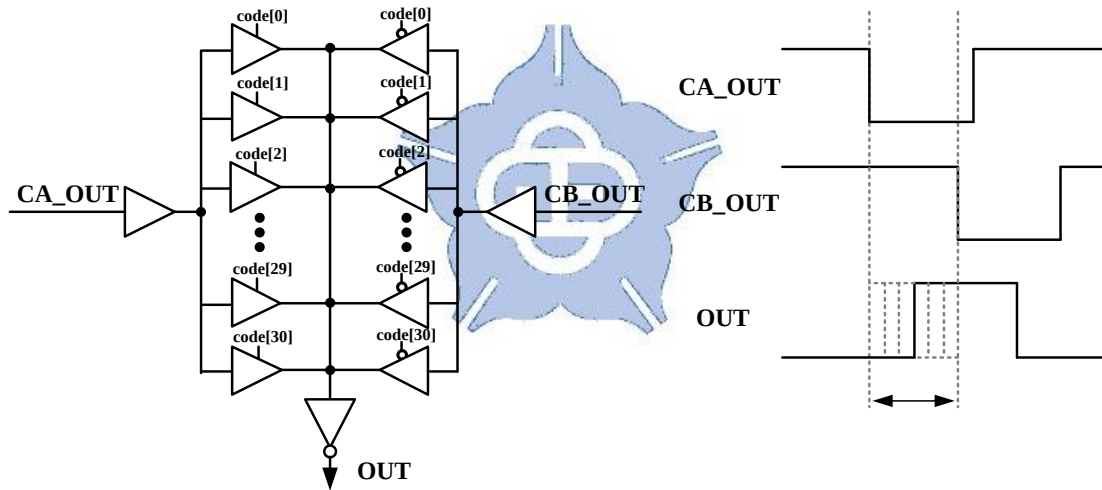


Figure 2.8 The FDL

Fig. 2.8 shows the proposed FDL architecture, and it is composed of two parallel connected tri-state buffer arrays, two buffers, and an inverter. The delay time difference between CA_OUT and CB_OUT is one coarse-tuning resolution, as shown in Fig. 2.7. The control code (code[30:0]) can control the driving strength of the tri-state buffers. When the fine-tuning code is fully opened (31'h7FFF_FFFF), the rising edge of OUT will phase align with the falling edge of CA_OUT. Oppositely,

when the fine-tuning code is fully closed (31'h0000_0000), the rising edge of OUT will phase align with the falling edge of CB_OUT. The FDL can divide one coarse-tuning resolution into 31 parts to achieve fine-tuning resolution, and it also provides a total delay controllable range equal to one coarse-tuning resolution.

Table 2.4 Properties of The Proposed FDL

	1.0V	
PVT	Intrinsic Delay (ps)	Resolution
FF	114.3	1.49
TT	149.9	1.92
SS	209.4	2.57



2.4 Experimental Results

2.4.1 Specifications of the ADDLL with two TSVs

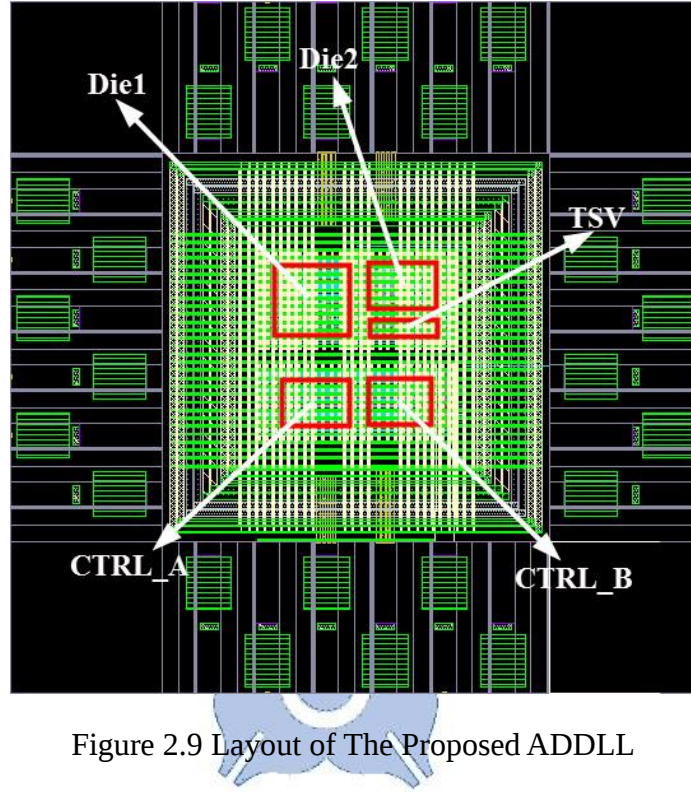


Figure 2.9 Layout of The Proposed ADDLL

The proposed ADDLL is implemented in a standard performance 90nm 1P9M CMOS process with a 1.0V power supply. Fig. 2.9 shows the layout of the test chip, and the active area of the test chip is 300 μm * 300 μm . The area of the proposed ADDLL per die is 0.045 μm , and two delay lines are added in the test chip for simulation of the TSV delay.

2.4.2 Simulation Results of the ADDLL with two TSVs

Fig. 2.10 shows the simulation waveform of the proposed ADDLL with an 1GHz input clock. After the ADDLL is reset, the path_control signal is set to zero, and DCDL_A, DCDL_B, DCV_A, and DCV_B are set to provide a minimum delay time. The CTRL_B adjusts the DCV_A and DCV_B according to the PD_B's output to increase the delay time of the DCV_A or DCV_B until the phase error between dcva_to_pd signal and dcvb_to_pd is eliminated which means the delay variations between TSV1 and TSV2 is compensated.

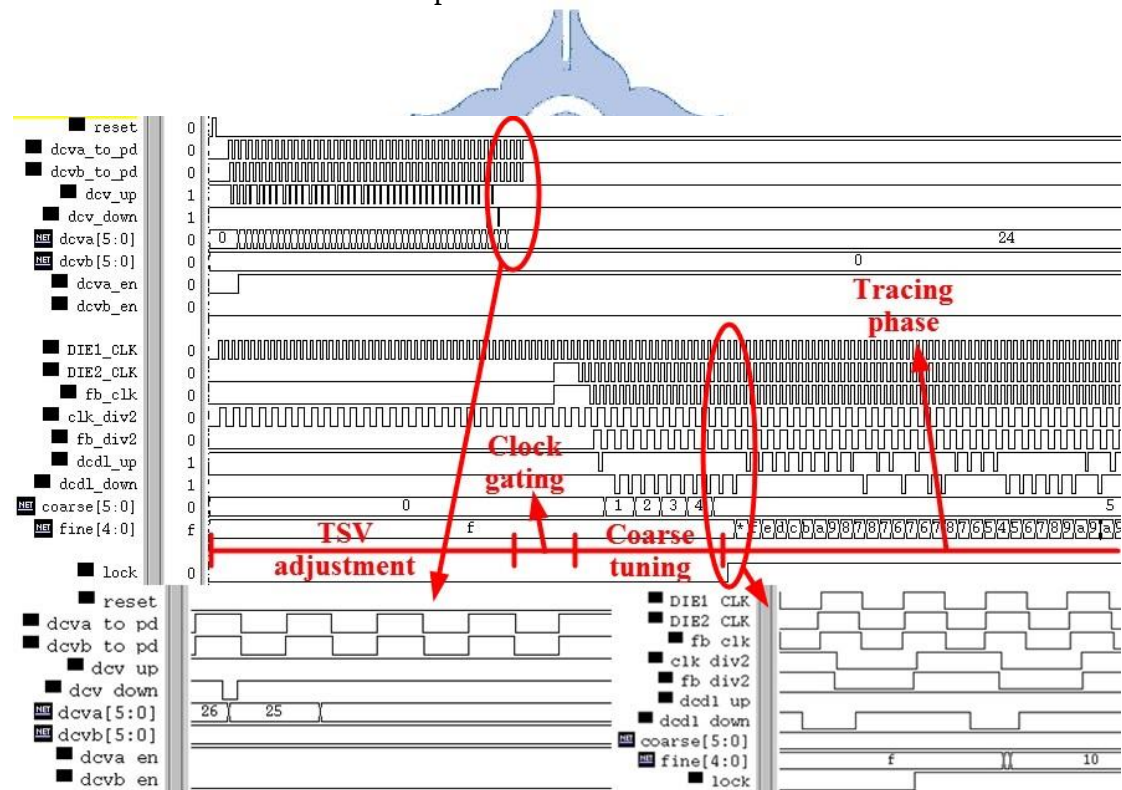


Figure 2.10 Simulation waveform of the proposed ADDLL

After TSV delay variations are compensated, the DCV-based delay line control code (dcva[5:0] and dcvb[5:0]) is fixed. Then, path_control signal is pulled high, and the CTRL_A adjusts the DCDL_A and DCDL_B according to the PD_A's output to reduce the phase error between clk_div2 signal and fb_div2 signal. After the ADDLL is locked, the phase error between clk_div2 signal and fb_div2 signal is eliminated, and the phase error between the DIE1_CLK signal and DIE2_CLK signal is also cancelled, as explained in Section 2.2. In Fig. 2.10, the delay variations between TSV1 and TSV2 is 176.4ps, after the proposed ADDLL is locked, the phase error between DIE1_CLK signal and DIE2_CLK signal is reduced to 21.9ps.



2.4.3 Comparison Table

Table 2.5 Performance Comparisons

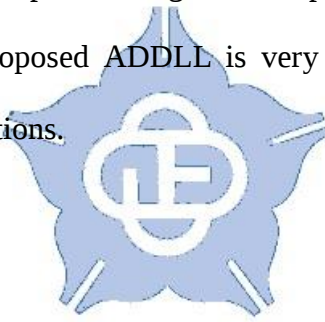
	Proposed	JSSC'13 [30]	TCAS-I'13 [31]	ISCAS'12 [32]
Type	All-Digital	All-Digital	All-Digital	Analog
Process	90nm	130nm	90nm	0.18 μ m
Supply Voltage	1.0V	1.2V	1.0V	1.8V
Frequency	300MHz ~ 1 GHz	200MHz ~ 1.6GHz	50 MHz ~ 600 MHz	556 MHz ~ 1.5 GHz
Phase Error	< 21.9ps	<50ps*	< 15.8ps	< 2ps
Area per Die (mm ²)	0.045	0.06	0.0044	N/A
Power	3.27mW @1GHz	0.9mW @1.6GHz	1.8mW @600MHz	56mW @1.5GHz

*if replica delay matched perfectly

Table 2.5 shows the performance comparisons with the state-of-the-arts. In the DBDA [30], they needs to replicate the delay of the inter-die TSV wire delay, Therefore, the unexpected TSV delay variations can greatly increase the phase error of clock signals in multiple layers of a 3D-IC after the DLL is locked. In the dual-locking DLL [31], after the DLL is locked, the dual-locking DLL needs to continuously fine-tunes the two DLLs in an interleaved manner to keep maintaining the phase alignment. However, the regularly switching the direction of the forward path and the feedback path and performing fine-tuning in two DLLs may cause a relatively large error during phase maintaining mode. The dual-delay-locked loop (D-DLL) [32] does not need to switch the direction of the forward path and the feedback path since a bidirectional buffer is applied. However, two DLLs are working

at the same time which increases the design complexity to maintain the stability of the D-DLL. The relative high power consumption is also the disadvantage of the analog charge-pump-based D-DLL.

An all-digital delay locked loop (ADDLL) for 3D-IC die-to-die synchronization with two TSVs is presented. The delay variations of TSVs will be compensated before the ADDLL's normal operation. As compared with current DLLs for 3D-IC clock deskew applications, the proposed ADDLL does not need to switch the path during phase maintaining mode. The proposed ADDLL can operate with a 300MHz to 1GHz input clock, and the maximum phase error is smaller than 21.9ps. In addition, the lock-in time is 79 cycles at 1GHz. Furthermore, the proposed ADDLL is implemented with standard cells, and the proposed design can be ported to different process in a short time. Therefore, the proposed ADDLL is very suitable for 3D-IC die-to-die clock synchronization applications.



Chapter 3 3-D ICs clock

synchronization with a single TSV

3.1 Architecture Overview

Fig. 3.1 shows the proposed ADDLL for die-to-die clock synchronization in 3D-ICs. The ADDLL is composed of a digital controlled delay line (DCDL), a pulse generator (PG), a time-to-digital convertor (TDC) embedded controlled delay line (CDL), a phase detector (PD), two delay circuits (DELAY), two ADDLL controllers (DIE1_CTL and DIE2_CTL), a OR-logic gate, and six tri-state buffers.

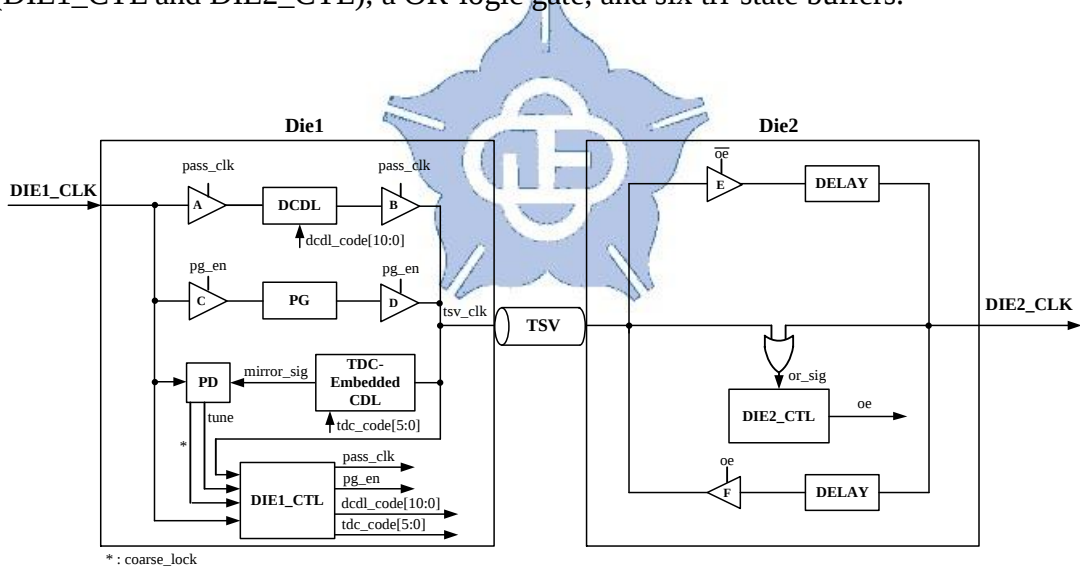


Figure 3.1 The proposed ADDLL architecture with a single TSV

The DIE1_CLK is the reference clock of Die1, and it will be transmitted to Die2 as reference clock of Die2. The goal of the proposed ADDLL is to phase align the clock signals between DIE1_CLK and DIE2_CLK. There are two steps in the proposed ADDLL to achieve die-to-die clock synchronization. **First**, when the ADDLL is reset, the pg_en signal is set to high, and the pass_clk signal is set to low.

The oe signal of Die2 is set to low. The DIE1_CLK inputs to the PG, and the PG generates a single-shot pulse signal. After a pulse is generated, the pg_en signal is set to low. The pulse will be transmitted to Die2 through the TSV channel, and it will circulate in Die2 from the upper delay circuit (tri-state buffer E + DELAY) to the bottom delay circuit (DELAY + tri-state buffer F), and then transmits back to Die1. At this moment, the TDC-Embedded CDL will start to calculate the time difference between the first pulse generated by Die1. Then, the delay time of TDC-Embedded CDL is set to half of the time difference (between two pulses) to mirror the delay time of the TSV channel. After the first step is finished, the oe signal is set to low forever.

Second, the ADDLL locking procedure starts to begin. The pass_clk signal is set to high, and the DIE1_CLK can be input to TDC-Embedded CDL through the TSV channel to Die2. The delayed signal mirror_sig is generated by TDC-Embedded CDL for mirroring the TSV channel delay. The DIE1_CTL starts to increase the delay time of the DCDL until the mirror_sig and DIE1_CLK are phase aligned. The DIE1_CLK can transmit to the Die2 and denoted as DIE2_CLK. When the DIE1_CLK and mirror_sig are phase aligned, the DIE1_CLK and DIE2_CLK are also phase aligned. Because the total delay time of the TSV, tri-state buffer, and DELAY is mirrored by the TDC-Embedded CDL circuit in the first step, the mirror_sig and DIE2_CLK are also phase aligned. Finally, when the ADDLL is locked, the DIE1_CTL starts to fine-tune the delay time of the DCDL to maintain the phase alignment between DIE1_CLK and mirror_sig in the maintain mode.

3.2 The Locking Procedure

Fig. 3.2 shows the locking procedure of the proposed ADDLL. **First**, when the ADDLL is reset, the DIE1_CLK inputs to the PG. The PG is controlled by the pg_en signal. The pg_en is set to high by the first negative edge of DIE1_CLK, and is set to low by the second negative edge of DIE1_CLK. That means, the pulse signal is generated by PG circuit between the first and second negative edge of DIE1_CLK. The pulse transmits from TSV to Die2. When the pulse is transmitted to Die2, the or_sig is generated by the OR-logic gate. Later, the pulse will pass to DIE2_CLK, and the second or_sig pulse is generated. At this moment, the oe is set to high to let the pulse back to Die1. When the pulse transmits back to Die1, the oe signal is set to low. After the pulse transmits from Die2 to Die1, the tdc_code[5:0] is setting to half of the delay of the pulse circulating time.

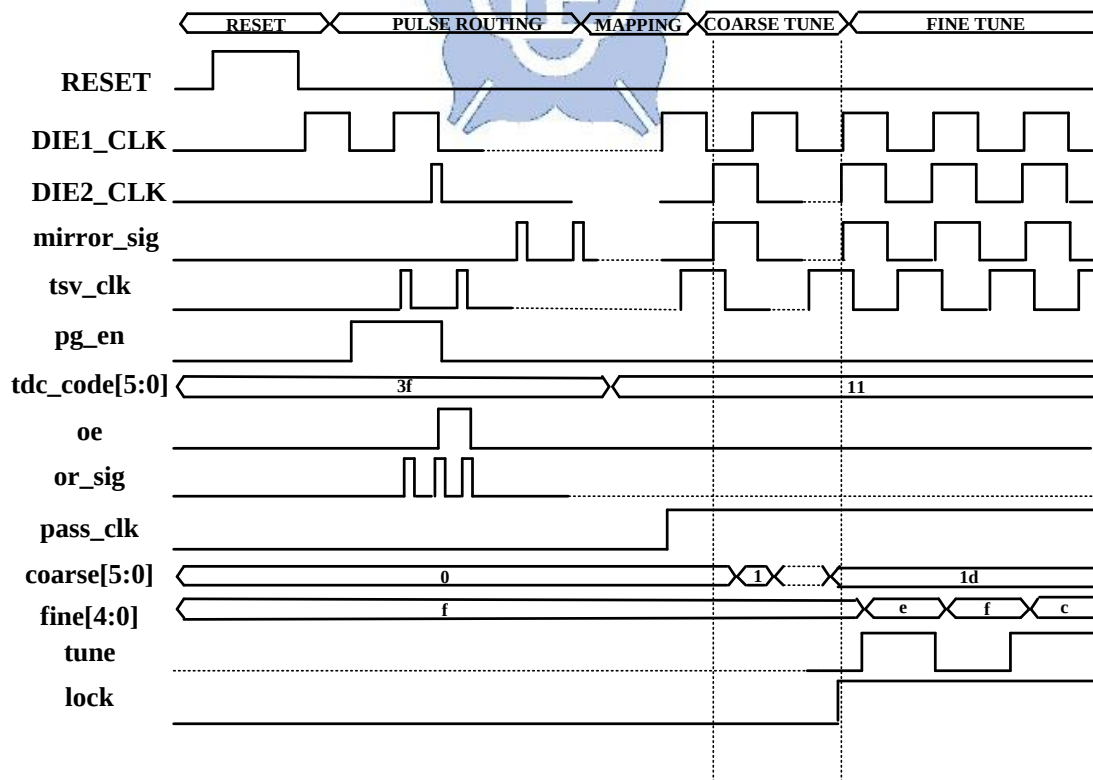


Figure 3.2 The timing diagram of locking procedure

Second, the `pass_clk` is set to high after the TSV delay time is mirrored by setting `tdc_code[5:0]`. When the `mirror_sig` is received by PD, the `DIE1_CTL` starts to increase the value of `coarse[5:0]` until the lock signal is set to high. That means, the rising edge of `mirror_sig` is arriving at the locking window of the PD. Because the total delay time of the unidirectional path is mirrored by the TDC-Embedded CDL, the `mirror_sig` and `DIE2_CLK` are phase aligned. The lock signal is set to high when the phase between `mirror_sig` and `DIE1_CLK` is aligned. To sum up, when the `mirror_sig` and `DIE1_CLK` are phase aligned, the phase between `DIE1_CLK` and `DIE2_CLK` is zero. Finally, the `DIE1_CTL` keeps fine-tuning the value of `fine[4:0]` to maintain the phase alignment between `DIE1_CLK` and `mirror_sig`.



3.3 Circuit Design and Implementation of ADDLL with a single TSV

3.3.1 Pulse Generator (PG)

In order to mirror the TSV delay time to the TDC-Embedded CDL, we should generate a pulse signal with an enough pulse width. Fig. 3.3 shows the proposed PG, and it is composed of two tri-state buffers, six buffers, and an inverter. The two tri-state buffers are used to avoid generating the second pulse signal, because we only need an one single-shot pulse.

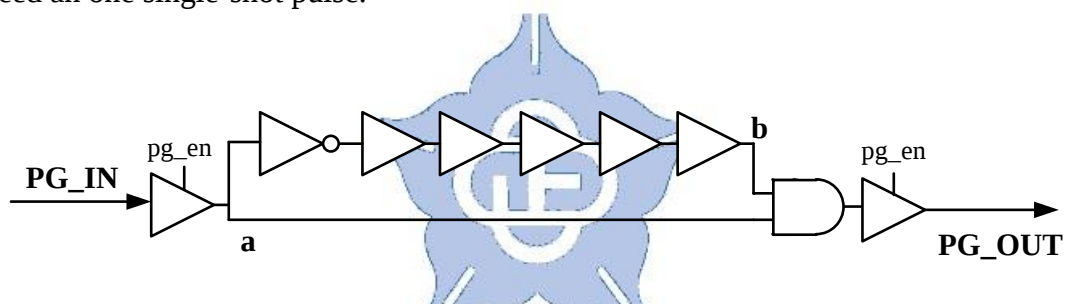


Figure 3.3 The Pulse Generator (PG)

Fig. 3.4 shows the timing diagram of the proposed PG. First, we set the pg_en signal to high, and the clock signal can input to the PG. The “a” signal is delayed after a tri-state buffer, and the “b” signal is delayed by a delay chain (one inverter and six buffers). At this moment, the AND-logic gate generates the pulse signal between “a” signal and “b” signal.

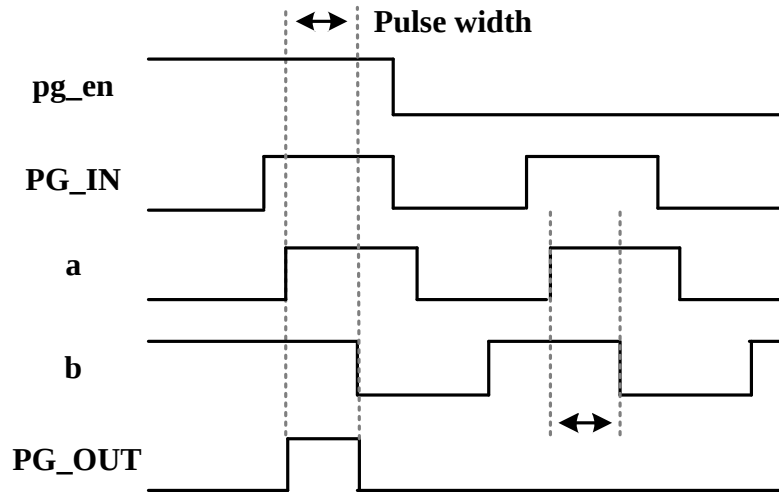


Figure 3.4 The timing diagram of PG

Table 3.1 illustrates the pulse width of the generated pulse by the proposed PG with process variations. The pulse width can't be too narrow, because it may be disappeared during the pulse routing path. Table 3.1 shows that the pulse is generated with PVT variations, and the pulse width is always larger than 200ps. Besides, when the **pg_en** is low, the PG circuit will not generate any pulse signal.

Table 3.1 Pulse width of The generated pulse

	1.0V
PVT	Pulse Width (ps)
FF	202.2
TT	248.1
SS	321.4

3.3.2 TDC-Embedded CDL

The proposed TDC-Embedded CDL is composed of 63 lattice delay units (LDUs), 64 DFFs (time-to-digital converter units), a TDC encoder, and a TDC decoder, as shown in Fig. 3.5. First, the delay time of the TDC-Embedded CDL is set to maximum value. That means, signal can transmit from all upper path to all bottom path. The first pulse generated by PG can propagate through the whole delay path. When the second pulse from the Die2 loops back to the TDC-Embedded CDL, the DFFs will be triggered to record the time difference between pulses. Then, the TDC encoder encodes the sampled value into $tdc_code[5:0]$. Finally, the TDC decoder decodes $tdc_code[5:0]$ as $code[62:0]$ which sets the delay time of the delay path to half of the timing difference between pulses.

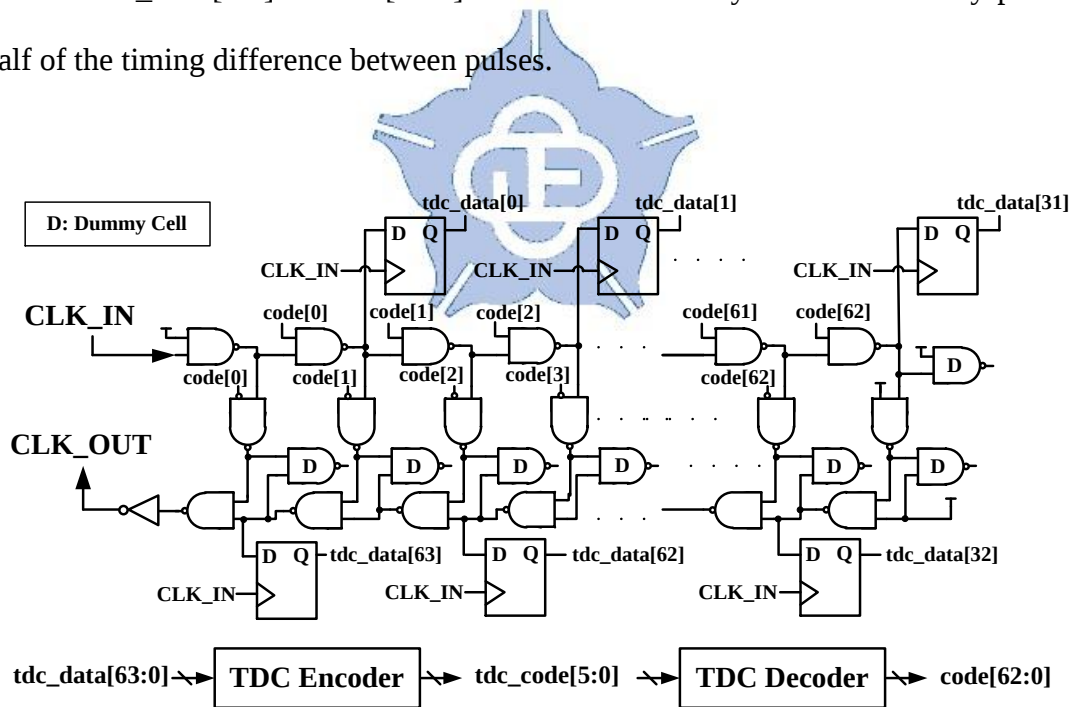


Figure 3.5 The TDC-Embedded CDL

3.3.3 Phase Detector (PD)

The phase detector is composed of three buffers, three DFFs, one XOR-logic gate, and one AND-logic gate, as shown in Fig. 3.6. The lock signal is high, when the positive edge of CLK_FB falls into the locking window, as shown in Fig. 3.7. The “tune” signal is for the controller to fine-tuning the DCDL.

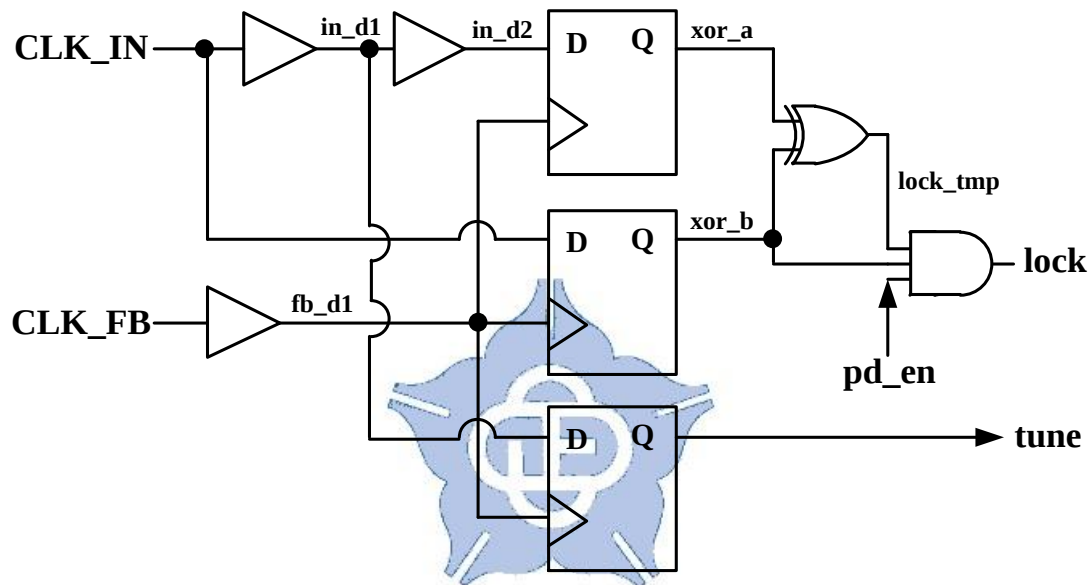


Figure 3.6 The Phase Detector

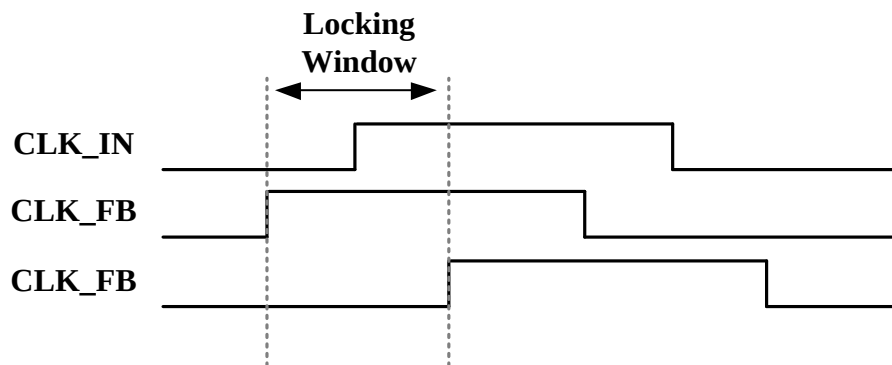


Figure 3.7 The concept of locking window

In order to avoid the ADDLL locking to the negative edge of CLK_IN, the xor_b is an important signal. As shown in Fig. 3.8, when two rising edges of CLK_IN and CLK_FB are aligned, the lock_tmp signal is set to high. At this moment, if the xor_b signal is low, the rising edge of CLK_FB locks to the falling edge of CLK_IN. Therefore, the lock signal is decided by lock_tmp, xor_b, and pd_en. Besides, when the tune signal is low, the ADDLL controller increases the delay time of CLK_FB. In contrast, when the tune signal is high, the ADDLL controller decreases the delay time of CLK_FB.

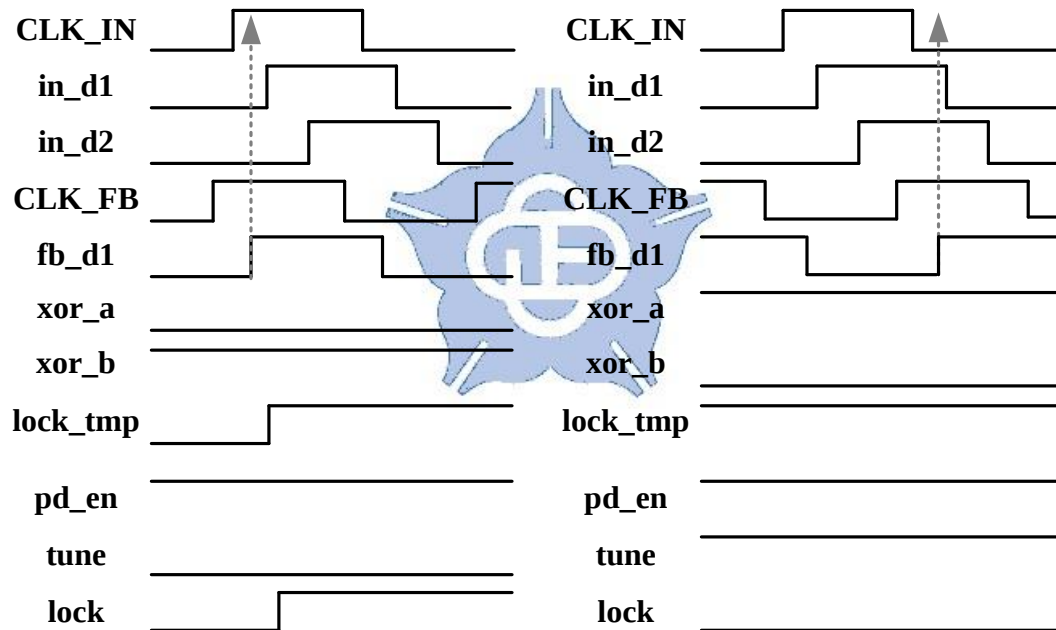


Figure 3.8 The timing diagram of PD

3.4 Experimental Results

3.4.1 Test Circuit Implementation

In order to solve the clock rate restriction on I/O pads, we propose a test circuit to provide ADDLL circuit a high-speed on-chip clock. The test circuit divides the frequency of clock signals in die1 and die2. Therefore, the internal clock signals can be observed. The test circuit also provides the working state of the ADDLL making the debug process easier.

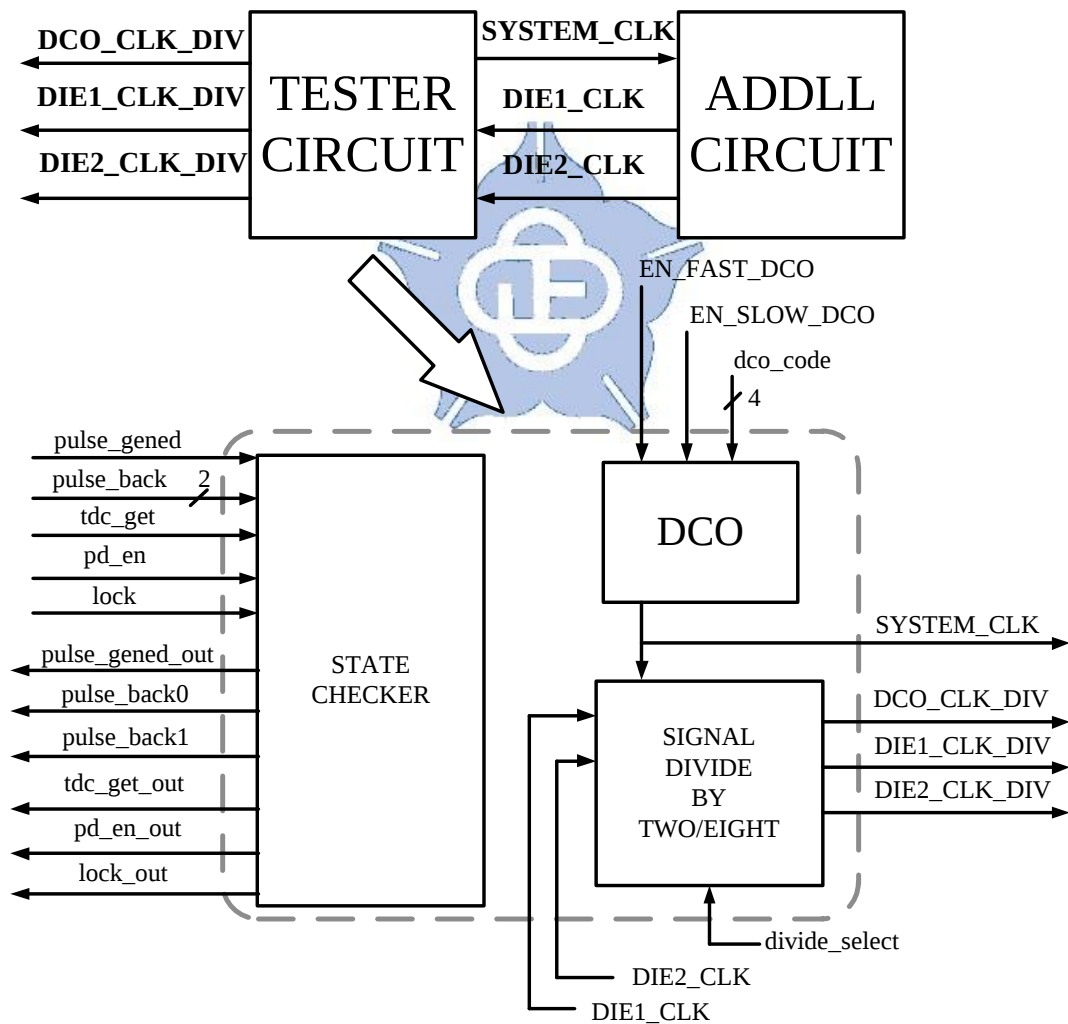


Figure 3.9 The test circuit

The tester circuit is composed of a state checker, a digital controlled oscillator (DCO), and a divide circuit, as shown in Fig. 3.9. The DCO provides a 150MHz to 1GHz clock signal for the ADDLL. When the ADDLL is locked, the high-speed clocks cannot pass through the I/O pads due to the I/O pad speed limitations. The signal divide circuit can divide the frequency of the clock signals by two or eight, and let the divided clock signals can pass through the low-speed I/O pads.



3.4.1.1 DCO

The DCO is composed of a MUX-typed slow DCO, a fast DCO, and a DCO decoder, as shown in Fig. 3.10. The MUX-typed slow DCO is composed of a NAND-logic gate to enable the slow DCO, and 15 delay units (a MUX and a delay buffer) to provide with different frequency ranges. The fast DCO is composed of a NAND-logic gate, a delay buffer chain, and three tri-state buffers. The DCO decoder can encode the `dco_code[3:0]` into `SLOW[14:0]` and `FAST[2:0]` for controlling the DCO frequency range. Besides, the signals of `EN_FAST_DCO` and `EN_SLOW_DCO` are used to enable and disable the fast DCO and slow DCO, respectively.

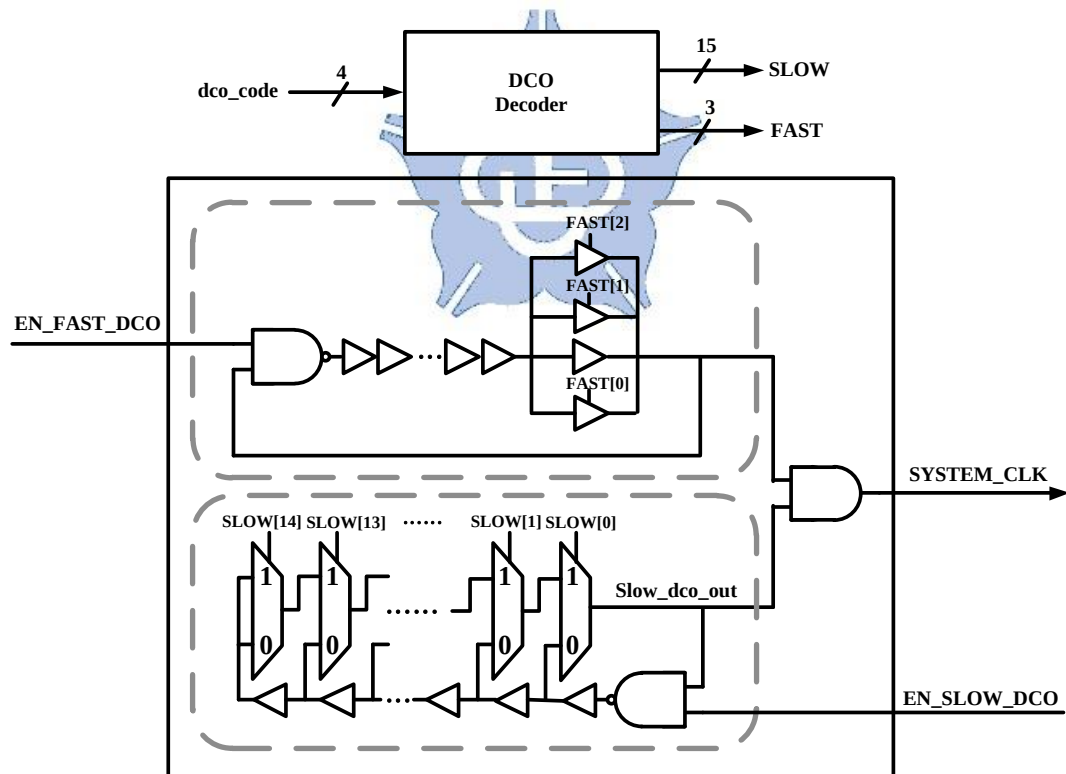


Figure 3.10 The DCO

Table 3.2 lists the frequency range of the slow DCO. It shows that the slow DCO can provide ADDLL with a 150MHz to 770MHz clock.

Table 3.2 The output frequency range of the slow DCO

dco_code[3:0]	Output Frequency @1.0V (MHz)
4'b 0000 (4'd0)	771
4'b 0001 (4'd1)	603
4'b 0010 (4'd2)	496
4'b 0011 (4'd3)	421
4'b 0100 (4'd4)	365
4'b 0101 (4'd5)	323
4'b 0110 (4'd6)	289
4'b 0111 (4'd7)	262
4'b 1000 (4'd8)	239
4'b 1001 (4'd9)	220
4'b 1010 (4'd10)	204
4'b 1011 (4'd11)	190
4'b 1100 (4'd12)	178
4'b 1101 (4'd13)	167
4'b 1110 (4'd14)	157
4'b 1111 (4'd15)	149

Table 3.3 lists the frequency range of the fast DCO. It shows that the fast DCO can provide ADDLL with a 982MHz to 1011MHz clock.

Table 3.3 The output frequency range of the fast DCO

dco_code[1:0]	Output Frequency @1.0V (MHz)
2'b 00 (2'd0)	982
2'b 01 (2'd1)	1001
2'b 10 (2'd2)	1007
2'b 11 (2'd3)	1011



3.4.1.2 Divider

The divider circuit is composed of two type dividers, as shown in Fig. 3.11. One is composed of three DFFs, a MUX, and an inverter. The other is only composed of three DFFs. The difference between two dividers is that the SYSTEM_CLK signal is only divided by eight, but the clock signals of die1 and die2 are divided by two or eight controlled by the divide_select signal. Besides, when the lock signal is high, the divider starts to divide the clock signals.

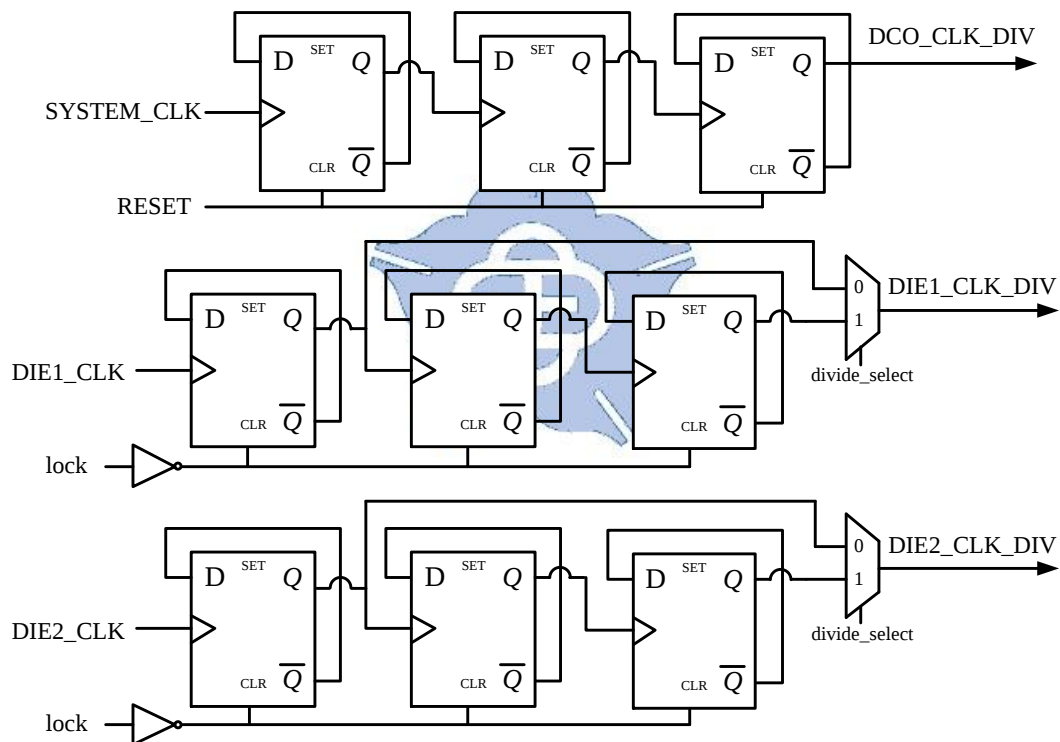


Figure 3.11 The Divider

3.4.2 Specifications

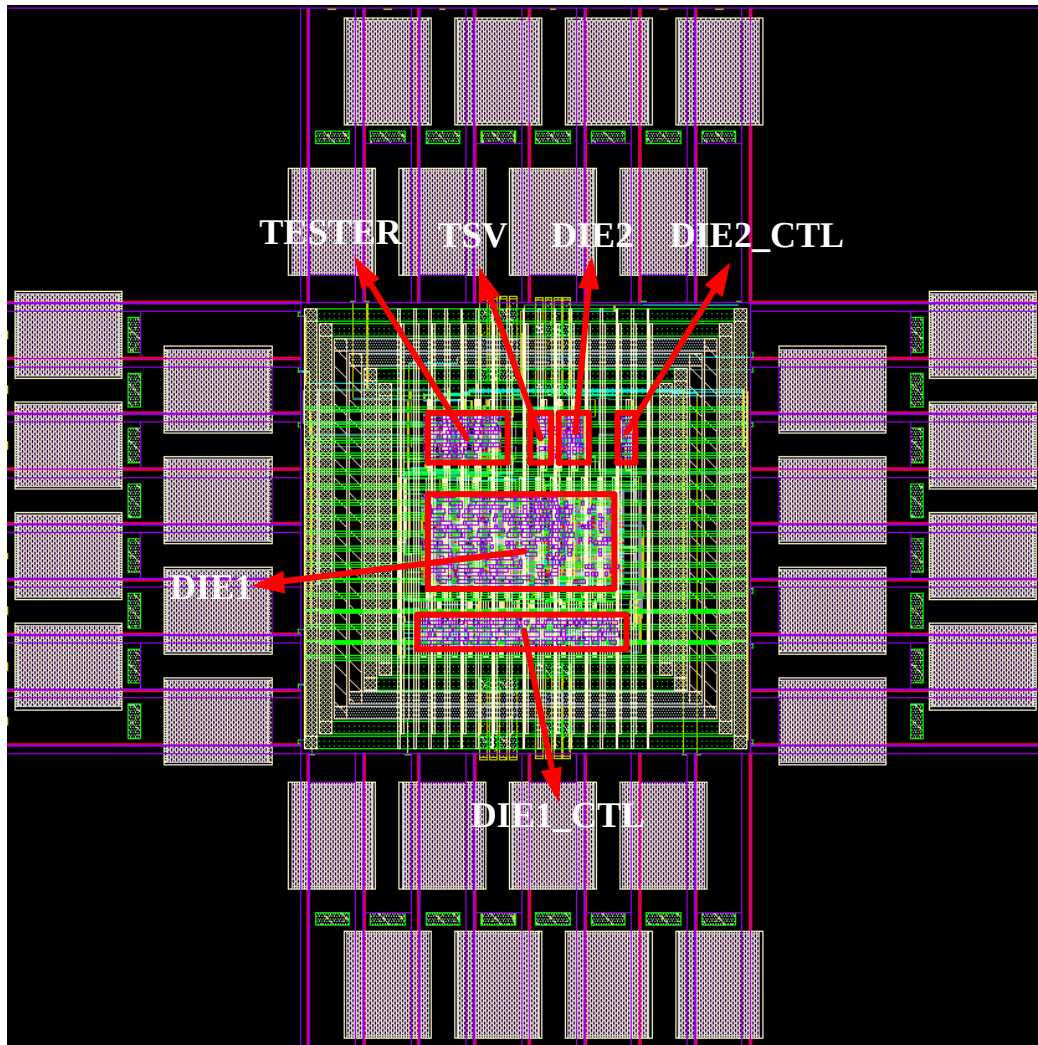


Figure 3.12 The layout of the ADDLL with a single TSV

The test chip is fabricated in TSMC 90nm standard performance CMOS process. Fig. 3.12 shows the layout of the proposed ADDLL for 3-D ICs clock synchronization with a single TSV. The core area occupies $170 * 170 \mu\text{m}^2$ and the chip area including I/O pads occupies $670 * 670 \mu\text{m}^2$. The chip is composed of an ADDLL and a tester circuit. The tester circuit can generate a on-chip high-speed clock, and divided the clock signals in die1 and die2.

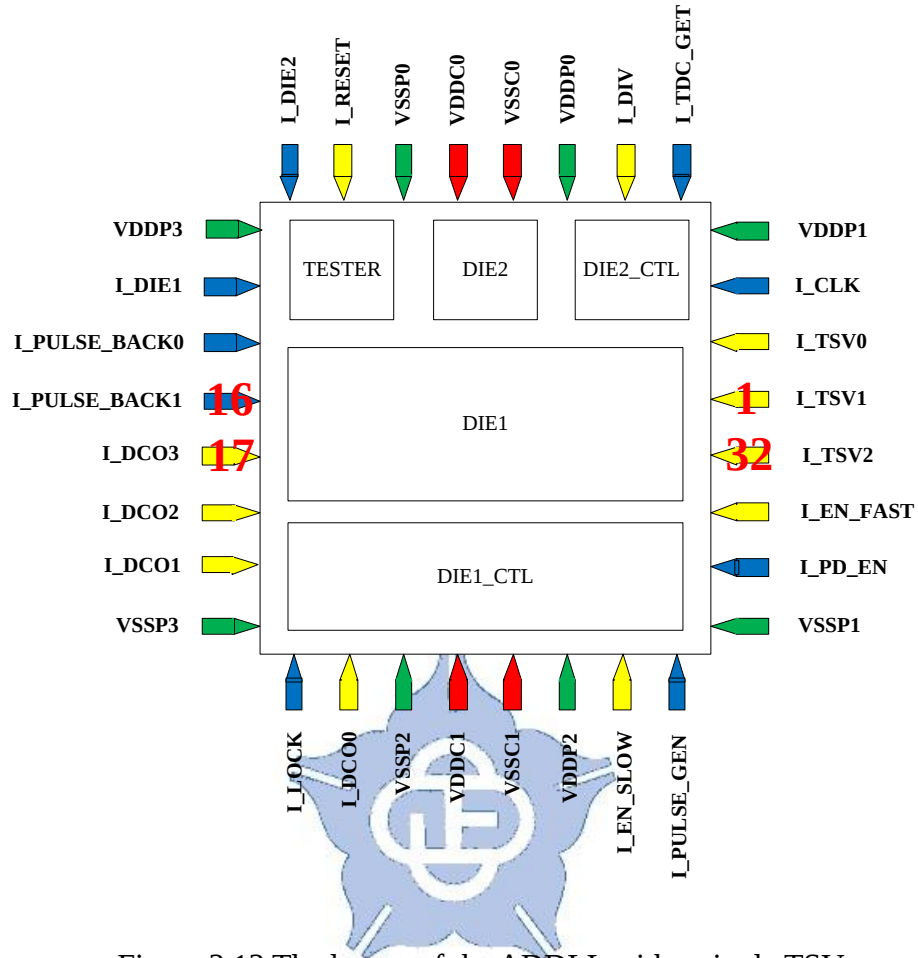


Figure 3.13 The layout of the ADDLL with a single TSV

Fig. 3.13 shows the chip I/O and the floorplanning of the ADDLL with a single TSV. The ADDLL with a single TSV has 9 output pins, 11 input pins, and 12 power pins. Table 3.4 illustrates the detail I/O pads information.

We use the I_CLK to observe the system clock frequency to ensure the proposed DCO works normally. The I_DIE1 and I_DIE2 are generated to observe the phase error when the ADDLL is locked.

Table 3.4 I/O pins information of ADDLL with a single TSV

Pin Number	Pin Name	Input/ Output	Information
1	I_TSV1	Input	TSV Delay Control Code
2	I_TSV0	Input	TSV Delay Control Code
3	I_CLK	Output	DCO CLK Divided By 8
4	VDDP1	Input	Pad Power
5	I_TDC_GET	Output	TDC Mapping Finish
6	I_DIV	Input	DIE1_CLK & DIE2_CLK Divided By 2 or 8
7	VDDP0	Input	Pad Power
8	VSSC0	Input	Core Power
9	VDDC0	Input	Core Power
10	VSSP0	Input	Pad Power
11	I_RESET	Input	ADDLL RESET
12	I_DIE2	Output	DIE2_CLK
13	VDDP3	Input	Pad Power
14	I_DIE1	Output	DIE1_CLK
15	I_PULSE_BACK0	Output	PG Pulse Out (First)
16	I_PULSE_BACK1	Output	PG Pulse Back (Second)
17	I_DCO3	Input	DCO Control Code
18	I_DCO2	Input	DCO Control Code
19	I_DCO1	Input	DCO Control Code
20	VSSP3	Input	Pad Power
21	I_LOCK	Output	ADDLL LOCK
22	I_DCO0	Input	DCO Control Code
23	VSSP2	Input	Pad Power
24	VDDC1	Input	Core Power
25	VSSC1	Input	Core Power
26	VDDP2	Input	Pad Power
27	I_EN_SLOW	Input	Enable Slow DCO
28	I_PULSE_GEN	Output	Pulse Generated By PG
29	VSSP1	Input	Pad Power
30	I_PD_EN	Output	Locking Procedure Start
31	I_EN_FAST	Input	Enable Fast DCO
32	I_TSV2	Input	TSV Delay Control Code

3.4.3 Simulation Results

Fig. 3.14 shows the post-layout simulation of ADDLL with a single TSV, and the operation frequency is 1GHz. The proposed ADDLL with a single TSV can operate with PVT variations. The operation frequency of proposed ADDLL with a single TSV ranges from 200MHz to 1GHz. First, as we mentioned in section 3.2, the PG generates a pulse signal to transmit from die1 to die2, and the TDC_Embedded CDL mirrors the delay time of the TSV channel. At this moment, the mirror_sig and DIE2_CLK are phase aligned. Second, the controller starts to increase the coarse code of DCDL until the lock signal of PD is high. Finally, the controller updates the fine-tuning code of the DCDL to maintain the phase alignment between DIE1_CLK and DIE2_CLK.

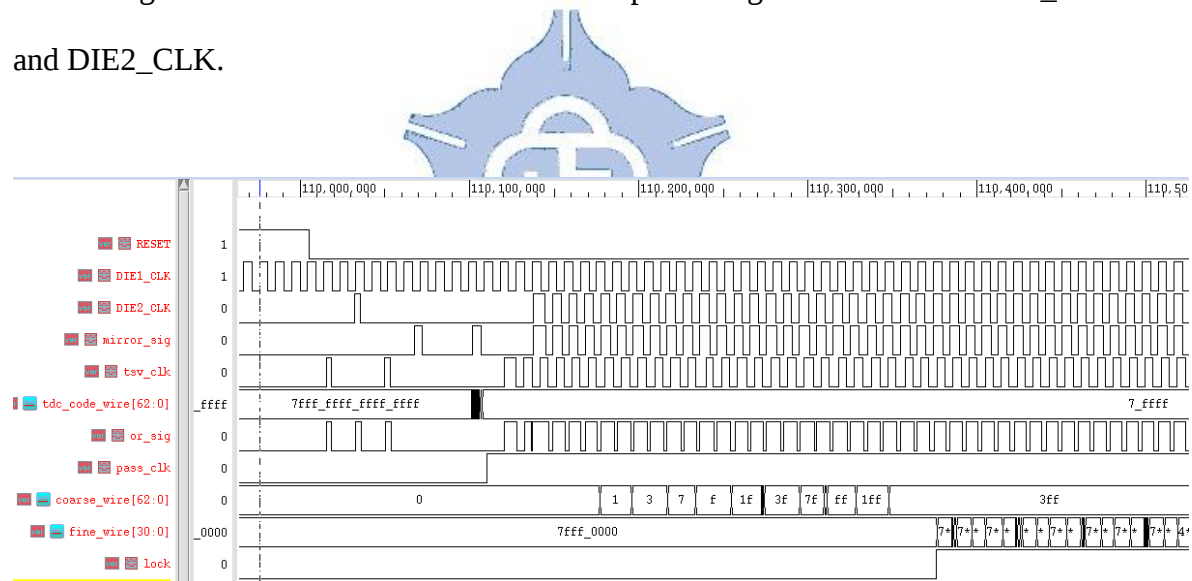


Figure 3.14 The post-layout simulation of ADDLL with a single TSV

To ensure that the ADDLL with a single TSV operates normally, and we also observe the phase error between DIE1_CLK and DIE2_CLK. After the ADDLL is locked, we sample 1000 numbers of phase error with PVT variations. In FF case, the proposed ADDLL operates with 420MHz and 1.5GHz clock signals. The phase error is smaller than 70ps after the ADDLL is locked, as shown in Fig. 3.15 and Fig. 3.16. In TT case, the proposed ADDLL operates with 300MHz and 1GHz clock signals. The phase error is smaller than 80ps after the ADDLL is locked, as shown in Fig. 3.17 and Fig. 3.18. In SS case, the proposed ADDLL operates with 187MHz and 648MHz clock signals. The phase error is smaller than 170ps after the ADDLL is locked, as shown in Fig. 3.19 and Fig. 3.20.

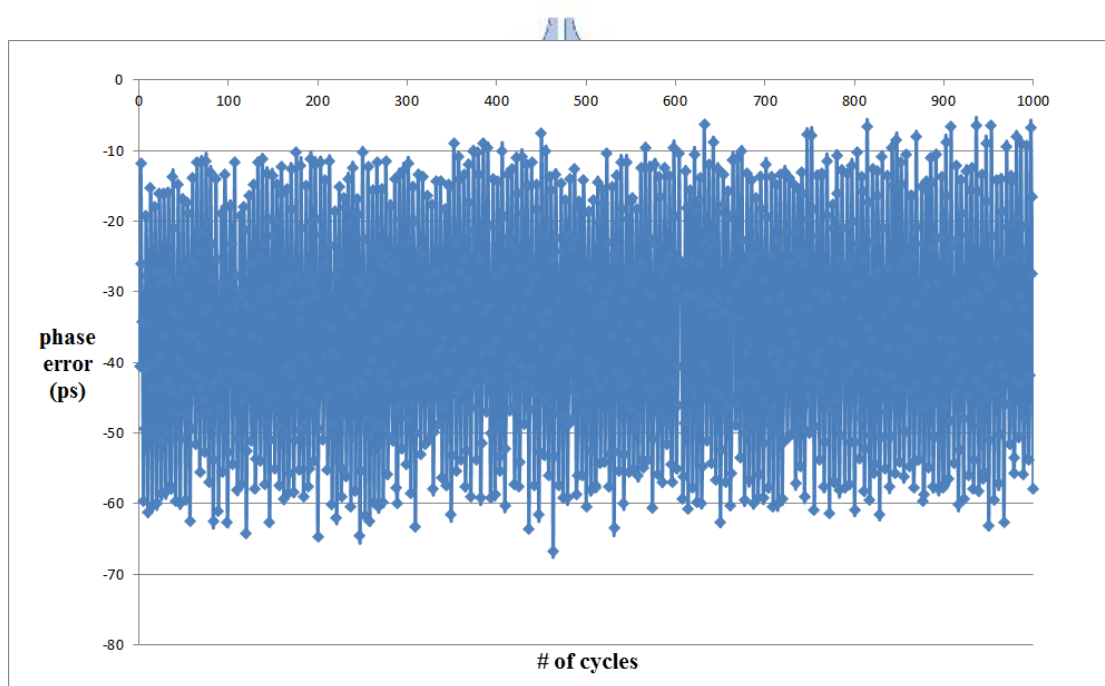


Figure 3.15 The phase error between DIE1_CLK and DIE2_CLK at FF corner with 1GHz operation frequency.

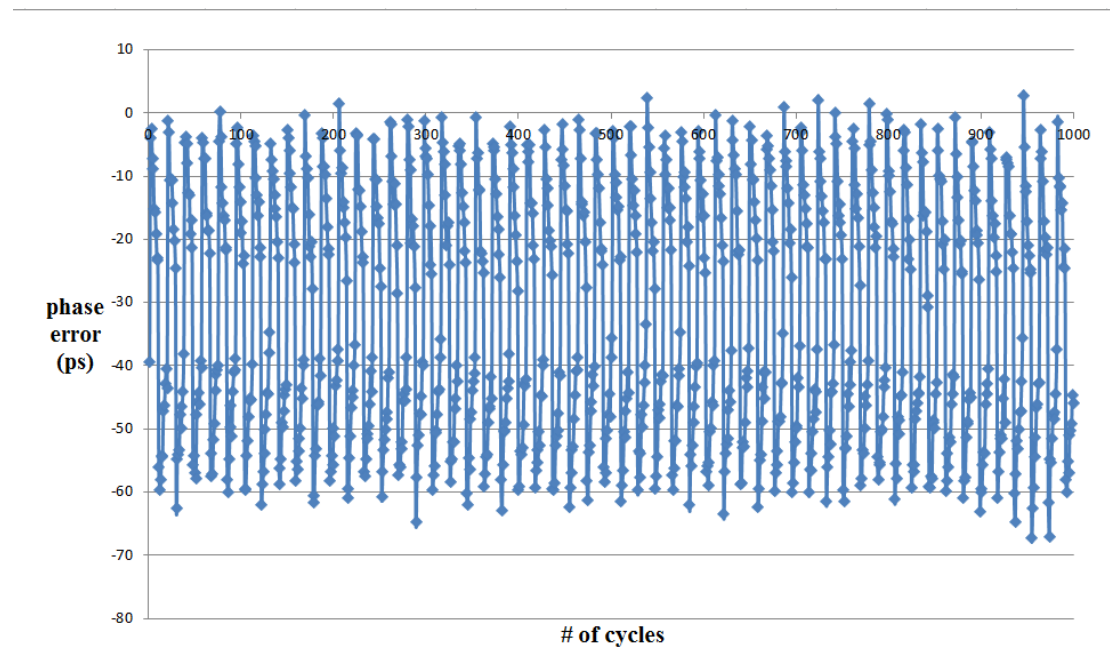


Figure 3.16 The phase error between DIE1_CLK and DIE2_CLK at FF corner with 300MHz operation frequency.

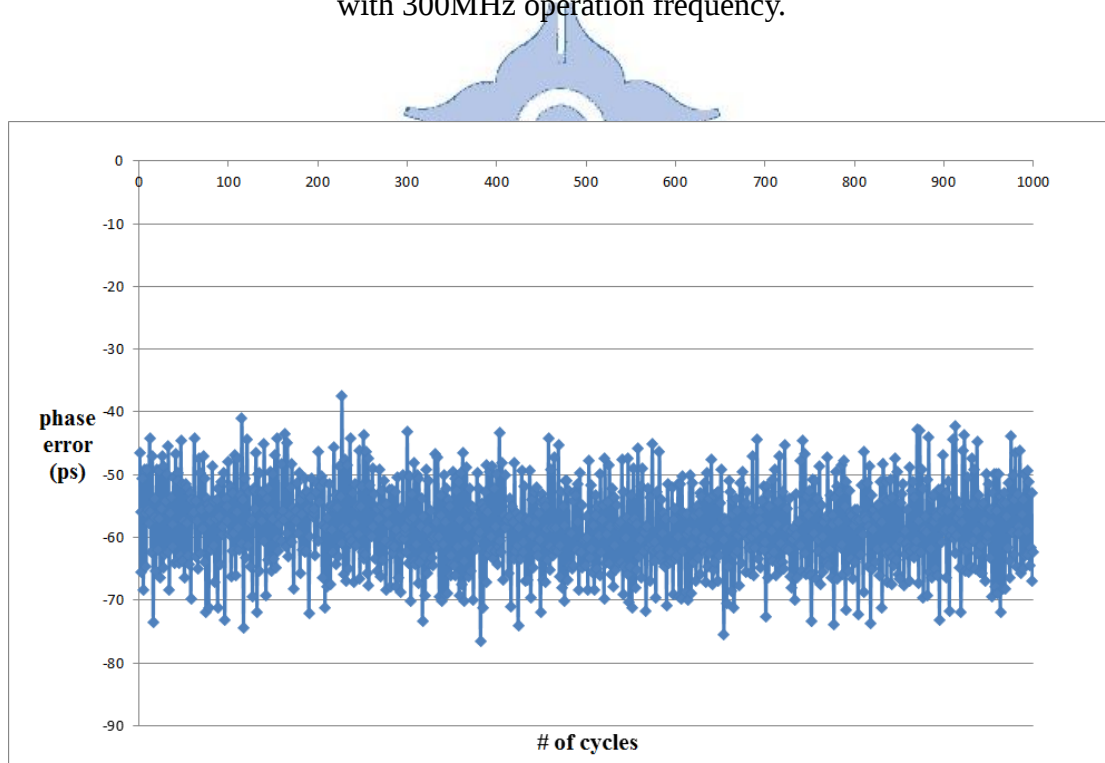


Figure 3.17 The phase error between DIE1_CLK and DIE2_CLK at TT corner with 1GHz operation frequency.

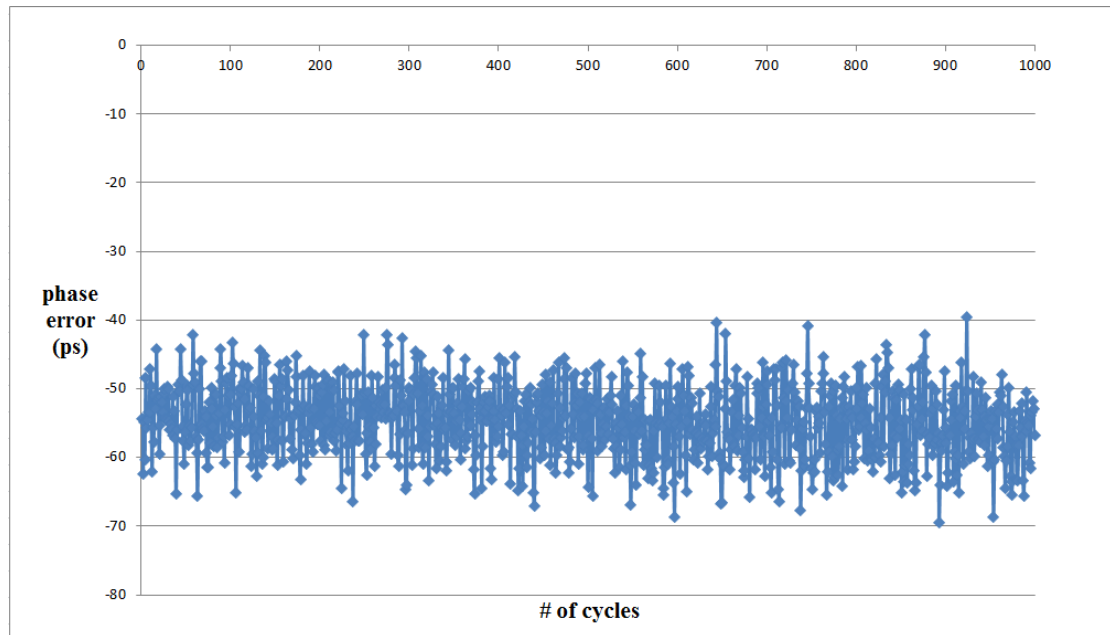


Figure 3.18 The phase error between DIE1_CLK and DIE2_CLK at TT corner with 300MHz operation frequency.

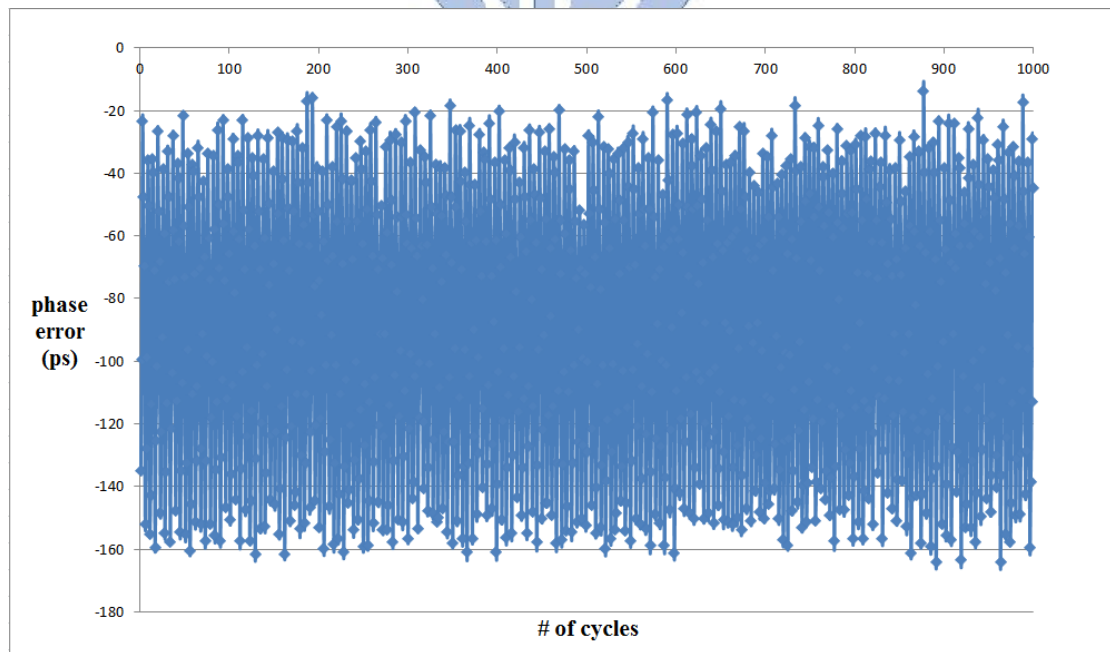


Figure 3.19 The phase error between DIE1_CLK and DIE2_CLK at SS corner with 1GHz operation frequency.

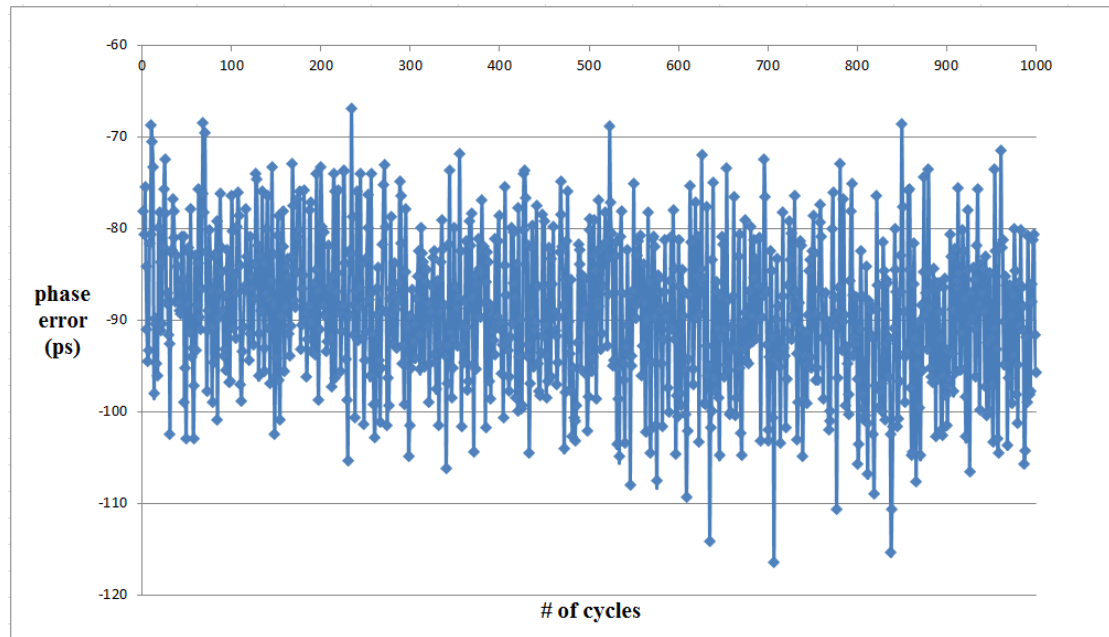


Figure 3.20 The phase error between DIE1_CLK and DIE2_CLK at SS corner with 300MHz operation frequency.



3.4.4 Phase Error

In section 3.4.3, the reasons of phase error are composed of the TSV delay mirror mismatch, the deadzone of phase detector, and the signal dividers. The TSV delay mirror mismatch is composed of two possible reasons. The first reason is caused by the capacitance unbalance between upper path and bottom path in die2. The second reason is caused by the TSV delay mirror mismatch by the TDC-Embedded CDL, as shown in Table 3.5.

Table 3.5 The TSV mirror mismatch

	FF	TT	SS
TSV delay Mirror Mismatch(ps)	< 22	< 30	< 47

The deadzone of phase detector is limited by the DFFs, and the deadzone value of the phase detector is shown in Table 3.6.

Table 3.6 The deadzone of the phase detector

	FF	TT	SS
Deadzone (ps)	19	< 31	< 51

3.5 Performance Comparisons

3.5.1 Two Proposed ADDLLs

Table 3.7 shows the comparison table between the proposed ADDLL with two TSVs and the proposed ADDLL with a single TSV. Both of two architectures are implemented in 90nm process. The proposed ADDLL with two TSVs can eliminate the TSV delay variation by the DCV-based delay line before the ADDLL's normal operation. That means, the TSV delay variation problem can be solved. As compared with ADDLL with a single TSV architecture, the phase error is smaller. However, the area of the proposed ADDLL with two TSVs is larger than the ADDLL with a single TSV due to the high resolution DCV-based delay line. Besides, the proposed ADDLL with a single TSV only uses a single TSV channel, and thus, the TSV delay variation can be avoided. The area of ADDLL with a single TSV is smaller, and the cost for TSV manufacturing is also lower. To sum up, both of two architectures have its advantages, and they are both suitable to be applied to 3-D ICs die-to-die clock synchronization.

Table 3.7 Comparison table of ADDLL between a single TSV and two TSVs

	ADDLL with two TSVs	ADDLL with a single TSV
Type	All-Digital	All-Digital
Process	90nm	90nm
Supply Voltage	1.0 V	1.0V
Number of TSV channel	2	1
Operation Frequency	300MHz ~ 1GHz	200MHz ~ 1GHz
Phase Error	< 21.9ps	< 80ps
Area (mm ²)	0.09	0.0289
Power (mW)	3.27 @ 1GHz	4.88 @ 1GHz

Table 3.8 illustrates the gate count numbers of two proposed ADDLL, and it shows that the gate count of two proposed ADDLL is almost same. That means, the core utilization of ADDLL with two TSVs is not enough, and its layout can be compacted.

Table 3.8 Gate count of ADDLL between a single TSV and two TSVs

	Gate count of ADDLL with two TSVs	Gate count of ADDLL with a single TSV
DIE1	3102	3206
DIE2	427	298
Tester Circuit	N/A	266

3.5.2 Comparison with prior arts

Table 3.9 illustrates the performance comparison with prior arts. The proposed two ADDLL architectures can solve the TSV delay variation phenomenon. If the TSV delay variation cannot be solved, [2] may cause a large phase error due to the mirrored TSV delay line. Besides, the area of the proposed two ADDLL architectures is smaller than [2]. As compared to [3], the operation speed of the proposed design is higher. Furthermore, the [3] needs to switch the forward path and feedback path in the phase maintain mode, it may cause a large phase error during this mode. [4] is an analog architecture, and its power consumption is higher than the proposed two ADDLL architectures. Besides, the two DLLs work at the same time with the bidirectional buffers will increase the design complexity. In the advanced COMS process, the analog charge-pump-based D-DLL faces the design challenges, such as high voltage gain with a low supply voltage and leakage current of MOS transistors.

In summary, the proposed two ADDLL architectures can prevent the TSV delay variation problem, and it is suitable for 3-D ICs die-to-die clock synchronization.

Table 3.9 Performance Comparison with prior arts

	ADDLL with two TSVs	ADDLL with a single TSV	JSSC'13 [30]	TCAS-I'13 [31]	ISCAS'12 [32]
Type	All-Digital	All-Digital	All-Digital	All-Digital	Analog
Process	90nm	90nm	130nm	90nm	0.18 μ m
Supply Voltage	1.0V	1.0V	1.2V	1.0V	1.8V
Number of TSV channel	2	1	2	2	2
Frequency	300MHz ~ 1 GHz	200MHz ~ 1 GHz	200MHz ~ 1.6GHz	50 MHz ~ 600 MHz	556 MHz ~ 1.5 GHz
Phase Error	< 21.9ps	< 80ps	<50ps*	< 15.8ps	< 2ps
Area (mm ²)	0.09	0.0289	0.12**	0.0088	N/A
Power	3.27mW @1GHz 1.06mW @600MHz	4.88mW @1GHz 2.61mW @600MHz	0.9mW @1.6GHz	1.8mW @600MHz	56mW @1.5GHz

*if replica delay matched perfectly

**two dies area

Table 3.10 illustrates that the power consumption of ADDLL with a single TSV can be further decreased by the clock gating of the 64 DFFs of the TDC-Embedded CDL. However, the trigger clock signals of 64 DFFs are not gated in the current tape-out version.

Table 3.10 The power consumption of the DFFs

	Power Consumption of 64 DFFs
64 DFFs @ 600MHz	0.611mW
64DFFs @ 1GHz	1.012mW

Chapter 4 Conclusion and Future Works

4.1 Conclusion

Two ADDLL for 3-D ICs die-to-die clock synchronization with PVT variations are proposed in this thesis. First, the ADDLL with two TSVs can solve the TSV delay variation with the proposed DCV-based delay line, and it can operate with an input frequency ranging from 300MHz to 1GHz. However, the larger chip area is the disadvantage of this architecture. Second, the ADDLL with a single TSV can avoid the TSV delay variation, because this architecture only requires a single TSV channel. It can operate with an input frequency ranging from 200MHz to 1GHz. The proposed architectures are easy to be ported to different process in a short time, because they are implemented with standard cells. Therefore, both of two ADDLL architectures are suitable for 3-D ICs die-to-die clock synchronization.

4.2 Future Works

In recent years, the TSV package technology is more and more popular, and it has many advantages. The advantages of TSV are increasing numbers of I/O saving, power consumption, and reducing propagation delay time. With the skillful advanced process, the TSV package technology can improve the SoC performance. However, the TSV package technology has many design challenges.

For the 3D-ICs RAM application, many dies are connected with TSVs, but the TSV delay values of each die are different from each other. That's a serious problem to transfer and receive data. That's why we propose the ADDLL architectures for 3-D ICs die-to-die clock synchronization. However, the ADDLL for 3-D ICs die-to-die clock synchronization also faces the design challenges about the multi-layer dies. The multi-layer die-to-die clock synchronization problem should be solved in the future. Besides, the numbers of chip implemented with TSVs becomes more and more, and the reference clock signal given by the master chip transmits to slave dies. The multi-layer die-to-die clock synchronization problem must be solved, or the other slave dies may not work correctly.

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