國 立 中 正 大 學

資訊工程學系研究所

碩士論文

1Mbps - 40Mbp 人體通道傳收器設計與實現

Design and Implementation of a 1 Mbps – 40 Mbps human body channel communication transceiver

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摘要

在台灣，穿戴式科技以及半導體製造技術的進步，使得可以穿戴在人體身上的裝備變得越來越小也越來越多功能。尤其是結合到生物醫學的領域中，隨著老齡化的人口比例越來越嚴重，再加上年輕人口越來越少。為了更有效率的照顧老人，所以必須改善生物醫學方面行動裝置的使用方式。透過裝置間的相互資料傳輸與統合，才能得到更精準的數據。至於裝置間資料傳輸的方法有很多種，在此我們使用最新的資料傳輸方法，也就是人體通道傳輸。而人體通道傳輸其實就是透過人體皮膚傳導訊號，來達到裝置間的溝通效果。比起傳統的有線傳輸，人體通道傳輸有著皮膚當傳輸媒介的方便性，比起傳統的無線傳輸，人體通道傳輸有著更省電及方便攜帶的好處。但是受到了人體天線效應的影響，外界的雜訊會被人體皮膚吸收，進而干擾到訊號傳導，增加了接收端資料以及時脈修復的困難度。

本論文提出了一個低硬體成本、低功率消耗、高傳輸速率與高干擾容忍度的人體通道傳收器。在傳送端部分，我們加入了展頻時脈產生器去減少對外部的電磁干擾。展頻時脈產生器是在一般的時脈產生器中加入頻率的調變，而所產生時脈訊號頻率會在一個範圍內上下擺盪，達成展開頻率的效果。比起其他抗電磁干擾的技術，展頻時脈產生器的成本便宜許多。

在傳收器的接收端前端類比放大器部分，我們使用了可調式的放大器架構來針對因為不同的傳輸長度的不同接收電壓大小的訊號進行放大。在數位電路部分，我們採用了 7 倍頻率超取樣時脈與資料回復電路架構，搭配選舉機制來提升修復效果。所以本論文所提出的人體通道傳收器非常適合應用在人體通道傳輸上。

本論文之晶片是以 90 奈米製程的標準元件庫實現，具有很好的製程移轉能力。工作範圍為 1Mb/s 到 40Mb/s，晶片面積為 0.2mm^2，功率消耗在 40Mb/s 為 1.94 mW.

關鍵字：身體傳輸通道，接收器，高雜訊容忍，高傳輸速率，低功率。

Abstract

In recent years, biomedical applications with semiconductor technologies had become more and more popular. Body area network (BAN) is one of the applications. Traditionally, there are many approaches to implement the BAN and the body channel communication (BCC) is a novel concept of the communication scheme. BCC uses the human body as the signal transmission medium to transmit physiological signals. There are many advantages of BCC than wire-less communication, such as low power consumption and easy to use. However, because of the body antenna effect, there are many external electromagnetic interferences around the human body that will interfere the reliability of the human body channel and increase the design complexity of the clock and data recovery (CDR) circuit.

In this thesis, we propose a low hardware cost, low-power consumption, high-speed and large jitter tolerance wideband signaling (WBS) transceiver. At the transmitter part, we use the spread spectrum clock generator (SSCG) to reduce electromagnetic interference to the nearby devices. The SSCG performs frequency modulation on the output clock, while the generated clock frequency will be spread within a range. As compared to other anti-electromagnetic interference techniques, the cost of the SSCG is lowest.

At the receiver, in the analog front end (AFE) circuit, we use an variable gain amplifier to amplify the received signal that will be different in different distance. In addition, we use a seven times oversampling CDR circuit with the vote mechanism to reduce the bit error rate with frequency drift and random jitter. Therefore, the proposed transceiver is very suitable for the human body channel communication.

The test chip is implemented in TSMC 90nm standard performance CMOS process, and the proposed architecture has good portability over different processes. The core area of the test chip is 0.2mm^2, and the power consumption is 1.94 mW at 40Mb/s.

Keyword: BCC, transceiver, high-jitter tolerance, high data rate, low power consumption

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Chapter 1

Introduction

1.1. Human Body Area Network Overview

In field of biomedical,there are more and more demands with wearable devices to get the body information. Because of semiconductor technologies become more and more advanced, these wearable devices got smaller area and lower power consumption.

Traditionally, wireline connectionsare used to pass the human body information, such as electrocardiography (ECG), electromyography (EMG), thermometer and sphygmomanometer. Wireline devices will cause patients very inconvenientlywhile gathering the human body information.

Therefore, wireless technologies are applied to get the human body information. Wireless communication around the human body forms thewireless body area network (WBAN). The WBAN is organized by IEEE 802.15 Task Group 6 (TG6) [1]. By the way, the TG6 had been standardizedthe frequency band and protocols for medical and multimedia communications around a human body. We can use the WBAN technique to create many applications, such as earphones, video eyeglasses and head-mounted displays, from healthcare to multimedia [2]. Fig. 1.1 shows the various applications based on the WBAN. However, the devices with WBAN technique are usually battery-poweredwith mobility. There are some requirements for these applicationsthat must be satisfied.For

example, light-weight, small-size, and low-power consumption [3].The applications requirements for the human body are shown in Table 1.1 [4]. In this thesisthe proposed designshould cover both medical and multimedia applications. As a result, we need at least 10 Mbps data rate. However, the protocols in IEEE 802.15.1 standard and IEEE 802.15.4 standard cannot meet this requirement. Therefore, we usesthe human body communication (HBC) to achieve a data rate up to 40 Mbps.

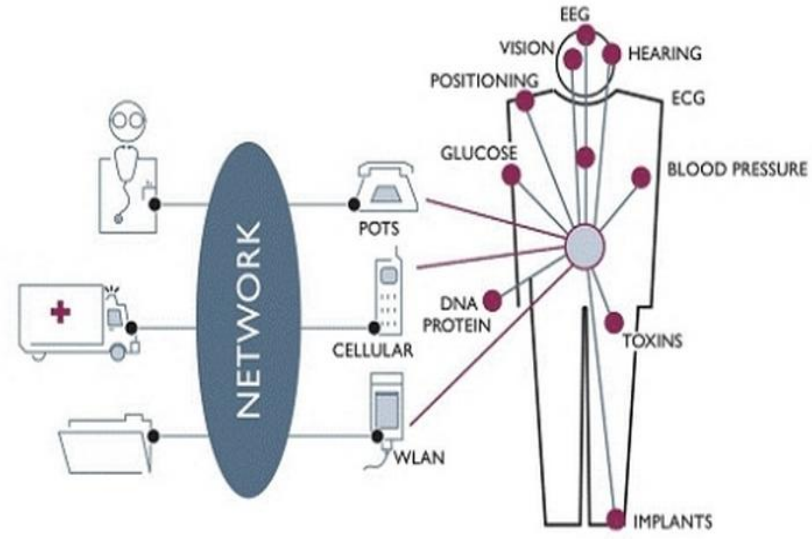


Fig. 1.1: Various applications based on WBAN
http://www.wifinotes.com/computer-networks/body-area-network.html.

Table 1.1 :Applications requirements on human body [4].

Application	Target Data Rate	BER	Latency	Duty cycle	Target Lifetime
Deep Brain Stimulation	**1 Mbps**	**< 10^{-3}**	**< 250 ms**	**< 50%**	**> 3 years**
Capsule Endoscope	**1 Mbps**	**< 10^{-10}**	**< 250 ms**	**< 10%**	**> 24 hours**
ECG	**72 kbps**	**< 10^{-10}**	**< 250 ms**	**< 10%**	**> 1 week**
EEG	**86.4 kbps**	**< 10^{-10}**	**< 250 ms**	**< 10%**	**> 1 week**
EMG	**576 kbps**	**< 10^{-10}**	**< 250 ms**	**< 10%**	**> 1 week**
Audio	**1 Mbps**	**< 10^{-5}**	**< 20 ms**	**< 50%**	**> 24 hours**
Video/Medical Imaging	**10 Mbps**	**< 10^{-3}**	**< 100 ms**	**< 50%**	**> 12 hours**
Voice	**50-100 kbps per flow**	**< 10^{-3}**	**< 10 ms**	**< 50%**	**> 24 hours**
Hearing Aid	**200 kbps**	**< 10^{-10}**	**< 250 ms**	**< 10%**	**> 40 hours**
Drug Dosage	**< 1 kbps**	**< 10^{-10}**	**< 250 ms**	**< 1%**	**> 24 hours**
O2/CO2/BP/temp/respiration/ glucose monitoring, accelerometer	**< 10 kbps**	**< 10^{-10}**	**< 250 ms**	**< 1%**	**> 1 week**

Traditionally, the air isthe transmission medium for WBAN. For example, the radio frequency (RF) wireless techniques such as Bluetooth and ZigBee use the 2.4 GHz ISM band [5]-[7]. Fig. 1.2 shows a typical RF transceiver.

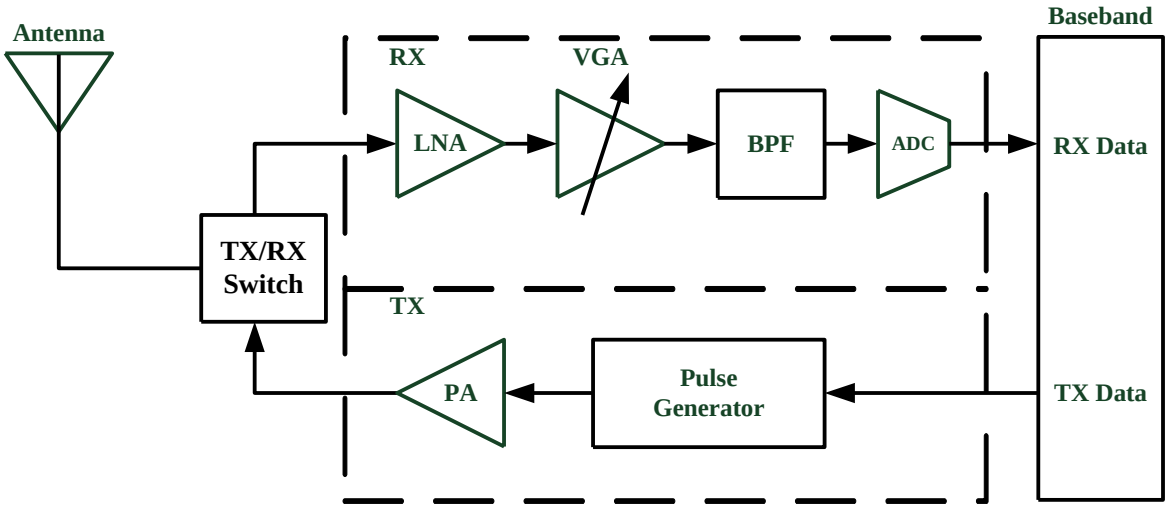


Fig. 1.2:Typical RF transceiver.

The RF transceiver is composed of an antenna, a TX/RX switch, a power amplifier (PA), a pulse generator, a low noise amplifier (LNA), a variable gain amplifier (VGA), a band pass filter (BPF) and an analog to digital converter (ADC). The RF wireless technique can provide in short range transmission.Although RF wireless technique have a great performance at short range. Once there are someone who uses the same RF band at 2.4-GHz nearby, the RF transceivers will interfere each other such that the data transmission will be broken.

In recent studies, there are three major types of RF wireless technique, such asIEEE 802.15.1 standard and IEEE 802.15.3 standard and IEEE 802.15.4 standard. The IEEE 802.15.1 standard is known as Bluetooth, it has 720 kbps data rate within 10 m, and the power consumption is at least 1 mW. But the IEEE 802.15.1 standard uses the 2.4 GHz ISM band that will decrease the data transmission quality. The IEEE 802.15.3 standard have 110 Mbps and 200 Mbps data rate within 10 m, and the power consumption is 100 mW and 250 mW, respectively. But the IEEE 802.15.3 standard uses the 3.1~10.4 GHz ultra wide band that is not licensed at Taiwan. The IEEE 802.15.4 standard is known as ZigBee, and it has at most 240 kbps data rate within 10 m, and the power consumption is at least 0.5 mW. But the

IEEE 802.15.4 standard uses the 2.4 GHz and 915 MHz and 868 MHz ISM band that will decrease the data transmission quality same as the same reason as IEEE 802.15.1 standard.In addition, RF wireless techniques are easily affected by the body shadowing effect and results in large path loss. As a result, the RF wireless technique must use the power amplifier to increase the transmission power and has high power consumption. The maximum data rate of Bluetooth v 2.0 is 3Mbps.As compared to the maximum data rate of body channel communication (BCC)and the power consumption of BCC. The power consumption of the BCC runs at 10 Mbps is only 2 mW.

There is a new technique for WBAN, body channel communication (BCC) was proposed to solve the problems of wireless techniques. The first introduced BCC is Zimmerman [8]. Unlike other wireline transmission which uses lines as the transmission medium, BCC uses the human body skin as a signal transmission medium to transmit physiological signals between transceivers that there are pads contacted on human body skin[9].After receiving the signals from the human body, the wearable devices analyze these physiological signals immediately and then send these physiological signals to medical center to achieve healthcare purpose.

In BCC, there are two types of transmission : a)the transmission line approach; b)the capacitive approach, as shown in Fig. 1.3 [10].Using the transmission line approach, the transmitter use two electrodes directly attached to the human body to transmit the physiological signals. Based on the same concept, two electrodes directly attached to the human body at receiver side, which are used to sense the differential signal. In this approach, we can say that the human body is treated as a special kind of transmission line. Oppositely using the capacitive approach, we use the environment as a reference to force or detect a variation of the electric potential of the human body. This will be our main method to be implemented.

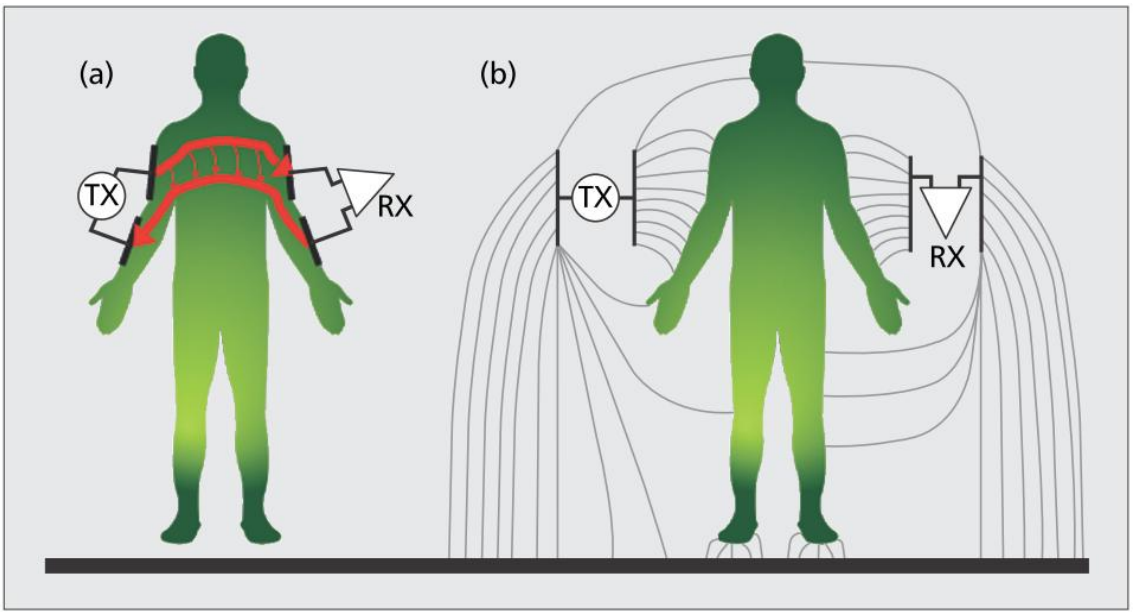


Fig. 1.3:(a)the transmission line approach; (b)the capacitive approach [10].

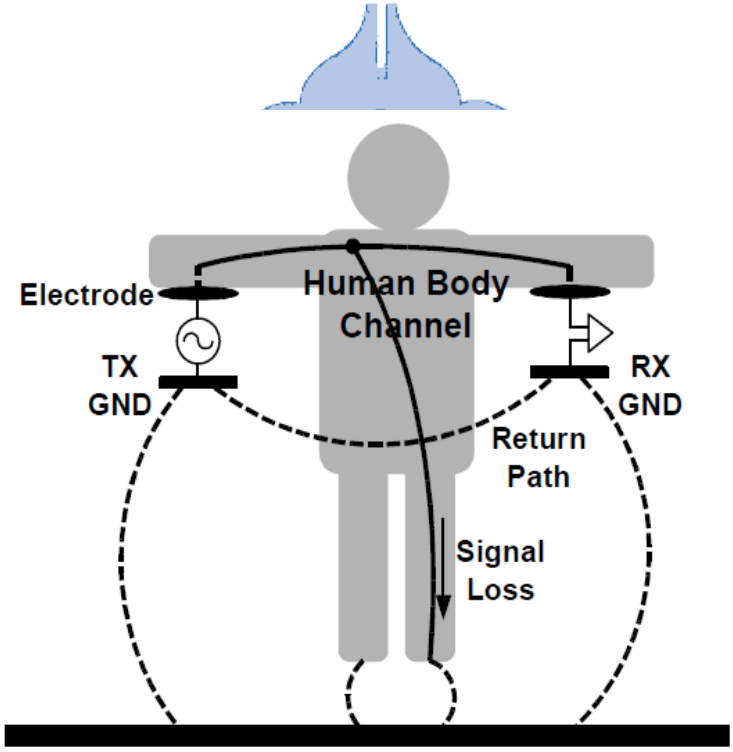


Fig. 1.4: Concept of the human body channel communication [11].

Fig. 1.4 shows the concept of the human body channel communication [11]. There are one electrode on the receiver part and one electrode on the transmitter part.The electrodes

are made of Ag/Agcl attaching on human body skin, and human body skin acts as the transmission medium. There are three reasons that why we choose the BCC approach. First, because of the high conductivity of the human body channel as compared to the air, the human body channel has smaller path loss than the air channel. Second, because the BCC technique is based on near-field coupling, the signal transmission will be rapidly disappeared that cause less interfering with adjacent electronic devices. Third, because the physiological signal is directly transmitted to the human body channel, there is no needs to use antennas with power amplifier that causes huge power consumption. In addition, the communication distance usually ranges from 10 cm to 120 cm, depending on the devices performance and devices location on human body. The communication frequency is from 10 kHz to 100MHz on human body channel because of the small power attenuationfrom skin as shown in Fig. 1.5 [12] and the data transmission rate depends on the transmission schemes in the BCC devices.

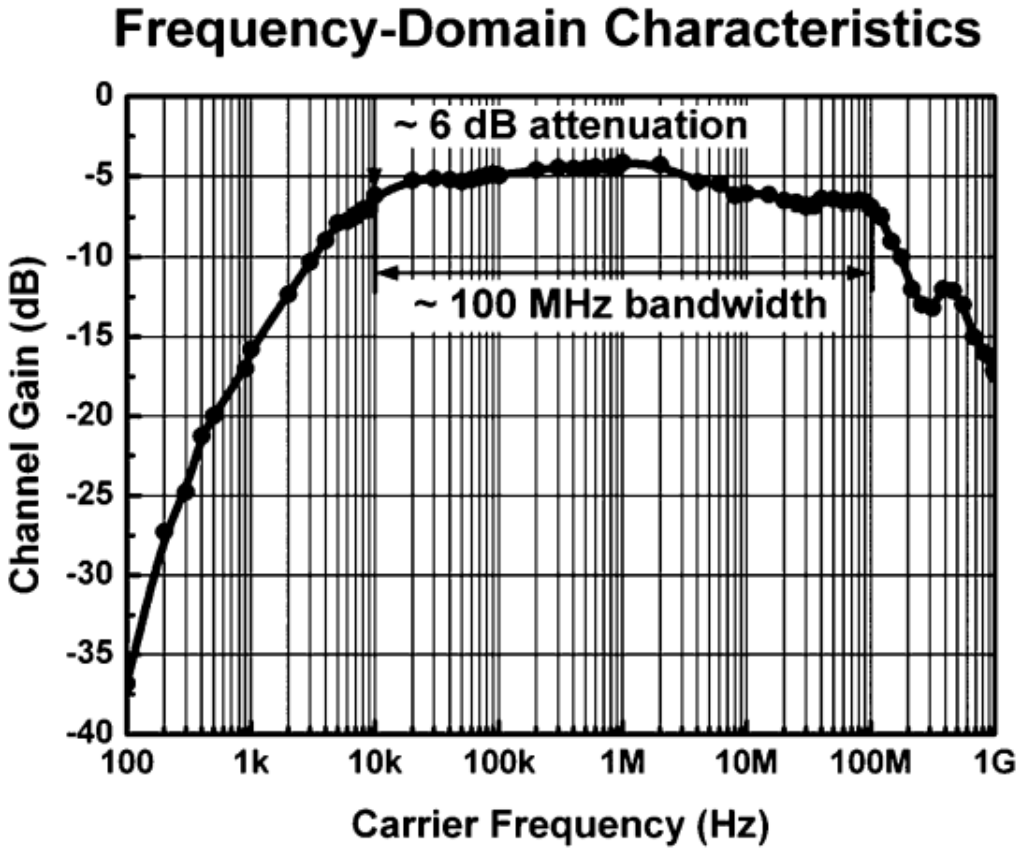


Fig. 1.5: Transmission attenuation in frequency-domain characteristics analysis [12].

1.2. Characteristics of Human Body Channel

To more understand the BCC technique, we need to know the characteristics of the human body channel, and there have been studied and investigated in [8],[13],[14],[15]. In addition, these reference papers mainly explain that at different distance and transmission frequency between the transmitter and the receiver will cause some stationary result.Thus the reference papers show that the human body channel can be explainedby a discrete RC circuit model.

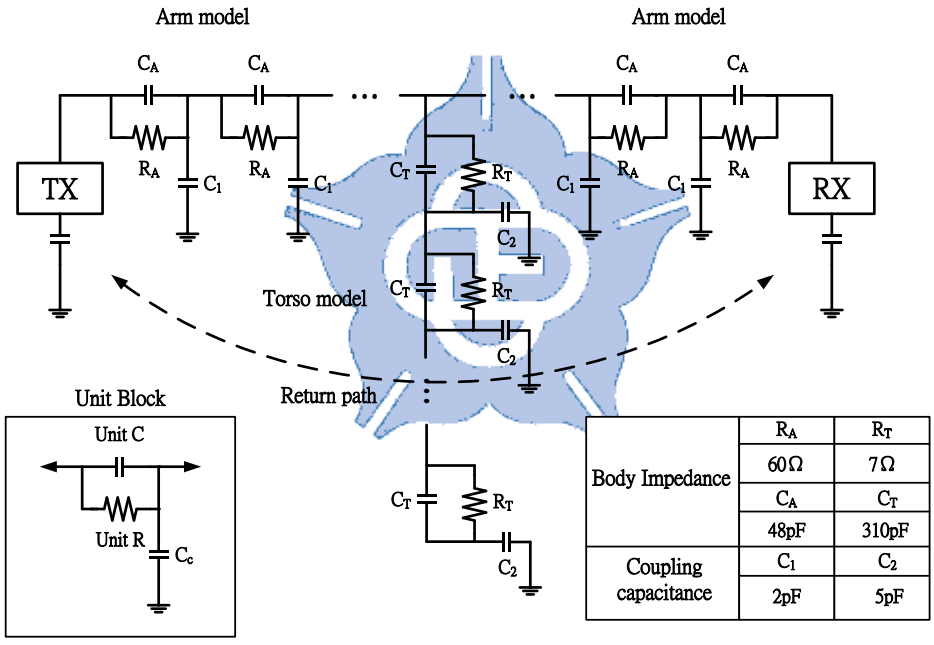


Fig. 1.6: Near-field coupling RC model of the human body.

Fig. 1.6 shows the near-field coupling RC circuit model of human body [13]. In this near-field coupling RC circuit model, we can see that there are two arms and a body trunk. Either the arm or the body trunk consists of many RC circuit units. Every RC circuit unit consists ofcomplex impedanceand the coupling capacitance to the external ground, and

these RC values are calculated by Gabriel's experimental result [14] and Zimmerman's method [8]. Every RC circuit unit representspart of the human body skin segment which is 10 cm length.We can simulate the human body channel by using this RC model. In addition, the return path in Fig. 1.6 is a parasitic capacitor associated with the parasitic air coupling between the ground of the transmitter and the receiver.

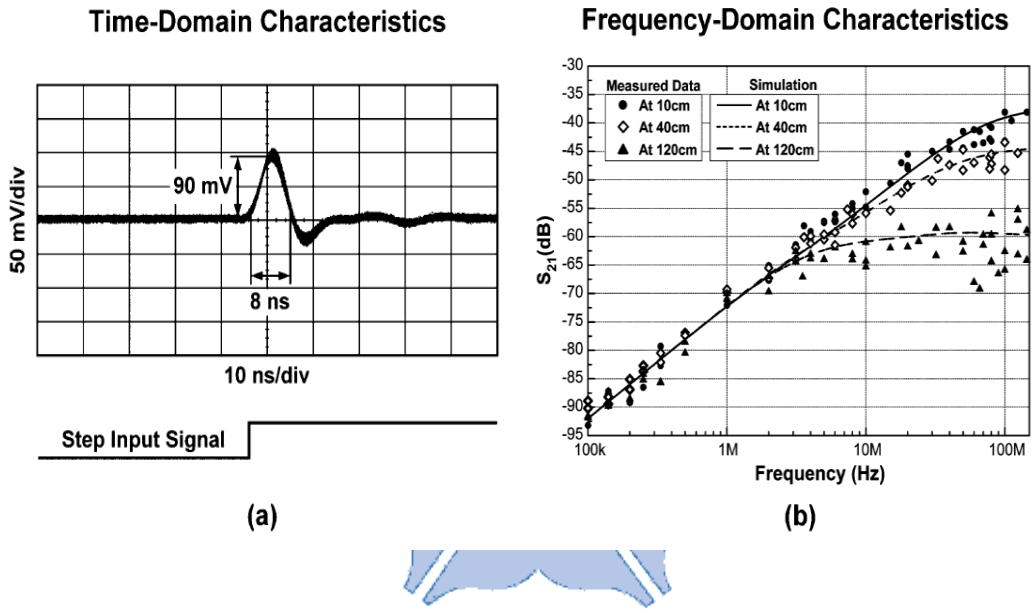


Fig. 1.7: Characteristics of human body channel. (a) In the time-domain (b) In the frequency-domain [12]

According to the RC circuit model previously mentioned,we send the digital square waveform into the human body channel and analyzethe time-domain and the frequency-domain characteristic of the human body channel.Fig. 1.7 (a) shows the time-domain analysis with a step input signal waveform with 3V amplitude and finally a wide-band pulse signal with no DC offset is shown in the receiver part.We can see that the wide-band pulse signalhave 90mV peak amplitude with8ns pulse width.Therefore, the

attenuation (S_{21}) is 20*ln(0.09V/3V) = -70dB. Fig. 1.7 (b) shows the measurement for power attenuation at 10cm/40cm/120cm between the transmitter and the receiver. The measured frequency range is from 100kHz to 150 MHz. When the frequency is smaller than 10MHz, there are huge power attenuation no matter the transmission distance. This phenomenon is unfavorable to the receiver, because the receiver needs more cost to receive wide-band pulse signal and recover to the original digital square waveforms.

In addition, HBC exists a problem that is human body antenna effect. There are some studies about human body antenna effect [13], [16], [17].

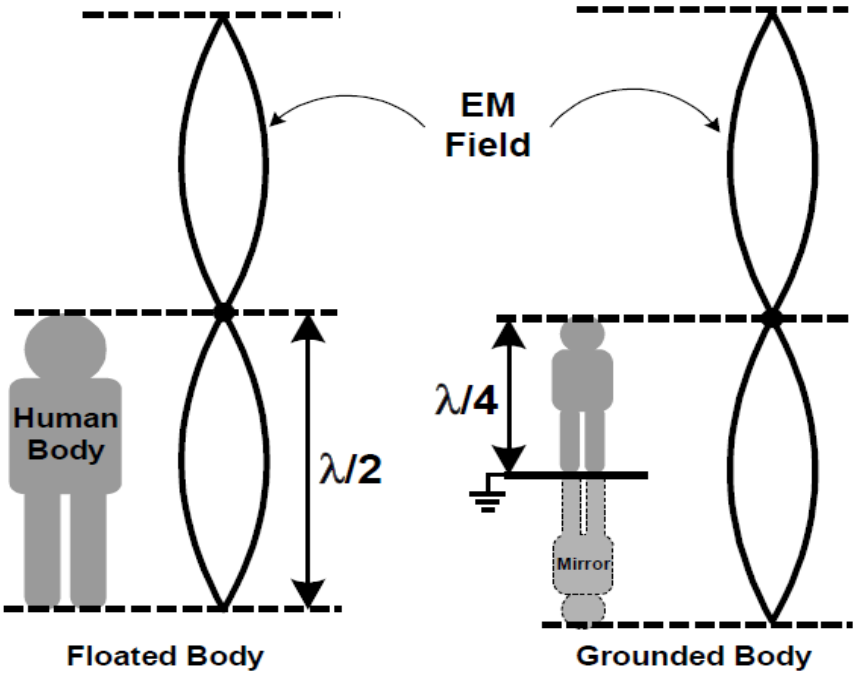
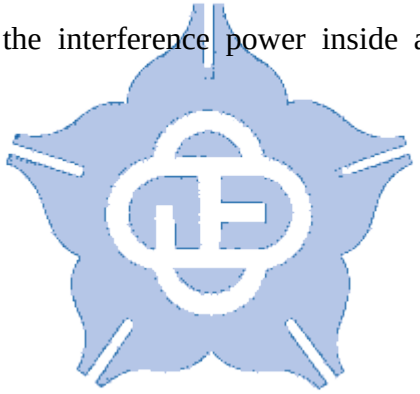


Fig. 1.8 : Human body antenna effect [16].

Fig. 1.8 shows thehuman body under external electromagnetic fields,and the human body is similar to an antenna [16]. The wavelength of resonant frequency of the human

body (λ) is double or quadruple as much as the height of the human body. On the other hand, the wavelength is multiple of the height of the human body, this situation will cause the mirror effect [17]. Therefore, human body antenna effects will absorb external electromagnetic interferences or radio signals into the human body channel.This will cause the huge signal interference and reduce the signal to interference ratio (SIR). Since the human body is a lossy conductor with conductance value of < 0.1 S/m and has a complex shape, the peaking of resonance is not sharp but broadly distributed. Therefore, the human body operates as a wideband antenna in 30-400 MHz frequency range, which overlaps the suitable frequency band for human body channel communication range from 10 kHz to 100 MHz [13], [15].

Next, we discuss about the interference power inside and outside thehuman body channel.



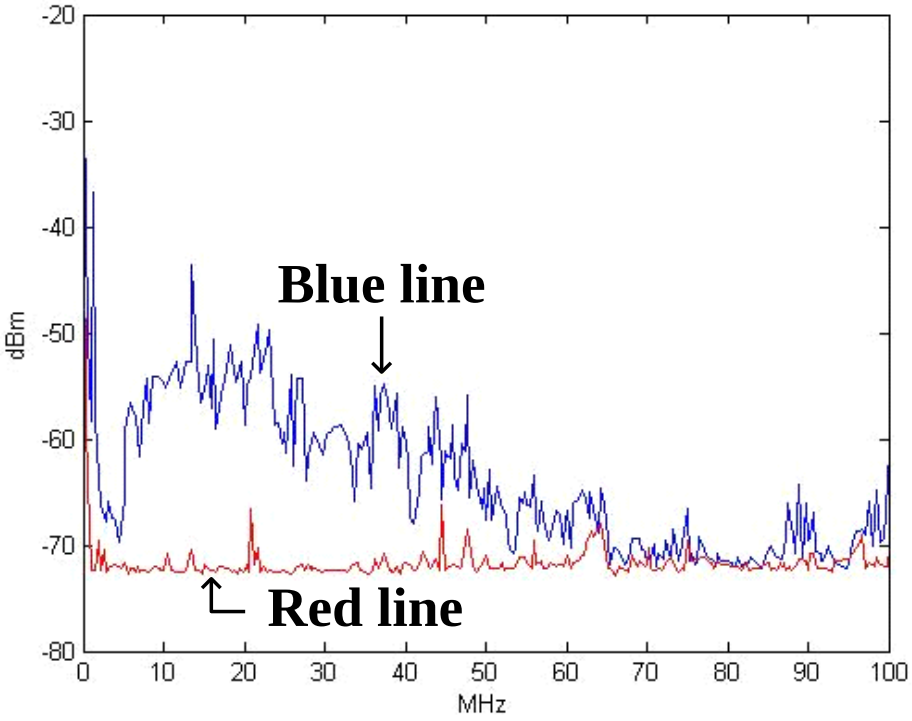


Fig. 1.9 : Measured in-band interferences to the body channel receiver.

Fig. 1.9 is the measured in-band interferences coupled to the body channel receiver from wireless sources nearby. The red line represents the power spectrum of RX electrodewhen the RX electrode didn't attach to the human body skin. Therefore, there is only air coupling between the TX electrode and RX electrode. The blue line represents the power spectrum of RX electrode when RX electrodeattaches to the human body skin.Thus the red line means the absorbed interferences by the human body. Consequently, we can obviously detect that there are many interferences from some near-by devices, such as cell phone, FM radio broadcasting tower, and walkie talkie, and other electrical devices, which use the 10 MHz –100MHz frequency band.

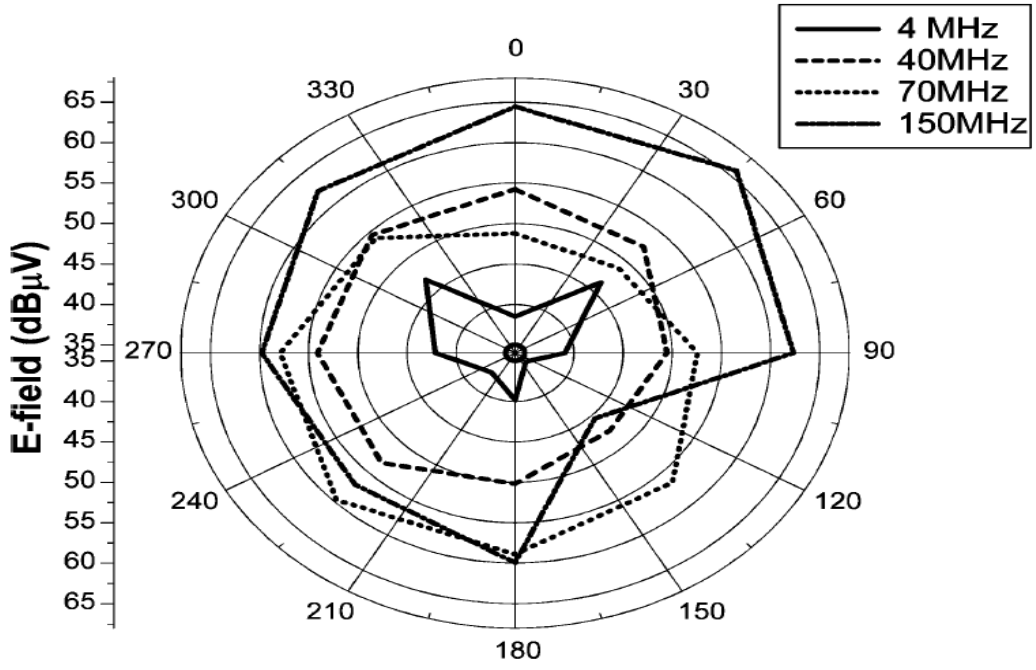


Fig. 1.10 : E-field pattern around a person [13].

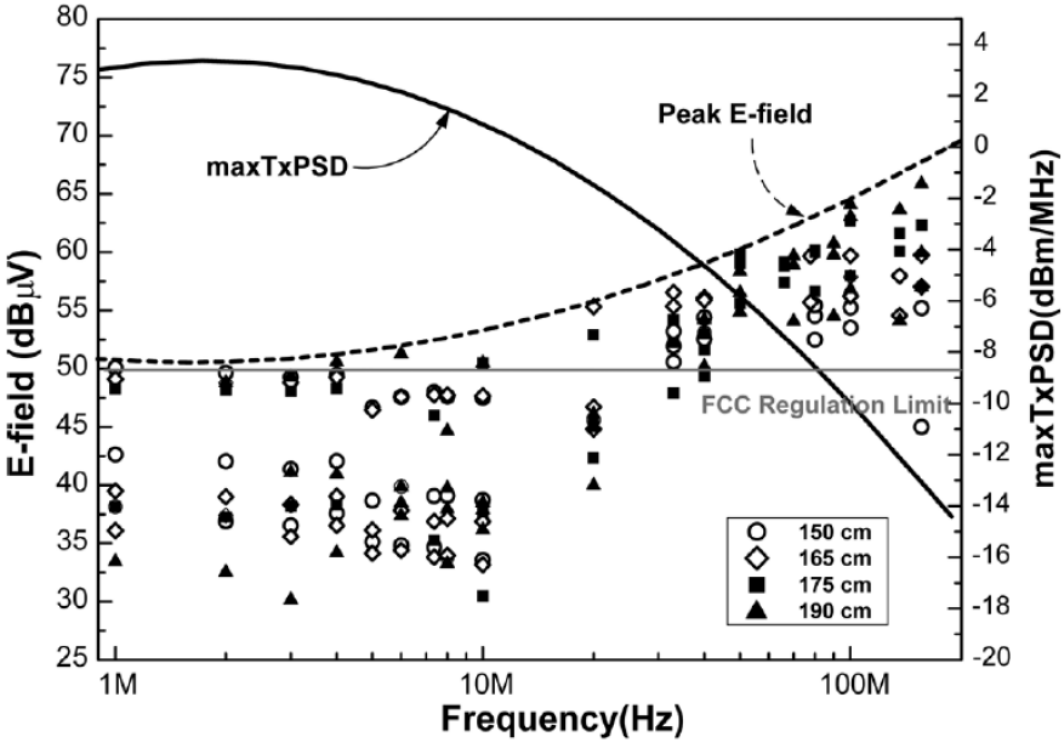


Fig. 1.11 :FCC limitation [13].

On the other side, the BCC circuit also becomes the source that interferes the near-by devices. Therefore, in order to investigate the body antenna effect that interfere the near-bydevices, the electric-field (E-field) strength is measured around human body as shown in Fig. 1.10 [13].

In Fig. 1.10, there are four kinds of frequencies that transmit in the human body channel at the transmitter, and inductors are away from the human body in 3 meters to sense the power emission from the human body.The power of the transmitted signal is fixed at 3 dBm (= 2 mW), and the transmitter is at 0 degree. We can see that the electric-field becomes larger when the transmission frequency is higher. Themeasured maximum signal power at 150 MHz is 30 times larger than the measured maximum signal power at 4 MHz. However, the shape of measurement results will be influenced by the pose of human body, and thus these shapes are not perfect circles segments. In addition, we must comply the FCC limit (Federal Communication Commission Regulation) that results in the maximum transmission power spectral density (PSD), as shown in the curve of maxTxPSD of Fig. 1.11. When we use a low frequency as transmission frequency, we can increasethe transmission power that will not violate the FCC limit. However, for the human body channel, the low frequency will cause larger power attenuation. Therefore, the suitable frequency band is between 10 MHz to 150 MHz.

1.3. Measurement of Human Body Channel

To measure the relevant data of real human body channel and build up a simple discrete RC model, and therefore, a measurement platform is built at NCTU Si2 LAB as shown in Fig. 1.12.A spectrum analyzer is connected to the right hand of a 1.78m human subject by using a metal electrode and coaxial cables. In measurement process, we must notice that all of measurement instruments, such as the signal generator and the spectrum analyzer are powered by uninterruptible power supply (UPS) in order to float the ground. As described inchapter 1.2, the common ground causes a return path from the transmitter to the receiver and that influences the measurement results.

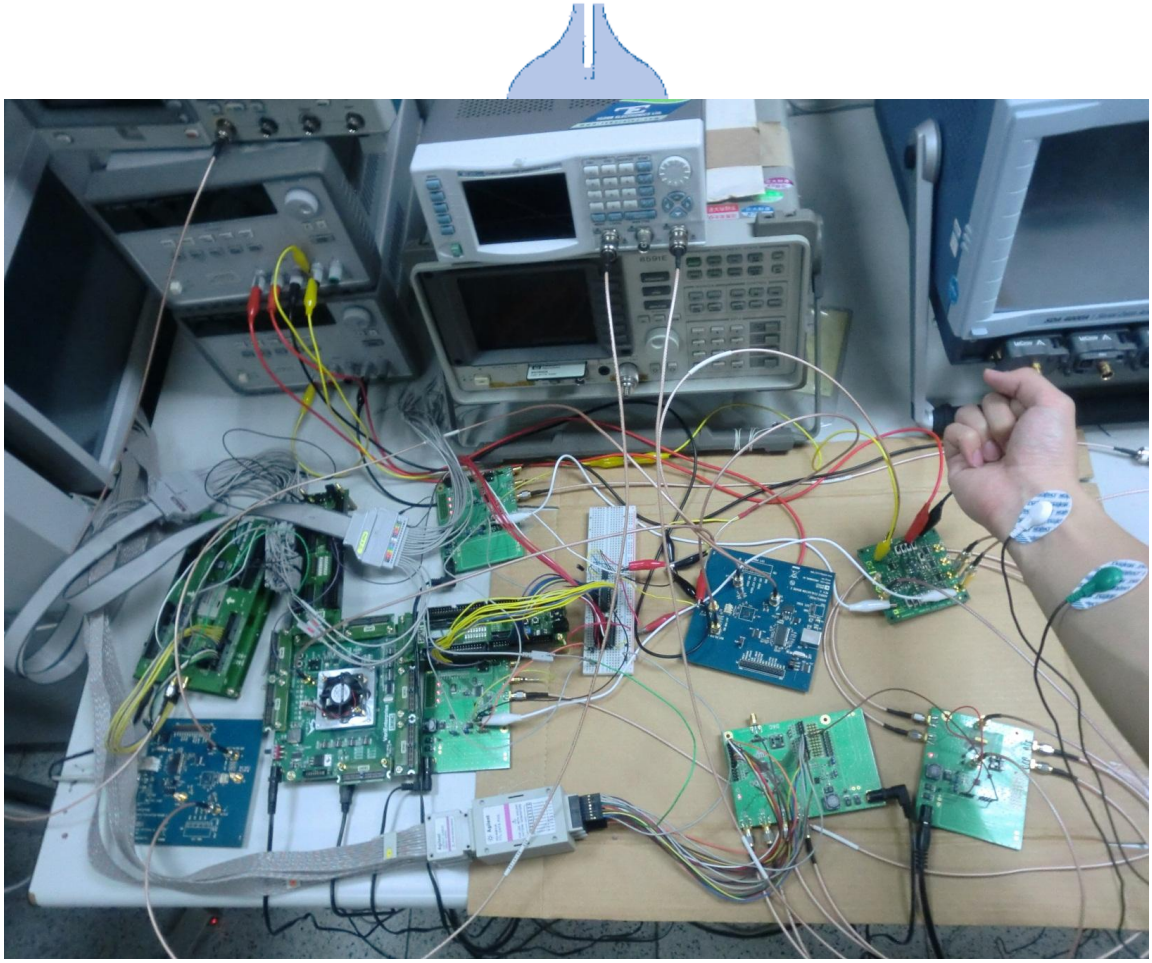


Fig. 1.12: NCTU Si2 LAB prototype of measurement platform.

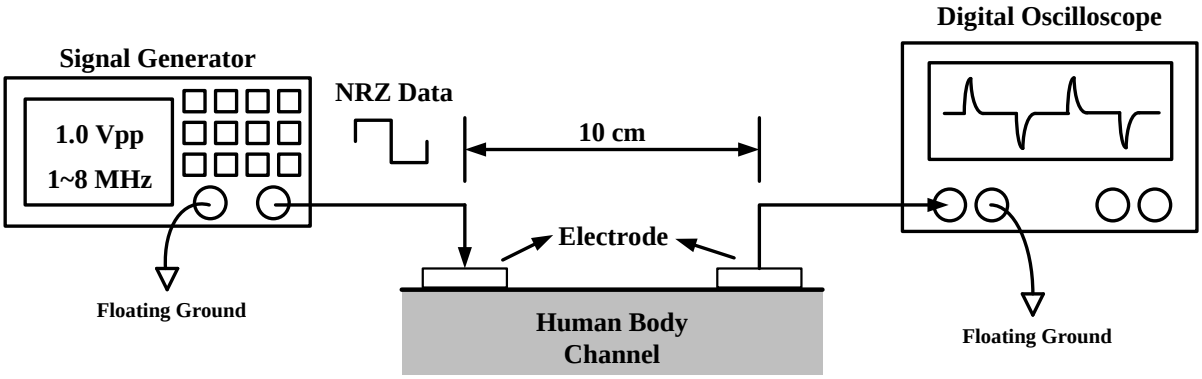


Fig. 1.13: Measurement setup for the investigation of the HBC [12].

A simple schematic diagram illustrates the measurement setup as shown in Fig. 1.13. The distance between the electrode of transmitter and the electrode of receiver is 10cm. The transmitter is a square wave signal generator. The amplitude of the square waveform is 1V and the measured frequency range is from 1MHz to 8 MHz. The transmission signal is transferred to the HBC through the electrode of the transmitter. The electrode of the receiver is connected to the digital oscilloscope. The groundsbetween the transmitter and the receiver are floated.

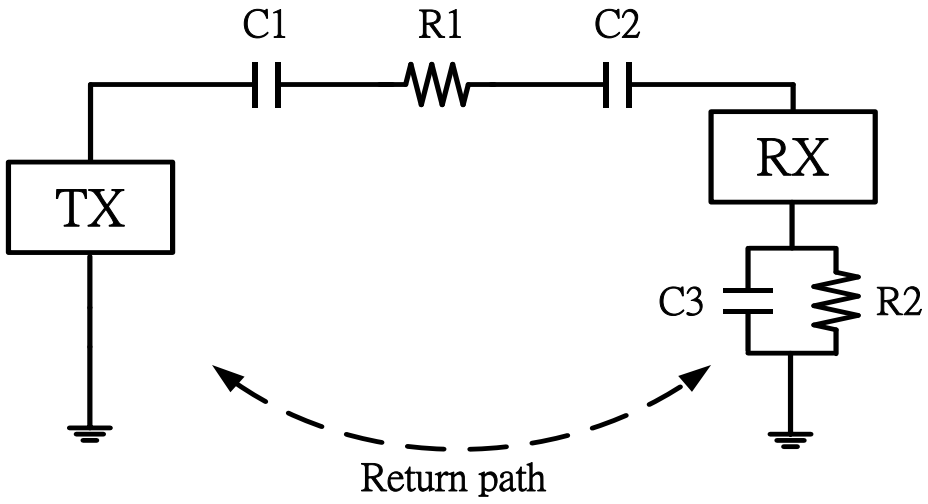


Fig. 1.14: Simple discrete RC model

Fig. 1.14 shows a simple discrete RC model, this is according to the near-field coupling RC model in chapter 1.2. We can see that the simple discrete RC model consists of two resistors and three capacitors. In addition, we adjust the parameters of the simple discrete RC model to make the simulated waveforms similar to the measured wide-band pulse signal at different frequencies.Therefore, we can use this model to easily simulate the performance of the proposed transceiver.

Fig. 1.15 and Fig. 1.16 show the characteristics of human body in time-domain. The left figures are the measured waveforms and the right figures are the simulation waveform by the simple discrete RC model. The input signal is a digital square wave with a 1V amplitude and the frequency range is from 1MHz to 8MHz at 10-cm distance.

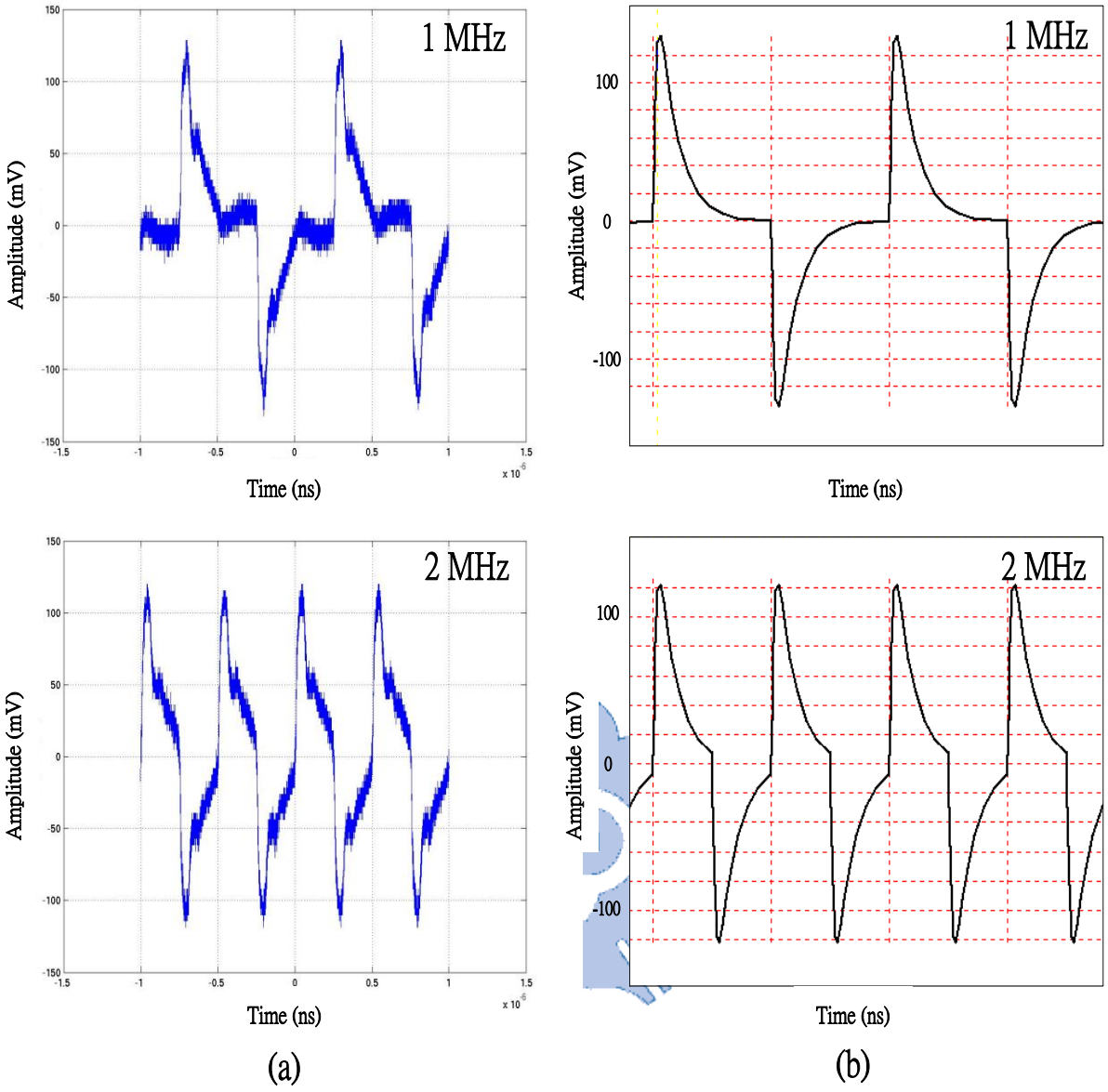


Fig. 1.15: Transient channel response from 1 MHz to 2 MHz. (a) Measured step response. (b) Simulation step response.

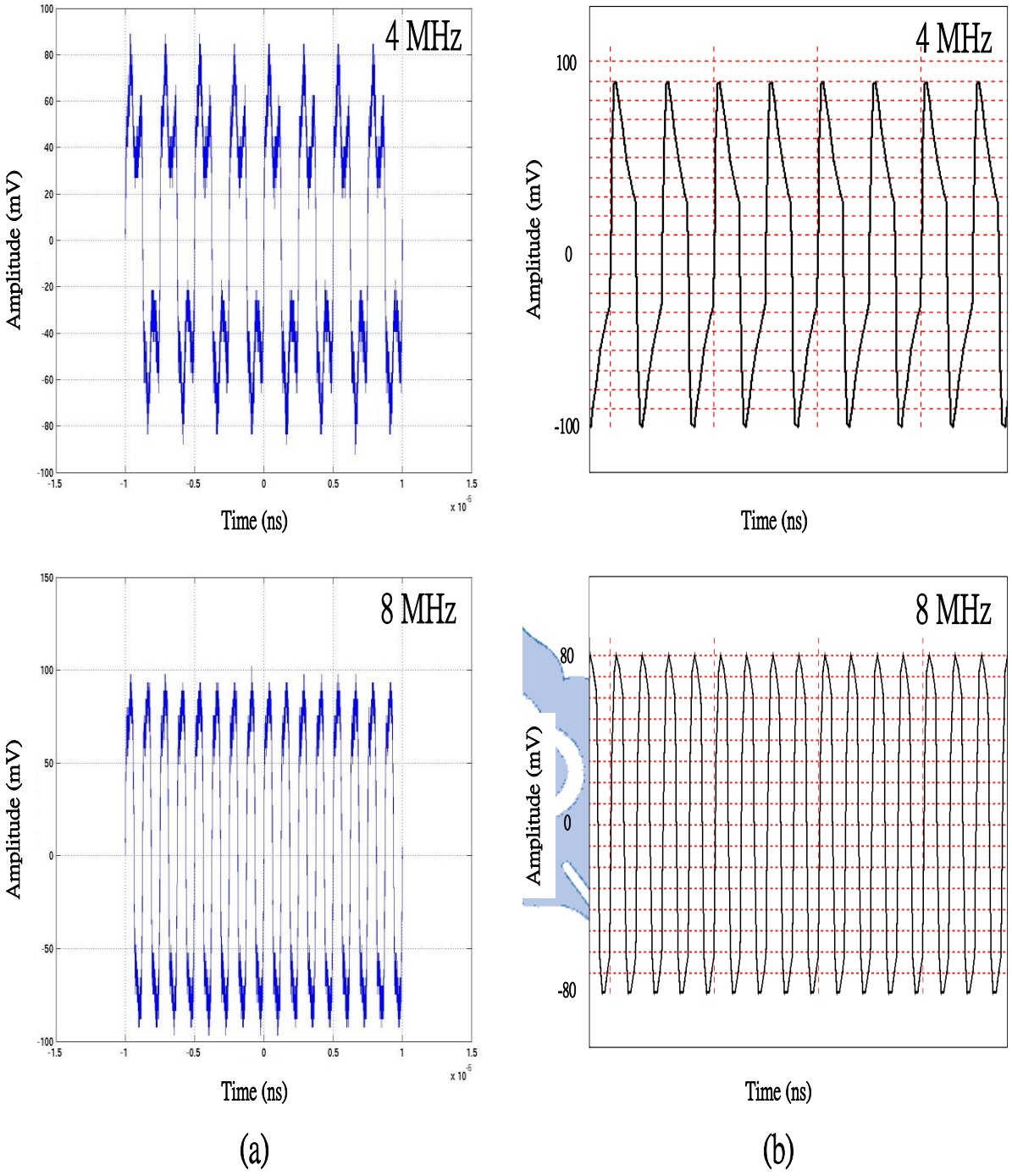


Fig. 1.16: Transient channel response from 4 MHz to 8 MHz. (a) Measured step response. (b) Simulation step response.

In Fig. 1.15 and Fig. 1.16, we can see that the peak voltage of the pulse becomes smaller when the transmission frequency is larger. Because of the noise effects of the environment, the measured waveform has little different from the simulation waveform.

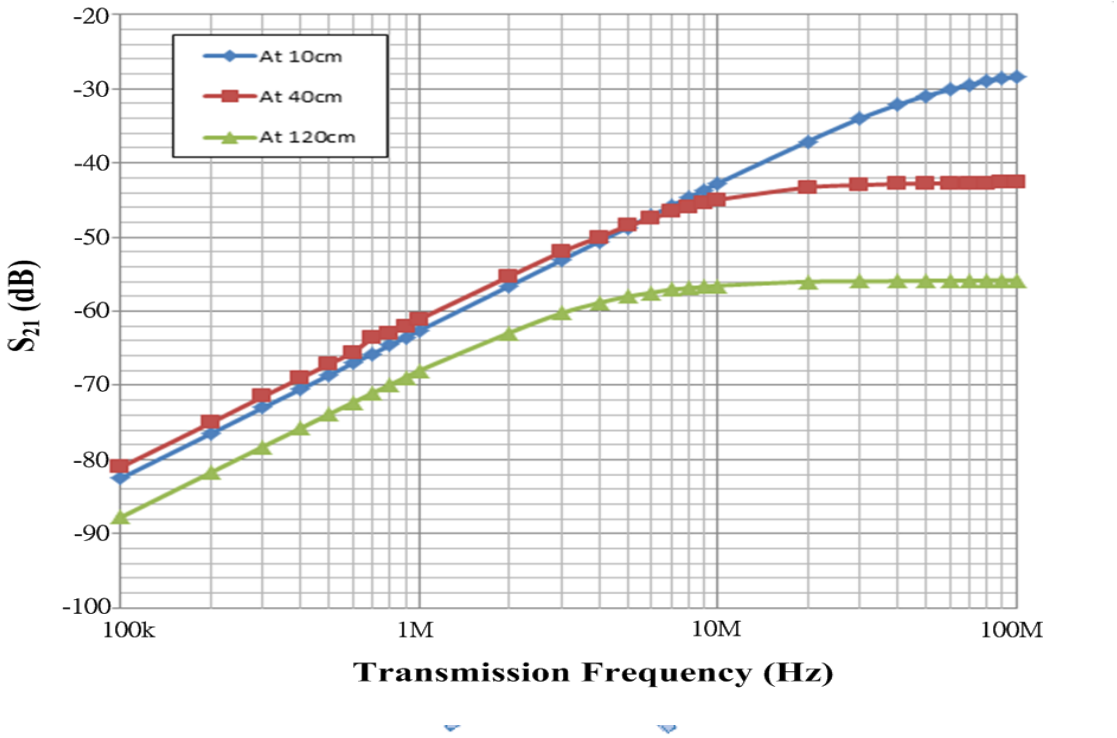


Fig. 1.17: Characteristics of the simple discrete RC model in frequency-domain.

Fig 1.17 shows the characteristics of the human body in frequency-domain thatusesthe proposed simple discrete RC model.In frequency-domain analysis, S_{21} parameter of the simple RC discrete model is measured. The simulation result is similar to the Fig. 1.7(b). The simulation result shows that the body channel model is relatively deterministic below 4 MHz with at most 7 dB of derivation regardless of the distance. However, beyond 10MHz, the length of transmission distance has great impact on the received signal power.

1.4. Survey of Body Channel Communication Transceiver

1.4.1 Basic Components of BCC Transceiver

1.4.1.1 Transmitter

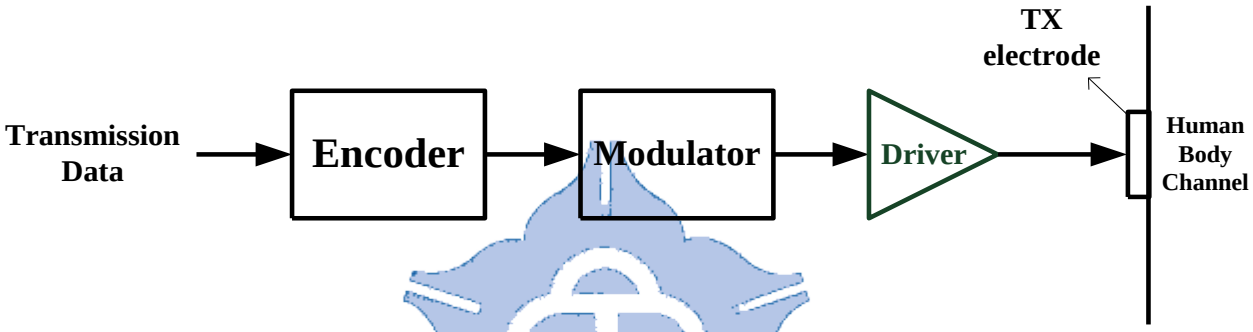


Fig. 1.18: Block diagram of BCC transmitter.

Fig. 1.18 shows the common block diagram of the BCC transmitter. The transmitter consists of an encoder, a modulator, a driver and a transmitter (TX) electrode. When the transmission data is sent from the transmitter, the transmission data is encoded by the encoder, for example, a NRZI encoder, and then is modulated by the modulator, such as FSK modulator, and then through the driver, and finally is sent to the human body channel through the transmitter electrode.

1.4.1.2 Receiver

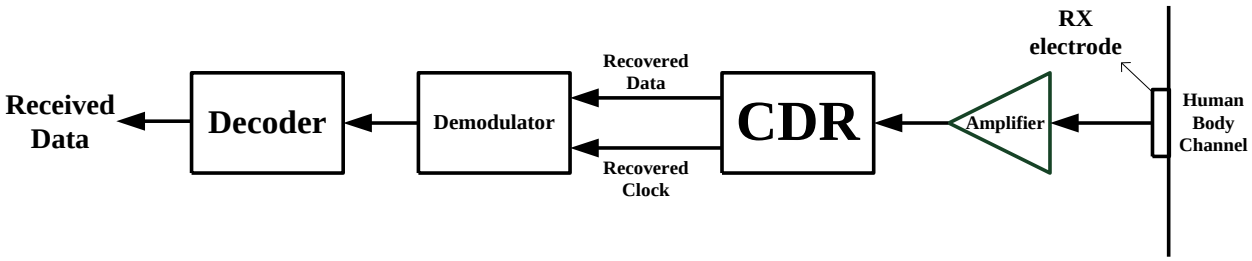


Fig. 1.19: Block diagram of BCC receiver.

Fig. 1.19 shows the common block diagram of the BCC receiver. When the BCC receiver receives the signal from the human body channel, the signal will have huge power attenuation.Thus we amplify the signal amplitude to a normal working voltage by the amplifier. Then, the CDR circuit recoversthe data and the clock.Finally, the demodulator and decoder demodulate and decode the received data.

1.4.2 Conventional BCC Transceiver

1.4.2.1 Near-Field Electrostatic Coupling Scheme

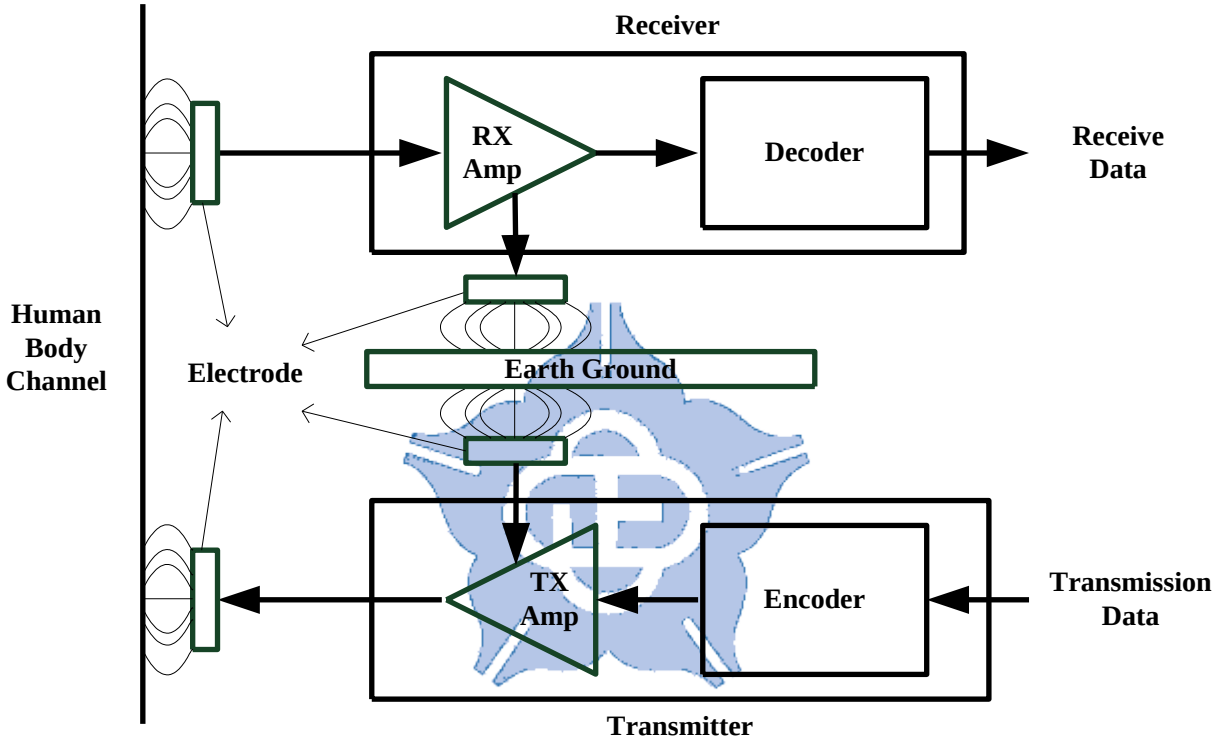


Fig. 1.20 : Block diagram of near-field electrostatic coupling transceiver.

Fig. 1.20 shows the blockdiagram of the near-field electrostatic coupling transceiver. The near-field electrostatic coupling scheme that uses a narrowband low frequency was first introduced by Zimmerman [8]. The transceiver consists of a encoder and a amplifier in the transmitter, and a decoder and a receiver amplifier at the receiver. In addition, there are two electrodes at transmitter and receiver, one alwaysattach on human body skin and another is floated. At the electrodes near the human body, the transmitter capacitive generate a

modulating pico-ampere displacement current through the human body skin to the receiver. At the floated electrodes, we can regard as a return path. In addition, in order to avoid the shorting of the electrostatic coupling transceiver, the floated electrodes must be isolated from the earth ground.

However, the near-field electrostatic coupling scheme still has drawbacks. First, when the near-field electrostatic coupling transceiver is working, the surrounding environment play an important role. The measurement results described previously show that the body skin to the environment degrades the quality of the BCC. Second, the usable narrowband in transmission is 400 kHz [18], [19], and the near-field electrostatic coupling scheme has limitationof data rate of 2.4 kb/s. This kind of data rate dose not enough for advanced multimedia applications.

1.4.2.2 Electromagnetic Wave Scheme

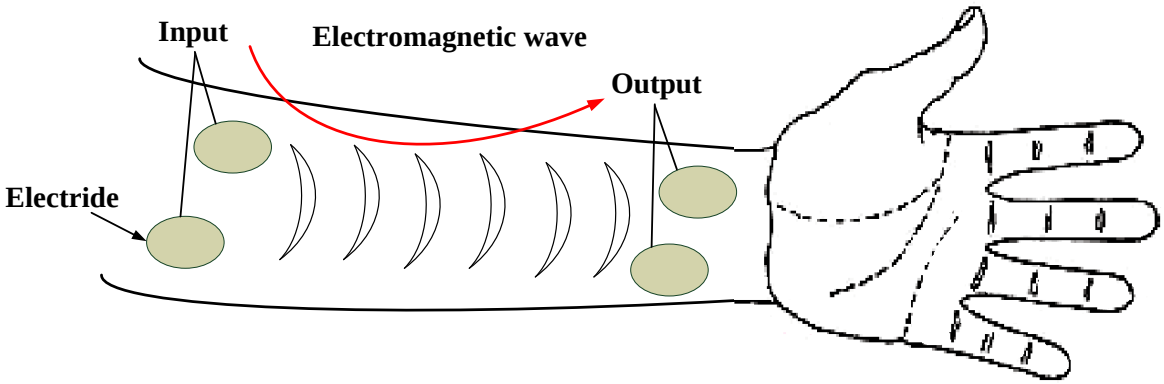


Fig. 1.21: Electromagnetic wave scheme.

Fig. 1.21 illustrates the electromagnetic wave scheme [20]. Similar to near-field electrostatic coupling scheme, there are also two pairs of electrodes. However, these two pairs of electrodes attach on the human body skin to transmit the data. The electromagnetic wave schemehas a faster data rate from 1 Mbps to 40 Mbps than the near-field electrostatic coupling scheme and the pulse voltage of transmission signal is 1 V. Although electromagnetic wave scheme can transmit signal at high-frequency carrier, it is easily interfered by the externalenvironment.

1.4.2.3 Galvanic Coupling Scheme

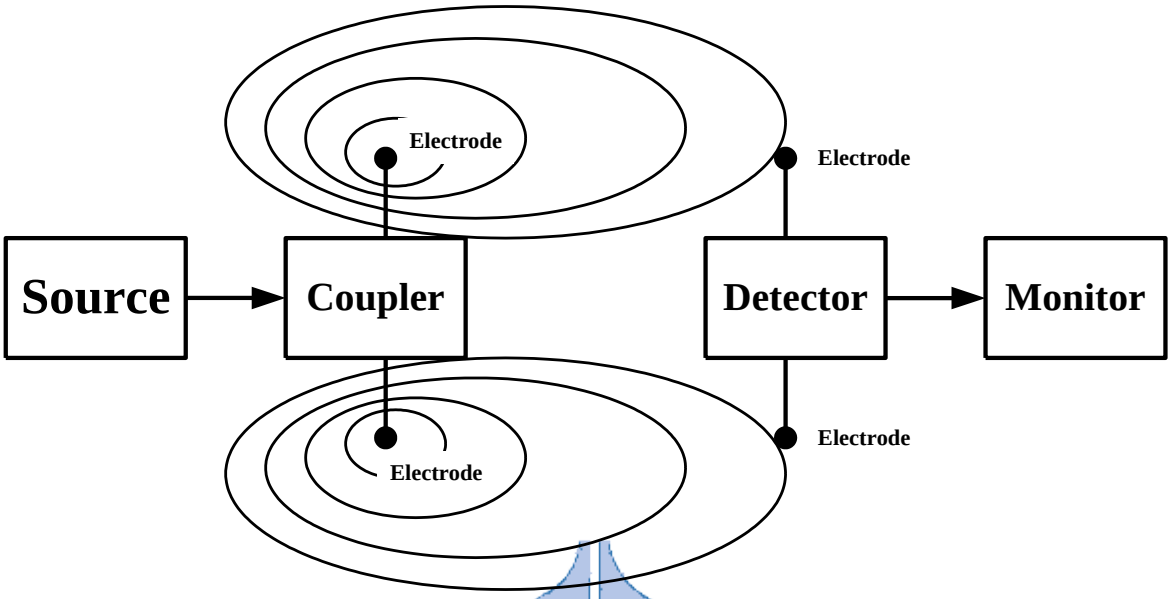


Fig. 1.22: Block diagram of galvanic coupling scheme.

The galvanic coupling scheme was investigated by Oberle [21]. Fig. 1.22 shows the diagram of galvanic coupling scheme [22], [23]. Similar to near-field electrostatic coupling scheme, there are also two pairs of electrodes. The transmission data is applied differential signals at two coupler electrodes and received the differential signal at two detector electrodes. The galvanic coupling scheme has a data rate from 10 kbps to 1 Mbps. However, the coupler transfers the coupling signal currents galvanically about 1 mA into the human body skin. For safety requirements, we can not apply this scheme.

1.4.2.4 Wideband Signaling with Direct-Coupled interface Scheme

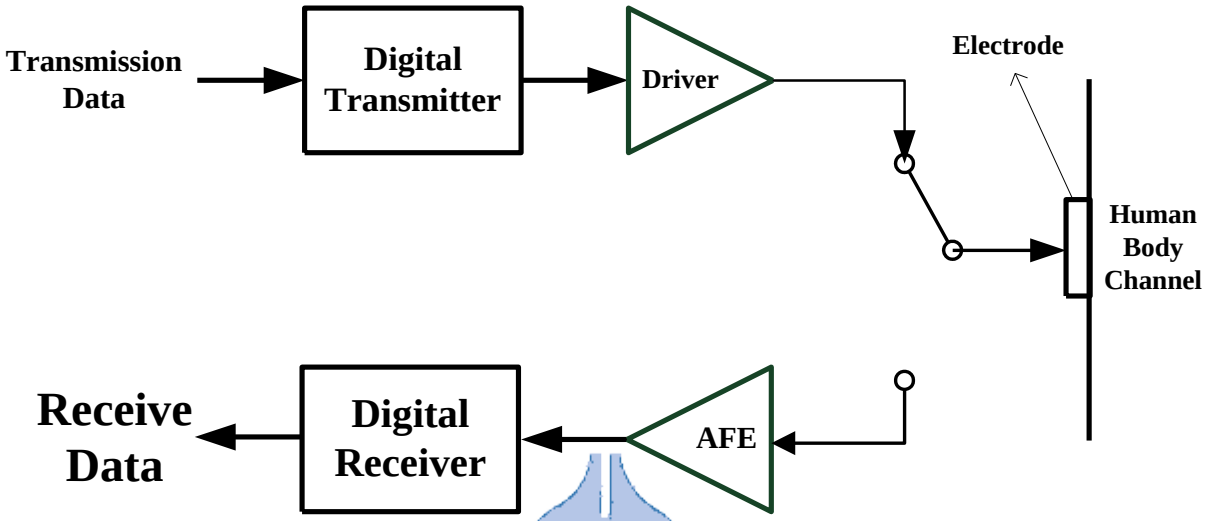


Fig. 1.23: Block diagram of wideband signal with direct-coupled interface.

Fig. 1.23 shows theblock diagram of wideband signal (WBS) with a direct-coupled interface (DCI). The DCI is an interface scheme that the \chip connect the human body skin directly. Thewideband signal scheme is proposed by [24]. The transmitter consists of a digital transmitter and a driver.The receiver consists of a AFE circuit and a digital receiver. Compared to the other BCC schemes described before, the wideband signal scheme uses only one electrode at the transmitter part and the receiver part to transmit the data. Moreover, the wideband signal scheme has a data rate that is up to 40 Mbps so far and the pulse voltage of the transmission data is 1 V that is safe for the human body. The wideband signal scheme can fully integrate all function into a single chip, thus it reduces the physical size and achievesa low cost.

1.4.3 Summary

Table 1.2 summarizes the prior body channel communication transceiver schemes. These schemes all have some advantages and disadvantages. In this thesis, we adopted the wideband signaling transceiver with a direct-coupled interface to increase the data rate. Therefore, the application for the BAN can be greatly extended.

Table 1.2: Conventional BCC transceiver comparisons.

BCC transceiver scheme	**Advantages**	**Disadvantages**
Near-Field Electrostatic Coupling [8]	Low power consumption than RF Small transceiver size than RF	Devices need to be grounded Weakness to interference Low data rate
Electromagnetic Wave [20]	Devices no need to be grounded	Weaknessto interference Low data rate Bulky device
Galvanic Coupling [22]	Devices no need to be grounded	Weaknessto interference Low data rate Bulky device
Wideband Signaling with Direct-Coupled Interface [24]	High data rate Simple interface Low power consumption Highly integration	Complexity of CDR circuit design

1.5 Survey of Conventional CDR Circuit

1.5.1 Requirements of CDR circuit

Because the data will be distorted by some interferences when passing though the HBC. Thus, we need a clock and data recovery (CDR) circuit and a AFE circuit to recovery the distorted data to receive the correct data. As a result, we survey many kinds of CDR architectures, and select a suitable CDR circuit for our applications.

1.5.2 PLL-based CDR circuit

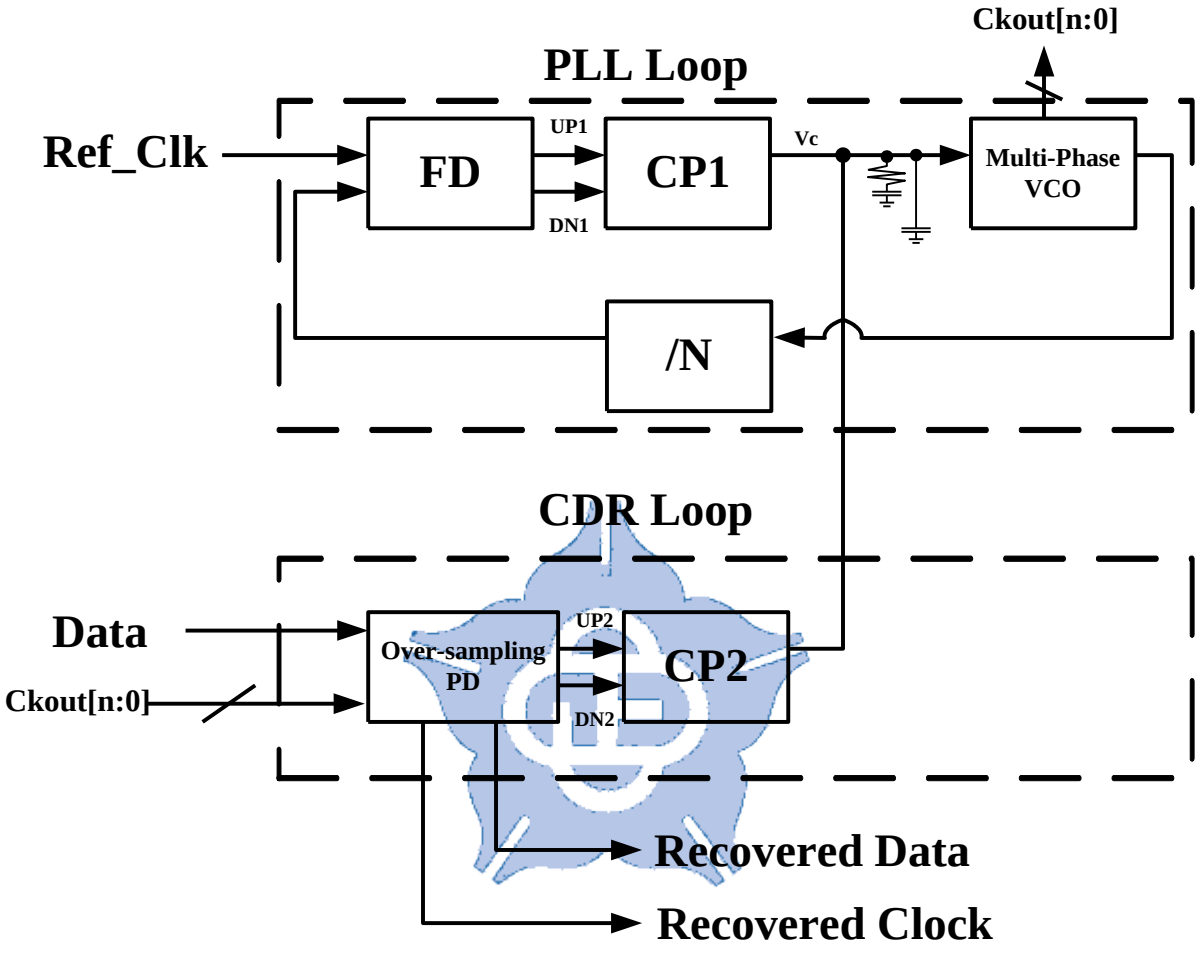


Fig. 1.24: Architecture of the PLL-based CDR circuit.

Fig. 1.24 shows the diagram of the PLL-based CDR circuit [12], [25]. The PLL-based CDR circuit mainly consists of two loops, one is the PLL loop and the other is the CDR loop. First,in the PLL loop, the multi-phase voltage controlled oscillator (VCO) generatesmulti-phase clock signals CKout[n:0] that is usually slower than the recovered clock to save the power consumption of the VCO. Second, in the CDR loop, the over-sampling PD uses the multi-phase clock signals CKout[n:0] to sample the data and

finally generatestherecovered data and therecovered clock. At the same time, the over-sampling phase detector (PD) synchronizes the multi-phase clock signals CKout[n:0] and outputs UP/DN signals.

The advantage of this architecture is the power consumption of the multi-phase VCO is decreased due to the VCO clock rate is reduced to half or quarter of the recovered clock rate. However, there are some disadvantages,for example, the transistor leakage current problem in advanced CMOS process (< 90 nm) and the increased design complexity of the multi-phase clock generation and over-sampling circuit.

1.5.3 Continuous Rate CDR circuit

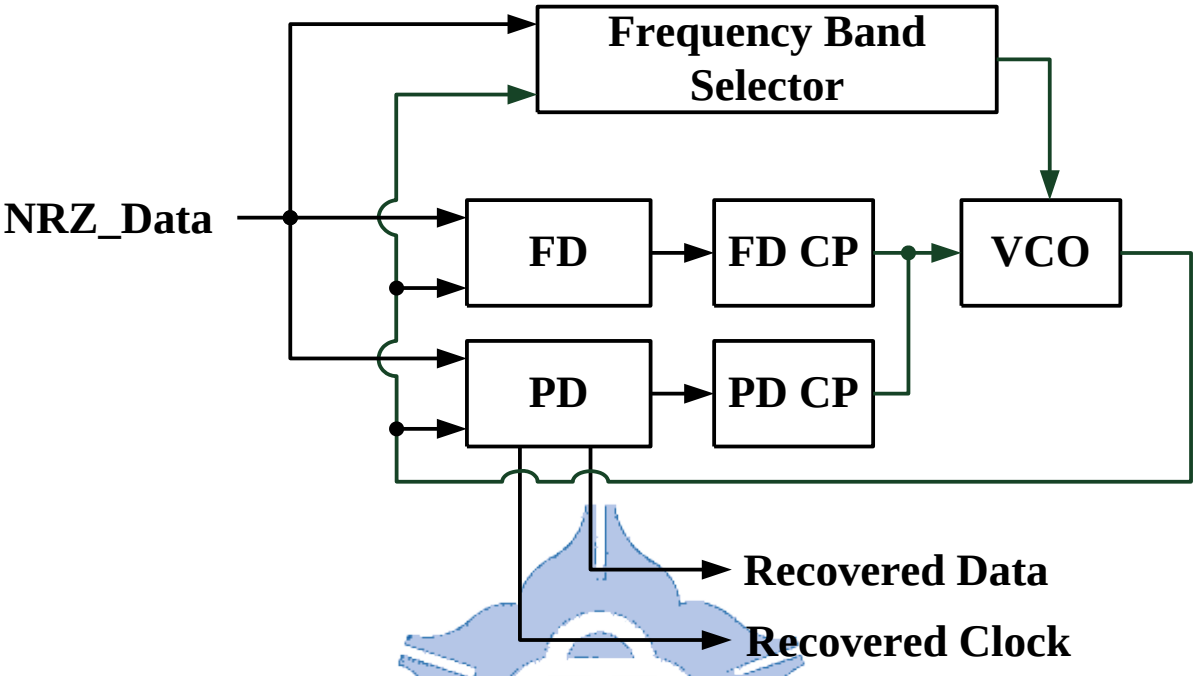


Fig. 1.25: Architecture of the continuous rate CDR circuit.

Fig. 1.25 showsdiagram of the continuous rate CDR circuit. This architecture is broadly used and can continuously track the input data rate [26]-[28]. The continuous rate CDR circuit consists of a frequency band selector, a frequency detector (FD),a phase detector (PD) and a VCO circuit. First, the frequency band selector selects a suitable VCO frequency band that is close to the input data rate. Second, the FD compares the VCO clock and the input data rate and adjusts the VCO clock until the CDR circuit is converged. Third, the PD compares the phase error between the VCO clock phase and the input data transition phase. Finally, we can get the recovered data and the recovered clock after VCO clock synchronizing with the input data.

1.5.4 Phase Interpolator Based CDR circuit

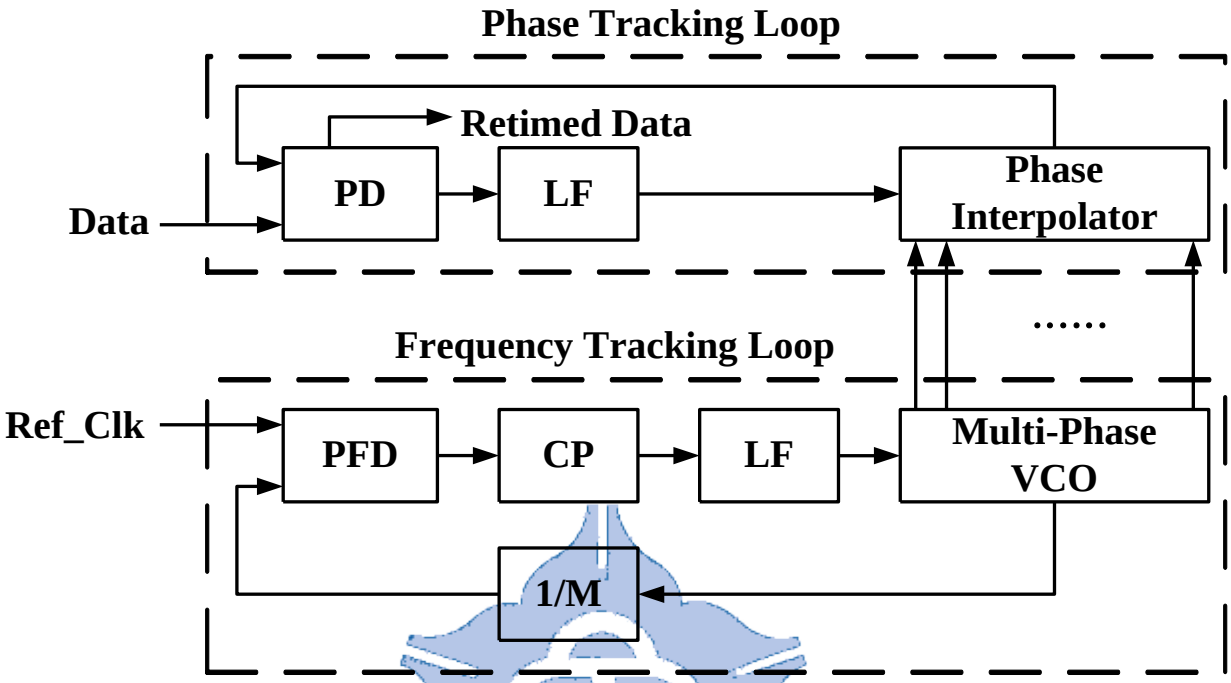


Fig. 1.26: Architecture of the phase interpolator based CDR circuit.

Fig. 1.26 shows the block diagram of the phase interpolator based CDR circuit. Not like the the continuous rate CDR, the phase interpolator based CDR is used in SATA applications [29], [30]. The phase interpolator based CDR can be divided into two parts, one is the phase tracking loop and the other is the frequency tracking loop.First, the frequency tracking loop use the reference clock, Ref_Clk, to generate high speed multi-phase signals and sent these high speed multi-phase signals to the phase interpolator in the phase tracking loop. Second, in the phase tracking loop, the PD compares the data transition phase and the clock from the phase interpolator to adjust the clock from the phase interpolator. Finally, after adjustment, the PD generates a retimed data.

The architecture of the phase interpolator based CDR is very suitable for multichannel data transmission because each channel can share these multi-phase signals. However, it still needsan external reference clock to generate high speed multi-phase signals.

1.5.5 Blind Oversampling CDR circuit

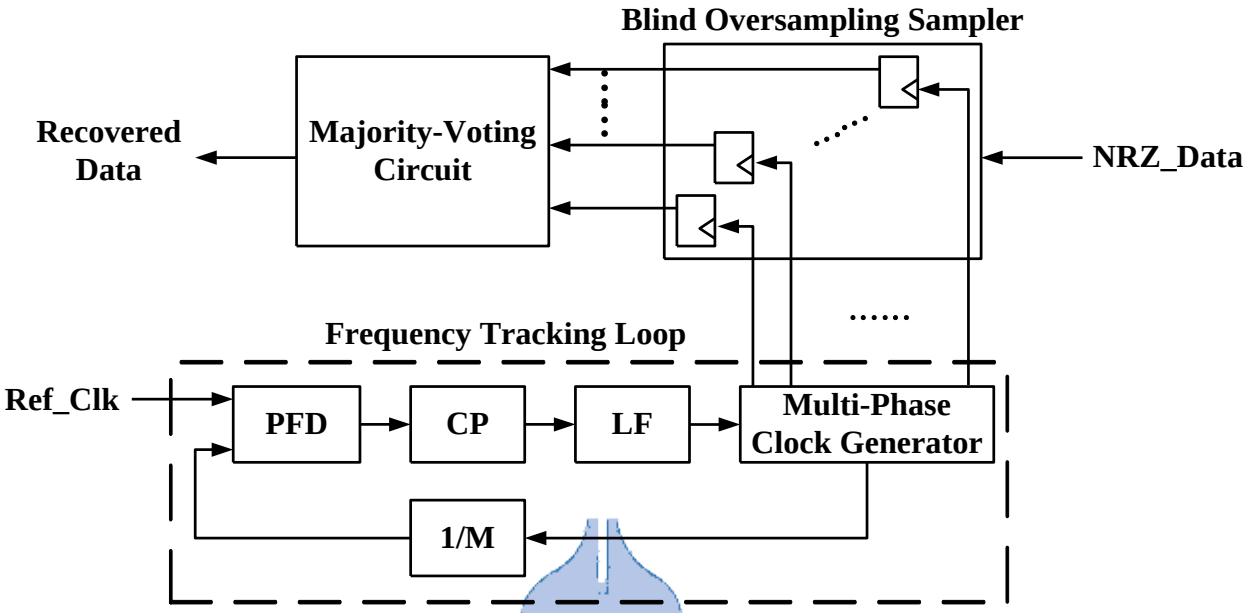


Fig. 1.27: Architecture of the blind oversampling CDR circuit.

Fig. 1.27 shows the block diagram of the blind oversampling CDR circuit [31]-[33].First, the frequency tracking loop uses the external reference clock, Ref_Clk, to generate the multi-phase clocks and sent to the blind oversampling sampler. Second, the blind oversampling sampler samples the input data, NRZ_Data, and sent to the majority-voting circuit. Finally, the majority-voting circuit generates the recovered data.

The architecture of the blind oversampling CDR has no feedback loop to track the phase of input data and has fast phase acquisition ability. However, it still needs an external reference clock and the multi-phase clock generator will havelarger power consumption.

The multi-phase clock rate is usually 2X, 3X, or higher clock rate than the data rate. Generally, the higher sampling clock will achieve better bit error rate (BER) performance.

However,with the higher sampling clock, the blind oversampling CDR circuit will consumes more power consumption.

1.5.6 Summary

Table 1.3: CDR architecture comparison.

CDR Architecture	Advantages	Disadvantages
PLL-based [24]	Ability of tracking input frequency jitter tolerance	Long lock-in time Large loop filter area External reference clock needed Multiphase clocks needed
Continuous rate [26]	Ability of tracking input frequency jitter tolerance No need external frequency	Long lock-in time Complexity of frequency band selector
Phase interpolator [29]	Multichannel can share input clock	External reference clock needed Multiphase clocks needed
Blind oversampling [31]	Fast lock-in Fast acquisition	External Reference clock needed Multiphase clocks needed

Table 1.3 summarizesthe conventional CDR architectures. All of CDR architectures in the table have some disadvantages such as long-lock time, external reference clock needed.

In order to tolerate large jitter effects, we propose anall-digital 7X blind oversampling CDR circuit witha fast lock-in time withouta multi-phase clock generator.We adopt the vote mechanism to recover data. The vote mechanismcan reduce the impact of jitter

accumulation and the AFE circuit duty-cycle distortion. As a result, we can easily recover the transmission data which is suffered from serious attenuation by the human body channel.

Chapter 2

The Proposed Wideband Signaling Transceiver

2.1 The Proposed Wideband Signaling Transceiver Overview

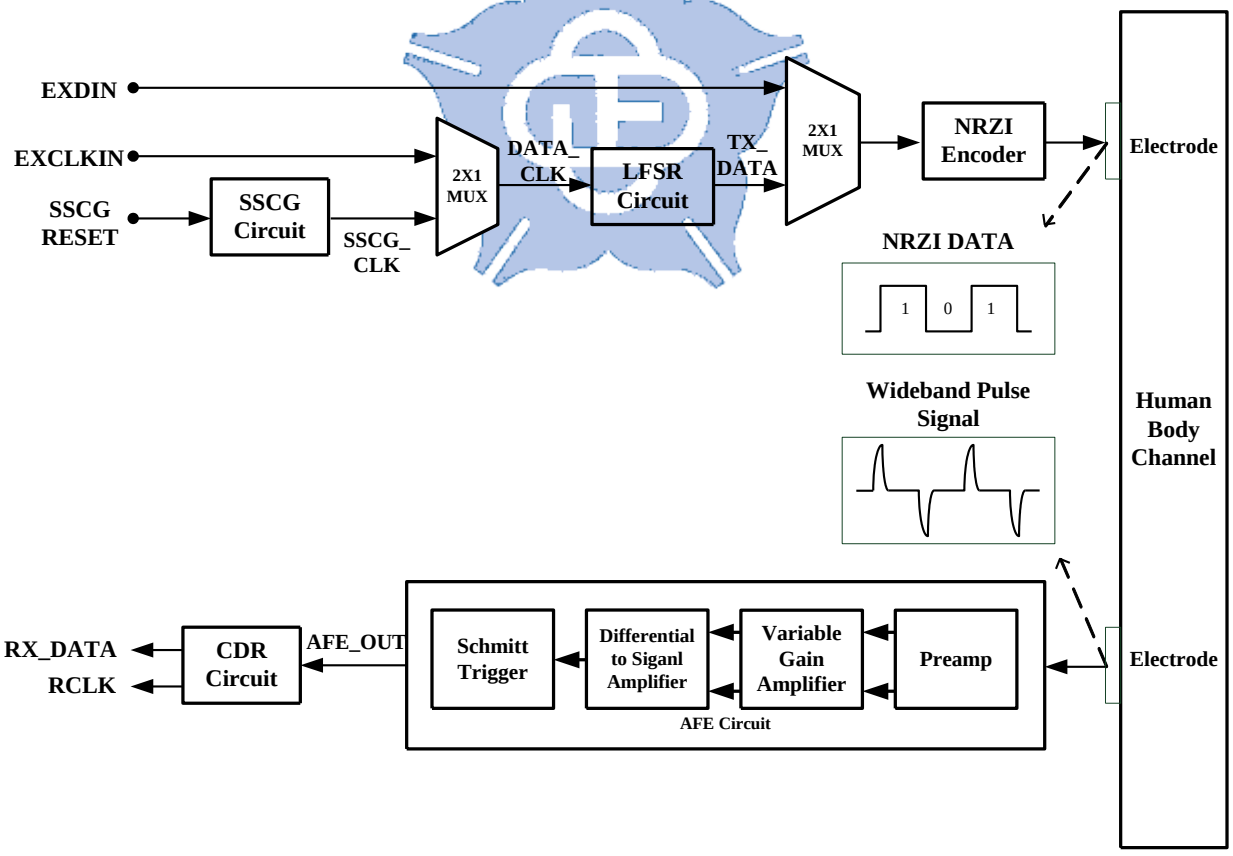


Fig. 2.1 : Proposed wideband signaling transceiver architecture.

Fig. 2.1 shows the block diagram of the proposed wideband signaling (WBS) transceiver. The upper part is the transmitter and the lower part is the receiver. In the transmitter is composed ofspread spectrum clock generator (SSCG) circuit,two 2X1 multiplexers, a linear feedback shift register(LFSR) circuit and a non-return-to-zero(NRZI) encoder. The receiver is composedof there are ananalog front-end(AFE) circuit and a 7X oversampling clock and data recovery (CDR) circuit. First, the SSCG circuit generates the clock signal, SSCG_CLK, to trigger the LFSR circuit. Second, the LFSR circuit generates a series of random pattern, TX_DATA, and sends the TX_DATA signalto the NRZI encoder. Third, the NRZI encoder encodesthe TX_DATA signalinto NRZI format and then transfers the NRZI datato the human body channel. When the AFE circuit receives the wideband pulse signal, the AFE circuit recovers the wideband pulse signal back to the digital square waveforms. Finally, the CDR circuit takes these digital waveformsand recovers the data (RX_DATA) and the clock (RCLK).

The advantages of the WBS scheme include a simple interface, the capability of high data rate and low power consumption.The WBS transceiveris connected to the human body skin through a single metal electrode. In addition, since the WBS scheme is independent of the surrounding environment, the data transmission have little effects by the surrounding environment. However, the body antenna effect is a major impact to the human body channel communication.

According to the study of human body channel, digital square waveform have better performance in different transmission distance and frequency. Comparing with other body channel communication schemes [34]-[37], adopting digital square waveformin transmission reduces the complexity of the transceiver design and more importantly reduces the power consumption of the transceiver.

2.2 Spread Spectrum Clock Generator based Transmitter

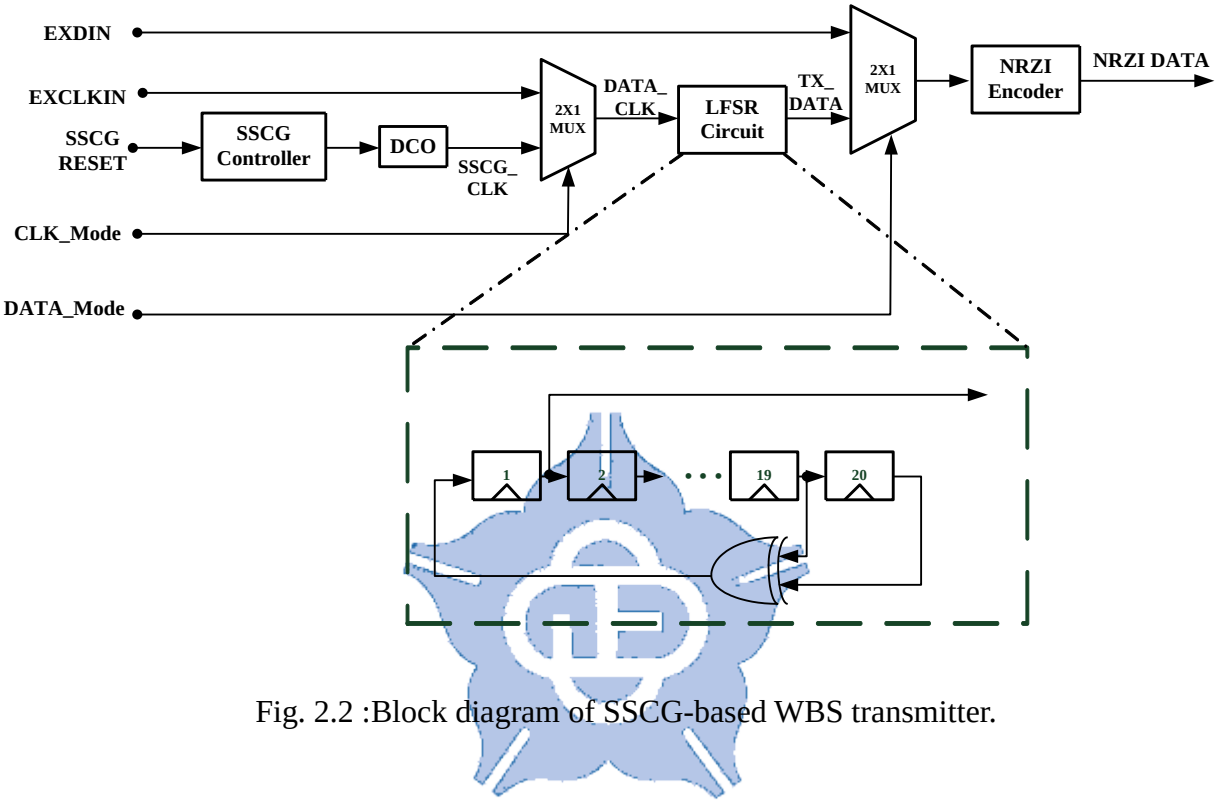


Fig. 2.2 :Block diagram of SSCG-based WBS transmitter.

Fig. 2.2 shows the block diagram of the proposed SSCG-based WBS transmitter. The transmitter consists of a spread spectrum clock controller circuit, a digital controlled oscillator (DCO), two 2-to-1 multiplexers, a linear feedback shift register (LFSR) circuit and a non-return-to-zero(NRZI) encoder.The LFSR circuit is used to automatically verify the bit error rate (BER) and there has a same LFSR circuit in the LFSR checker of the receiver part. The SSCG-based WBS transmitter can directly transmit the digital binary data to the human body skin.

When the SSCG controller is reset, the SSCG controller sends the DCO control code to the DCO. Therefore, the DCO can generate the clock frequency up to 40 MHz

withoutspread spectrum or with spread spectrum.Then the DCO clock triggers the LFSR circuit and the NRZI encoder circuit.

The SSCG circuit is used to reduce the EMI emission. The spreading ratio determines the amount of EMI reduction. The study of conventional SSCG [38] shows that the spreading ratio is chosen smaller than 5000 ppmand the modulation frequency is chosen between 30~33 kHz. However, if the spreading ratio can be higher than or equal to 10%, there will be more EMI reduction. Because of the NRZI encoding at the transmitter and the 7X blind oversampling CDR at the receiver, the maximum spreading ratio (α) can be up to 10% in the proposed design. Therefore, we set the spreading ratio (α) up to 10% and the modulation frequency is 30 kHz. The output frequency with spread spectrum at 40 MHz is from 38 MHz to 42 MHz.

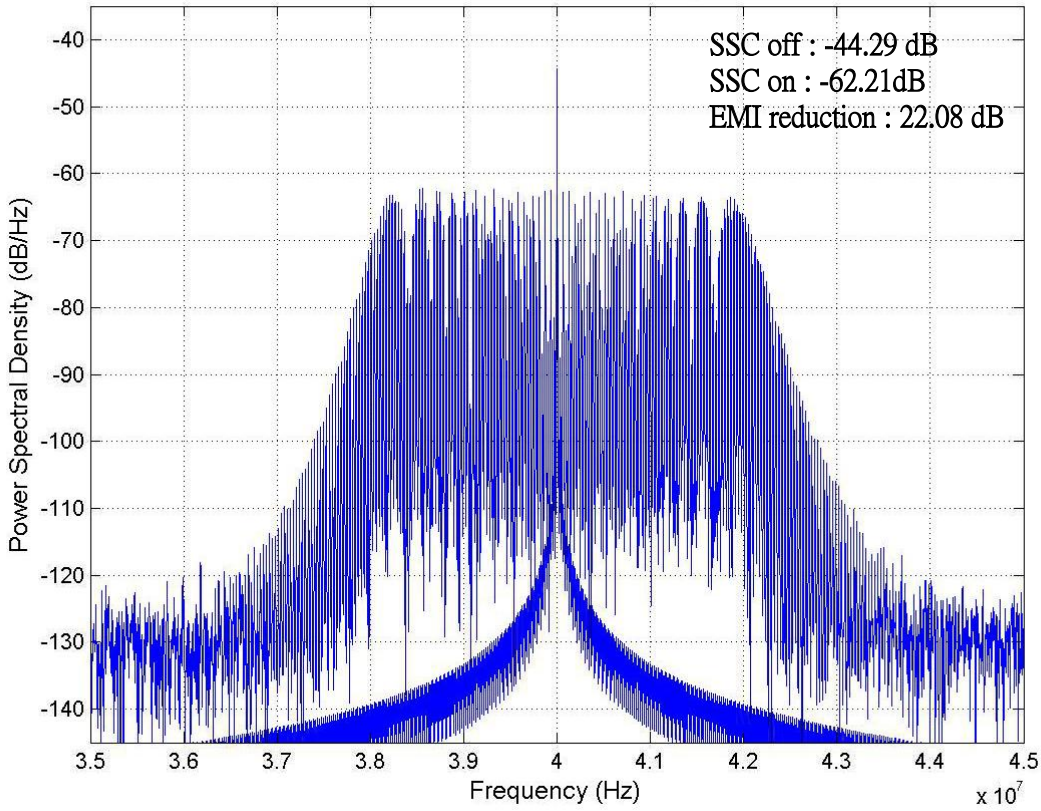


Fig. 2.3: Simulated power spectrum density at 40MHz with 10% spreading ratio.

Fig. 2.3 shows thesimulated power spectrum density of the SSCG_CLK at 40MHz with a 10% spreading ratio. The peak power of the SSC_CLK at 40 MHz without spread spectrum is -44.29dB. The peak power of the SSC_CLK with spread spectrum is -62.21dB. Therefore, the EMI reduction is 22.08dB.

As shown in Fig. 2.2, the linear feedback shift register (LFSR) circuit consists twenty registers and a XOR circuit to generate random patterns that the longest consecutive identical digits (CID) is 20 and about every 10^6bits random patternswill repeat again. However, the CID causesno data transitions, and the less data transitions will increase the difficulty of recovery databecause of the jitter accumulation and the AFE duty-cycle distortion. Therefore, we add the non-return-to-zero (NRZI) encoder at the transmitter. The

purpose of NRZI encoder with bit stuffing is to make more transitions.The function of NRZI encoder is described below. When the TX_DATA is "0", the NRZI encoder will reverse the previous NRZI_DATA. When the TX_DATA is "1", the NRZI encoder will keep the previous NRZI_DATA. However, for avoiding the long length of CID "1" of TX_DATA,the NRZI encoder will check the pattern of TX_DATA and insert a "0" after five continuous "1". As a result, the NRZI encoder with bit stuffing will make more data transitions and make sure that the maximum CID is 6 at NRZI_DATA.

2.3 Oversampling based Receiver

2.3.1 Analog Front-End Circuit

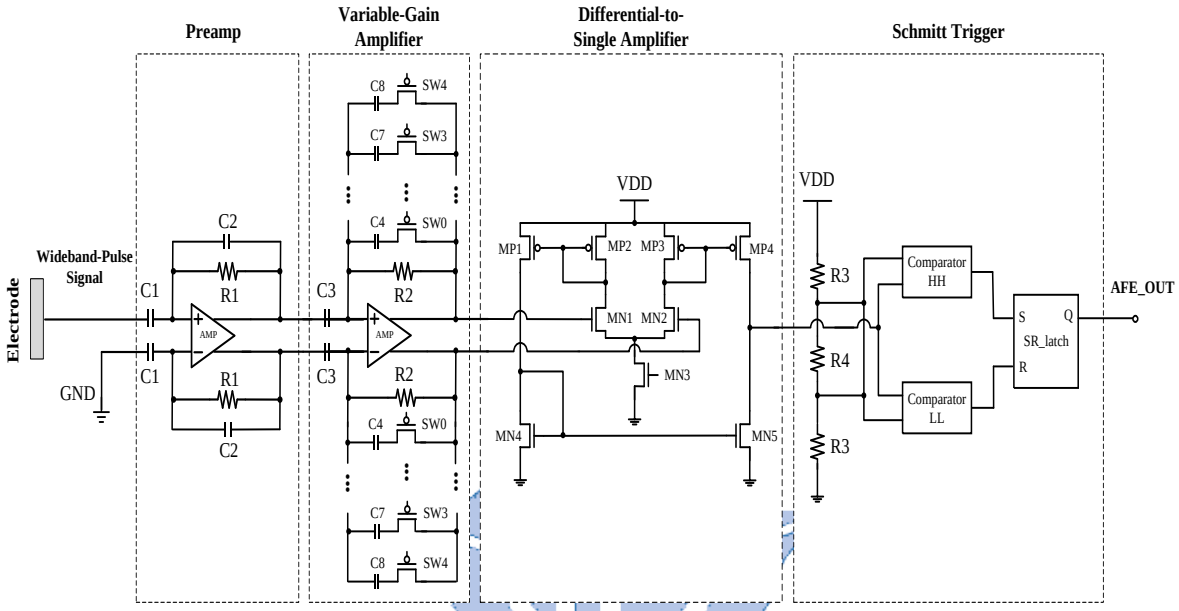


Fig. 2.4: Architecture of the analog frontend circuit.

Fig. 2.4shows the architecture of the analog front-end (AFE) circuit.The AFE circuit consists of a preamplifier circuit and a variable gain amplifier circuit and a differential to single-end amplifier circuit and a Schmitt trigger circuit. The AFE circuit can accept input frequency range of wideband pulse signal from 1 MHz to 40 MHz. The AFE circuit can amplifythe wideband pulse signal with the amplitude from 50 mV to 125 mV and filter out the noise about 15 mV to 25 mV at the same time.

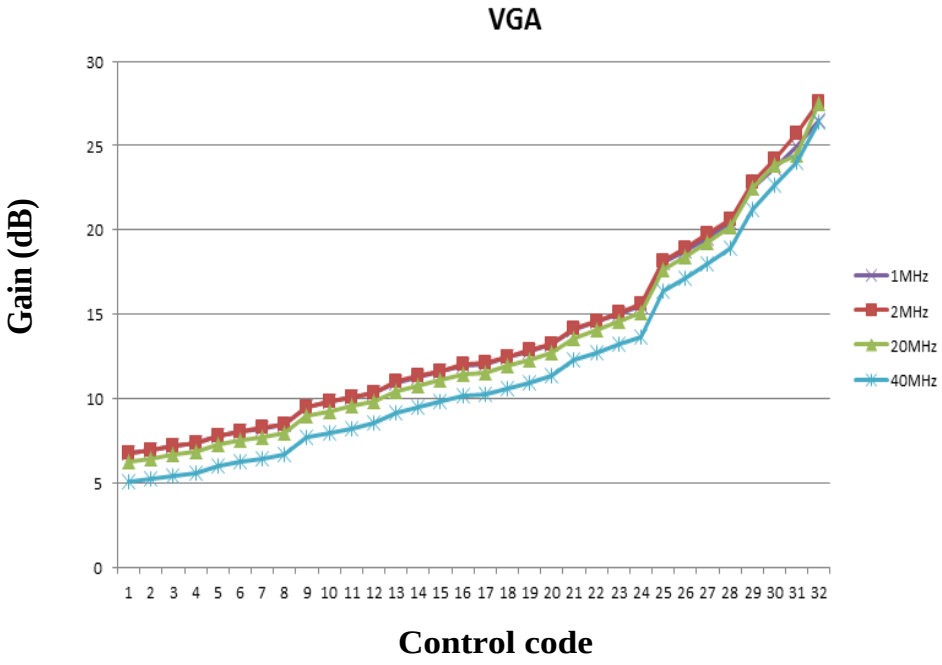


Fig. 2.5: VGA amplified gain.

The gain of the variable gain amplifier circuit is controlled by the CDR circuit. Therefore, the CDR circuit uses the digital control codeto control the variable gain amplifier and amplifies the wideband pulse signal such that the differential to signal amplifier circuit and the Schmitt trigger circuit can recover the correct digital square waveforms. As shown in Fig. 2.5, the variable gain amplifier circuit can achieves a gain tuning range from 5 dB to 28 dB.

Data rate	WBS peak	VGA gain	VDC	VDC1	VDC2	VHH	VLL
1Mbps	±130mV	0-28	0.4V	0.5V	0.6V	0.6V	0.5V
2Mbps	±80mV	0-23	0.4V	0.4V	0.6V	0.6V	0.5V
20Mbps	±40mV	20-28	0.4V	0.4V	0.6V	0.6V	0.4V
40Mbps	±50mV	28-31	0.4V	0.4V	0.6V	0.6V	0.4V

Table 2.1 : AFE circuit simulation results.

Table 2.1 shows the AFE circuit simulation results. The signal VDC, VDC1, VDC2, VHH and VLL is the working voltage of the AFE circuit. Every signal VDC, VDC1, VDC2, VHH and VLL have five voltage controlled switches to control the value of signal VDC, VDC1, VDC2, VHH and VLL in the AFE circuit that is the signal 03V, 04V, 05V, 06V and 07V and these signals represent 0.3V, 0.4V, 0.5V, 0.6V and 0.7V generated by the AFE circuit. All of these voltage controlled switches can be controlled by the digital circuit. The signal VGA gain is the gain of the variable gain amplifier circuit that the value of gain can be controlled by the digital circuit. The WBS peak is the simulated input WBS signal voltage. For example, as shown in signal WBS of the Fig.2.6 the WBS peak is ± 80 mV and the data rate is at 2 Mbps. Therefore, the signal VDC, VDC1, VDC2, VHH and VLL are set to 0.4V, 0.4V, 0.6V, 0.6V and 0.5V that have the best recovery performance as shown in the signal AFE_OUT of Fig. 2.6.

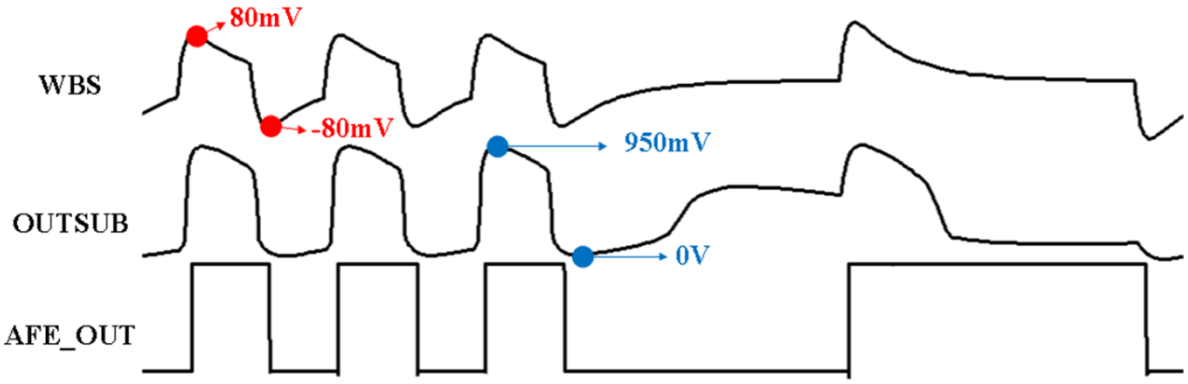


Fig. 2.6: Simulated waveform of the AFE circuit at 2 Mbps.

Fig. 2.6 shows the simulated waveform of the AFE circuit at 2 Mbps. When the signal WBS put into the AFE circuit, the peak voltage of WBS is ± 80 mV. Then, the recovery signal OUTSUB after the differential to single amplifier will amplify the peak voltage up to 950 mV. Finally, the Schmitt trigger will recover the signal AFE_OUT.

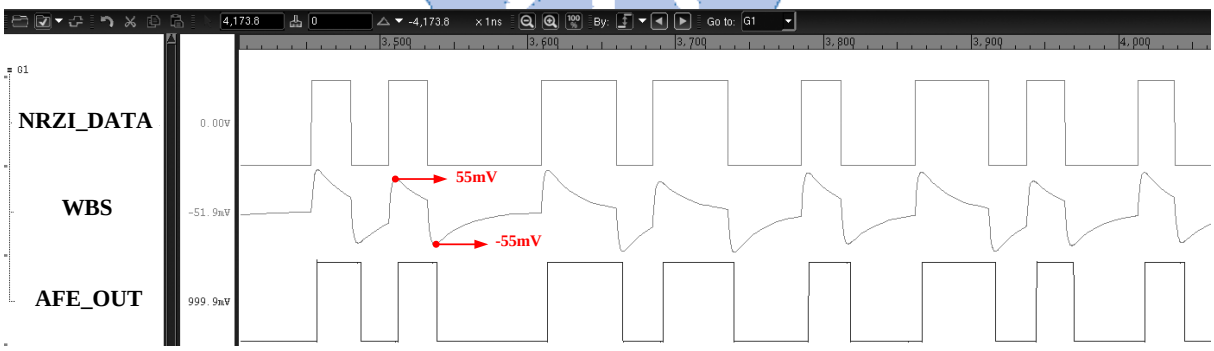


Fig. 2.7: Simulated waveform of the AFE circuit at 40 Mbps.

Another example, Fig. 2.7 shows the simulated waveform of the AFE circuit at 40 Mbps. As described previously, the signal VDC, VDC1, VDC2, VHH and VLL are set to 0.4V, 0.4V, 0.6V, 0.6V and 0.4V that have the best recovery performance as shown in the signal AFE_OUT of Fig. 2.7.

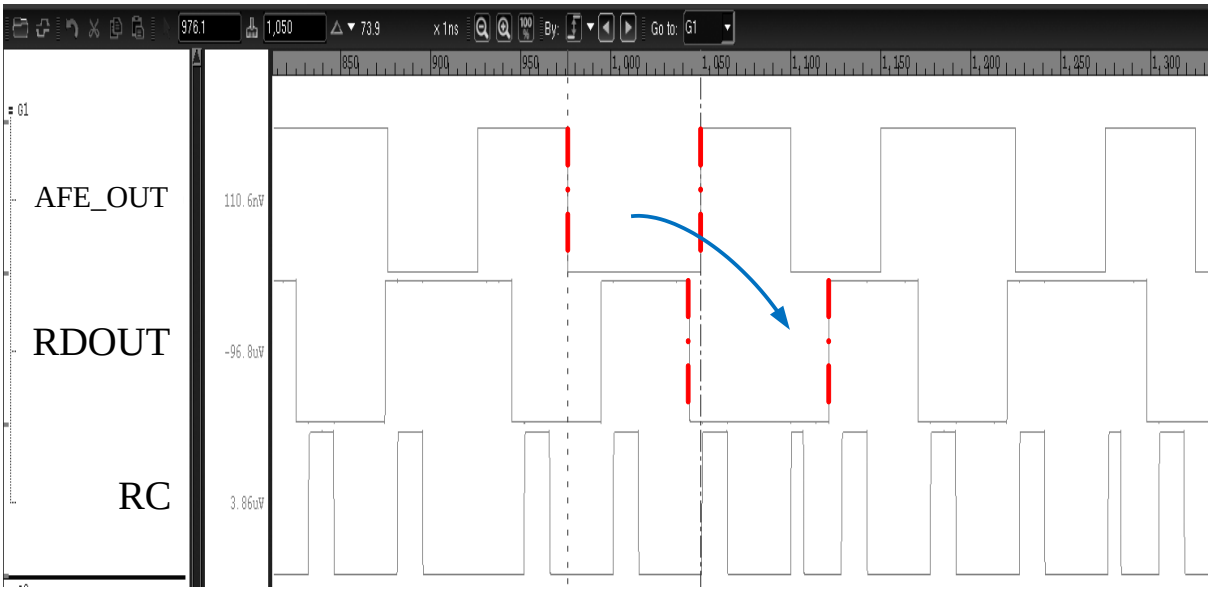


Fig. 2.8: Simulated waveform of the proposed CDR performance with AFE_OUT upper bound duty distortion at 20 Mbps.

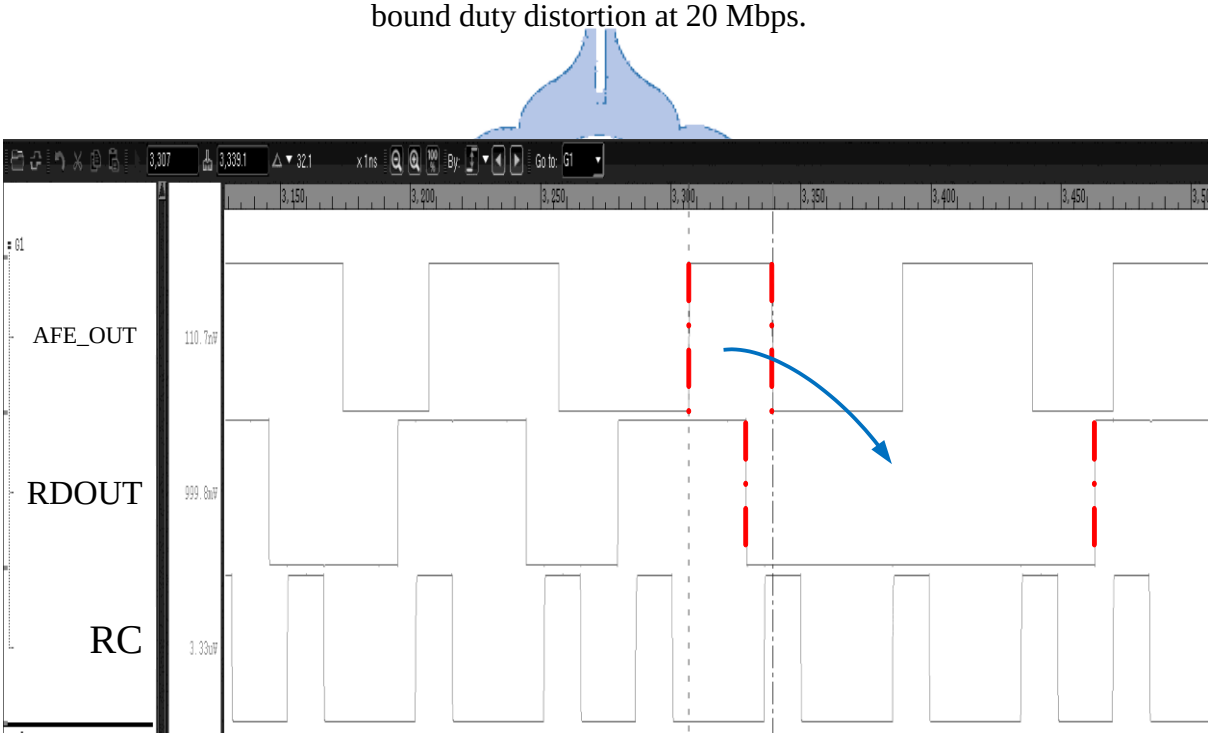


Fig. 2.9: Simulated waveform of the proposed CDR performance with AFE_OUT lower bound duty distortion at 20 Mbps.

However, another issue is the range of recovery distortion of AFE circuit that the proposed CDR circuit can recover correct waveform. For example, when the AFE circuit receives a standard 20 MHz clock waveform. Because there are the jitter accumulation and the recovery distortion of the AFE circuit. As shown in the Fig. 2.8, there is one "0" in signal AFE_OUT that is extended from 50 ns to 73 ns. Therefore, the duty cycle is from 50% to 73% (= 73 ns / (50 ns + 50 ns)) and the proposed CDR circuit recovers two "0". As shown in the Fig. 2.9, there is one "1" in signal AFE_OUT that is compressed from 50 ns to 33 ns. Therefore, the duty cycle is from 50% to 33% (= 33 ns / (50 ns + 50 ns)) and the proposed CDR circuit will ignore this "1". Most important is that there are the same CDR performance at 1MHz, 2MHz, 40MHz.

2.3.2 7X Blind Oversampling CDR

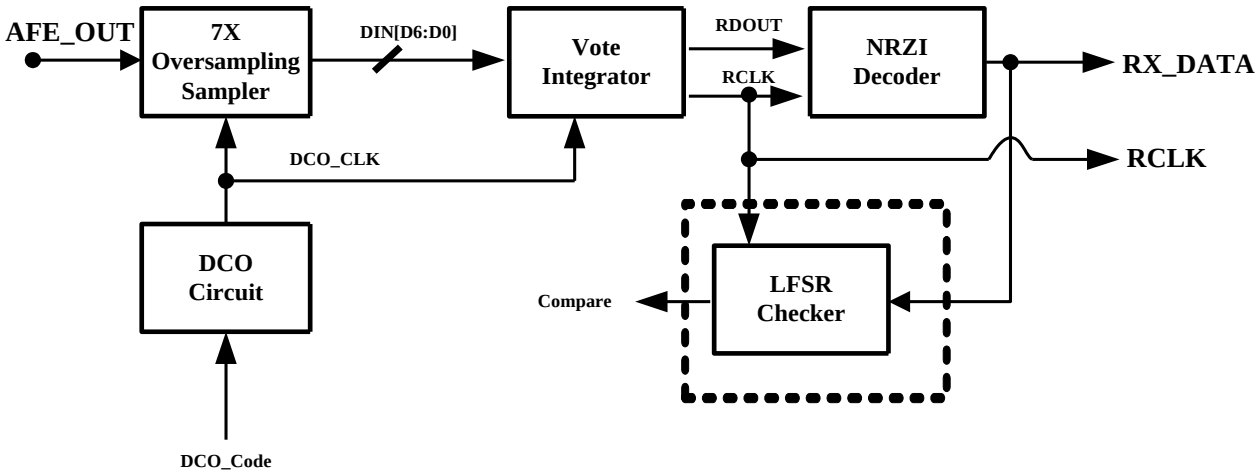


Fig. 2.10 : Block diagram of the proposed 7X oversampling CDR circuit.

Fig. 2.10 shows the block diagram of the proposed 7X oversampling CDR circuit.The proposed 7X oversampling CDR circuit consists of a 7X oversampling sampler, a vote integrator, a DCO circuit, a NRZI decoder and a LFSR checker.

The AFE circuit recovers the wideband pulse signal to the digital square waveform, AFE_OUT, and sends the AFE_OUT to the 7X oversampling sampler.The external input DCO control code, DCO_Code, controls the DCO circuit and generates a 280 MHz frequency, DCO_CLK, to the 7X oversampling sampler and the vote integrator.The 7X oversampling sampler samples the AFE_OUT and there are 7 sample points in a symbol period.Thus the 7X oversampling sampler outputs the 7 sample data signals, DIN[D6:D0],and sends the DIN[D6:D0] to the vote integrator. The vote integrator uses the DIN[D6:D0] to integrate values from the DIN[D6:D0] and generates the recovery data, RDOUT, and the recovery clock, RCLK.Because the RDOUT is NRZI encoded data, the RDOUT must be decoded to the original data, RX_DATA.In order to compare the RX_DATA in the receiver part and the TX_DATA in the transmitter part, the same LFSR

circuit of the transmitter is put in the LFSR checker tocheck whether the RX_DATA is the same as the TX_DATA. When the RX_DATA is exactly the same as the TX_DATA, the "Compare"signal that is output of the LFSR checker will be "0". If the RX_DATA is not equal to the TX_DATA, the "Compare"signal will be "1".

2.3.2.1 Integration Method

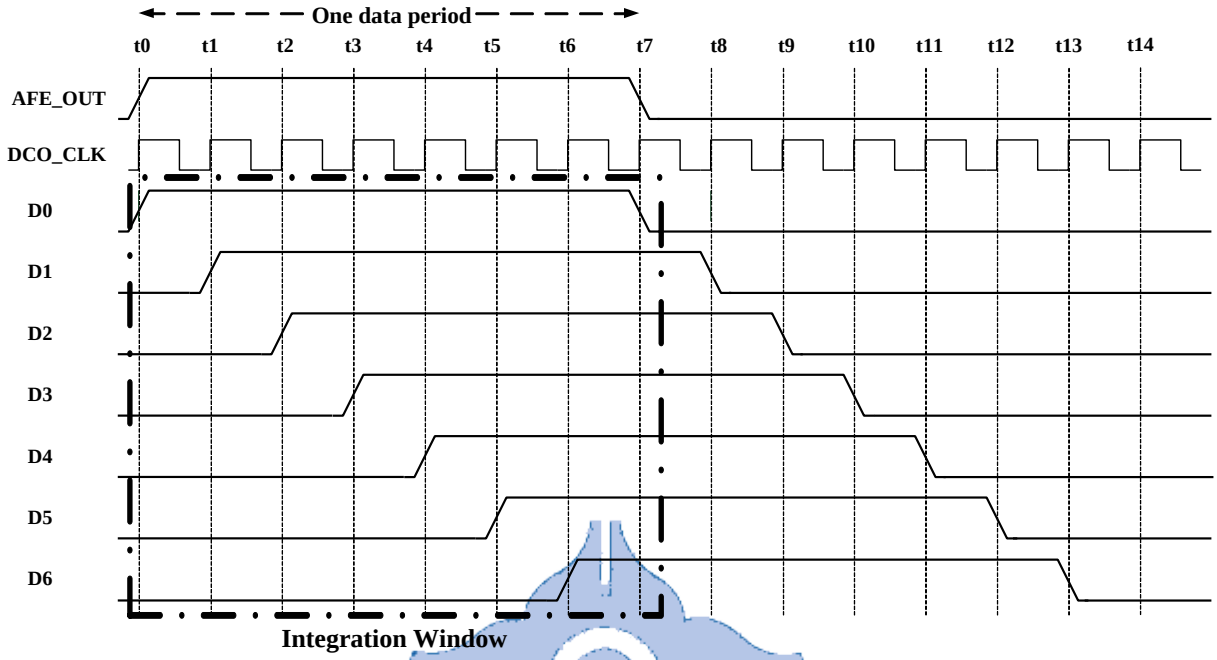


Fig. 2.11 :Timing diagram of integration window of the vote integrator .

The 7X oversampling sampler samples seven data points in one symbol period and outputs the DIN[D6:D0] signals, as shown in Fig. 2.11. Subsequently, the DIN[D6:D0] signals are sent to the vote integrator. In the vote integrator, it creates an integration window, as indicated in Fig. 2.11. The voltage integrator counts the number of "1" inside the integration window, and the maximum value of the integrator output is 49=(7X7). As shown in Fig. 2.12, when the value of the integrator has a rise transition over the threshold line, the RDOUT signal is set to "1". When the value of the integrator has a fall transition through the threshold line, the RDOUT signal is set to "0". The threshold value is set to the half of the maximum value of the integrator output.

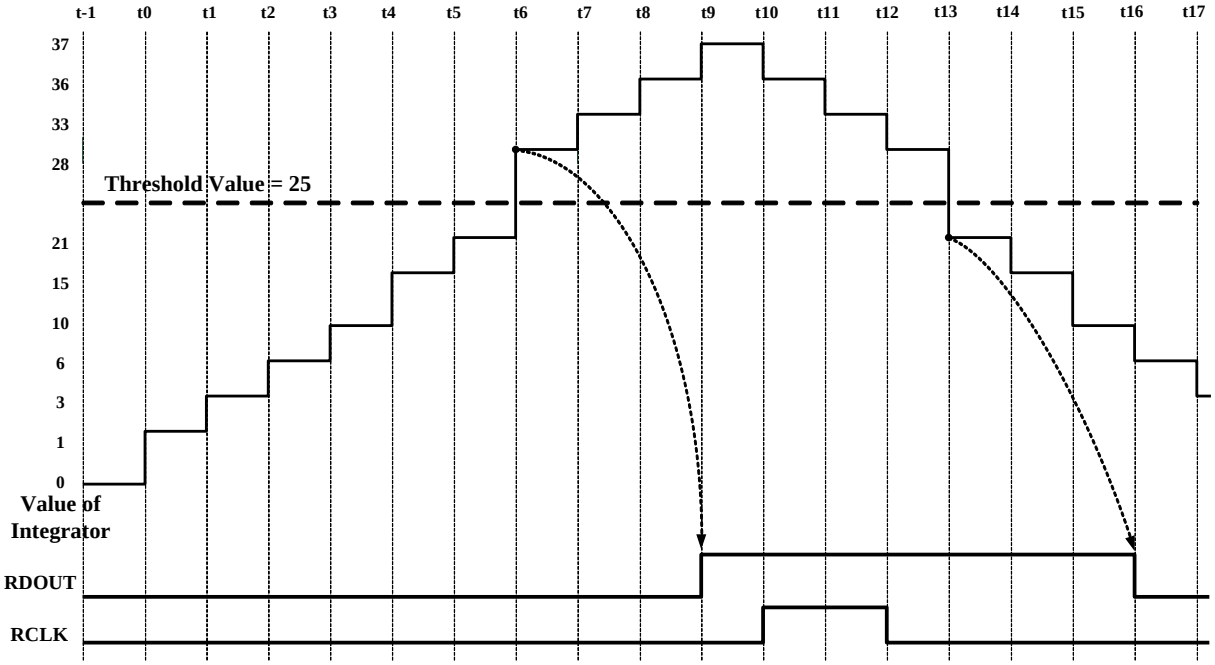


Fig. 2.12 :Clock and data recovery from the value of the integrator.

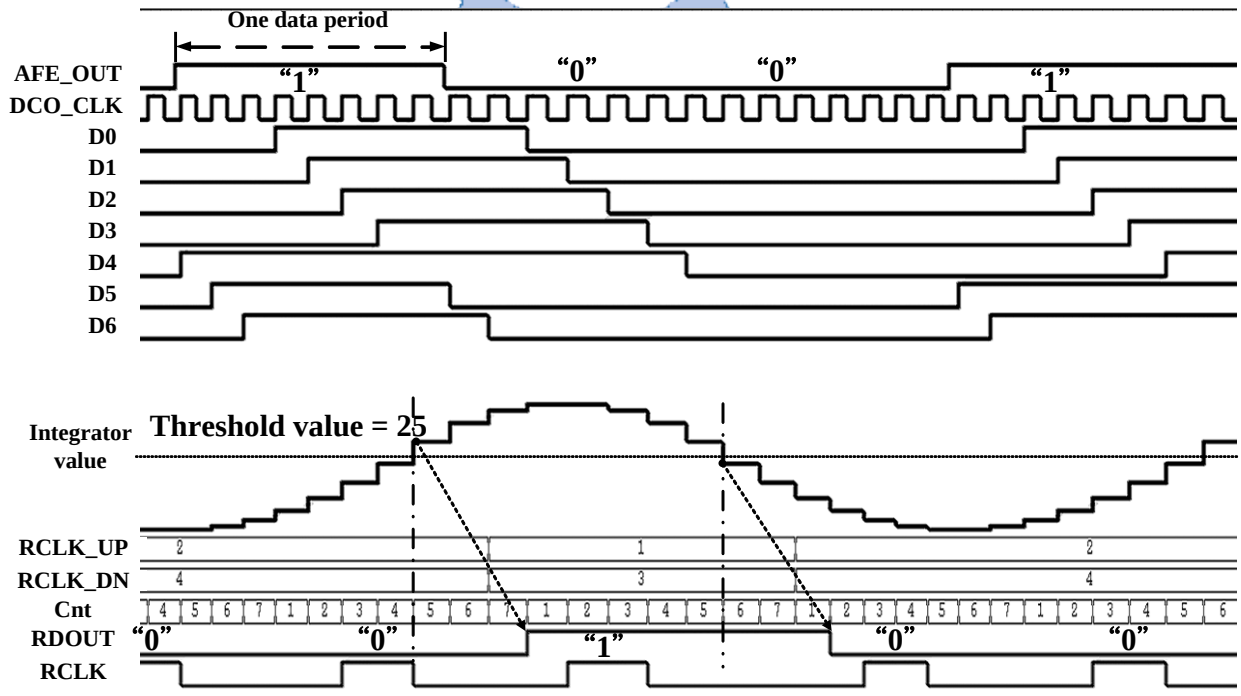


Fig. 2.13 : Simulation waveform of the vote integrator.

Fig. 2.13 shows the simulation waveform of the vote integrator. Because of the jitter accumulation and phase asynchronization between the transmitter and receiver, the waveform of sample points D0~D6 is not like the waveform in Fig. 2.11 that is an ideal situation.

It takes three clock cycles to calculate the RDOUT signal and the RCLK signal. Whenever there has a rise or fall transition over the threshold line, the data clock position (RCLK_UP and RCLK_DN) is updated by the value of Cnt signal. For example, as shown in Fig. 2.13, at the first rise transition of the integrator value, the value of Cnt signal is 5. Then, the RCLK_UP and RCLK_DN are updated as 1=((5+3) mod 7) and 3=((5+5) mod 7), respectively. Similarly, at the first fall transition of the integrator value, the value of Cnt signal is 6, and then, the RCLK_UP and RCLK_DN are updated as 2 and 4, respectively. Finally, when the Cnt value is equal to the RCLK_UP value, the RCLK is set to “1”, and when the Cnt value is equal to the RCLK_DN value, the RCLK signal is set to “0”. The proposed vote integrator can tolerate large frequency drift or random jitter in the AFE_out signal, and therefore, the maximum frequency drift can be up to 24,000 ppm with 2.5ns peak-to-peak jitter at 40Mbps.The NRZI decoder receives the RDOUT signal andthe RCLK signal and outputs RX_DATA signal. The LFSR checker is for error free measurement. It generates the random pattern sequence which is equal to the LFSR circuit in the transmitter part. Therefore, we can detect if there has bit errors in the recovered data (RX_DATA).

Comparing with the traditional PLL-based CDR, the proposed 7X blind oversampling CDR have some advantages. ThePLL-based CDR requires constantly tracking the phase and frequency of the data depending on the data transitions. If there has noise interferences, the data will have large jitter in a short period. Therefore, the PLL-based CDR needs many clock cycles to relock the phase and frequency of the data and causes worse BERperformance.However, the proposed 7X blind oversampling CDR does not use many

clock cycles to track the phase and frequency of the data. In addition, the proposed 7X blind oversampling CDR uses the vote mechanism to improve BER performance.

2.4 Digital Controlled Oscillator

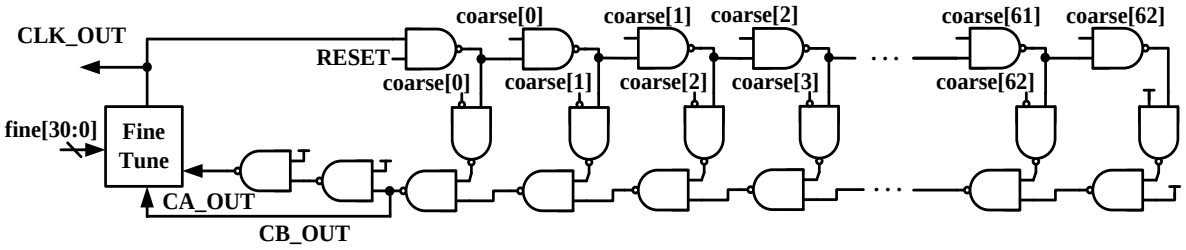


Fig. 2.14: Coarse tuning stage of DCO.

Fig. 2.14 shows the ring type DCO architecture that is constructed by a coarse-tuning delay line and a fine-tuning delay line [39]. We adopt this DCO architecture in the SSCG and the CDR. In addition, The DCO in the SSCG have a frequency divider to divide the DCO output frequency and output the desired frequency. The coarse-tuning delay line consists of 64 coarse-delay cells (CDC),and each CDC consists of three NAND-gates. We use the coarse-tuning code to enablesomeCDC circuits and disable unused CDC circuits. Therefore, the coarse-tuning code is used to select the delay path and output the requiredclock. Besides, in order to enhance the resolution of DCO, there are two signals CA_OUT and CB_OUT are fed into the fine-tuning circuit to perform interpolation.

Fig. 2.15 shows the fine-tuning stage architecture. This fine-tuning circuit is designed with interpolating scheme [40]. The fine-tuning circuit consists of two parallel tri-state buffer arrays, and sets different states to interpolate an appropriate output clock phase. The fine-tuning circuit divides one coarse-tuning delay time into 32 parts and is controlled by the fine-tuning code. The delay time difference of CA_OUT and CB_OUT is equal to one CDC delay time, when more tri-state buffers in the left hand side are turned on, the output

clock (CLK_OUT) is more closed to CA_OUT. Oppositely, if more tri-state buffers in the right hand side are turned on, the output clock is more closed to CB_OUT.

The fine-tuning circuit can provide a fine resolution sampling clock for the sampler, the more accurate sampling clock can reduce the frequency drift problem between the transmitter and the receiver.

Fig. 2.16 shows the simulation result of the DCO control code versus period with PVT variations, and the range and step of each stage is shown in Table 2.1.

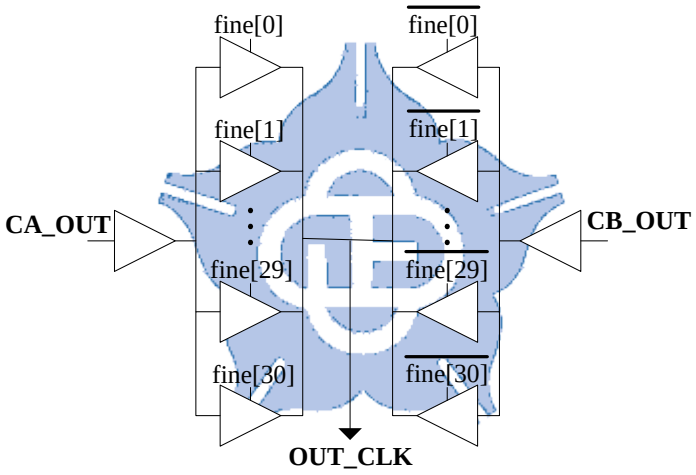


Fig. 2.15: Architecture of interpolating fine-tuning circuit.

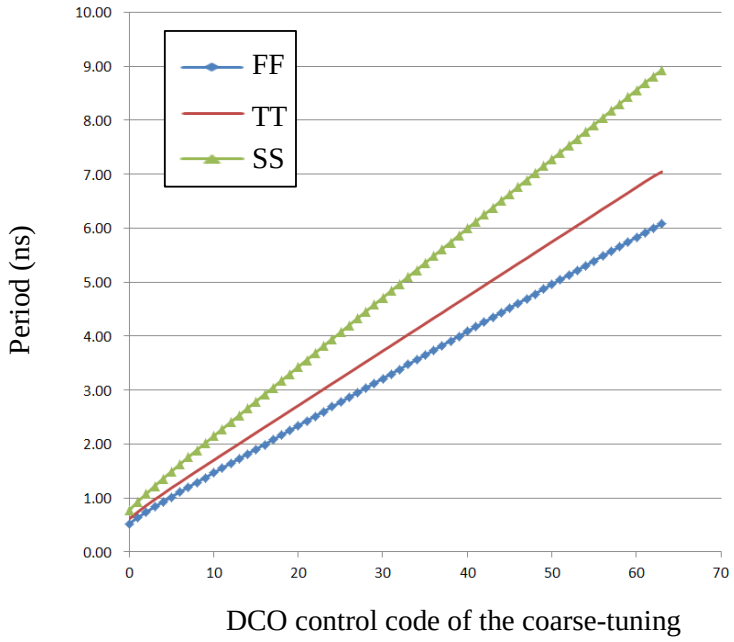


Fig. 2.16: DCO delay line simulation with PVT variations.

Table 2.2: Coarse/Fine step in PVT variations

PVT corner	Slow Case	Typical Case	Fast Case
	Step	Step	Step
Coarse tune stage	129.4 ps	102 ps	88.1 ps
Fine tune stage	4.04 ps	3.18 ps	2.75 ps
Output frequency	77MHz~1300MHz	141MHz~1632MHz	164MHz~1903MHz

Chapter 3

Experimental Results

3.1 Test Chip Implementation

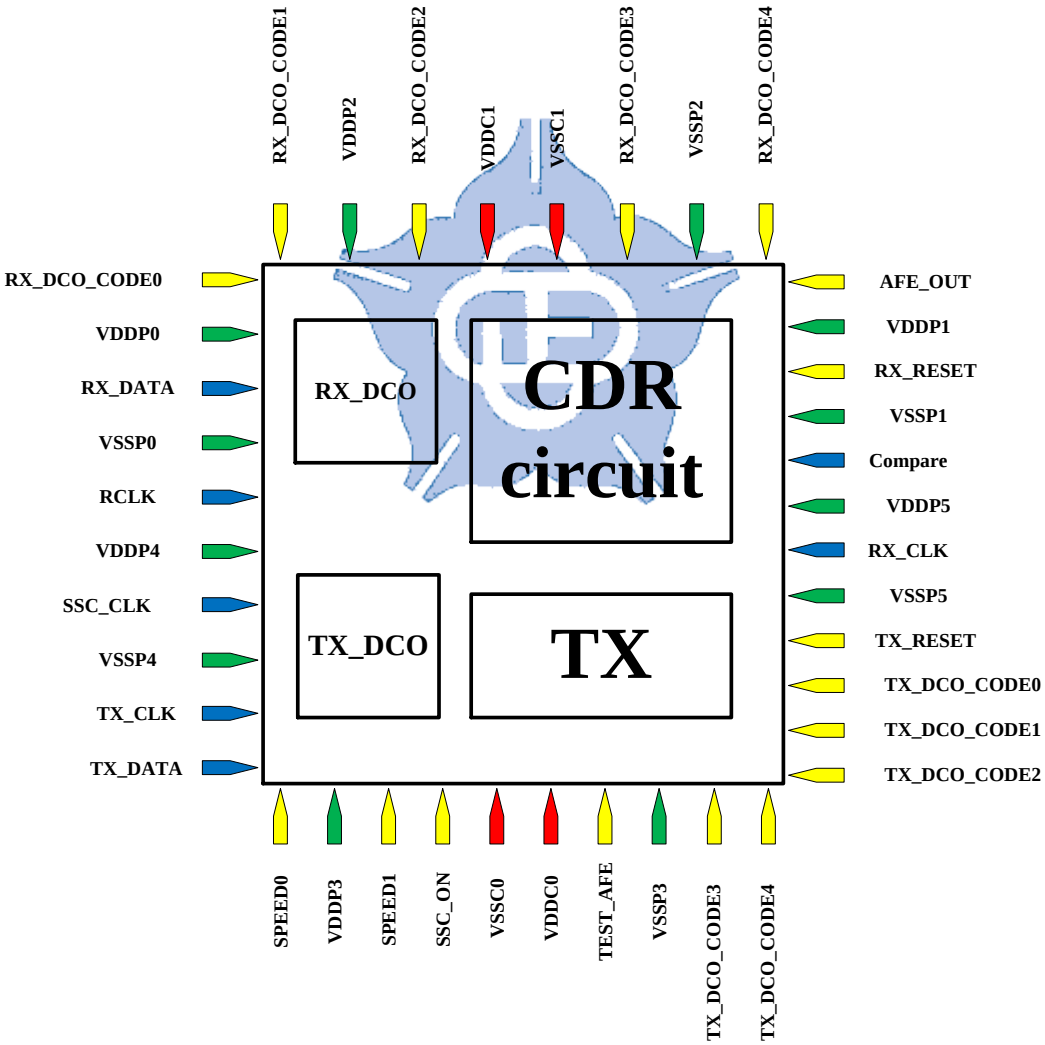


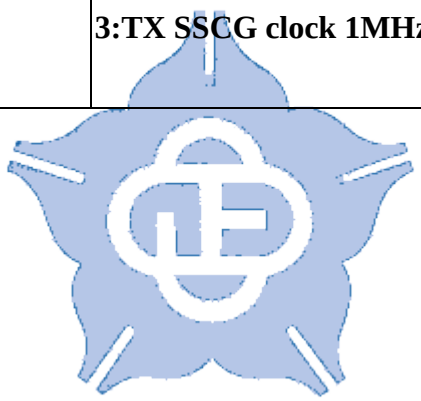
Fig. 3.1 :Test chip floor planning and I/O planning.

Fig. 3.1 shows floor planning and I/O planning of the proposed wideband signaling transceiver. There are 19 I/O PADs and 14 power PADs. The detail I/O description is shown in Table 3.1. The test chip consists of a TX circuit and a TX_DCO in the proposed WBS transmitter, and a CDR circuit and a RX_DCO in the proposed WBS receiver.

Table 3.1 I/O PADs description.

Output	Bit	Function
RX_DATA	1	CDR circuit recovery data
RCLK	1	CDR circuit recovery clock
COMPARE	1	LFSR checker circuit output
RX_CLK	1	RX_DCO clock output
SSC_CLK	1	TX_DCO clock output
TX_CLK	1	Divided clock from TX_DCO clock output
TX_DATA	1	Random data pattern
Input	**Bit**	**Function**
RX_RESET	1	Receiver reset
RX_DCO_CODE	5	RX_DCO control code
AFE_OUT	1	Recovery signal from the AFE circuit

TX_RESET	**1**	**Transmitter reset**
TX_DCO_CODE	**5**	**TX_DCO control code**
SSC_ON	**1**	**SSCG on at 40MHz**
TEST_AFE	**1**	**Regular pattern from transmitter**
SPEED	**2**	**0:TX SSCG clock 40MHz** **1:TX SSCG clock 20MHz** **2:TX SSCG clock 2MHz** **3:TX SSCG clock 1MHz**



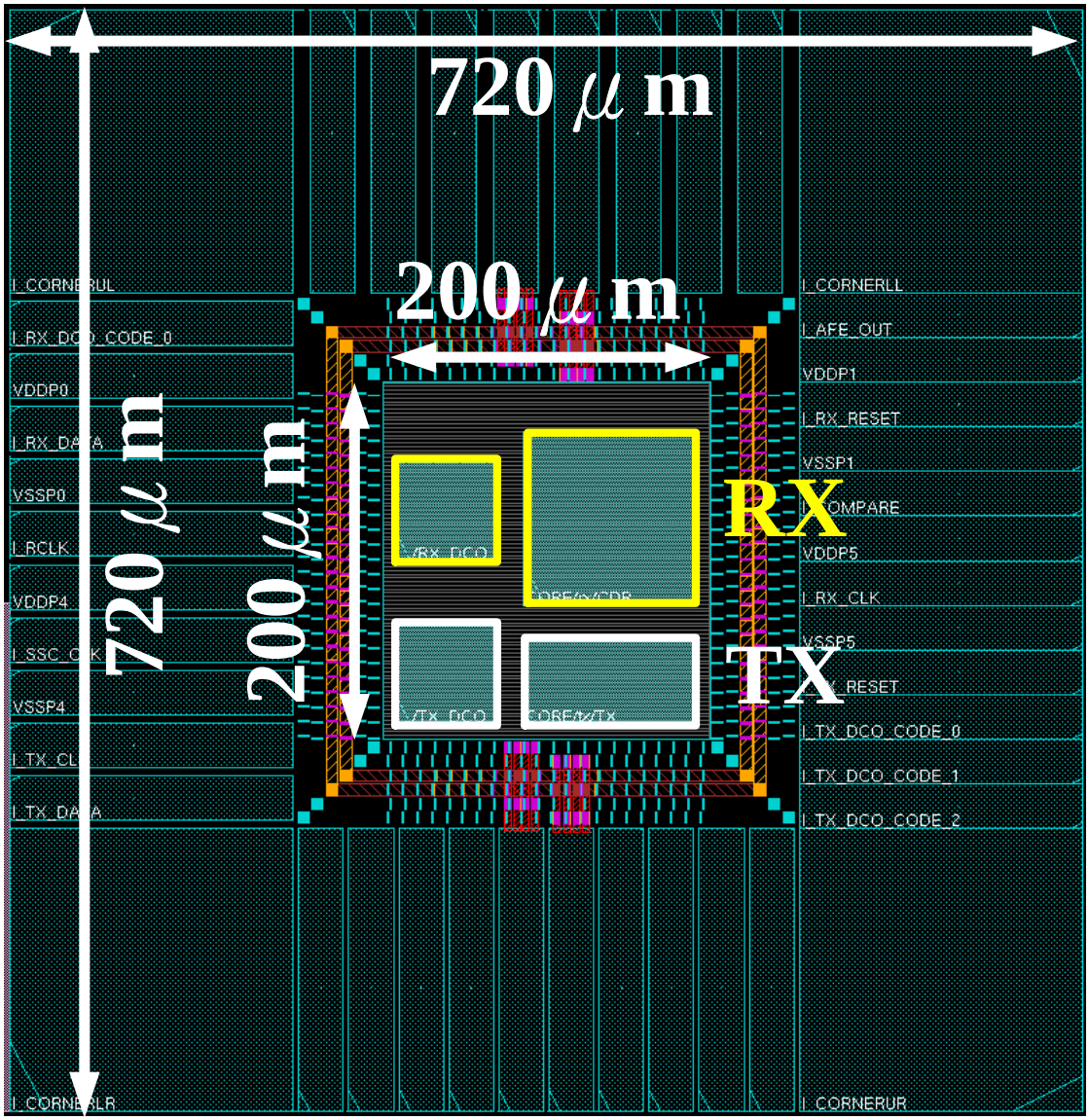


Fig. 3.2 :Layout of the test chip.

Fig. 3.2 shows the layout of the test chip. Thetest chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The chip core size is 200*200μm^2 and chip size including I/O PADs is 720*720 μm^2.

3.2 Error Free Measurement in RTL Simulation

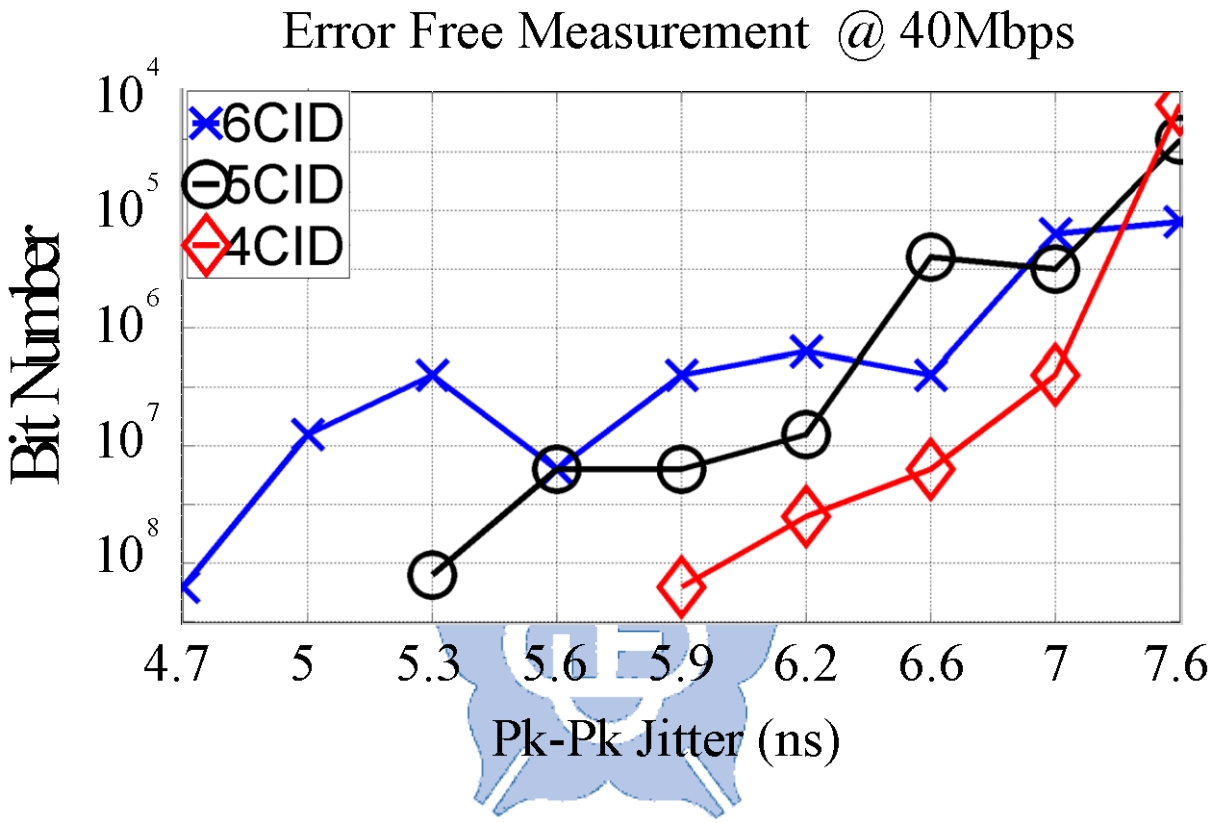


Fig. 3.3 : Error-Free CDR simulation resultswith different CID parameters.

Fig. 3.3 shows the error-free simulation results with different CID parameters in the NRZI encoder at the transmitter,with 40 Mbps data rate. The 4 CID represents thatthe number of consecutive identical digits is 4 in the NRZI_DATA. The 5 CID and the 6 CID represent that the number of consecutive identical digits in the NRZI_DATA is 5 and 6, respectively. Therefore, the number of data transitions of NRZI_DATA of 4 CID is larger than the case with 6 CID. For the CDR circuit, if there has more data transitions, this situation will improve the CDR performance. The line of 6 CID has a bit-error-rate

(BER)<10^{-8} with P_k-P_k jitter 4.7 ns. However, the line of 4 CID has a BER < 10^{-8} withlarger P_k-P_k jitter 5.9 ns. Therefore, 4 CID case has a better jitter tolerance performance than the case with 5 CID or 6 CID case.However, 4 CID case also means there are many redundant bits added in the data transmission.

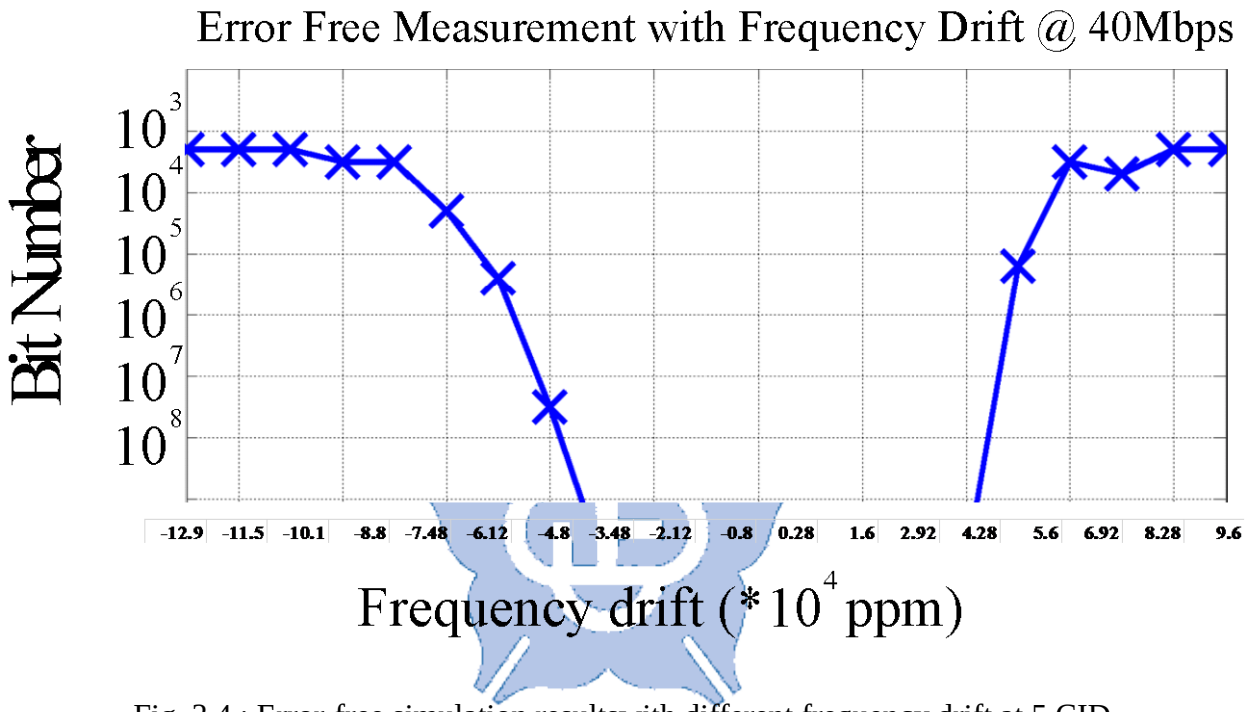


Fig. 3.4 : Error-free simulation resultswith different frequency drift at 5 CID.

Fig. 3.4 shows the error-free simulation with different frequency drift at 5 CID. The definition of frequency drift is the average frequency difference between the clock frequency generated by the SSCG circuit and the ideal 40 MHz clock. The performance of the CDR circuit has a BER < 10^{-8} within the range from -48000 ppm to 42800 ppm at 40Mbps.

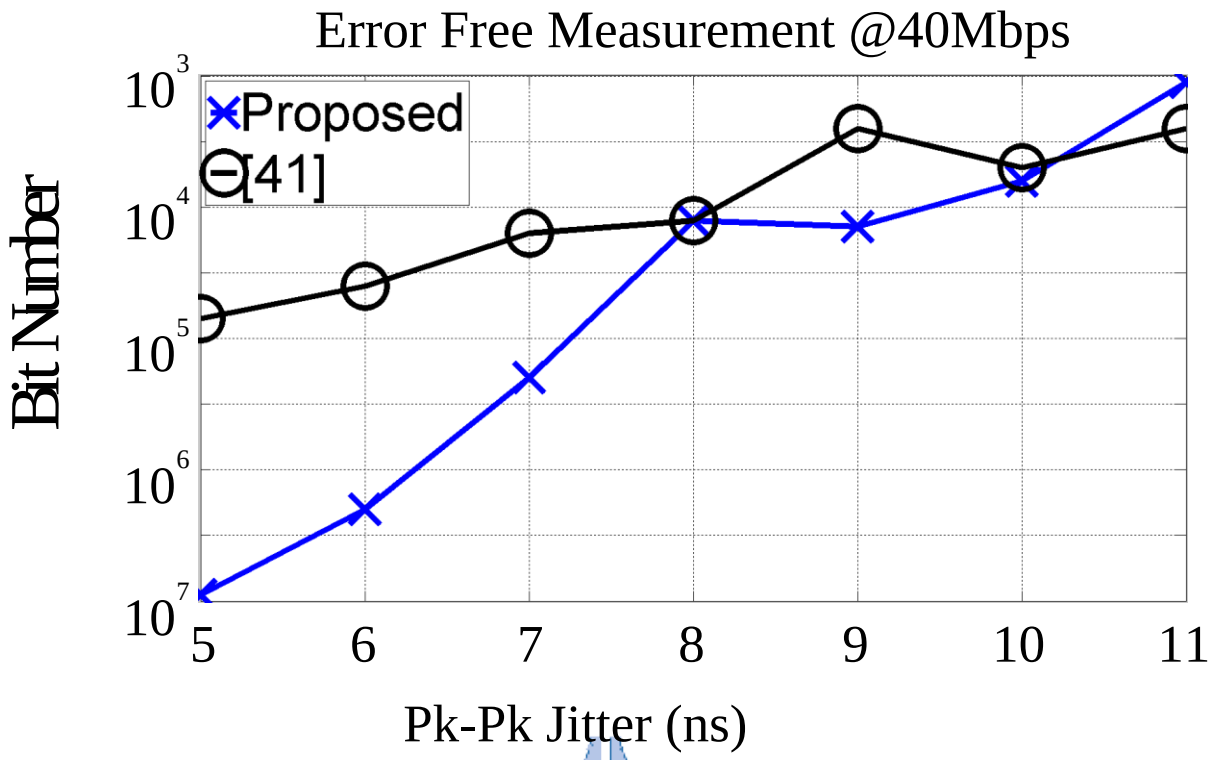


Fig. 3.5 : Error-Free CDR simulation results compared with [41].

Fig. 3.5 shows the error-free simulation results compared with [41] at 40 Mbps. The model of the jitter pattern has a normal distribution. We can see that the proposed design has better jitter tolerance performance than [41]. On the other hand, the proposed design has a BER < 10^{-7} with a 5 ns P_k-P_k jitter.However, when the P_k-P_k jitter is larger than 8 ns, the performance between the proposed design and [41] are similar.

3.3 Chip Summary and Comparison Table

Process	90nm CMOS
Operating Range	1 Mb/s ~ 40 Mb/s
Supply Voltage	1.0V
Core Area	0.04 mm^2
Power Consumption	1.94mW (40Mb/s) (with AFE circuit)
Frontend Voltage Gain	38 dB
Sensitivity	-36dBm
BER	10^{-8} (40 Mb/s)
Energy/bit	0.0485nJ/b (40 Mb/s)

Table 3.2: Chip summary

Thechip summary is shown in Table 3.2. The chip is implemented in TSMC 90nm standard performance CMOS process with 1.0V supply. The core area is 0.04mm^2. The data rate of the proposed WBS transceiver ranges from 1Mb/s to 40Mb/s. The power consumption with the AFE circuit is 1.94 mW at 40 MHz. The sensitivity of the analog front-end circuit is -38 dBm. The bit error rate (BER) is 10^{-8} at 40 Mb/s. The energy consumption per bit at 40 Mb/s is 0.0485 nJ/b.

The performance of proposed WBS transceiver and the comparison with related works are shown in Table 4.3.

Table 3.3: Comparison table

	[8] Zimmerman'96	[34] Shinagawa'04	[24] JSSC'07	[35] JSSC'09	[36] ISSCC' 09	[37] ISSCC'12	Proposed
Communication Method	Narrowband Modulation	Electrooptic Conversion	Wideband Signaling	FSK	Body-couple	FSK	Wideband Signaling
Process	N/A	N/A	0.25-μm	0.18-μm	0.13-μm	0.18-μm	90 nm
Data Rate	2.4 kb/s	10 Mb/s	2 Mb/s	60 kb/s ~ 10 Mb/s	8.5 Mb/s	1 kb/s ~ 10 Mb/s	1 Mb/s ~ 40 Mb/s
Modulation	OOK/DSSS	No	No	Adaptive Frequency Hopping FSK	Correlation Direct Digital	Double FSK	No
Supply	9 V	5 V	1 V	1 V	1.2 V	1 V	1 V
Sensitivity	N/A	N/A	-35 dBm	-65 dBm	-60 dBm	-66 dBm	-36 dBm
Power Consumption	400 mW	650 mW	5 mW	4.6 mW	2.75 mW	2.4 mW	1.94 mW
Area	N/A	N/A	0.85 mm^2	2.30 mm^2	0.19 mm^2	12.5 mm^2 (with I/O pad)	0.04 mm^2
BER	N/A	$4.7*10^{-8}$	$1.1*10^{-7}$	10^{-5} (10Mb/s) $<10^{-9}$ (60kb/s)	10^{-3}	10^{-5}(10Mb/s) 10^{-12}(10kb/s)	$<10^{-8}$(40Mb/s)
Energy/bit	170 μJ/b	65 nJ/b	2.5 nJ/b	0.37 nJ/b	0.32 nJ/b	0.24 nJ/b	0.0485nJ/b

[8] and [34] use a high voltage to transmit the data into the HBC, thus the power consumption is very high. [24], [35], [36] and [37] use the direct-coupled interface scheme

and the difference is the communication methods are different. However, the data rate of [24], [35], [36] and [37]is smaller than 10 Mbps and high power consumption comparing with the proposed design.

Table 3.4 : Comparison table with [41]

	proposed	**[41]**
Process	**90nm CMOS**	**90nm CMOS**
Operating Range	**1 Mb/s ~ 40 Mb/s**	**1 Mb/s ~ 40 Mb/s**
Supply Voltage	**1.0 V**	**1.0 V**
Core Area	**0.04 mm^2**	**0.2 mm^2**
	(w/o AFE circuit)	**(with AFE circuit)**
Power Consumption	**1.94 mW (40 Mb/s)**	**1.69 mW (40 Mb/s)**
(with AFE circuit)		
BER	**$<10^{-8}$ (40 Mb/s)**	**$<10^{-6}$ (40 Mb/s)**
Energy/bit	**0.0485 nJ/b (40 Mb/s)**	**0.04225 nJ/b (40 Mb/s)**

Table 3.4 is the comparison table with [41]. The BER of the proposed circuit is better than [41]. However, the power consumption of the proposed circuit is larger than [41].

Chapter 4

Conclusion and Future Works

4.1 Conclusion

In this thesis, a low power, low hardware cost, high speed and large jitter tolerance WBS transceiver for the human body communication is presented.

The spread-spectrum clock generator is adopted to achieve EMI reduction in the transmitter. Although the body antenna effect will radiates the signal power to the air and interferes the neighbor circuits. Beside, we use the NRZI encoder to generate more data transitions such that the CDR circuit in the receiver can correctly recover data.

The proposed WBS receiver uses the 7X oversampling CDR architecture which adopts the vote mechanism to reduce the impact of jitter accumulation and the AFE duty-cycle distortion.

With the direct-coupled interface, the NRZI binary data can be directly transmitted into the human body channel and it can not only reduces the complexity of the transceiver design but also reduce the power consumption. Therefore, it can fully integrate all function blocks into a silicon chip and also reduce the physical size and achieve low cost.

The test chip is implemented in TSMC 90nm standard performance CMOS process, and thus it has good portability over different processes. The core area is 0.04 mm^2 and the power consumption is 1.94 mW at 40 Mbps.

4.2 Future Works

Because the BCC uses the human body as the transmission medium, the jitter accumulationphenomenon which caused by the body antenna effect still plays a critical rule when the transmission is in progress.

Although in our proposed WBS receiver, we can adopt the appropriate scheme and algorithm with very low hardware cost to recover the interfered data. However, we still need something to improve our proposed WBS transceiver such that our proposed WBS transceiver can be easily used. Therefore, in the CDR circuit,we still need a more reliable compensation mechanism to ensure that there is no frequency drift between the transmitter and the receiver. In addition, we also need to add the standard cyclic redundancy check (CRC) mechanism to ensure the correction of the packet transmission.In the AFE circuit, because the human body motion will change that cause the noise, we need an auto-calibration ofthe gain of AFE circuit that can regularly monitor and calibrate the CDR circuit for recovering the data correctly.

With these schemes, we can make the entire BCC transmission mechanism becomes more reliable, so that the BCC transmission can be applied to more applications.

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