國 立 中 正 大 學

資訊工程研究所碩士論文

使用標準邏輯元件設計並可補償製程電壓及溫度變異對輸出頻率影響之嵌入式矽振盪器

A cell-based on-chip silicon oscillator for frequency compensation with PVT variations

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使用標準邏輯元件設計並可補償製程電壓及溫度變異對輸出頻率影響之嵌入式矽振盪器(A cell-based on-chip silicon oscillator for frequency compensation with PVT variations)

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摘要

在此論文中，我們針對全數位全矽晶片震盪器，探討了混合了製程、電壓以及溫度的同時變化下，穩定一單一輸出頻率所會面臨到的各種問題及挑戰。本論文所提出的架構，當晶片運作的時候，可以自動地估計當時的工作電壓及溫度，並透過校正的方式將製程的漂移給消除，透過這樣的方法，使得此震盪器可在不同的製程、電壓以及溫度的變化下，仍然可以作為系統中一個穩定的頻率參考時脈。

論文中包含各種傳統的矽晶片震盪器介紹，並且針對各種架構中的優缺點加以分析，其中，傳統的架構大多為類比，需要客製化設計，且無法同時抵抗製程、電壓以及溫度的同時變化。

本論文中的全數位全矽晶片震盪器，利用多個環形震盪器的週期比值建立相對參考模型，我們根據相對參考模型去建立了 1.使用多點校正的自動估計電壓以及溫度範圍的全數位全矽晶片震盪器 2.使用四點校正的自動估計電壓以及溫度範圍的全數位全矽晶片震盪器。

在這篇論文中，我們提出了一個新的全數位全矽晶片震盪器，採用 90 奈米製程技術實現。 該研究可在 1.0 伏特的電壓下工作，非常適用應用於低成本以及低功率消耗的系統單晶片上。

關鍵字：全數位，震盪器，抗製成電壓溫度飄移，低功耗。

Abstract

In this thesis, we explore the problems and challenges for a cell-based on-chip silicon oscillator (CBOCSO) with combination of process, voltage and temperature (PVT) variations at the same time. The proposed CBOCSO architecture can estimate the supply voltage and operation temperature at chip run time, and thus, it can eliminate PVT variations by the proposed methodology. In this way, the proposed CBOCSO can provide a stable frequency output as the reference clock for the system.

In this thesis, we introduce various kinds of conventional on-chip silicon oscillators, and we also analyze the advantages and disadvantages of each architecture. Actually, most of the conventional architectures are full-custom analog approaches, and most of them cannot resist PVT variations at the same time.

The proposed CBOCSO uses a relative reference modeling (RRM), which are delay ratios among multiple ring oscillators. According to the RRM, we present the architecture and operation flows to perform automatic voltage and temperature range selection with two calibration methods: 1.multi-point and 2.four-point.

In this thesis, we have presented a novel fully digital CMOS on-chip silicon oscillator implemented in 90nm CMOS technology. The CBOCSO can operate with a 1.0V supply voltage and is very suitable for low-power and low-cost system-on-a-chip applications.

Keyword: all-digital, oscillator, tolerance PVT variations, low power

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Chapter 1

Introduction

1.1 Reference Clock of the System

In recent years, there are more and more complex integrated circuit designs, these complex circuits should be synchronized. Thus, we need a reference clock to synchronize between these different timing circuits.

The integrated circuits and the system-on-chip(SoC) all require a reference clock. However, these circuits often use an external quartz crystal oscillator as the system reference clock.

The quartz crystal is a combination of silicon and oxygen atoms, which chemical name called Silicon Dioxide (SiO2). When the quartz crystal is pressed by a direction of the electric field, the direction of the quartz crystal may be shocked because of the piezoelectric effect.

When we grasp the quartz crystal characteristics of piezoelectric effect, we can use resonance phenomenon to generate precise oscillation frequency, which can be used as the reference clock for the clock generator.

Fig. 1.1 shows various kinds of quartz crystal oscillators, including the quartz crystal oscillator (XO), Temperature compensated crystal oscillator (TCXO), Oven-controlled crystal oscillator (OCXO) and Voltage-controlled crystal oscillator (VCXO). The quartz oscillators are widely used in the market, such as, motherboards, CPU, and large-scale

medical equipments. According to different applications, these circuits will choose a suitable quartz crystal oscillator. In addition, integrated circuit or system-on-chip (SoC) often use the TCXO, because TCXO can against temperature variations. In these circuits, price, size, and power consumption are not major consideration, but frequency accuracy is more important.

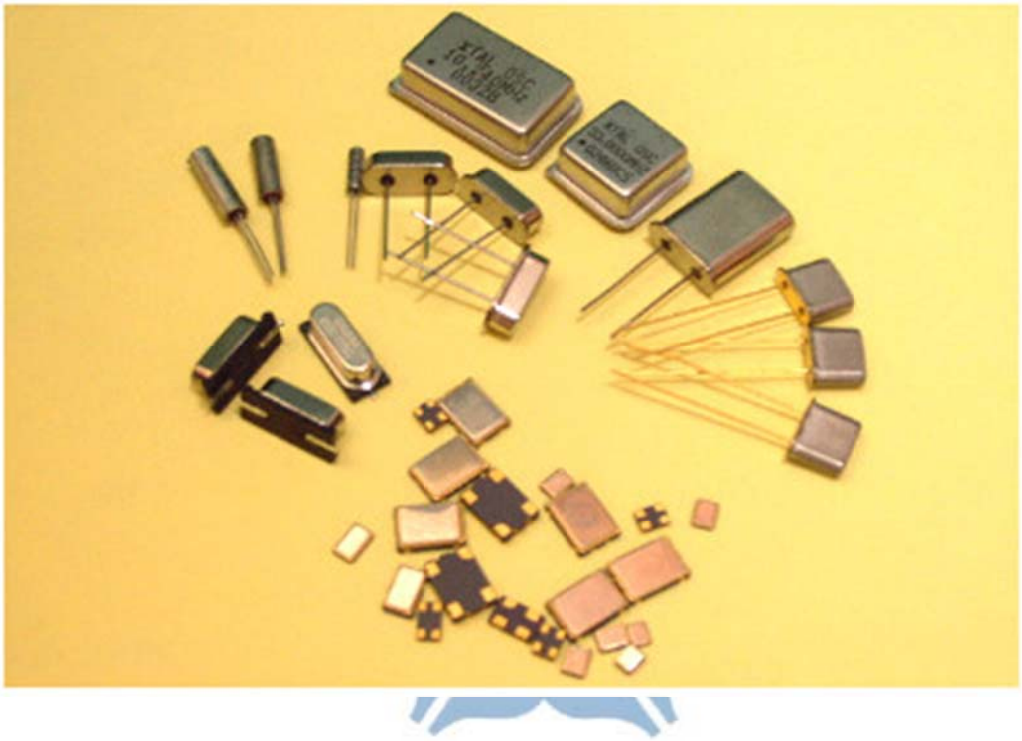


Fig. 1.1: various quartz oscillator.

From the shimmer enterprise website of

http://www.shimmer-co.com.tw/quartz_crystal_oscillator.htm

Although using the quartz crystal oscillator as a reference clock has a high accurate frequency output, the volume of quartz crystal oscillator is too large, and has high cost, and most important is that it cannot be integrated into the COMS process.

1.2 Motivation

In wireless sensor networks and biomedical devices, these systems operate with batteries and are highly integrated. Timing references are essential parts of these systems. However, these type circuits usually not require a very precise reference clock, but they are requested to be low cost, small size and low power. Therefore, we can integrate the reference clock into the chip for this requirement.

Currently, the external quartz crystal oscillator can be replaced by Micro-Electro Mechanical Systems (MEMS) [45] or CMOS-compatible on-chip ring oscillator, two main technologies. The MEMS technology requires extra manufacturing handling and the cost is higher. In addition, as compare to CMOS-compatible on-chip reference clock, the MEMS technology is not convenient.

In recent years, many researches had been devoted to develop CMOS-compatible on-chip oscillators [1]-[35] for replacing off-chip quartz crystal oscillators. When we use CMOS technology to design the reference clock circuit, the integrated circuit makes the volume of the system become smaller with lower power consumption and cost reduction. However, using CMOS technology to design the reference clock circuit has many challenges with process, voltage and temperature (PVT) variations. In order to overcome design problems, many approaches have been proposed for on-chip oscillator design to against process[2]-[4][21][27]-[31][34][39][40], or voltage[7][12]-[15][23] or temperature [1][6][8]-[11][21][22][24]-[26] variations, respectively. However, when the PVT variations both exist [16]-[18][27]-[31], these methods are not applicable. In the next section, we will discuss advantages and disadvantages of these architectures, and to explore some issues can be improved.

1.3 These Organization

In this thesis, we discuss about the implementations of a cell-based on-chip silicon oscillator (CBOCSO) in TSMC 90nm CMOS technology. The proposed four-point calibration methodology can reduce the testing cost of the CBOCSO. The rest of the thesis is organized as follows.

In chapter 2, we discuss about conventional on-chip silicon oscillator architectures. Subsequently, we discuss and analyze the relative reference modeling (RRM).

In chapter 3, the first version of proposed CBOCSO with multi-points calibration is presented. In this chapter, we propose RRM with two delay ratios and explain how to build this model by the delay ratio estimator (DRE), the digital control oscillator (DCO) and the CBOCSO controller. In addition, we also propose the cell selection rules to choose the suitable cells for the delay ratio estimator from the TSMC 90nm standard cell library.

In chapter 4, the second version of the proposed CBOCSO with four-point calibration is presented. In this version, we improve the resolution of the DCO with fine tuning delay line and the new CBOCSO controller, and with improve algorithms to reduce the testing cost in calibration.

In chapter 5, the specifications and measurement results of the CBOCSO with four-point calibration are discussed. In chapter 6, we use the proposed CBOCSO with minor modifications for the all-digital temperature sensor application with voltage variations. In chapter 7, we make a conclusion and describe the further work about some design issues that can be improved in the near future.

Chapter 2

Conventional On-Chip Silicon Oscillator

2.1 The Band gap Voltage Reference-Based On-Chip Silicon Oscillator

In the prior researches, most of the on-chip silicon oscillators use an external temperature sensor or an input reference voltage [1]-[5][34][35] to replace the external quartz crystal. These type of circuits, we call them band gap voltage reference-based on-chip silicon oscillator.

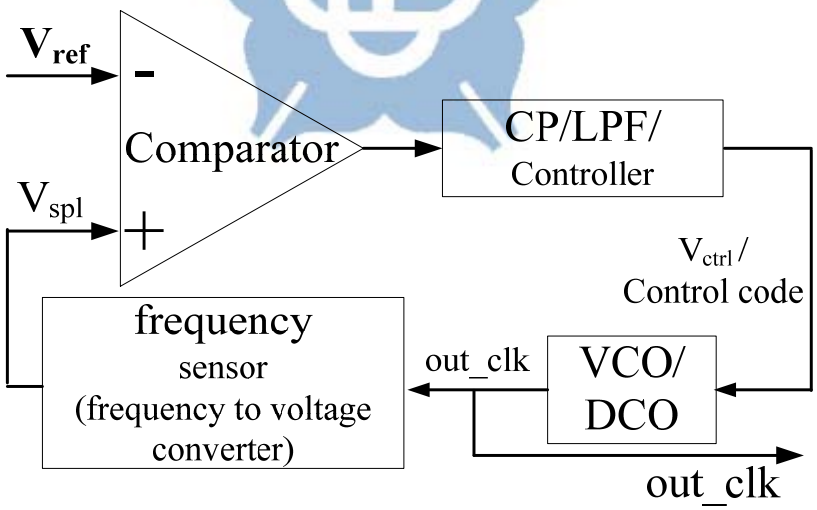


Fig. 2.1: The architecture of the band gap voltage reference-based on-chip silicon oscillator.

Fig. 2.1 shows block diagram of a band gap voltage reference-based on-chip silicon oscillator [4] compensation loop. When this circuit uses analog charge pump, it is composed

of a comparator, charge pump (CP), loop filter (LPF), a frequency sensor and a voltage controlled oscillator (VCO). When this circuit uses the digital approach, it is composed of a comparator, the digital controller, a frequency sensor and a digital controlled oscillator (DCO). When the VCO/DCO generates the difference frequency (out_clk) by the difference voltage (V_{ctrl}) or the difference digital control code, the frequency sensor detects the VCO/DCO frequency, and the frequency is converted to the voltage value (V_{spl}) by the frequency sensor.

When there has an external stable DC voltage reference (V_{ref}). The comparator compares the difference between V_{spl} and V_{ref}. When V_{spl} is smaller than V_{ref}, this circuit will speed up the VCO/DCO by increasing the V_{ctrl} or digital control code. Similarly, if V_{spl} is larger than V_{ref}, this circuit will slow down the VCO/DCO by decreasing the V_{ctrl} or digital control code. Therefore, this compensation mechanism can against process and temperature variations.

Although, this circuit does not require a reference clock. However, it needs an external reference voltage (V_{ref}) to eliminate the process and temperature variations. In addition, when the frequency sensor converts frequency into voltage value, it generates some errors. However, the band gap reference-based on-chip silicon oscillator cannot against process, voltage and temperature variations at same time.

2.2 The Band gap Temperature Sensor-Based On-Chip Silicon Oscillator

Fig. 2.2 shows the block diagram of the temperature sensor-based on-chip silicon oscillator [21] compensation loop. It is composed of a temperature sensor, a non-linear

mapper, a divider, a phase detector (PD), loop filter, a digital/voltage controlled oscillator (DCO/VCO) and an electrothermal filter (ETF)[24] /Oscillator(OSC).

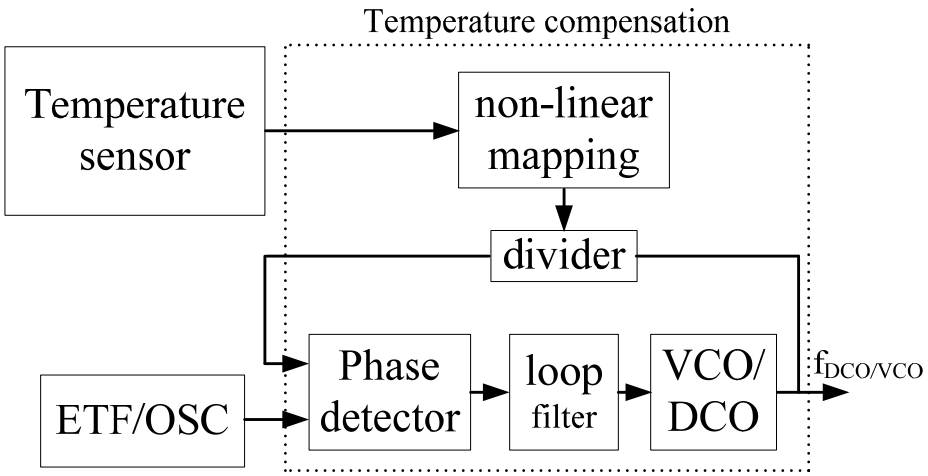


Fig. 2.2: The architecture of the band gap temperature sensor-based on-chip silicon oscillator.

Firstly, this circuit uses a temperature sensor to estimate the operating temperature. In addition, they build a temperature compensation to the DCO control code tables. Subsequently, they use the PD to compare the phase difference between ETF/OSC and DCO/VCO. According to the temperature value, the non-linear mapping table can be used to calculate the control code to the DCO/VCO. Then the frequency of the DCO/VCO can be adjusted by the control code with temperature variation.

A mobility-based frequency reference [21][22] and thermal diffusivity-based frequency reference [24]-[26] are based on the band gap temperature sensor-based on-chip silicon oscillator. They have high accuracy, low power, and they can cover wide temperature range variations, but they cannot against voltage variation. In addition, they have relatively small process variations, but their approaches have strong temperature dependency. Thus, they need accurate temperature sensors to compensate for the output frequency with temperature variations, and their approaches occupy a large chip area.

2.3 The Bias-Based On-Chip Silicon Oscillator

Fig. 2.3 shows block diagram of a bias current compensation mechanism frequency-locked loop technique of on-chip silicon oscillator [12]. It is composed of a current comparator, a VCO, an amplifier (AMP), and a digital-to-analog converter(DAC).

The bias circuit generates a bias current (I_{BIAS}), and then the AMP will amplify the difference between I_{BIAS} and I_{OUT} into V_{OUT} to the VCO, The frequency-to-current converter converts the frequency of f_{OUT} into current I_{OUT}, and these circuits form a feedback loop. The current comparator compares the difference between I_{BIAS} and the converter output current I_{OUT}. They will adjust the control voltage (V_{OUT}) of the VCO until the I_{OUT} equal to I_{BAS} in this feedback loop.

This type of architecture [12]-[15][32] improved the band gap voltage reference-based on-chip silicon oscillator, and this circuit do not require an external reference voltage [1]-[5][34][35], However, the design challenges of this circuit are the accuracy of the reference bias circuit with PVT variations and the conversion error in the frequency-to-current converter.

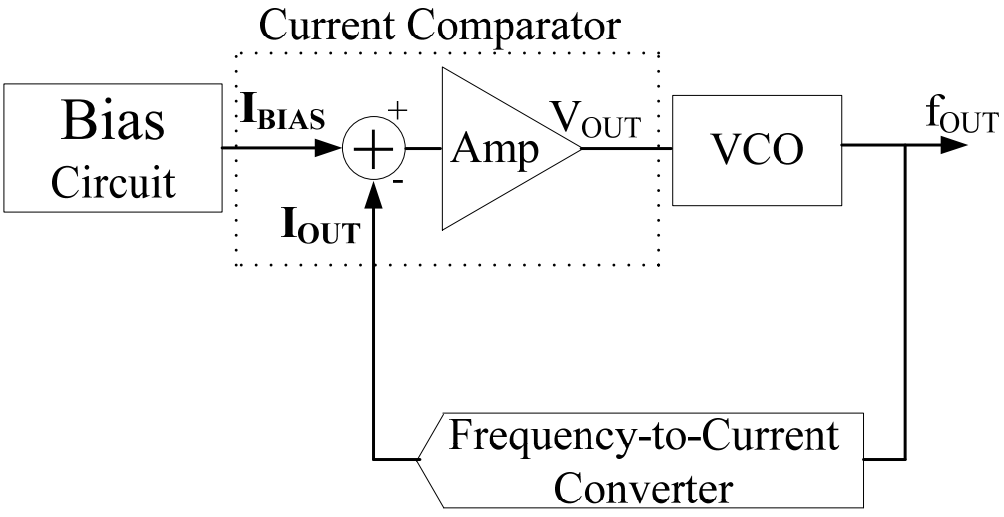


Fig. 2.3: The architecture of the current comparator on-chip silicon oscillator.

Fig. 2.4 shows block diagram of a two voltages controlled on-chip silicon oscillator [15]. It is composed of a voltage-swing controller, a bias current controller, and a ring voltage controlled oscillator (RVCO).

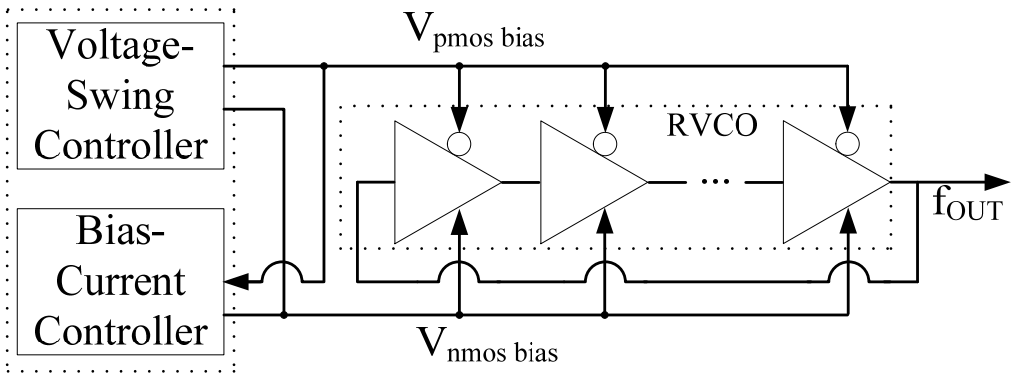


Fig. 2.4: The architecture of the two voltage controlled on-chip silicon oscillator.

This architecture uses on-chip bias-current controller and voltage-swing controller to compensate for the RVCO frequency with process and voltage variations.

The voltage-swing controller generates the difference voltage to control PMOS and NMOS of the RVCO, and the bias-current controller generates the different current to control PMOS and NMOS of the RVCO at the same time.

Fig. 2.5 shows the simulation results of voltage-swing controller and the bias-current controller different voltage (V_{swing}) and different current (I_{bias}) to compensate the RVCO [15]. According to the Fig. 2.5, we can see that the output frequency of the RVCO remain stable with process and voltage variations. However, the voltage-swing controller and the bias-current controller are required to generate the difference voltage to compensate for the frequency of the RVCO with process and voltage variations. Thus, this circuit requires full custom design. In addition, this design method is not suitable to against temperature variations.

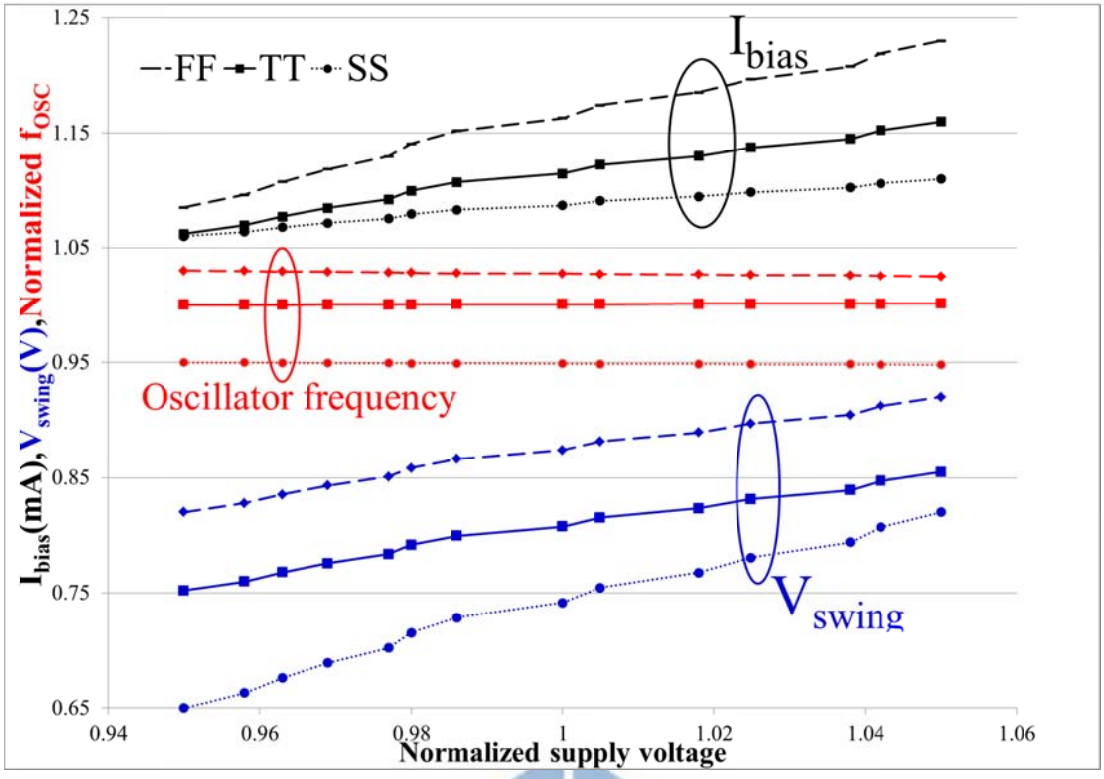


Fig. 2.5: The two voltage controlled on-chip silicon oscillator frequency with process and voltage variation.

2.4 Relaxation-Based On-Chip Silicon Oscillator

The Relaxation Oscillator [16]-[20] is an improved design of the RC-oscillator. Fig. 2.6 shows architecture of the conventional RC-oscillator [16]. It is composed of two comparators, a SR latch, some resistors and some capacitors. The conventional RC-oscillator runs through a resistor to charge a capacitor from a current source. In this circuit, the current source I_1 and I_2 have flicker noise, and thus when it uses for a long time, the comparator and other circuit have process, voltage and temperature (PVT) variations and the accuracy of frequency will be degraded.

In recent years, the relaxation oscillator [16]-[20] wants to reduce the comparator to output delay time changes (t_d) with PVT variations.

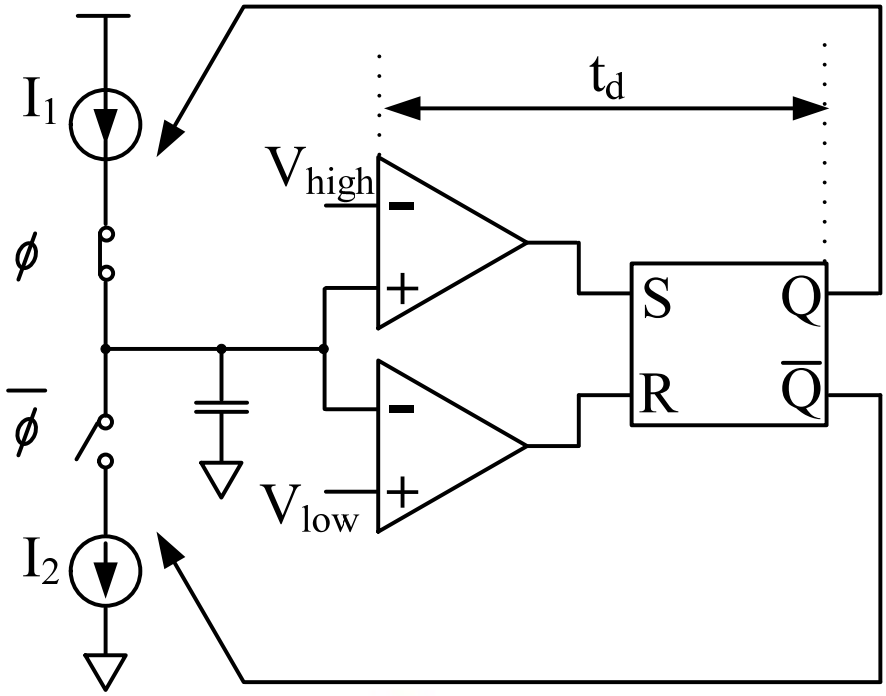


Fig. 2.6: The architecture of conventional RC-oscillator.

Fig. 2.7 shows architecture of voltage averaging feedback (VAF) relaxation oscillator [16], it is composed of a VAF and a relaxation oscillator.

The relaxation oscillators [16][17] with power averaging feedback can tolerate both temperature and voltage variations. However, the resistive divider for the voltage reference requires cancelling of temperature dependency. Thus, a small voltage variations on the reference voltage (i.e. 2mV) can cause 0.4% frequency error [16], and thus, they are sensitive to the supply noise and process variations. Relaxation oscillators [16]-[18][20] requires a bias generator to overcome voltage and temperature variations. However, the bias generator occupies a large chip area.

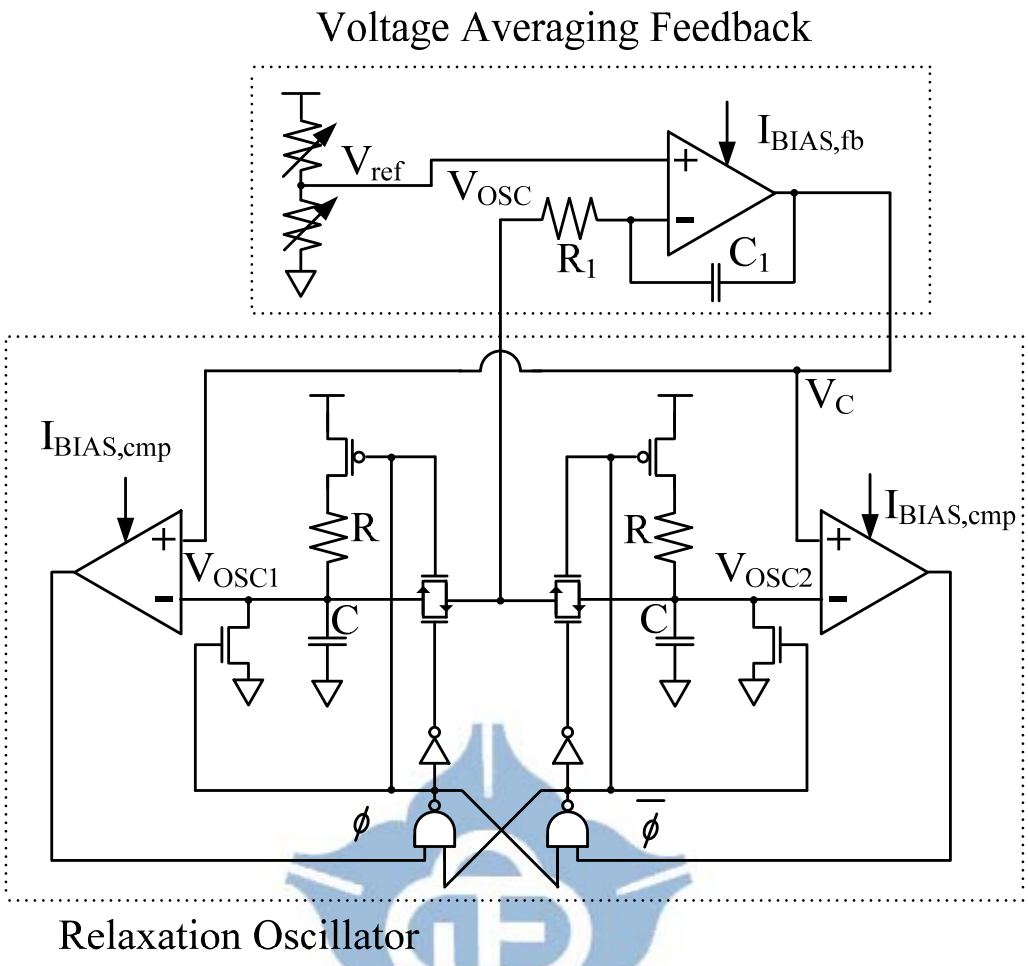


Fig. 2.7: The architecture VAF relaxation-oscillator.

2.5 The Addition-based Current Source On-Chip Silicon Oscillator

The addition-based Current Source On-Chip Silicon Oscillator [23] is shown in Fig. 2.8. If we assume W/L ratio of M1 and M3 are the same and they are matched devices. Hence the current through M1 and M3 will be the same. In this circuit, when the current I_1 increase due to process variation, the current I_2 will decrease. Oppositely, when the current I_1 decrease, the current I_2 will increase. Thus, we can adjust ratio of M1/M3 and M2, which can get a stable current source by $I = I_1 + I_2$ with process variations.

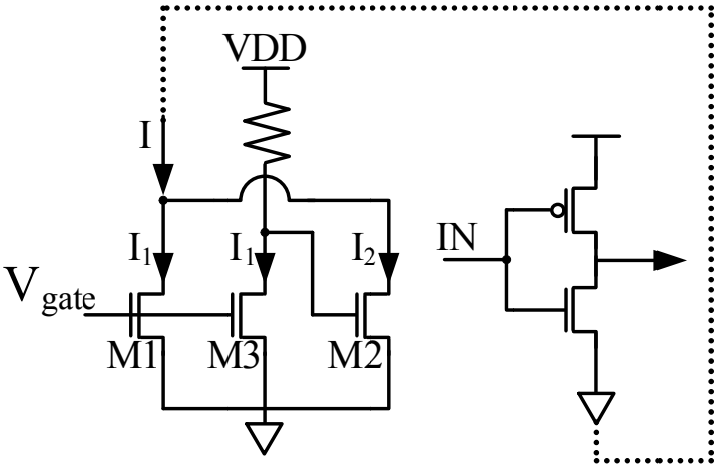


Fig. 2.8: Schematic of the addition-based current source.

We try to build up a ring oscillator with addition-based current source. Fig. 2.9 shows the simulation results of the addition-based current source on-chip silicon oscillator with PVT variations. We adjusted W/L of M1 and M3, and the period of the output clock can remain stable at 1.00V with temperature variations. However, the period of output clock will drift due to voltage variations. This method can effectively against process and temperature variations. However, the period drift due to the voltage variations cannot be overcome.

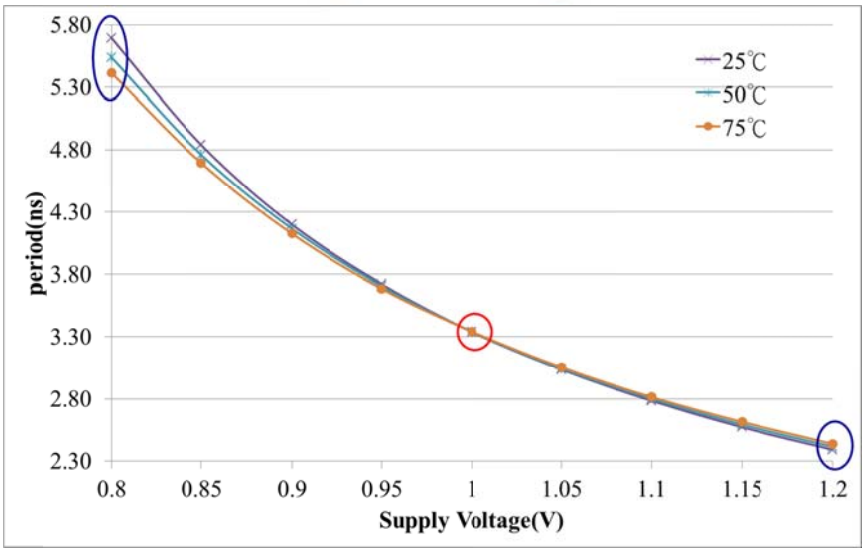


Fig. 2.9: The simulation results of the addition-based current source on-chip silicon oscillator with PVT variations.

2.6 The Relative Reference Modeling On-Chip Silicon Oscillator

An all-digital on-chip oscillator with the relative reference modeling (RRM) is proposed in [27]-[31]. The propagation delay time of the logic cells are easily affected by process, voltage, and temperature (PVT) variations. In RRM, They choose two logic cells from the standard cell library, and one of them uses as a reference delay cell (RDC), and the other cells use as the compare delay cell (CDC). With PVT variations, delay time of the RDC and the CDC will both increase and decrease. However, delay time variations in the RDC and the CDC are not the same. In RRM, they define the delay ratio between these logic cells can be expressed as Eq. 2.1.

$$R(P,V,T) = \frac{D_{CDC}(P,V,T)}{D_{RDC}(P,V,T)} \quad \text{(Eq. 2.1)}$$

where $D_{RDC}(P,V,T)$ and $D_{CDC}(P,V,T)$ are delay time of the RDC and CDC, respectively.

The block diagram of the delay ratio estimator (DRE) is shown in Fig. 2.10. In DRE, two logic cells, RDC and CDC are used to create two ring oscillators, the reference ring oscillator (RRO) and the compared ring oscillator (CRO), respectively. The output of the ring oscillator is connected to the counter to record the oscillation cycles of the oscillator. The value of two counters can be used to calculate the delay ratio R(P,V,T) as Eq. 2.2.

$$R(P,V,T) = \frac{RRO_{CNT}}{CRO_{CNT}} \quad \text{(Eq. 2.2)}$$

where CRO_{CNT} and RRO_{CNT} are the output of the CRO counter and the RRO counter, respectively. The CRO counter will count from 0 to N_{TIME}, and then the two ring oscillators are stopped. The value of N_{TIME} is power of two, thus the delay ratio R(P,V,T) can be computed without a divider.

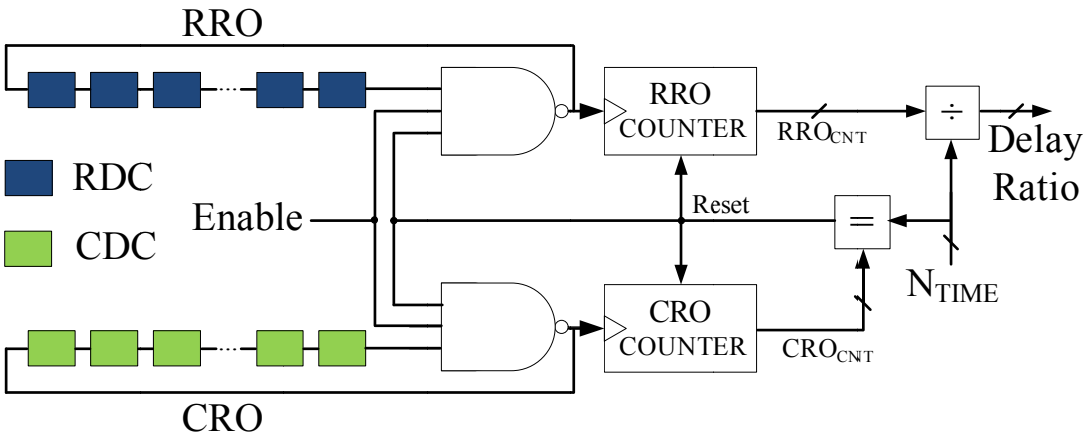


Fig. 2.10: The architecture the delay ratio estimator (DRE).

Fig. 2.11 shows the map of the relationship between R(P,V,T) and D_{RDC} in typical corner, where D_{RDC} is the period of the reference ring oscillator. The D_{RDC} can be estimated in terms of R(P,V,T) as expressed in Eq. 2.3.

$$D_{RDC}(P,V,T) = coef_0 + coef_1 R(P,V,T) + coef_2 R^2(P,V,T) + \cdots + coef_n R^n(P,V,T) \quad \text{(Eq. 2.3)}$$

where $coef_0$ to $coef_n$ is the coefficients of nth-order curve modeling. In RRM, the high order of curve modeling results in high cost. As a result, they need to trade-off accuracy and design cost. Finally, they uses a second-order mapper to implement the Eq.2.3.

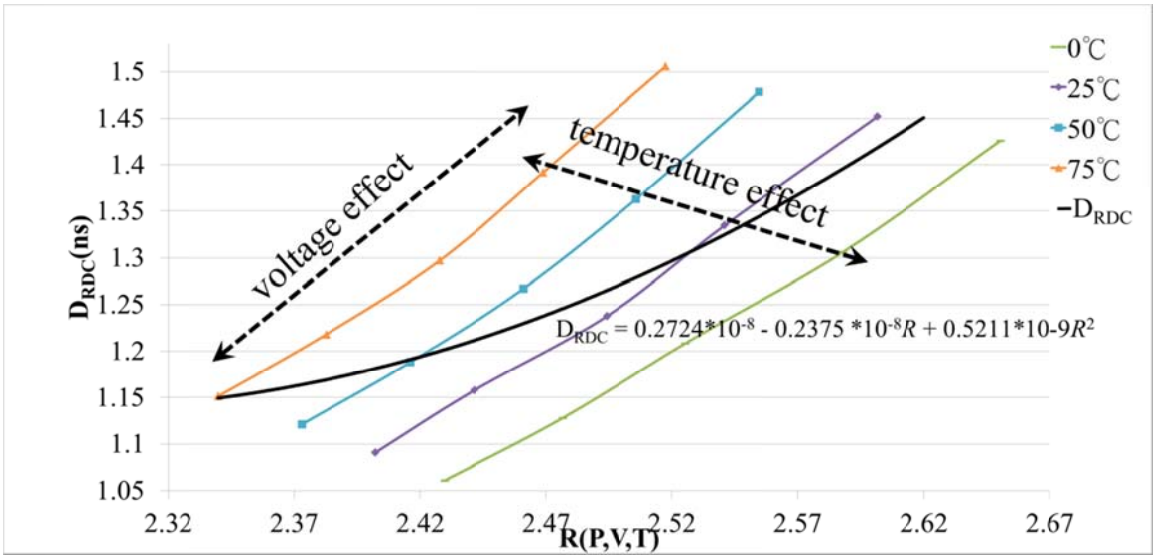


Fig. 2.11: The R(P,V,T), D_{RDC}, and the second-order curve modeling diagram.

Fig. 2.12 shows the system architecture of the RRM. It is composed of a delay ratio estimator (DRE), a mapper and a DCO. The DRE computes the R(P,V,T) at chip run time with voltage and temperature variations. Firstly, the RRM requires multi point calibration. In the calibration mode, the DRE estimates the R(P,V,T) and D_{RDC} at different voltage and temperature combinations. According to R(P,V,T) and D_{RDC} values to build up the second-order curve modeling diagram as shown in Fig 2.11. The mapper is used to to replace the second order equation calculatio. Then the mapper outputs control code to the DCO.

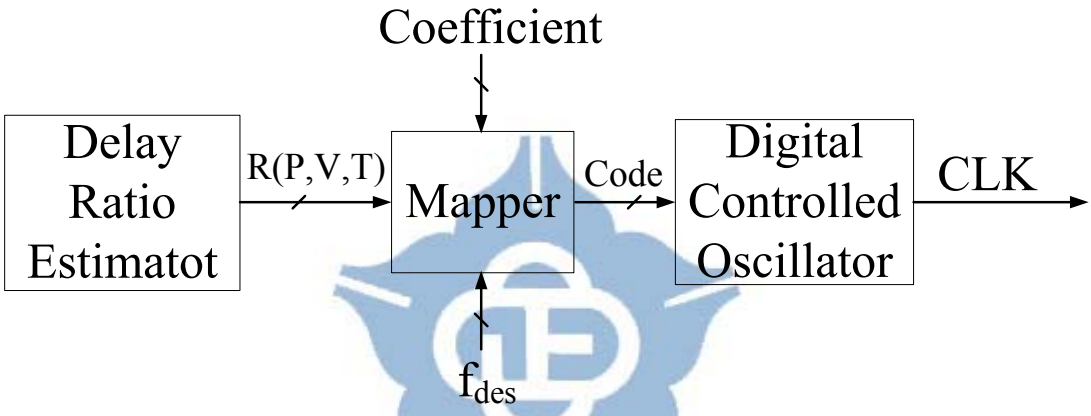


Fig. 2.12: The architecture of the Relative Reference Modeling On-Chip Silicon Oscillator.

The digital approach of the RRM makes it easy to design the on-chip oscillator. However, a high order polynomial is required to minimize the modeling error, and thus, a mapper is required to reduce the area cost. In addition, in RRM, multi-points calibration is required. The high testing cost make it is not suitable for mass production.

2.7 The Ring Oscillator and Relative Reference Modeling Analysis

In section 2.6, we discuss an all-digital on-chip oscillator with the relative reference modeling (RRM). The RRM uses a delay ratio can be reduced output frequency error of the oscillator with PVT variation. In this these, we use two delay ratios of RRM. In this section, we analyze the characteristics of the ring oscillator and RRM and shows the relationship between the frequency of the ring oscillator and RRM.

Figs. 2.13, 2.14, and 2.15 show the periods of three ring oscillators with PVT variations. These three ring oscillators are the reference ring oscillator (RRO), the compared ring oscillator 1 (CRO1), and the compared ring oscillator 2 (CRO2). The period of RRO, CRO1 and CRO2 can be divided into different groups in different process corners. In different process corners, the period variations of RRO, CRO1 and CRO2 like nth-order polynomial curve with voltage variations. However, the period variations of RRO, CRO1 and CRO2 are linear change with temperature variations. In addition, under process or voltage or temperature variations, the period variations of these oscillators will not be the same.

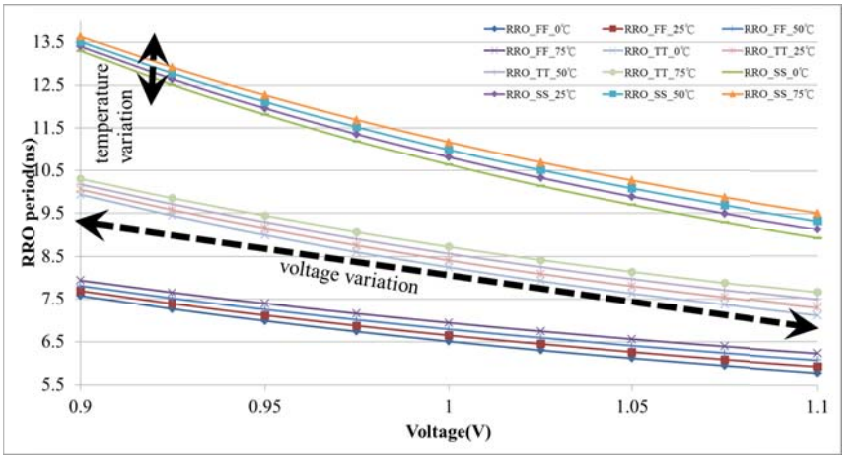


Fig. 2.13: The simulation result of RRO with PVT variations.

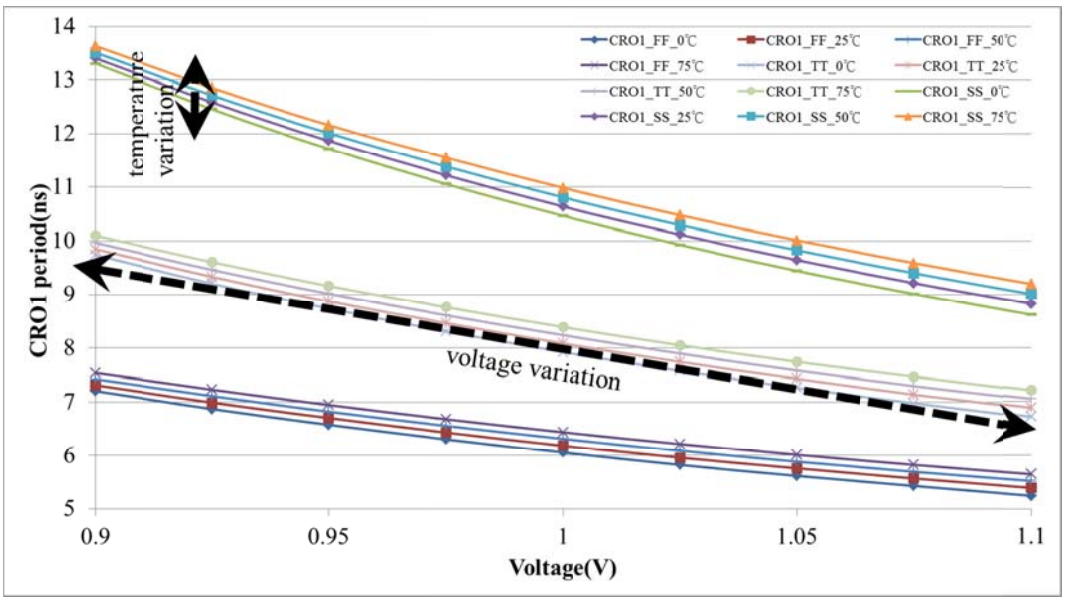


Fig. 2.14: The simulation result of CRO1 with PVT variations.

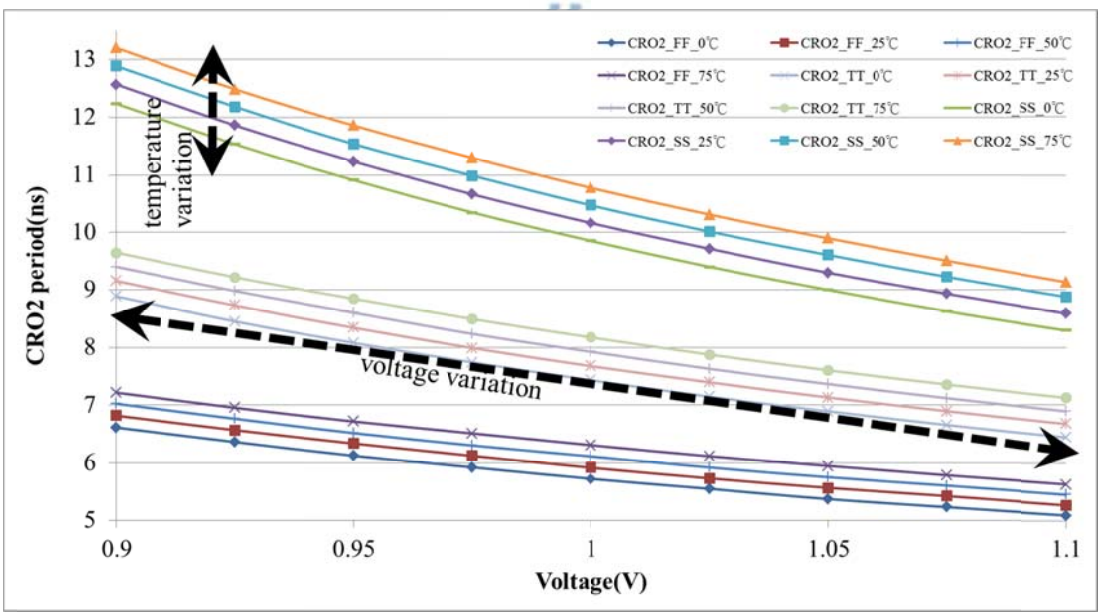


Fig. 2.15: The simulation result of CRO2 with PVT variations.

The relative reference modeling (RRM) can build up the relationship of these oscillators. Since the period of the oscillator is changed with voltage and temperature variations, the ratio method of the RRM can cancel some of period variations. Thus, the RRM method can reduce the amounts of period variations.

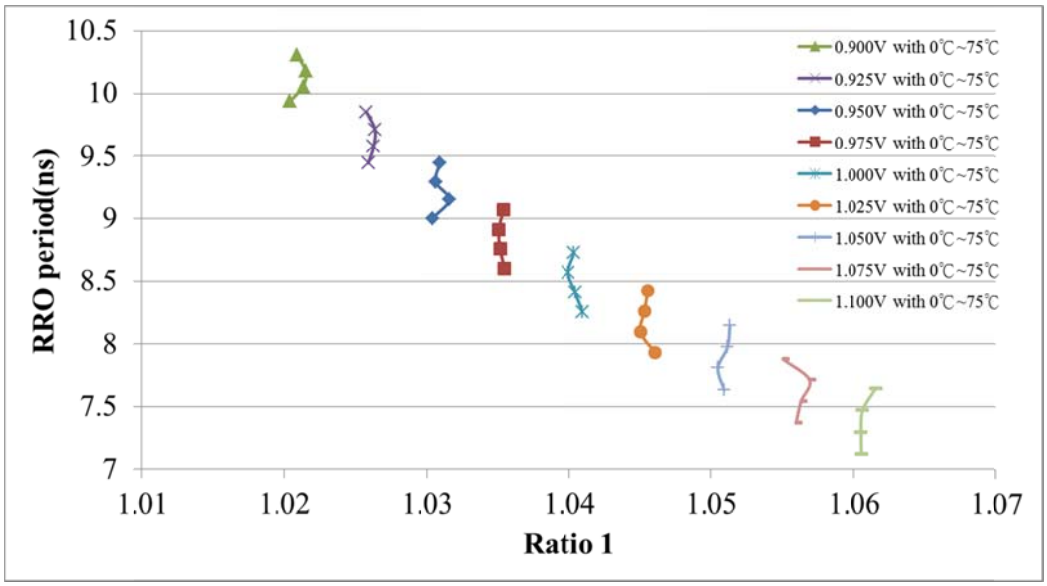


Fig. 2.16: Delay ratios R1(V, T) versus RRO's period (V,T) in typical process corner.

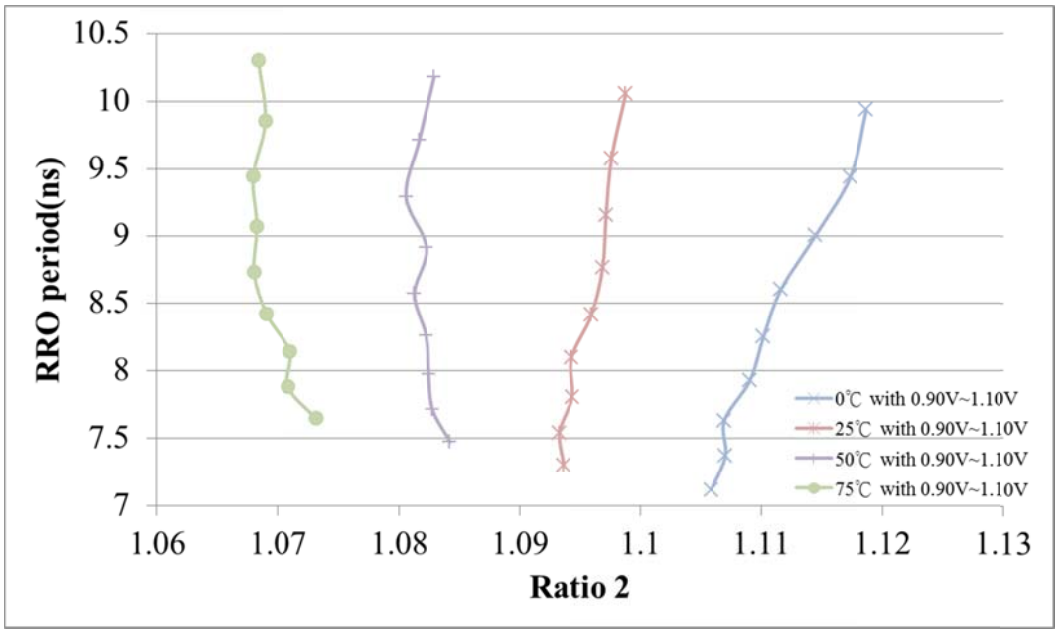


Fig. 2.17: Delay ratios R2(V, T) versus RRO's period (V,T) in typical process corner.

Fig. 2.16 shows the delay ratios R1(V, T) versus RRO's period (V,T) in typical process corner. In this figure, the R1(V, T) is a delay ratio between the period of RRO and CRO1. The temperature coefficient of RRO and CRO1 are similar, and the ratio method would reduce the temperature coefficient between RRO and CRO1. Thus, with different supply voltages the R1(V, T) value are quite close with temperature variation. Similarly, Fig. 2.17 shows the delay ratios R2(V, T) versus RRO (V,T) in typical process corner. In this figure,

the R2(V, T) is a delay ratio between period of RRO and CRO2, the voltage coefficient of RRO and CRO2 are similar, and the ratio method would reduce the voltage coefficient between RRO and CRO2. Thus, in different operating temperature values, the R2(V, T) value are quite close with voltage variations. As a result, we can use the delay ratios R1(V,T) and R2(V,T) to estimate the current temperature and current voltage of the chip at run time.

2.8 Summary

Most of the conventional on-chip ring oscillators require an external band gap reference. In addition, the bias circuit and other current compensation circuit are full-custom. Also, these circuits cannot resist PVT variation at the same time.

In this thesis, we design a CBOCSO circuit without an external band gap reference. The proposed design also uses the relative modeling to build up the on-chip oscillator. A voltage and temperature classifier is proposed to reduce the modeling error of the RRM [27]-[31] achieve a better accuracy of the output frequency.

In addition, to make our design more suitable for mass production, the proposed four-point calibration methodology can effective reduce the testing cost of the CBOCSO during calibration.

Chapter 3

Cell-Based On-Chip Silicon Oscillator with Multi-points Calibration

3.1 Relative Reference Modeling with Two Delay Ratios

The propagation delay time of the logic cells are easily affected by process, voltage, and temperature (PVT) variations. If we choose any three logic cells from the standard cell library. One of them uses as a reference delay cell (RDC), and the other cells use as the compare delay cell 1 (CDC1) and the compared delay cell 2 (CD2).The delay ratio between these logic cells can be expressed as Eq. 3.1 and Eq. 3.2.

$$R1(P,V,T) = \frac{D_{RDC}(P,V,T)}{D_{CDC1}(P,V,T)} \quad \text{(Eq. 3.1)}$$

$$R2(P,V,T) = \frac{D_{RDC}(P,V,T)}{D_{CDC2}(P,V,T)} \quad \text{(Eq. 3.2)}$$

where D_{RDC}(P,V,T), D_{CDC1}(P,V,T), and D_{CDC2}(P,V,T) are the delay time of the RDC, CDC1, and CDC2, respectively.

For a fixed supply voltage (V) and certain process corner (P), D_{RDC}(P,V,T) and D_{CDC1}(P,V,T) are both increased and decreased with temperature variations. Thus, the range of R1(P,V,T) means the temperature coefficients difference between RDC and CDC1.

Therefore, if there exists a RDC and CDC1 pair, which the range of the R1(P,V,T) at all

process corners with different voltages are not overlapped. Then, R1(P,V,T) can be used to roughly determine the current supply voltage of the chip. Similarly, for a fixed temperature (T) and certain process corner (P), D_{RDC}(P,V,T) and D_{CDC2}(P,V,T) are both increased and decreased with voltage variations. Thus, if there exists a RDC and CDC2 pair, which the range of the R2(P,V,T) at all process corners with different temperatures are not overlapped. Then, R2(P,V,T) can be used to roughly determine the current temperature of the chip.

In this method, the R1(P,V,T) and R2(P,V,T) are used by the proposed voltage and temperature classifier, and the output frequency accuracy of the on-chip ring oscillator can be significantly improved.

3.2 Design of Delay Ratio Estimator

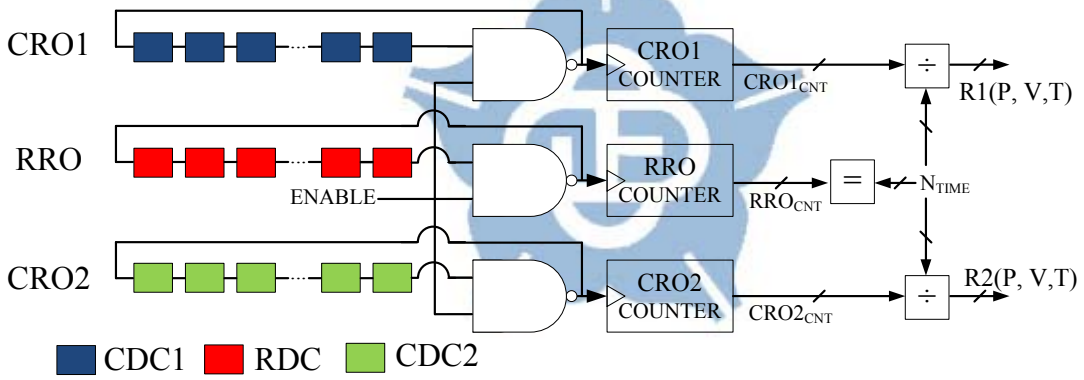


Fig. 3.1: The architecture of the delay ratio estimator.

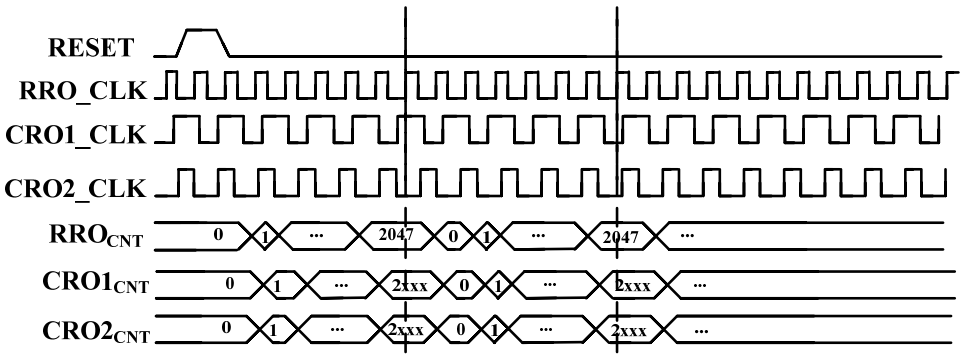


Fig. 3.2: Timing diagram of the delay ratio estimator.

The block diagram of the proposed delay ratio estimator (DRE) is shown in Fig. 3.1 [46]. Fig. 3.2 shows the timing diagram of the DRE. In DRE, three logic cells, RDC, CDC1, CDC2 are used to create three ring oscillators, the reference ring oscillator (RRO), the compared ring oscillator 1 (CRO1), and the compared ring oscillator 2 (CRO2), respectively.

The output of the ring oscillator is connected to the counter to record the oscillation cycles of the oscillator. The value of these counters can be used to calculate the delay ratio R1(P,V,T) and R2(P,V,T) as follows Eq. 3.3 and Eq. 3.4.

$$R1(P,V,T) = \frac{CRO1_{CNT}}{RRO_{CNT}} \qquad \text{(Eq. 3.3)}$$

$$R2(P,V,T) = \frac{CRO1_{CNT}}{RRO_{CNT}} \qquad \text{(Eq. 3.4)}$$

where $CRO1_{CNT}$, $CRO2_{CNT}$ and RRO_{CNT} are the output of the CRO1 counter, the CRO2 counter, and the RRO counter, respectively. The RRO counter will count from 0 to N_{TIME}, and then these three ring oscillators are stopped.

The value of N_{TIME} is set to 2047, thus the delay ratio R1(P,V,T) and R2(P,V,T) can be computed without divider circuits. When the value of N_{TIME} is equal to 2047, the RRO_CLK will gating three cycles, then the CRO1_CLK and CRO2_CLK latch the $CRO1_{CNT}$ and $CRO2_{CNT}$ as R1 and R2, respectively. Thus, the values of R1 and R2 may occur ± 1 error due to the asynchronous in three oscillators.

3.3 Design of Digitally Controlled Oscillator

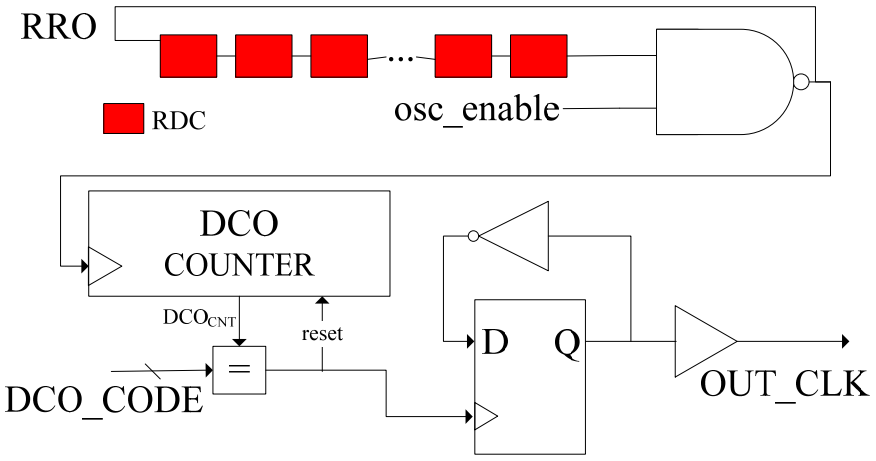


Fig. 3.3: The architecture of the DCO.

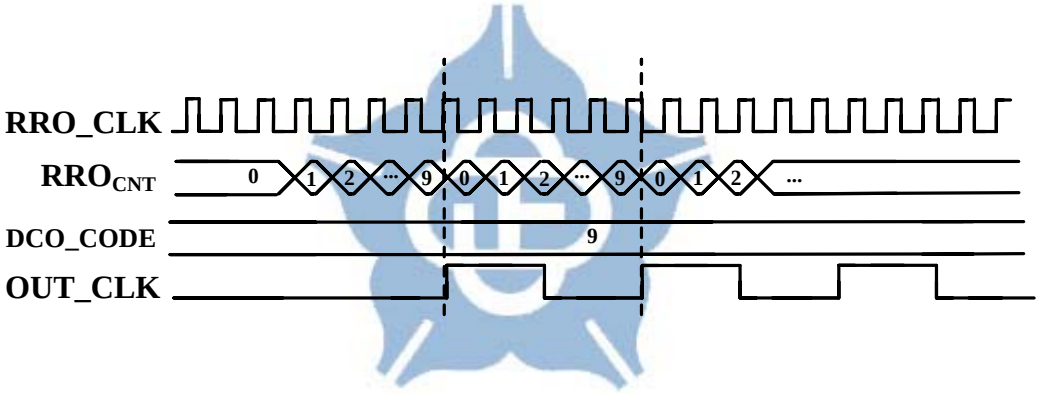


Fig. 3.4: Timing diagram of the DCO.

The proposed DCO architecture is shown in Fig. 3.3 [46] and Fig. 3.4 shows the timing diagram of the DCO. The output of the RRO triggers the DCO counter, and when the output value of the DCO counter equals to the input control code (DCO_CODE), a pulse is generated, and then the DCO counter is reset. To generate the output clock with a 50% duty cycle, a divided-by-2 circuit is added before output. The output frequency of the DCO can be expressed as follows by Eq. 3.5.

$$F_{DCO} = \frac{1}{2} * \frac{1}{P_{RRO}(P,V,T) * DCO\_CODE} \quad \text{(Eq. 3.5)}$$

where $P_{RRO}(P,V,T)$ is the period of the RRO, and F_{DCO} is the output frequency of the DCO. The period of RRO is easily affected by PVT variations, thus the input control code (DCO_CODE) can be used to adjust the output frequency with PVT variations.

3.4 Cell Selection Rules for Delay Ratio Estimator

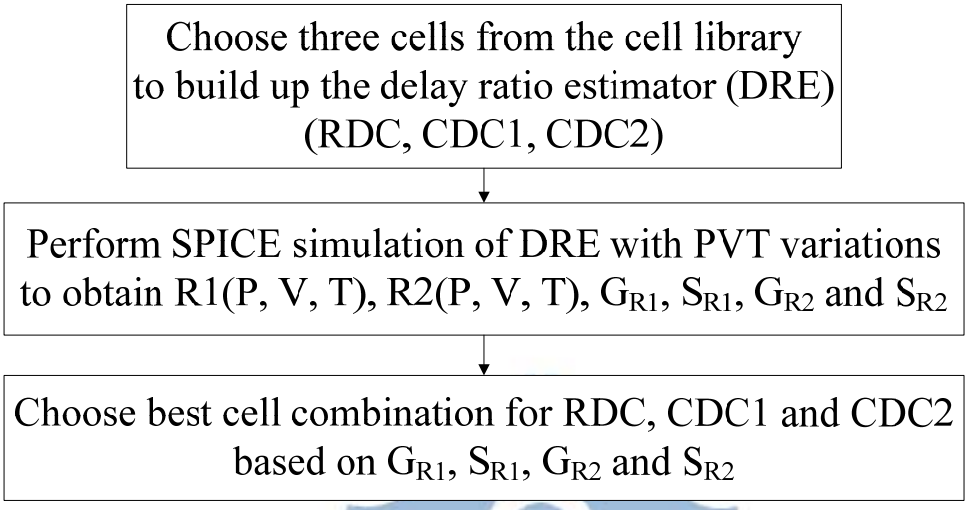


Fig. 3.5: Flow chart of how to choose cells from the cell library.

Fig. 3.5 shows the cell selection flow chart for RDC, CDC1, and CDC2. At first, any three logic cells are selected from the standard cell library to build up the delay ratio estimator DRE shown in Fig.3.1.

Subsequently, we need to perform SPICE simulation of the DRE with PVT variations to obtain delay ratios, R1(P,V,T) and R2(P,V,T). In this chapter, the voltage varies from V_1 to V_5 (V_1=0.90V, V_2=0.95V, V_3=1.00V, V_4=1.05V, and V_5=1.10V), and temperature varies from T_1 to T_4, (T_1=0ºC, T_2=25ºC, T_3=50ºC, and T_4=75ºC).

In addition, the process variations include typical process corner (TT), best process corner (FF), and worst process corner (SS). Therefore, it needs to simulate the DRE in totally 60=(3*5*4) different P,V,T combinations.

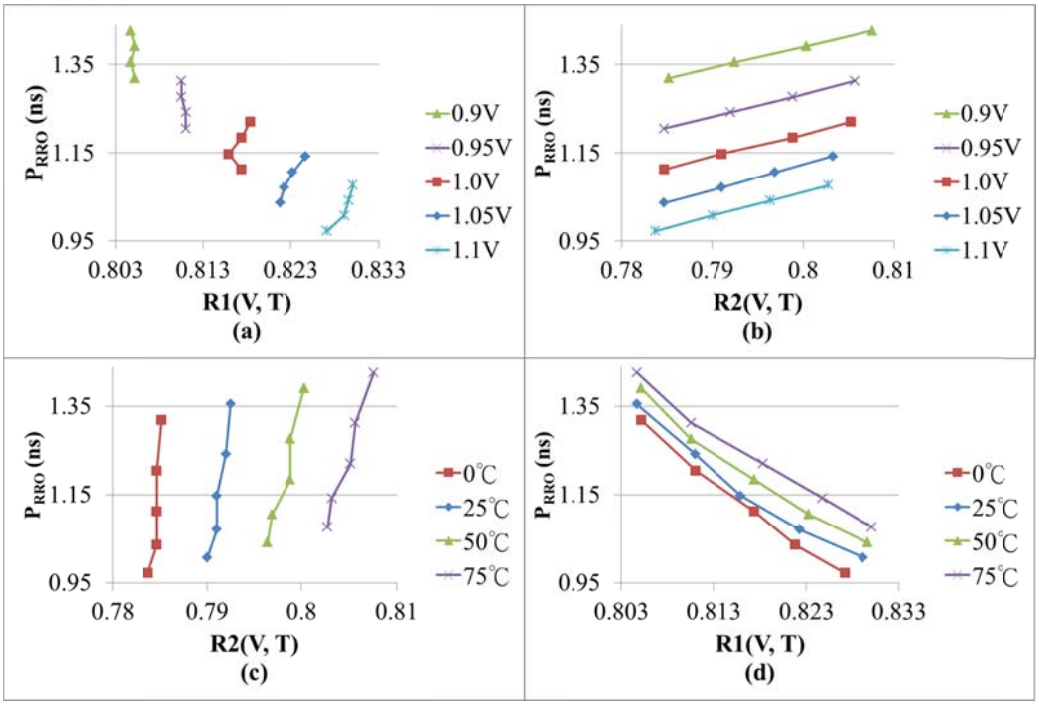


Fig. 3.6: Delay ratios R1(V, T) and R2(V,T) versus P_{RRO} (V,T) in typical process corner.

Fig. 3.6 shows the delay ratios R1(V,T) and R2 (V,T) versus the period of the RRO, P_{RRO}(V,T) in typical process corner. In Fig. 3.6(a), with a fixed voltage value, the delay ratio R1 varies with temperature variations.

ΔTT_{R1n} of Eq. 3.6 means the spacing between the R1 delay ratio curves with voltage V_n and voltage V_{n+1} in typical process corner. In Fig. 3.6(c), with a fixed temperature value, the delay ratio R2 varies with voltage variations. ΔTT_{R2j} of Eq. 3.7 means the spacing between the R2 delay ratio curves with temperature T_j and temperature T_{j+1} in typical process corner.

The values of ΔTT_{R1n} and ΔTT_{R2j} should be greater than zero, so that the delay ratios R1(V,T) and R2(V,T) can be used to roughly estimate the supply voltage and operation temperature at chip run time. Therefore, if the DRE fails to meet this requirement, the current cell combinations are dropped, and then, we need to choose other cell combinations and repeat the SPICE simulation of the DRE again.

$$\Delta TT_{R1n} = MIN(R1(TT, V_{n+1}, T)) - MAX(R1(TT, V_n, T)) \quad \text{(Eq. 3.6)}$$

$$\Delta TT_{R2j} = MIN(R2(TT, V, T_{j+1})) - MAX(R2(TT, V, T_j)) \quad \text{(Eq. 3.7)}$$

$$\sum_{n=1}^{4} = \Delta TT_{R1n} \quad \text{(Eq. 3.8)}$$

$$\sum_{j=1}^{3} = \Delta TT_{R2j} \quad \text{(Eq. 3.9)}$$

$$G_{R1} = \Delta TT_{R1} + \Delta SS_{R1} + \Delta FF_{R1} \quad \text{(Eq. 3.10)}$$

$$G_{R2} = \Delta TT_{R2} + \Delta SS_{R2} + \Delta FF_{R2} \quad \text{(Eq. 3.11)}$$

$$S_{R1} = Std(\Delta TT_{R1}, \Delta SS_{R1}, \Delta FF_{R1}) \quad \text{(Eq. 3.12)}$$

$$S_{R2} = Std(\Delta TT_{R2}, \Delta SS_{R2}, \Delta FF_{R2}) \quad \text{(Eq. 3.13)}$$

The DRE should be simulated with different process corners. In Eq. 3.10, G_{R1} of the current DRE is defined as the summation of ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1}, where ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1} are the summation of the R1(V,T) curve spacing in typical process corner, worst process corner, and best process corner, respectively.

Similarly, G_{R2} of the current DRE is defined as the summation of ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2}, where ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2} are the summation of the R2(V,T) curve spacing in typical process corner, worst process corner, and best process corner, respectively. In Eq. 3.12, S_{R1} is the standard deviation of ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1}, and S_{R2} is the standard deviation of ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2}.

We need to compute G_{R1}, G_{R2}, S_{R1}, and S_{R2} all possible cell combinations, and the cell combination with largest values of G_{R1} and G_{R2}, and smallest values of S_{R1}, S_{R2} is the best choice for design the DRE. However, if we cannot find this best choice, the cell combination with a larger G_{R1}value and smaller S_{R1} value is a better choice. In this chapter, we use a 90nm cell library to implement the DRE, and the best cell combination is

(AND3X1, NAND4XL, DLY1X1) for (RDC, CDC1, CDC2).

3.5 System Architecture

The proposed on-chip ring oscillator architecture which uses the relative reference modeling is shown in Fig. 3.7 [46], and Fig. 3.8 shows the timing diagram of this system architecture. It is composed of a delay ratio estimator (DRE), a voltage classifier, a temperature classifier, a linear calculator, and a digitally controlled oscillator (DCO). The DRE estimates the R1(V,T) and the R2(V,T) at chip run time under voltage and temperature variations.

In this chapter, we need to measure the values of R1(V,T), R2(V,T), and P_{RRO}(V,T) with five different voltages (V_1 to V_5) and four different temperatures (T_1 to T_4). Therefore, it needs to measure the values of R1(V,T), R2(V,T), and P_{RRO}(V,T) in totally 20 different (V,T) cases.

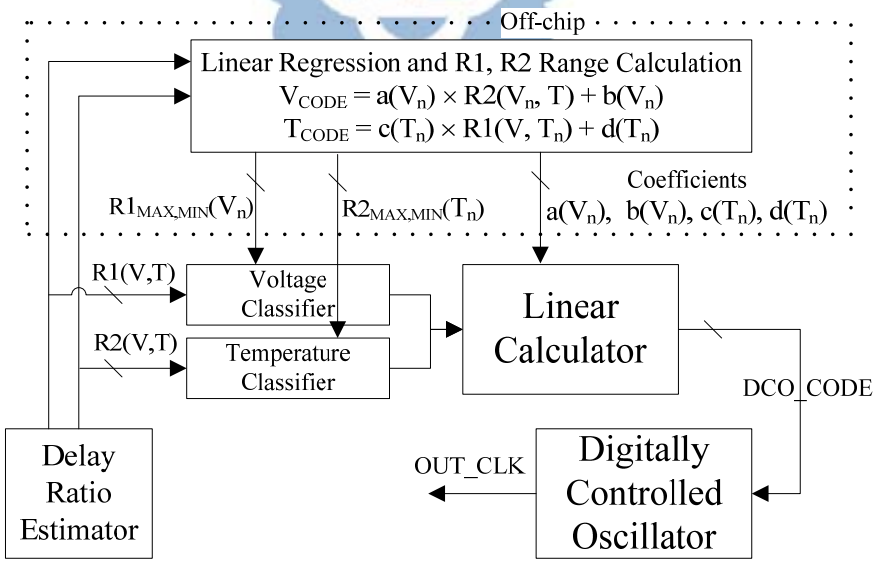


Fig. 3.7: System architecture of on-chip oscillator.

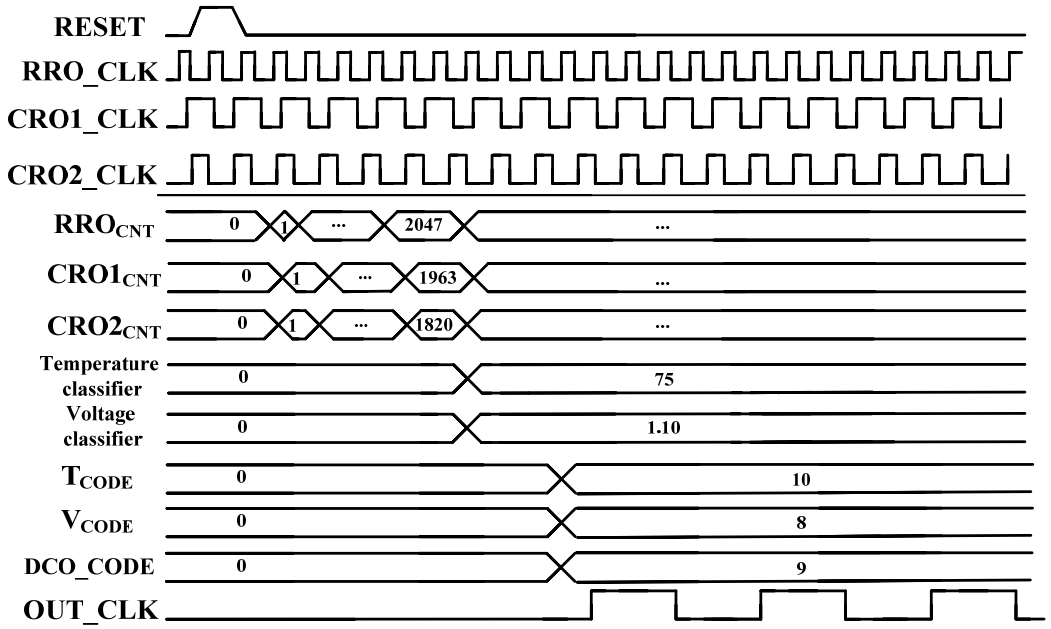


Fig. 3.8: Timing diagram of the System architecture.

The maximum value and minimum value of $R1(V_n, T)$ at voltage V_n with temperature variations (T_1 to T_4) will be found in the off-chip process, and are stored as $R1_{MAX}(V_n)$ and $R1_{MIN}(V_n)$, where V_n is V_1 to V_5. Similarly, the maximum value and minimum value of $R2(V, T_n)$ at temperature T_n with voltage variations (V_1 to V_5) will be found in the off-chip process, and are stored as $R2_{MAX}(T_n)$ and $R2_{MIN}(T_n)$, where T_n is T_1 to T_4.

In the off-chip process, we perform the linear regression on the $R2(V_n, T)$ versus DCO_CODE at voltage V_n to obtain the coefficients $a(V_n)$ and $b(V_n)$, where V_n is V_1 to V_5. In addition, we also perform the linear regression on the $R1(V, T_n)$ versus DCO_CODE at temperature T_n to obtain the coefficients $c(T_n)$ and $d(T_n)$, where T_n is T_1 to T_4. Thus there are totally 18 coefficients stored in the linear calculator for further voltage and temperature compensation at chip run time.

When the values of $R1_{MAX}(V_n)$, $R1_{MIN}(V_n)$, $R2_{MAX}(T_n)$, and $R2_{MIN}(T_n)$, $a(V_n)$, $b(V_n)$, $c(T_n)$, and $d(T_n)$ for V_1 to V_5 and T_1 to T_4 are determined in the off-chip process, the

proposed on-chip oscillator are now ready for generating the required target frequency (F_{DCO}).

At chip run time, the DRE estimates R1(V,T) and R2(V,T) with an unknown supply voltage (V) and an unknown operation temperature (T). The voltage classifier uses the $R1_{MAX}(V_n)$ and $R1_{MIN}(V_n)$ to roughly estimate the unknown supply voltage. For example, if R1(V,T) is smaller than $R1_{MAX}(V_2)$ but is larger than $R1_{MIN}(V_2)$, and then, the current supply voltage can be estimated as V_2. The temperature classifier uses the $R2_{MAX}(T_n)$ and $R2_{MIN}(T_n)$ to roughly estimate the unknown operation temperature. For example, if R2(V,T) is smaller than $R2_{MAX}(T_3)$ but is larger than $R2_{MIN}(T_3)$, and then, the current operation temperature can be estimated as T_3. Then, the linear calculator uses Eq. 3.14 and Eq. 3.15 to calculate two DCO control codes (V_{CODE} and T_{CODE}). Finally, the DCO control code for the DCO is the average of the V_{CODE} and T_{CODE} as follows Eq. 3.16.

$$V_{CODE} = \frac{1}{2} * \frac{1}{F_{DCO}} * \frac{1}{P_{RRO}(P,V,T)} = a(V_n) * R2(V_n, T) + b(V_n) \quad \text{(Eq. 3.14)}$$

$$T_{CODE} = \frac{1}{2} * \frac{1}{F_{DCO}} * \frac{1}{P_{RRO}(P,V,T)} = a(T_n) * R1(V, T_n) + d(T_n) \quad \text{(Eq. 3.15)}$$

$$DCO\_CODE = \frac{V_{CODE}+T_{CODE}}{2} \quad \text{(Eq. 3.16)}$$

In some special cases, for example, if R1(V,T) is smaller than $R1_{MIN}(V_3)$ but is larger than $R1_{MAX}(V_2)$, the voltage classifier can only determine the unknown supply voltage is between V_2 and V_3. In this case, the V_{CODE} can be expressed as Eq. 3.17. Similarly, if the temperature classifier determines the unknown operation temperature is between T_2 and T_3, the T_{CODE} can be expressed as Eq. 3.18.

$$V_{CODE} = \frac{a(V_2)+a(V_3)}{2} * R2(V,T) + \frac{b(V_2)+b(V_3)}{2} \quad \text{(Eq. 3.17)}$$

$$T_{CODE} = \frac{c(T_2)+c(T_3)}{2} * R1(V,T) + \frac{d(T_2)+d(T_3)}{2} \quad \text{(Eq. 3.18)}$$

3.6 Experimental Results

The proposed on-chip oscillator circuit is implemented in a standard 90nm 1P9M CMOS process. The operating voltage ranges from 0.90V to 1.10V, and temperature range is from 0ºC to 75ºC. The layout of the test chip is shown in Fig. 3.9. The active area is 180μm×180μm, and chip area including I/O pads is 830μm×830μm.

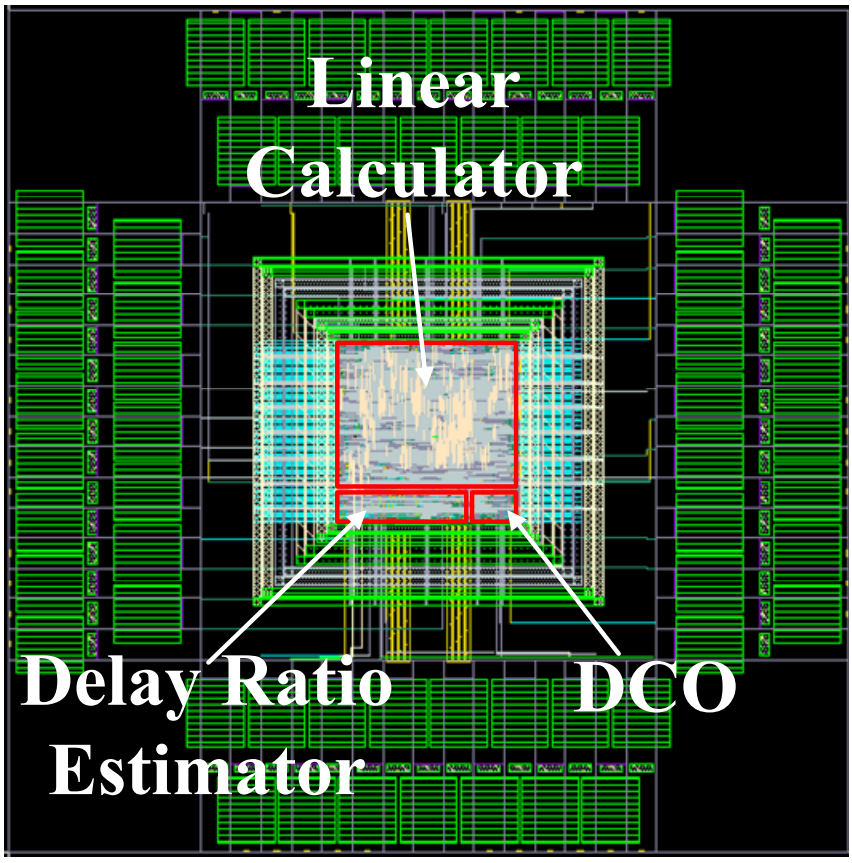


Fig. 3.9: Layout of the test chip.

Figs. 3.10 and 3.11 show the output frequency of the proposed on-chip oscillator with PVT variations. The target frequency is 5MHz. The frequency error of the proposed on-chip oscillator with temperature variations is 0.21% in typical process corner. The maximum frequency error of the proposed design with voltage variations is 0.97% in typical process corner. The maximum output frequency error with PVT variations ranges from -2.83% to +2.49%.

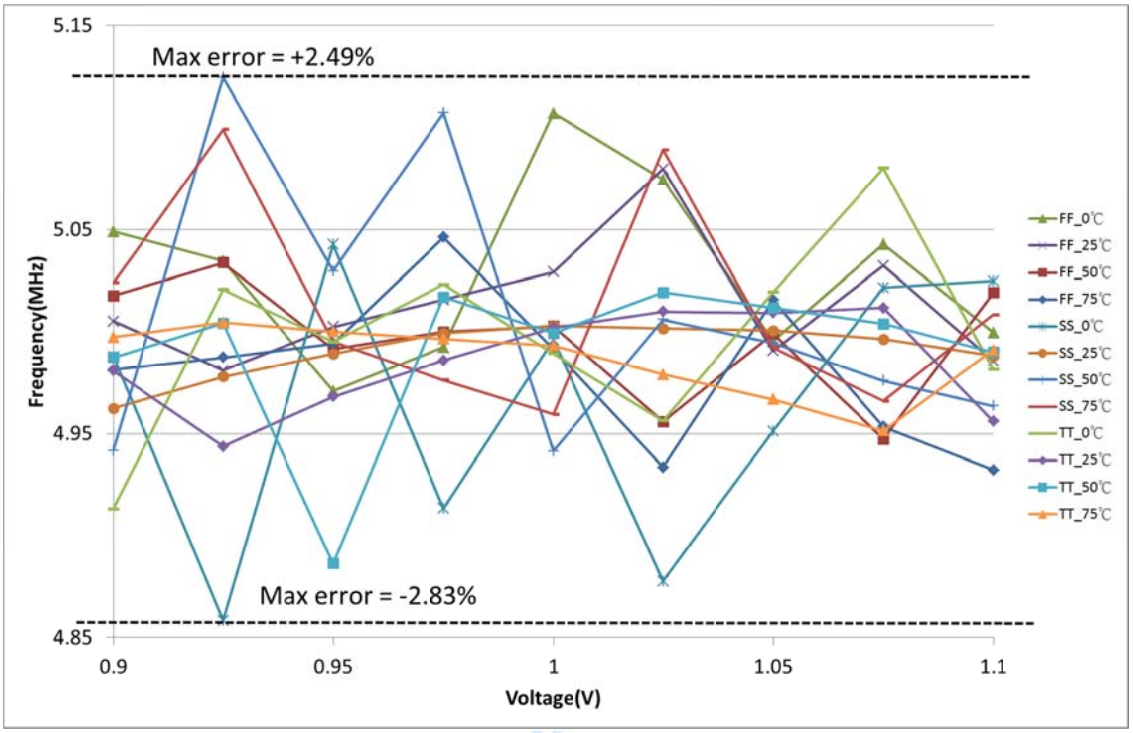


Fig. 3.10: Output frequency with PVT variations (x-axis is voltage).

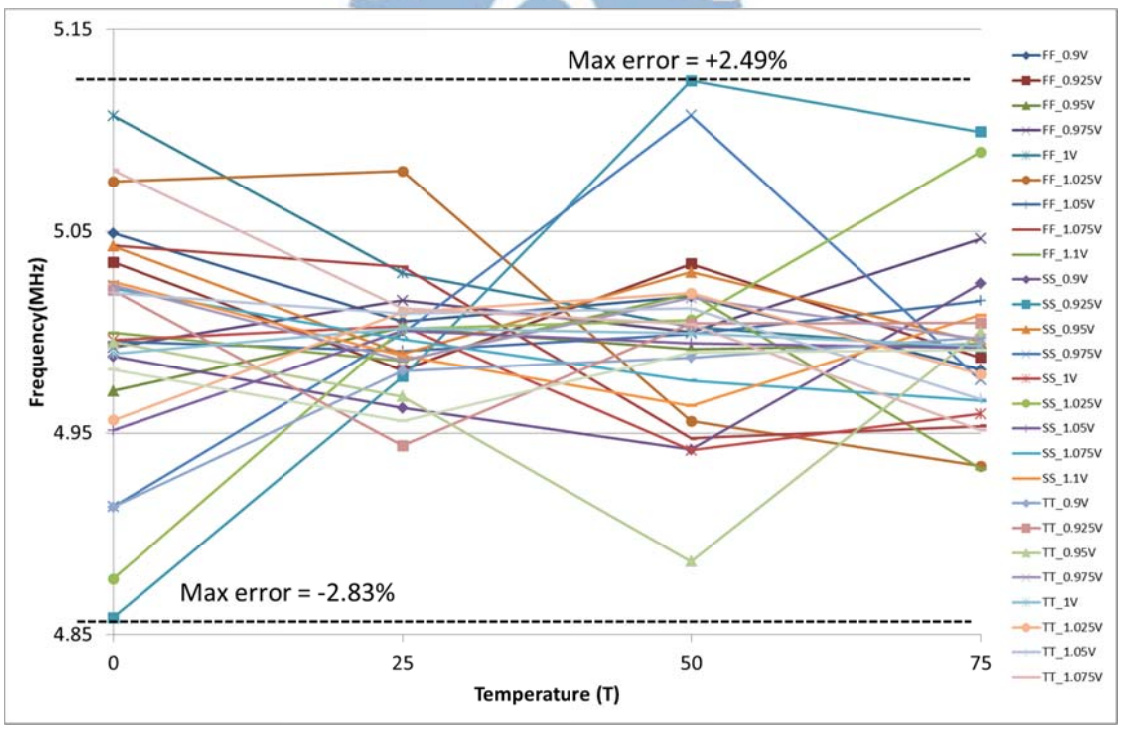


Fig. 3.11: Output frequency with PVT variations (x-axis is temperature).

3.7 Summary of the Proposed CBOCSO with Multi-Point Calibration

In this chapter, a 5MHz cell-based on-chip silicon oscillator is presented. The maximum frequency error with temperature and voltage variations are 0.21% and 0.97%, respectively.

The proposed on-chip oscillator with a relative modeling uses the voltage and temperature classifier to roughly estimate the supply voltage and operation temperature at chip run time.

Therefore, the frequency error can be significant reduced by a linear equation-based compensation approach. The proposed design can be implemented by standard cells, and we also propose the cell selection rules to choose the cells for the delay ratio estimator. As a result, the proposed design provides a systematic way to automatically generate the on-chip oscillator with PVT variations tolerance. Thus the proposed design can operate with a low supply voltage, and is very suitable for low-power and low-cost system-on-a-chip application.

However, in this version, we need to perform multi-point calibration after chip fabrication. Thus in the chapter 4, we proposed a new version design with only four-point calibration to reduce the testing cost.

Chapter 4

Cell-Based On-Chip Silicon Oscillator with Four-point calibration

4.1 Design of Delay Ratio Estimator

The block diagram of the proposed delay ratio estimator (DRE) is shown in Fig. 4.1 and 4.2 show the timing diagram of the DRE. In chapter 3, the frequency of RRO, CRO1 and CRO2 of DRE are set to 1.0 GHz and the value of N_{TIME} is set to 2047. In this chapter, the frequencies of RRO, CRO1 and CRO2 of DRE are slow down to about 200MHz for reducing power consumption and the value of N_{TIME} is set to 1023.

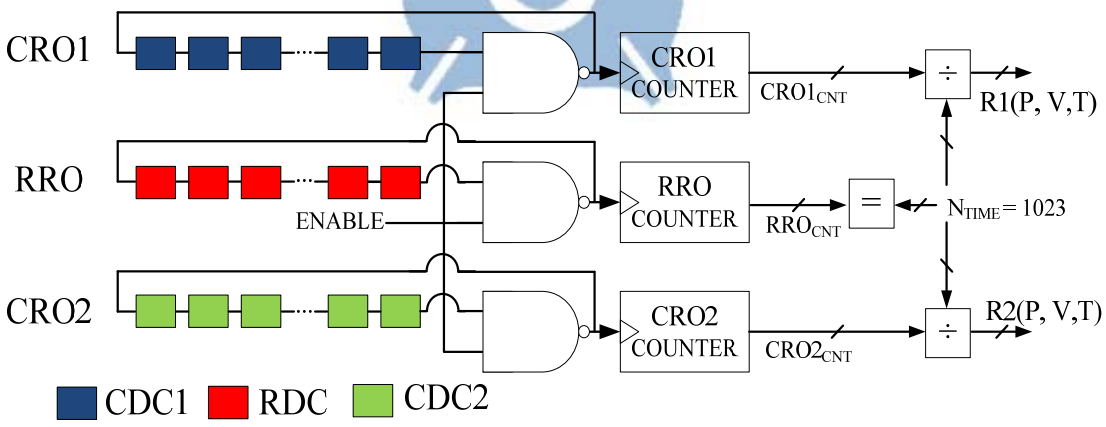


Fig. 4.1: The architecture of delay ratio estimator.

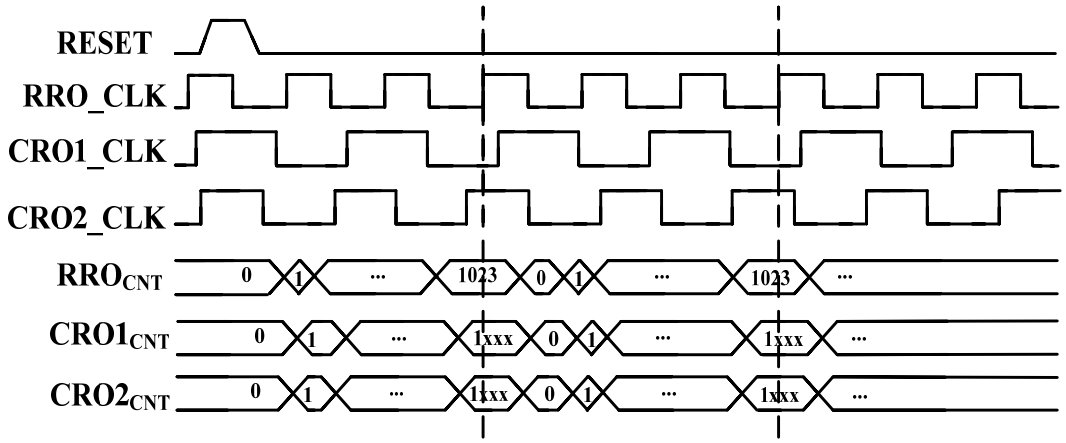


Fig. 4.2: Timing diagram of the delay ratio estimator.

4.2 Design of Fine Tune Delay line

In chapter 3, the frequency error of the period cell-based on-chip silicon oscillator (CBOCSO) with multi-points calibration is from -2.83% to +2.49%.

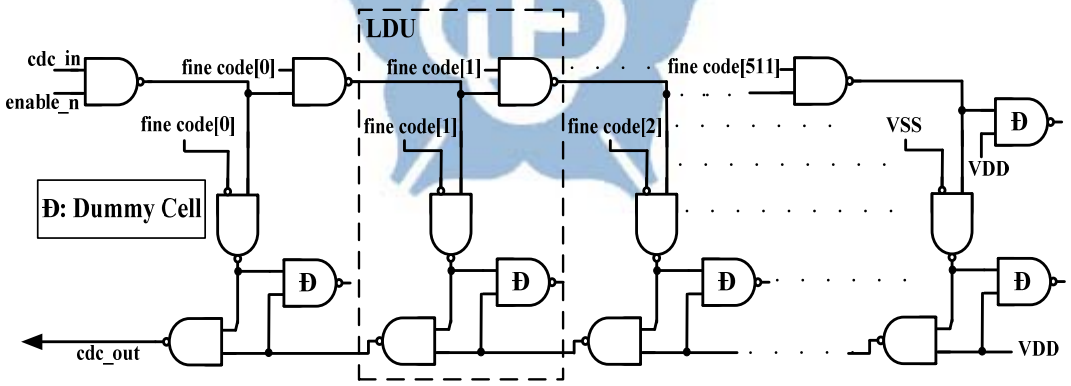


Fig. 4.3: The proposed fine delay line.

In order to decrease the output frequency error of the CBOCSO, it is necessary to improve the digitally controlled oscillator (DCO) resolution. Thus, we propose a fine-tuning circuit [36] which is design with standard cells as shown in Fig. 4.3 and add it to the proposed DCO. This fine-tuning circuit consists of 512 lattice delay unit (LDU). The LDU is composed with four NAND-gates, and this LDU can achieve the same function with one

NAND-gate and one inverted-multiplexer. With this approach, the fine-tuning resolution can enhance to two NAND-gates delay time, and the intrinsic delay is three NAND-gates delay time. In addition, the NAND-gate transition time is very small because it can be composed with only four transistors. This technique can make the DCO output frequency becomes more linearly.

4.3 Design of Digital Control Oscillator

The modified DCO architecture is shown in Fig. 4.4, and Fig. 4.5 shows the timing diagram of the DCO. The output of the CRO2 triggers the DCO counter, and when the output value of the DCO counter equals to the input control code (COARSE_CODE), the signal cdc_in of fine tune circuit will set to high. According to the fine code (0 to 511), the fine tune delay circuit can insert different delay between cdc_in and cdc_out. After the fine tune delay circuit, the cdc_out pulse will trigger a D flip-flop, a pulse is generated, and then the DCO counter.

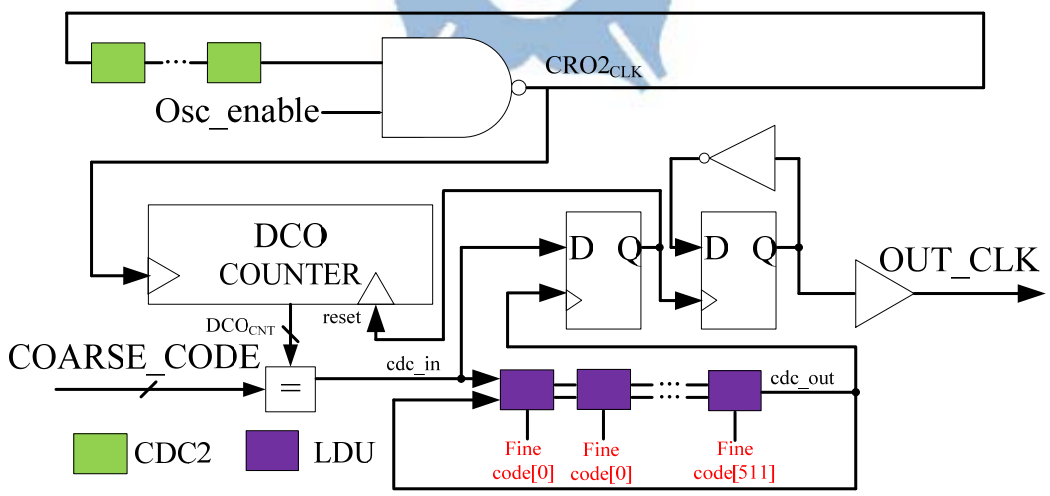


Fig. 4.4: The architecture of the DCO includes coarse-tuning and fine-tuning stages.

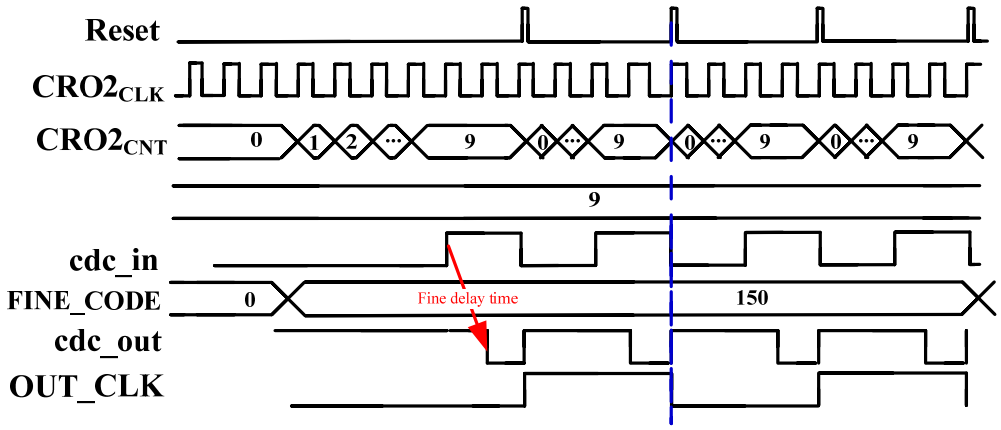


Fig. 4.5: Timing diagram of the DCO coarse-tuning and fine-tuning stages.

To generate the output clock with a 50% duty cycle, a divided-by-2 circuit is added before output. The output frequency of the DCO can be expressed as follows by Eq. 4.1.

$$F_{DCO} = \frac{1}{2} * \frac{1}{P_{CRO2}(P,V,T)*COARSE\_CODEe+Fine\_code*P_{LDU}(P,V,T)+intrinsic\ delay} \text{(Eq. 4.1)}$$

where $P_{CRO2}(P,V,T)$ is the period of the CRO2, $P_{LDU}(P,V,T)$ is the delay time of the two NANDs delay cell which is fine tuning resolution, intrinsic delay is delay time of the three NANDs delay cell, and F_{DCO} is the output frequency of the DCO. The period of CRO2 and fine tuning delay circuit are easily affected by PVT variations with a fixed COARSE_CODE. Thus, the input control code (Fine_code) can be used to adjust the output frequency with PVT variations.

4.4 Cell Selection Rules for Delay Ratio Estimator

Fig. 4.6 shows the cell selection flow chart for RDC, CDC1, and CDC2. At first, any three logic cells are selected from the standard cell library to build up the delay ratio estimator.

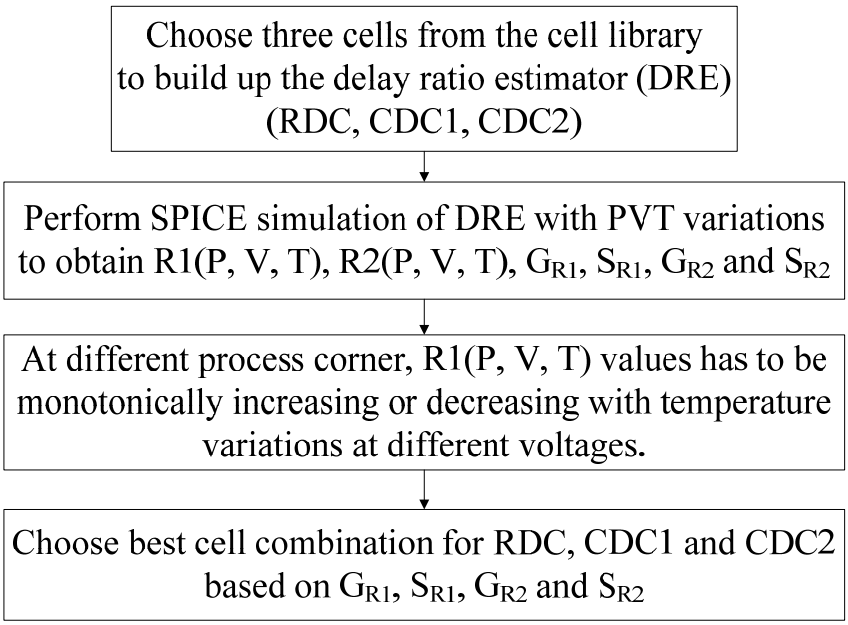


Fig. 4.6: Flow chart of how to choose cells from the cell library.

Subsequently, we need to perform SPICE simulation of the DRE with PVT variations to obtain the delay ratios, R1(P,V,T) and R2(P,V,T). In this chapter, the voltage varies from V_1 to V_9 (V_1=0.900V, V_2=0.925V, V_3=0.950V, V_4=0.975V, V_5=1.000V, V_6=1.025V, V_7=1.050V, V_8=1.075V, and V_9=1.100V), and temperature varies from T_1 to T_4, (T_1=0ºC, T_2=25ºC, T_3=50ºC, and T_4=75ºC). In addition, the process variations include typical process corner (TT), best process corner (FF), and worst process corner (SS). Therefore, it needs to simulate the DRE in totally 108=(3*9*4) different P,V,T combinations.

The cell selection rule is different from section 3.4 and we add a rule for cell selection. The new rule is that the R1(P,V,T) values is required to be monotonically increasing or decreasing with temperature variations at different voltages. With temperature variations, the R1(P,V,T) curves may have overlap region at different voltages. In order to solve this problem, we can narrow down the temperature range, but we will not do it. Instead, we improve the cell selection rules. Thus we can use the estimated temperature to estimate the supply voltage.

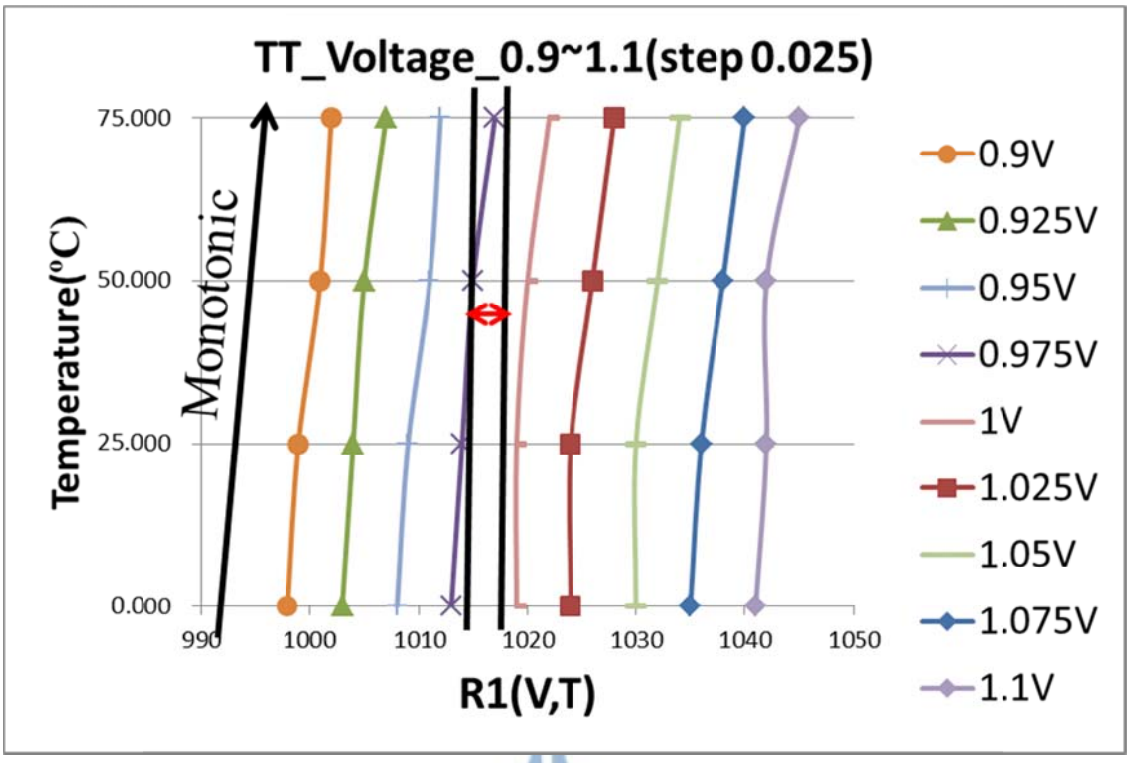


Fig. 4.7: Delay ratios R1(V, T) versus temperature with voltage and temperate variations in typical process corner.

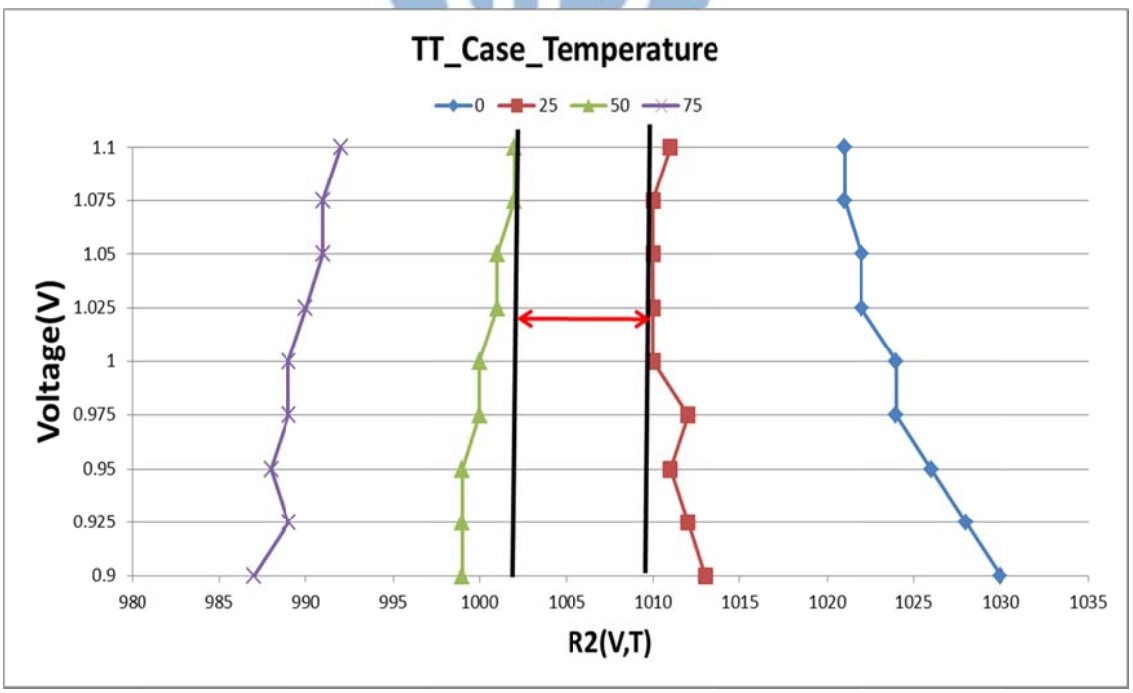


Fig. 4.8: Delay ratios R2(V, T) versus voltage with voltage and temperate variations in typical process corner.

Fig. 4.7 shows the delay ratios R1(V,T) versus temperature at different voltage in typical process. ΔTT_{R1n} of Eq. 4.2 means the spacing between the delay ratio R1 curves with voltage V_n and voltage V_{n+1} in typical process corner. If the delay ratios R1(V, T) is not monotonically increasing with temperature variation at different voltage, the delay ratio R1 cell combination can be dropped.

Fig. 4.8 shows the delay ratios R2(V,T) versus voltage at different temperature in typical process. In Fig. 4.8, with a fixed temperature value, the delay ratio R2 varies with voltage variations. ΔTT_{R2j} of Eq. 4.3 means the spacing between the R2 delay ratio curves with temperature T_j and temperature T_{j+1} in typical process corner. The values of ΔTT_{R1n} and ΔTT_{R2j} should be greater than zero, so that the delay ratios R1(V,T) and R2(V,T) can be used to roughly estimate the supply voltage and operation temperature at chip run time. Therefore, if the DRE fails to meet this requirement, the current cell combinations are dropped, and then, we need to choose other cell combinations and repeat the SPICE simulation of the DRE again.

$$\Delta TT_{R1n} = R1(TT, V_{n+1}, T_4) - R1(TT, V_n, T_1) \quad \text{(Eq. 4.2)}$$

$$\Delta TT_{R2j} = MIN(R2(TT, V, T_{j+1})) - MAX(R2(TT, V, T_j)) \quad \text{(Eq. 4.3)}$$

$$\sum_{n=1}^{8} = \Delta TT_{R1n} \quad \text{(Eq. 4.4)}$$

$$\sum_{j=1}^{3} = \Delta TT_{R2j} \quad \text{(Eq. 4.5)}$$

$$G_{R1} = \Delta TT_{R1} + \Delta SS_{R1} + \Delta FF_{R1} \quad \text{(Eq. 4.6)}$$

$$G_{R2} = \Delta TT_{R2} + \Delta SS_{R2} + \Delta FF_{R2} \quad \text{(Eq. 4.7)}$$

$$S_{R1} = Std(\Delta TT_{R1}, \Delta SS_{R1}, \Delta FF_{R1}) \quad \text{(Eq. 4.8)}$$

$$S_{R2} = Std(\Delta TT_{R2}, \Delta SS_{R2}, \Delta FF_{R2}) \quad \text{(Eq. 4.9)}$$

The DRE should be simulated with different process corners. In Eq. 4.6, G_{R1} of the current DRE is defined as the summation of ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1}, where ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1} are the summation of the R1(V,T) curve spacing in typical process corner, worst process corner, and best process corner, respectively.

Similarly, G_{R2} of the current DRE is defined as the summation of ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2}, where ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2} are the summation of the R2(V,T) curve spacing in typical process corner, worst process corner, and best process corner, respectively. In Eq. 4.8, S_{R1} is the standard deviation of ΔTT_{R1}, ΔSS_{R1}, and ΔFF_{R1}, and S_{R2} is the standard deviation of ΔTT_{R2}, ΔSS_{R2}, and ΔFF_{R2}. We need to compute G_{R1}, G_{R2}, S_{R1}, and S_{R2} of all possible cell combinations, and the cell combination with largest values of G_{R1} and G_{R2}, and smallest values of S_{R1}, S_{R2} is the best choice for design the DRE. However, if we cannot find this best choice, the cell combination with a larger G_{R1}value and smaller S_{R1} value is a better choice. In this chapter, we use a 90nm cell library to implement the DRE, and the best cell combination is (MXI4X2, NOR4BBX1,NAND3BXL) for (RDC, CDC1, CDC2).

4.5 Algorithm of Four-point Calibration

In this section, the voltage varies from V_1 to V_9 (V_1=0.900V, V_2=0.925V, V_3=0.950V, V_4=0.975V, V_5=1.000V, V_6=1.025V, V_7=1.050V, V_8=1.075V, and V_9=1.100V), and temperature varies from T_1 to T_4, (T_1=0ºC, T_2=25ºC, T_3=50ºC, and T_4=75ºC). The DRE estimates the R1(V,T) and the R2(V,T) at chip run time under voltage and temperature variations. The voltage classifier will compare R1(V,T) and $R1_{det}(V_n)$ to determine which $R1_{det}(V_n)$ is close to R1(V,T). For example, if the $R1_{det}(V_3)$ is closed to R1(V,T), the voltage classifier estimates supply voltage is V_3. Similarly, The temperature classifier will compare R2(V,T) and $R2_{det}(T_n)$, to determine which $R2_{det}(T_n)$ is close to R2(V,T). For example, if the $R2_{det}(T_1)$ is closed to R2(V,T), the operating classifier estimates operating temperature is T_1.

When the supply voltage and the operating temperature are determined, the linear calculator uses coefficient $a(V_n)$ and $b(V_n)$ to calculate the DCO control code (FINE_CODE). Therefore, we need these values at chip run time ($R1_{det}(V_n)$, $R2_{det}(T_n)$, $a(V_n)$, and $b(V_n)$). In the following section, we will introduce how to automatically calculate these values with four-point calibration.

In the calibration mode, we need to measure the values of R1(V,T), R2(V,T), and the period of the OUT_CLK with different two voltages and four different temperatures (V_3,T_2), (V_3,T_4), (V_7,T_1), (V_7,T_3). Therefore, it needs to measure the values of R1(V,T), R2(V,T), and the period of the OUT_CLK in totally four different (V,T) cases. The on-chip oscillator needs to against voltage variations from V_1 (0.90V) to V_9 (1.10V). If the calibration point is V_5 (1.00V), the voltage variation range is 10%. However, if we choose calibration points at V_3 (0.95V) and V_7 (1.05V), the range of voltage variation can be reduced to 5%.

Fig. 4.9 shows the delay ratios R1(V,T) versus temperature at different voltage in typical process, and in this example, we explain how to estimate the threshold value $R1_{det}(V_3)$ and $R1_{det}(V_7)$.

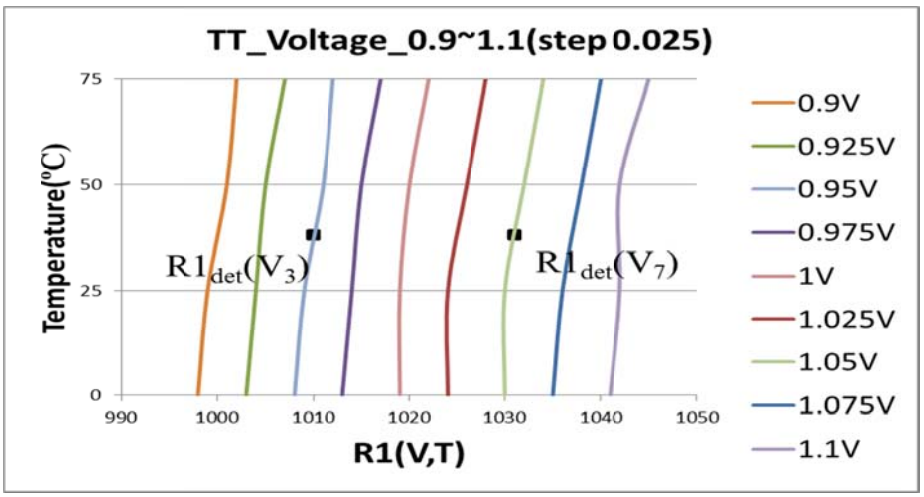


Fig. 4.9: The voltage classifier estimates current voltage value with $R1_{det}(V_3)$ and $R1_{det}(V_7)$ in typical process corner.

In the calibration mode, we measure the value of R1(V,T), R2(V,T), and the period of OUT_CLK at totally 4 different (V,T) cases (V_3,T_2), (V_3,T_4), (V_7,T_1), (V_7,T_3). Then the $R1_{det}(V_3)$ and $R1_{det}(V_7)$ can be estimated as Eq. 4.10 and Eq. 4.11.

$$R1_{det}(V_3) = round(\frac{R1(V_3,T_2)+R1(V_3,T_4)}{2}) \quad \text{(Eq. 4.10)}$$

$$R1_{det}(V_7) = round(\frac{R1(V_7,T_1)+R1(V_7,T_3)}{2}) \quad \text{(Eq. 4.11)}$$

Fig. 4.10 shows the delay ratios R1(V,T) versus temperature at different voltage in typical process corner, and in this example, we explain how to estimate threshold voltage value $R1_{det}(V_1)$ to $R1_{det}(V_9)$.

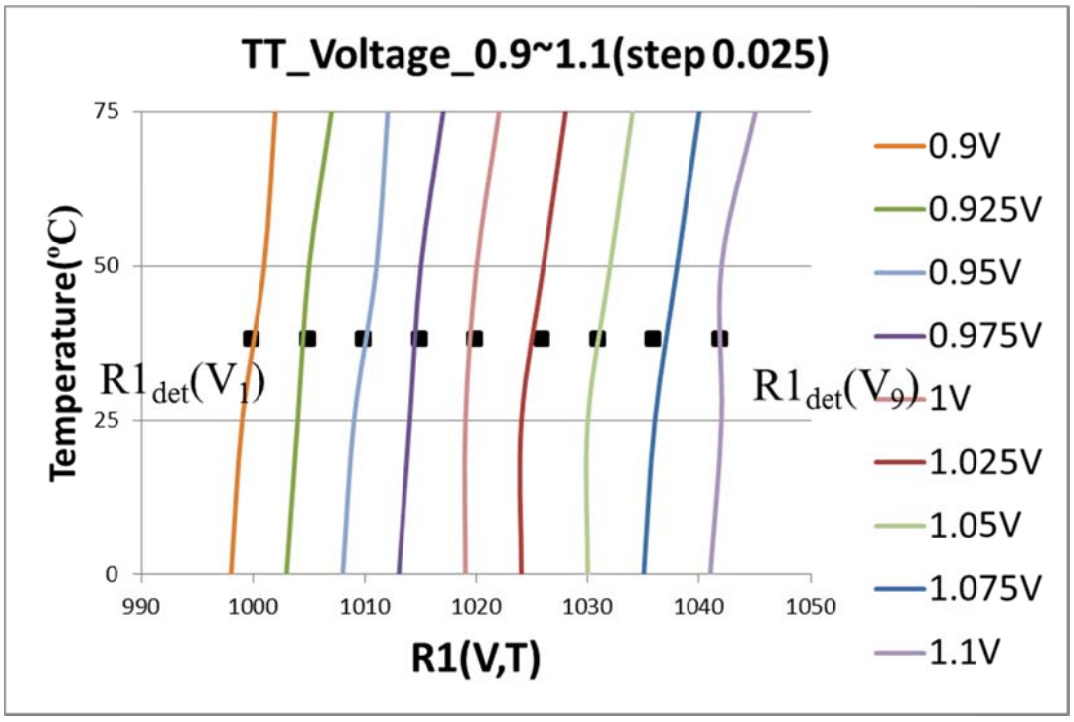


Fig. 4.10: The voltage classifier estimates voltage value $R1_{det}(V_1)$ to $R1_{det}(V_9)$ in typical process corner.

After computation of $R1_{det}(V_3)$ and $R1_{det}(V_7)$, the $R1_{det}(V_1)$ to $R1_{det}(V_9)$ can be calculated by interpolation and extrapolation method. The $R1_{det}(V_1)$ to $R1_{det}(V_9)$ can be expressed as Eq. 4.12 to Eq. 4.18.

$$R1_{det}(V_1) = R1_{det}(V_3) - \frac{R1_{det}(V_3)+R1_{det}(V_7)}{2} \quad \text{(Eq. 4.12)}$$

$$R1_{det}(V_2) = R1_{det}(V_3) - \frac{R1_{det}(V_3)+R1_{det}(V_7)}{4} \quad \text{(Eq. 4.13)}$$

$$R1_{det}(V_4) = R1_{det}(V_3) + \frac{R1_{det}(V_3)+R1_{det}(V_7)}{4} \quad \text{(Eq. 4.14)}$$

$$R1_{det}(V_5) = R1_{det}(V_3) + \frac{R1_{det}(V_3)+R1_{det}(V_7)}{2} \quad \text{(Eq. 4.15)}$$

$$R1_{det}(V_6) = R1_{det}(V_7) - \frac{R1_{det}(V_3)+R1_{det}(V_7)}{4} \quad \text{(Eq. 4.16)}$$

$$R1_{det}(V_8) = R1_{det}(V_7) + \frac{R1_{det}(V_3)+R1_{det}(V_7)}{4} \quad \text{(Eq. 4.17)}$$

$$R1_{det}(V_9) = R1_{det}(V_7) + \frac{R1_{det}(V_3)+R1_{det}(V_7)}{2} \quad \text{(Eq. 4.18)}$$

Then $R1_{det}(V_n)$ has been calculated. At chip run time, the voltage classifier will compare R1(V,T) and $R1_{det}(V_n)$ and determines which $R1_{det}(V_n)$ is closed to R1(V,T). For example, if the $R1_{det}(V_8)$ is closed to R1(V,T), the voltage classifier estimates supply voltage is V_8.

We need to measure the DCO period of OUT_CLK at two fine_codes: 0 and 511 with coarse code(Δcode) to obtain coarse-tuning resolution of the DCO at (V3,T2), (V3,T4), (V7,T1), (V7,T3). The period of OUT_CLK with fine tune delay circuit set to maximum and minimum delay can be expressed as Eq. 4.19 and Eq. 4.20.

$$MIN\_P_{OUT\_CLK} = FINE_{INT} + Fine\_code(0) * FINE_{RES} + \Delta C_{CODE} * C_{RES} \quad \text{(Eq. 4.19)}$$

$$MAX\_P_{OUT\_CLK} = FINE_{INT} + Fine\_code(511) * FINE_{RES} + \Delta C_{CODE} * C_{RES} \quad \text{(Eq. 4.20)}$$

Table 4.1: The terms in Eq. 4.19 to Eq. 4.25.

name	**description**
$FINE_{RES}$	fine tuning resolution
$FINE_{INT}$	intrinsic delay of the fine-tuning circuit
C_{RES}	coarse tuning resolution
ΔC_{CODE}	coarse code by simulation
C_{CODE}	coarse code by calculation
$MAX\_P_{OUT\_CLK}$	period with max fine tuning control code
$MIN\_P_{OUT\_CLK}$	Period with min fine tuning control code

Table 4.1 shows the terms used in Eq. 4.19 to Eq. 4.25. When we have the maximum period and the minimum period of OUT_CLK with coarse code(Δco de), we can calculate the corresponding on-chip oscillator control code (Fine_code). The control code can be expressed as Eq. 4.21 to Eq. 4.25. We can use the maximum period and the minimum period of OUT_CLK to calculate the fine tuning resolution. In Eq. 4.21, the fine tuning resolution is two NAND delay time as indicated in Fig. 4.3. In Eq. 4.22, we use the simulation coarse code (ΔC_{CODE}) to calculate the coarse tuning resolution. The intrinsic delay of the fine-tuning circuit is three NAND delay fine as indicated in Fig.4.3. Thus, the intrinsic delay of fine-tuning circuit can be expressed as Eq. 4.23. In Eq. 4.24, the coarse code (C_{CODE}) calculation will produce decimal point. Thus, we will eliminate the decimal point by Gaussian function.

$$FINE_{RES} = \frac{MAX\_P_{OUT\_CLK} - MIN\_P_{OUT\_CLK}}{511} \quad \text{(Eq. 4.21)}$$

$$C_{RES} = \frac{MIN\_P_{OUT\_CLK} - FINE_{INT}}{\Delta C_{CODE}} \quad \text{(Eq. 4.22)}$$

$$FINE_{INT} = FINE_{RES} * 1.5 \quad \text{(Eq. 4.23)}$$

$$C_{CODE} = \left\lfloor \frac{MIN\_P_{OUT\_CLK} - F_{INT} - Fine\_code(0) * F_{RES}}{C_{RES}} \right\rfloor - 1 \quad \text{(Eq. 4.24)}$$

$$Fine\_code = \frac{\frac{1}{2} * \frac{1}{F_{DCO}} - C_{CODE} * C_{RES} - FINE_{INT}}{FINE_{RES}} \quad \text{(Eq. 4.25)}$$

In Eq. 4.25 F_{DCO} is the output frequency of the DCO shown in Fig. 4.4. In this thesis, we expected the output frequency is 5MHz (200ns). When we fix a coarse code, the input control code (Fine_code) can be used to adjust the output frequency with PVT variations.

Fig. 4.11 shows R2(V,T) versus fine_code with voltage variations at different temperature values in typical process corner, and the temperature classifier estimates the threshold value $R2_{det}(T_1)$ to $R2_{det}(T_4)$. We measure the value of R2(V,T) at (V_3,T_2), (V_3,T_4), (V_7,T_1), and (V_7,T_3) as $R2_{det}(T_1)$, $R2_{det}(T_2)$, $R2_{det}(T_3)$, and $R2_{det}(T_4)$, respectively. At this time, $R2_{det}(T_n)$ has been determined. At chip run time, The temperature classifier will compare R2(V,T) and $R2_{det}(T_n)$ to determine which $R2_{det}(T_n)$ is close to R2(V,T). For example, if the $R2_{det}(T_3)$ is closed to R2(V,T), the temperature classifier estimates operating temperature is T_3.

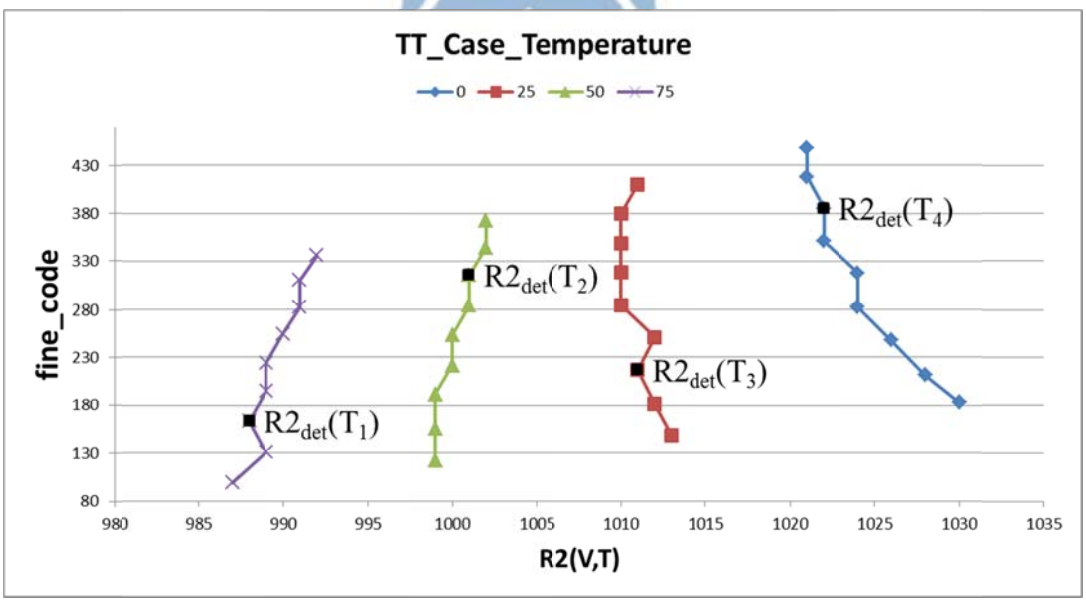


Fig. 4.11: The R2(V,T) versus fine_code with voltage variation at different temperature in typical process corner.

If we connect the points with the same voltage, we can redraw Fig. 4.11 as Fig. 4.12. However, since we only perform four-point calibration, Fig.4.13 shows the linear regression equation with two points measured at two voltages. In the off-chip process, we perform the two linear regression at the two voltages V_3 and V_7. First, we perform a linear regression of $R2(V_3, T_2)$ and $R2(V_3, T_4)$ versus fine_code to obtain the coefficients $a(V_3)$ and $b(V_3)$, similarly, we perform a linear regression of $R2(V_7, T_1)$ and $R2(V_7, T_3)$ versus fine_code to obtain the coefficients $a(V_7)$ and $b(V_7)$.

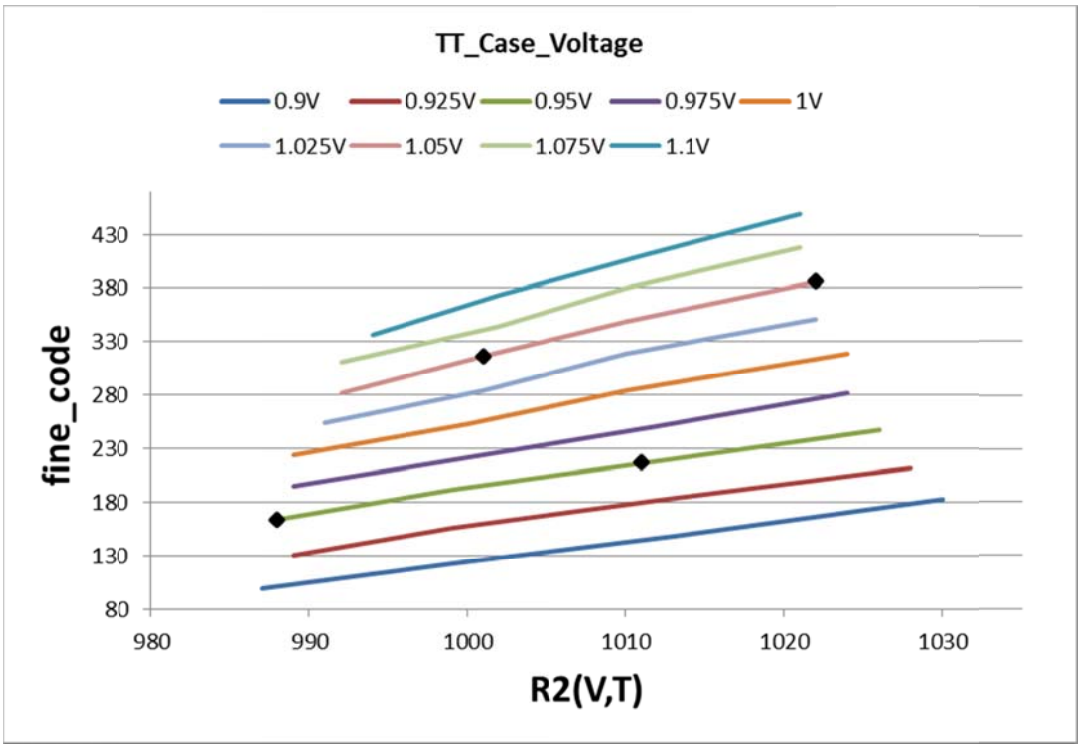


Fig. 4.12: The value R2(V,T) each point connected into lines with temperature variation at different voltages in typical process corner.

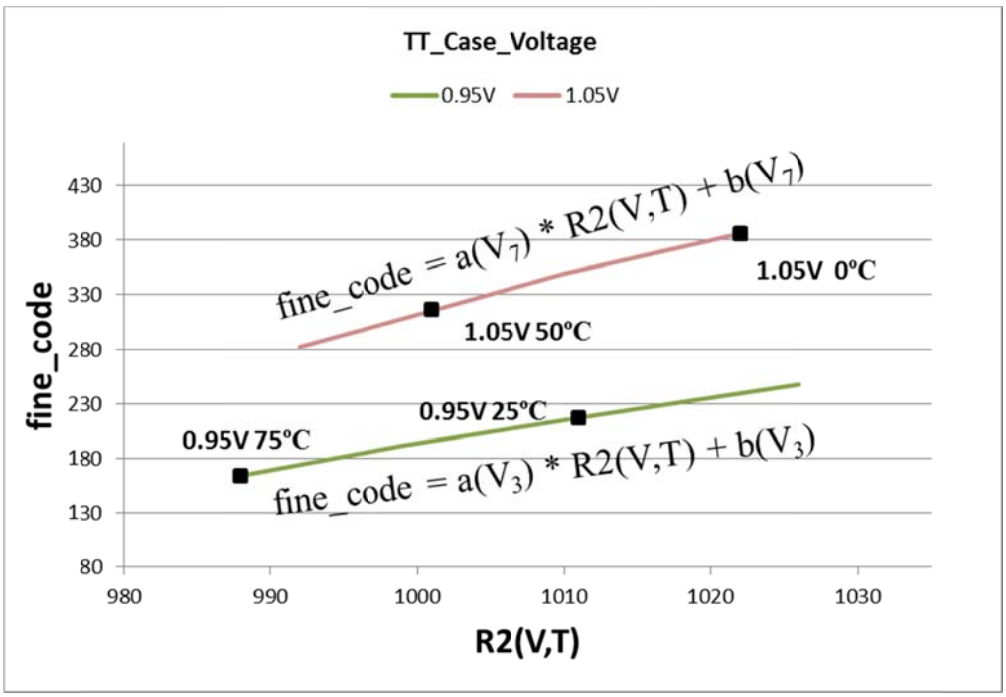


Fig. 4.13: The linear regression equation with two points measured at two voltages.

Fig. 4.14 shows each line with temperature variations at different voltage can be obtained by interpolation and extrapolation method.

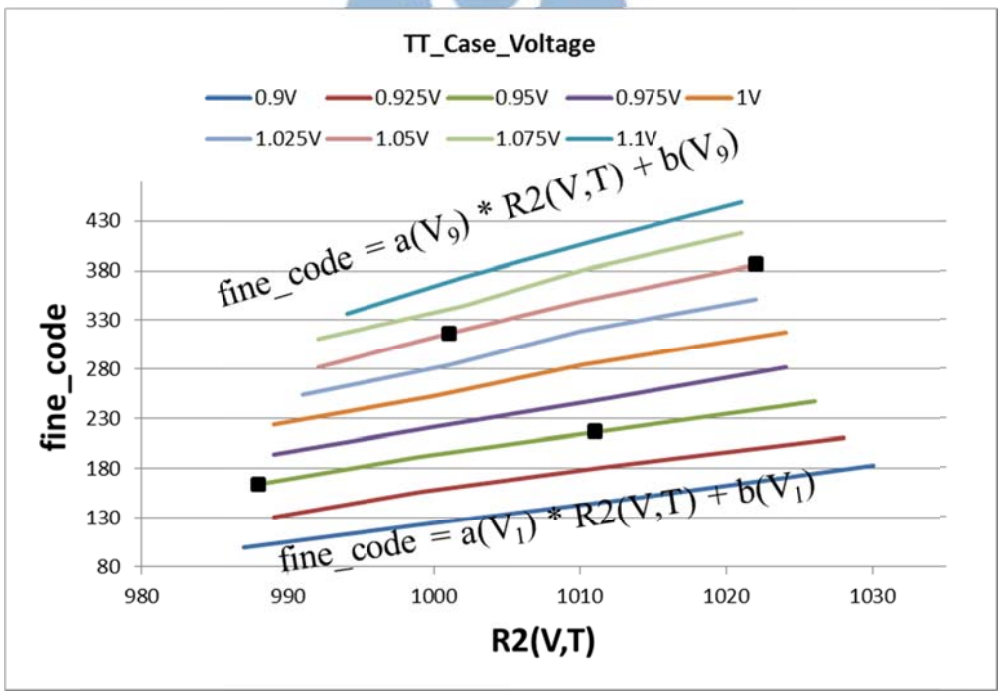


Fig. 4.14: Each line with temperature variations can be obtained at different voltages.

After computation of the coefficients $a(V_3)$, $b(V_3)$, $a(V_7)$ and $b(V_7)$, the coefficients of $a(V_1)$ to $a(V_9)$ and $b(V_1)$ to $b(V_9)$ can be calculated by interpolation and extrapolation method. The coefficients of $a(V_1)$ to $a(V_9)$ and $b(V_1)$ to $b(V_9)$ can be calculated as Eq. 4.26 to Eq. 4.32.

$$a(V_1) = a(V_3) - \frac{a(V_7)-a(V_3)}{2}$$
$$b(V_1) = b(V_3) - \frac{b(V_7)-b(V_3)}{2} \quad \text{(Eq. 4.26)}$$

$$a(V_2) = a(V_3) - \frac{a(V_7)-a(V_3)}{4}$$
$$b(V_2) = b(V_3) - \frac{b(V_7)-b(V_3)}{4} \quad \text{(Eq. 4.27)}$$

$$a(V_4) = a(V_3) + \frac{a(V_7)-a(V_3)}{4}$$
$$b(V_4) = b(V_3) + \frac{b(V_7)-b(V_3)}{4} \quad \text{(Eq. 4.28)}$$

$$a(V_5) = a(V_3) + \frac{a(V_7)-a(V_3)}{2}$$
$$b(V_5) = b(V_3) + \frac{b(V_7)-b(V_3)}{2} \quad \text{(Eq. 4.29)}$$

$$a(V_6) = a(V_7) - \frac{a(V_7)-a(V_3)}{4}$$
$$b(V_6) = b(V_7) - \frac{b(V_7)-b(V_3)}{4} \quad \text{(Eq. 4.30)}$$

$$a(V_8) = a(V_7) + \frac{a(V_7)-a(V_3)}{4}$$
$$b(V_8) = b(V_7) + \frac{b(V_7)-b(V_3)}{4} \quad \text{(Eq. 4.31)}$$

$$a(V_9) = a(V_7) + \frac{a(V_7)-a(V_3)}{2}$$
$$b(V_9) = b(V_7) + \frac{b(V_7)-b(V_3)}{2} \quad \text{(Eq. 4.32)}$$

4.6 System Architecture

The proposed on-chip ring oscillator architecture which uses the relative reference modeling with four-point calibration is shown in Fig. 4.15, and Fig. 4.16 shows the timing diagram of this system architecture. It is composed of a delay ratio estimator (DRE), a voltage classifier, a temperature classifier, a linear calculator, and a digitally controlled oscillator (DCO). The DRE estimates the R1(V,T) and the R2(V,T) at chip run time under voltage and temperature variations.

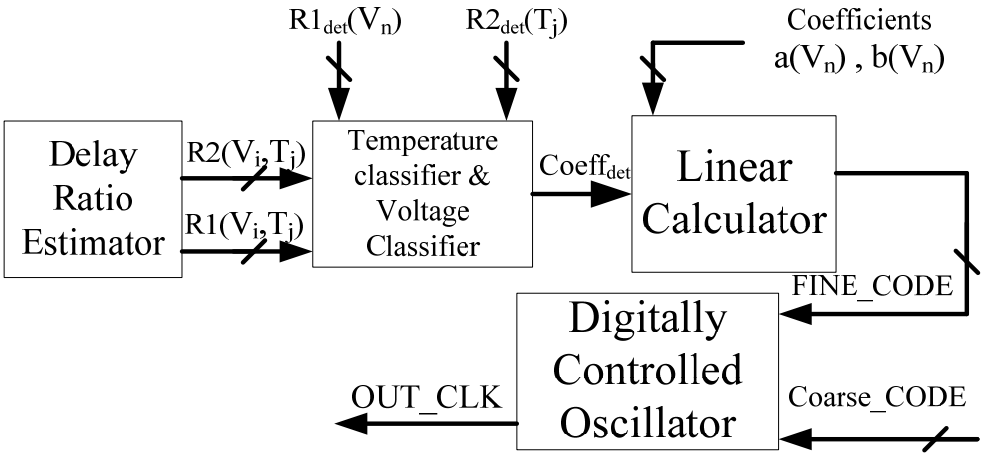


Fig. 4.15: System architecture of on-chip oscillator at chip run time.

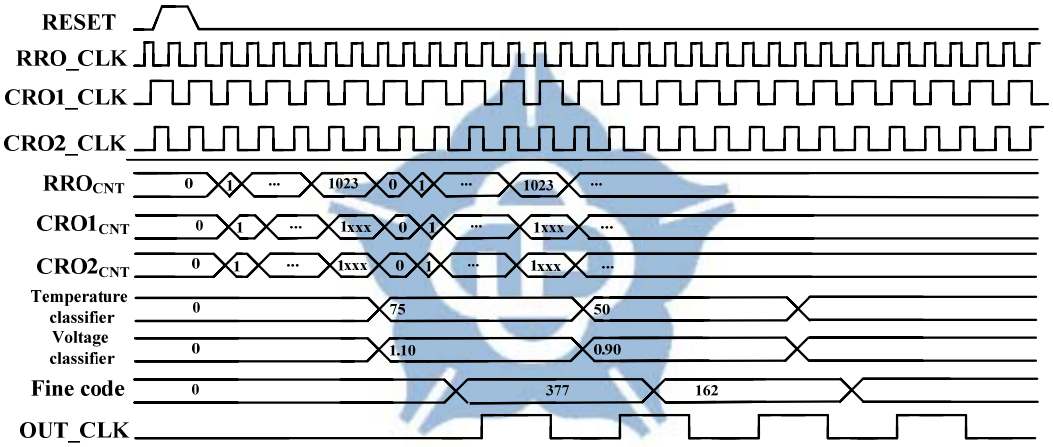


Fig. 4.16: Timing diagram of the system architecture at run time.

When the values of $R1_{det}(V_n)$, $R2_{det}(T_j)$, $a(V_n)$, and $b(V_n)$ for V_1 to V_9 and T_1 to T_4 are determined in the off-chip process, the proposed on-chip oscillator are now ready for generating the target frequency (F_{DCO}) at 5MHz.

At chip run time, the DRE estimates R1(V,T) and R2(V,T) with a unknown supply voltage (V) and a unknown operation temperature (T). The voltage classifier uses the $R1_{det}(V_n)$ to roughly estimate the supply voltage. The temperature classifier uses the $R2_{det}(T_j)$ to roughly estimate the operation temperature. When the voltage classifier and temperature

classifier determine the current supply voltage and operation temperature, the linear calculator uses Eq. 4.33 to calculate DCO control codes (fine_code). Than the DCO are controlled by the coarse code and the fine code to output the required frequency with voltage and temperature variations.

$$fine\ code = a(V_n) * R2(V,T) + b(V_n) \qquad \text{(Eq. 4.33)}$$

Fig. 4.17 shows the flow chart of the voltage classifier. The R1(V,T) curves maybe overlap at (V_n,T_3) and (V_{n+1},T_0). Thus, it cause voltage estimation problem. However, from R2(V,T) curve, we can roughly estimate the operation temperature and in the cell selection rules, R1(V, T) should have a monotonic response. Then with the estimated temperature information, we can solve the problem when R1(V,T) curves overlap at (V_n,T_3) and (V_{n+1},T_0).Thus, the supply voltage can be estimated more accurately.

If the distance between R1(V, T) and $R1_{det}(V_n)$ is shorter than the distance between R1(V, T) and $R1_{det}(V_{n+1})$ as shown in Fig 4.11, the current supply voltage can be estimated as V_n. Similarly, if the distance between R1(V, T) and $R1_{det}(V_{n+1})$ is shorter than the distance between R1(V, T) and $R1_{det}(V_n)$, the current supply voltage can be estimated as V_{n+1}.

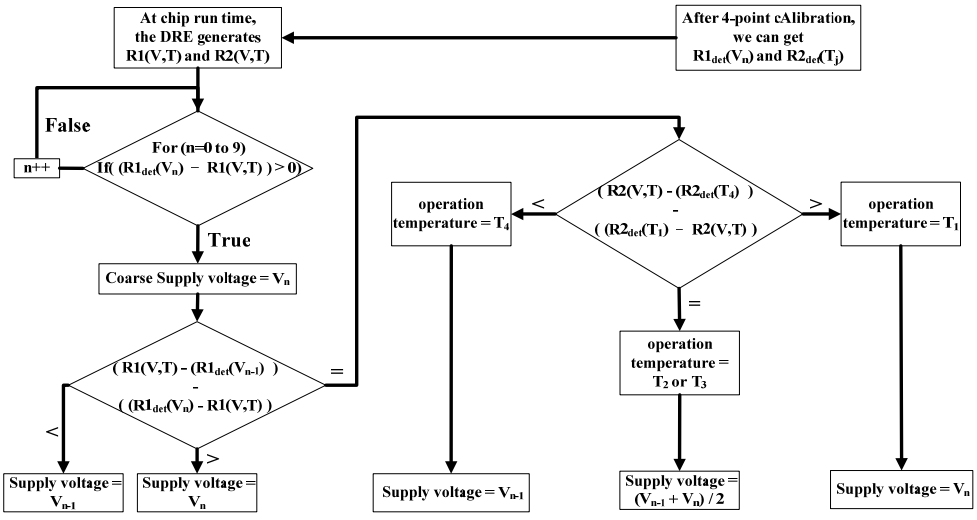


Fig. 4.17: Flow chart of the voltage classifier.

In addition, if the distance between R1(V, T) and $R1_{det}(V_n)$ is equal to the distance between R1(V, T) and $R1_{det}(V_{n+1})$, we need to use R2(V,T) value to determine the current supply voltage. In this case, if the temperature classifier estimates current operation temperature is T_3, the current supply voltage can be estimated as V_n. However, if the temperature classifier estimates current operation temperature is T_0, the current supply voltage can be estimated as V_{n+1}. In some special cases, if the temperature classifier estimates current operation temperature is T_2(25ºC0 to T_3(50 ºC), the current supply voltage can be estimated as Eq. 4.34 and the fine_code can be expressed as Eq. 4.35.

$$current\ supply\ voltage = \frac{1}{2} * (V_n + V_{n+1}) \qquad \text{(Eq. 4.34)}$$

$$fine\ code = \frac{a(V_n)+a(V_{n+1})}{2} * R2(V,T) + \frac{b(V_n)+b(V_{n+1})}{2} \qquad \text{(Eq. 4.35)}$$

For example, if the distance between R1(V, T) and $R1_{det}(V_5)$ is equal to the distance between R1(V, T) and $R1_{det}(V_6)$, and temperature classifier estimates current operation temperature is T_4(75ºC, the current supply voltage can be estimated as V_5. Under the same conditions, if the temperature classifier estimates current operation temperature is 0ºC, the current supply voltage can be estimated as V_6, if the temperature classifier estimates current operation temperature is T_2(25ºC0 to T_3(50 ºC), the current supply voltage can be estimated as Eq. 4.36 and the fine_code can be expressed as Eq. 4.37

$$current\ supply\ voltage = \frac{1}{2} * (V_5 + V_6) \qquad \text{(Eq. 4.36)}$$

$$fine\ code = \frac{a(V_5)+a(V_6)}{2} * R2(V,T) + \frac{b(V_5)+b(V_6)}{2} \qquad \text{(Eq. 4.37)}$$

4.7 Experimental Results

The proposed on-chip oscillator circuit is implemented in a standard 90nm 1P9M CMOS process. The operating voltage ranges from 0.90V to 1.10V, and the temperature ranges from 0ºC to 75ºC. The layout of the test chip is shown in Fig. 4.18. The active area is 250μm×200μm, and chip area including I/O pads is 815μm×765μm.

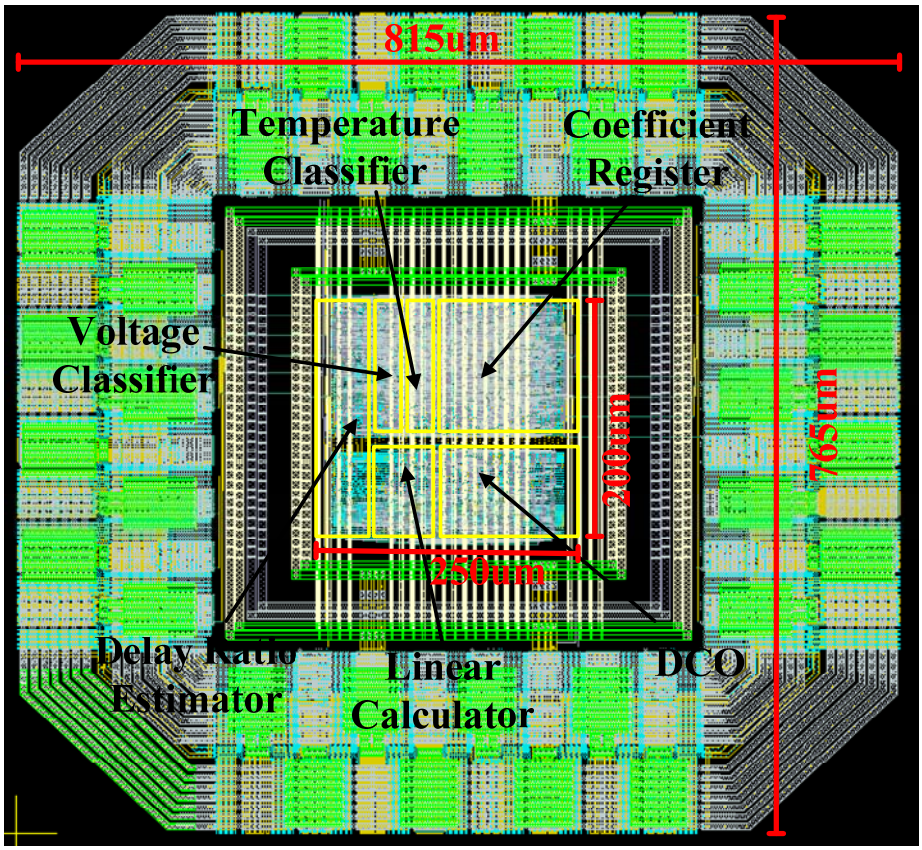


Fig. 4.18: Layout of the test chip.

Figs. 4.19 and 4.20 show the simulation results of the output frequency of the proposed on-chip oscillator with PVT variations. The target output frequency is 5MHz. The frequency error of the proposed on-chip oscillator with temperature variations is 0.28% in typical process corner. The maximum frequency error of the proposed design with voltage variations is 0.56% in typical process corner. The maximum output frequency error with PVT variations ranges from -1.36% to +0.91%.

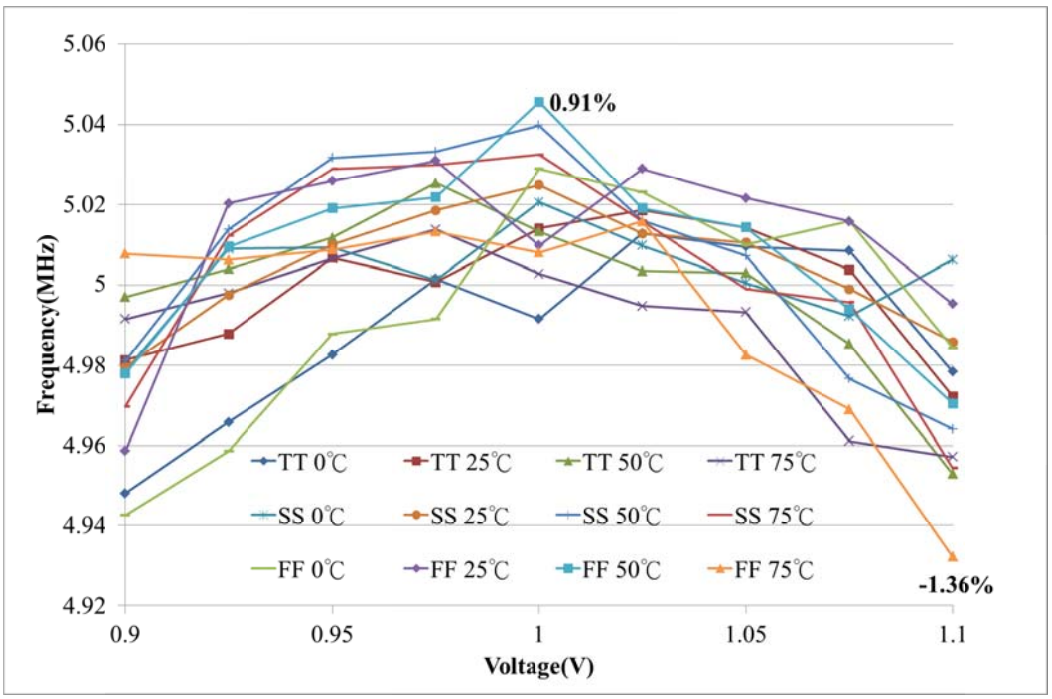


Fig. 4.19: The simulation results output frequency with PVT variations (x-axis is voltage).

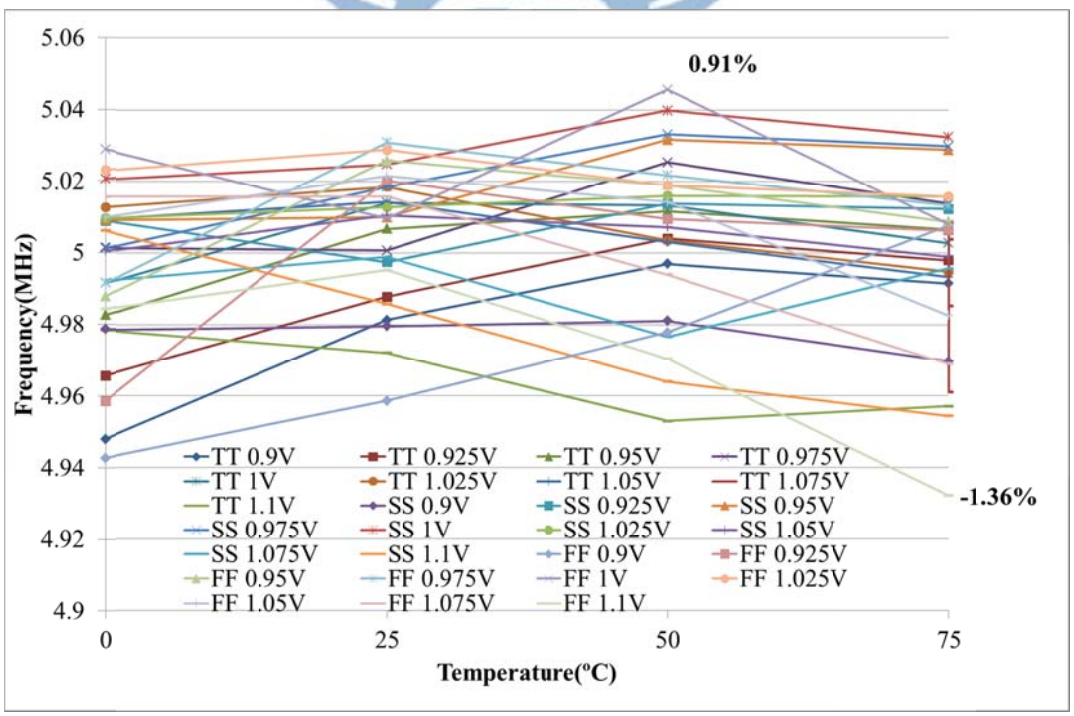


Fig. 4.20: The simulation results output frequency with PVT variations (x-axis is temperature).

4.8 Comparison of Proposed Two CBOCSO

In chapter 3 and chapter 4, the proposed CBOCSO with multi-points calibration and with four-point calibration are introduced, respectively. In this section, we summarize the difference between them.

In proposed CBOCSO with multi-points calibration (MPC) and the CBOCSO with four-point calibration (FPC), three are both composed of a delay ratio estimator (DRE), a voltage classifier, a temperature classifier, a linear calculator, and a digitally controlled oscillator (DCO).

Table 4.2: Comparison between MPC and FPC

Item	with multi-points calibration (MPC)	with four-point calibration (FPC)
Oscillator type	Only coarse delay line (cyclic DCO)	Coarse and fine delay line Combination
Frequency of DRE	MPC > FPC	
Power Consumption	MPC > FPC	
Area	MPC < FPC	
Calibration costs	MPC > FPC	
Frequency Error	MPC > FPC	

Table 4.1 shows the comparisons between MPC and FPC. In the DRE circuit, if the frequency of RRO, CRO1 and CRO2 runs too fast, the power consumption of the DRE will be very large. In the MPC, we use a DCO with only a coarse delay line. In order to make the DCO has a fine resolution, the frequency of RRO should be at high frequency. However, when the frequency goes up, the power consumption is also increased. In the FPC, we slow down the frequency of RRO, CRO1 and CRO2, and thus the power consumption of DRE can be greatly reduced. However, the resolution of DCO will be worse. Thus, we spend extra area in the DCO circuit by adding the fine tune delay circuit, so that DCO has a better

resolution.

In the MPC, we need to measure many voltage and temperature points, and thus the cost of calibration is too high. In the FPC, we proposed a four-point calibration with interpolation and extrapolation, the cost of calibration can be greatly reduced. In addition, we have improved the algorithm of voltage classifier and the temperature classifier, the voltage and temperature can be determined more accurately. So even with four-point calibration, the frequency error of the FPC is better than the MPC.

IF we perform multi-point calibration in the FPC and named is as FPCCM. Figs. 4.21 and 4.22 show the output frequency of the FPCCM with PVT variations. With the same setting with FPC, the frequency error of the FPCCM with temperature variations can be reduced to 0.18% in typical process corner. The maximum frequency error of the FPCCM with voltage variations can be also reduced to 0.39% in typical process corner. The maximum output frequency error of the FPCCM with PVT variations ranges from -0.92% to +0.85%.

Table 4.3: Comparison between FPC and FPCCM

Parameter	FPC	FPCCM
Temp. Range	0 ~ 75	
Vari. with Temp.	0.28%	0.18%
VDD Range	0.9~1.1	
Vari. with VDD	0.56%	0.39%
Max error %	1.36%	0.92%

Table 4.3 shows the comparisons between FPC and FPCCM. In the FPCCM, although we increase the calibration point but the frequency error is not greatly reduced. The DRE circuit calculates values of R1(V,T) and R2(V,T), these two values may generate ±1 calculation error. Temperature variations is not very linear, the linear calculator uses multi-point or two-point linear regression results would be similar. The FPCCM or the FPC

will cause some error by calculation. Thus, when the voltage classifier estimates a correct voltage, the error in FPCCM and FPC are not so different. In addition, the testing cost for FPCCM is too much, thus we didn't use this architecture.

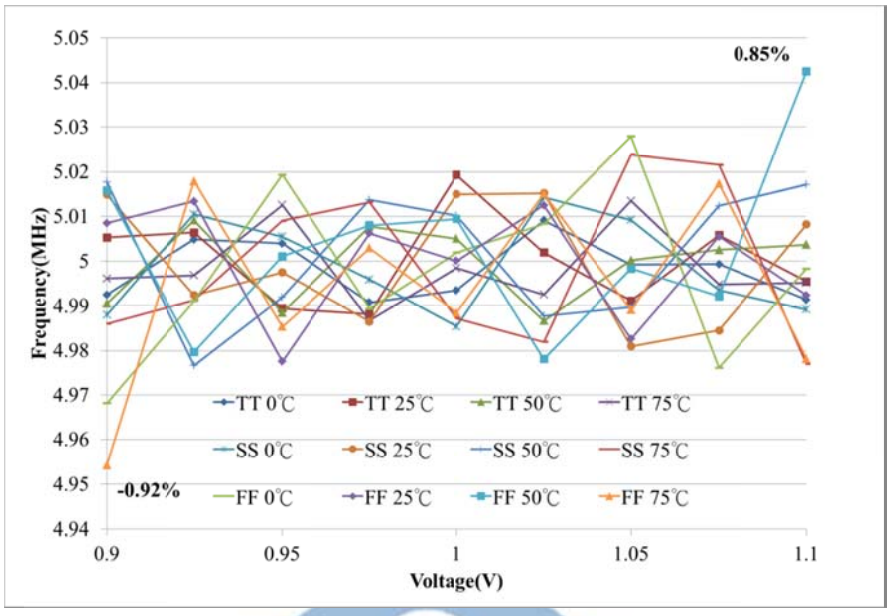


Fig. 4.21: The simulation results output frequency with PVT variations (x-axis is voltage).

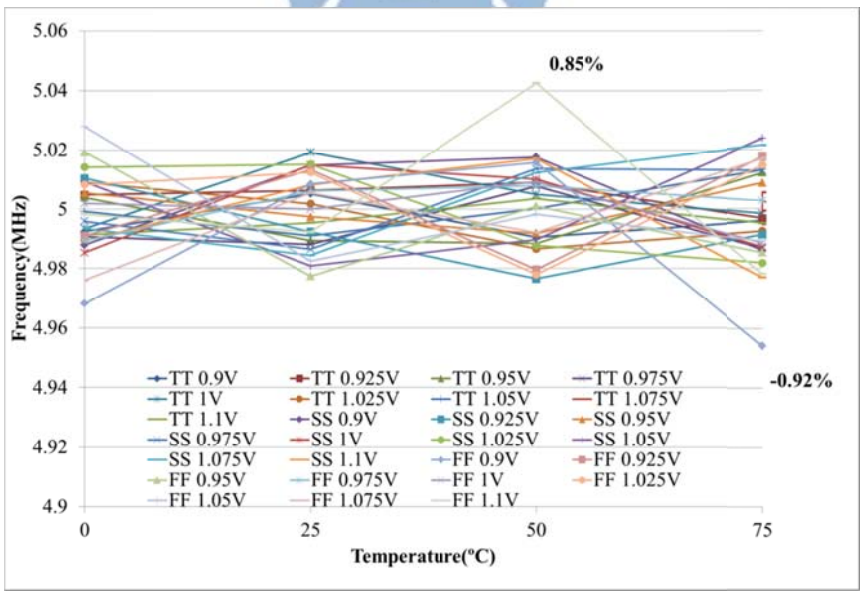


Fig. 4.22: The simulation results output frequency with PVT variations (x-axis is temperature).

Chapter 5

Circuit Measurement Results

5.1 Specifications

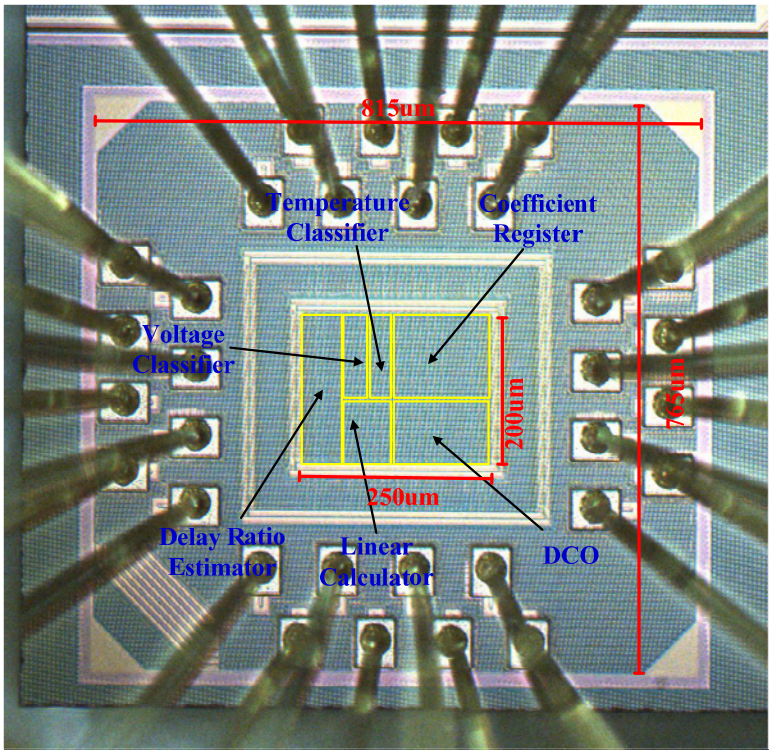


Fig. 5.1: Microphotograph diagram of the CBOCSO.

The proposed on-chip oscillator circuit with four-point calibration is fabricated in a standard 90nm 1P9M CMOS process. The operating voltage ranges from 0.90V to 1.10V, and temperature range is from 0ºC to 75ºC. The microphotograph of the test chip is shown in Fig. 5.1. The chip is consisted of a coefficient register, a delay ratio estimator (DRE), a voltage classifier, a temperature classifier, a linear calculator, and a digitally controlled oscillator (DCO).The active area is 180μm×180μm, and chip area including I/O pads is 830μm×830μm. The gate count is about 11396.

Fig. 5.2 shows the chip floor plan and I/O plan of the proposed CBOCSO with four-point calibration, and the pad description is shown in Table 5.1. The input pad I_RESET will reset the system pin. The I_OUT_CLK_0 is the CBOCSO DCO output pin, which output frequency should be kept at the 5MHz with PVT variations.

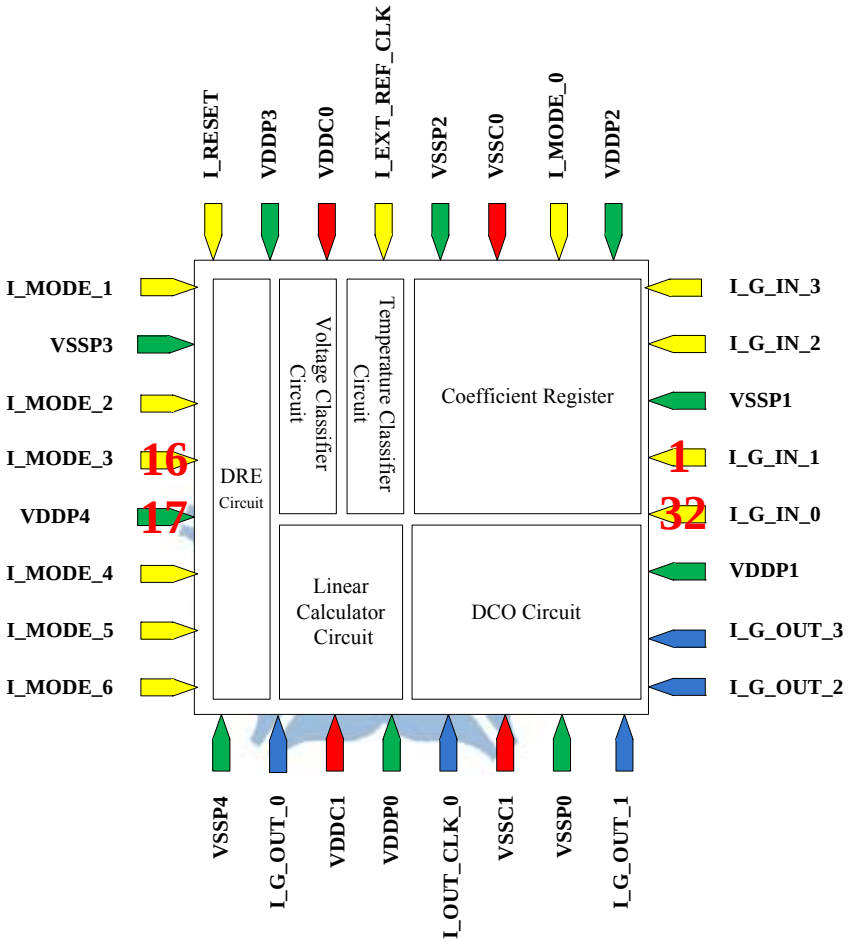


Fig. 5.2: Chip floor plan and I/O plan.

Table 5.1: The I/O PAD information of CBOCSO.

Pin Number	Pin Name	Input/Output	Information
1	I_G_IN_1	Input	Input value pin[1]

2	VSSP1	Input	Pad Power
3	I_G_IN_2	Input	Input value pin[2]
4	I_G_IN_3	Input	Input value pin[3]
5	VDDP2	Input	Pad Power
6	I_MODE_0	Input	Input / output Mode select [0]
7	VSSC0	Input	Core Power
8	VSSP2	Input	Pad Power
9	I_EXT_REF_CLK	Input	External CLK
10	VDDC0	Input	Core Power
11	VDDP3	Input	Pad Power
12	I_RESET	Input	Chip Reset Pin
13	I_MODE_1	Input	Input / output Mode select [1]
14	VSSP3	Input	Pad Power
15	I_MODE_2	Input	Input / output Mode select [2]
16	I_MODE_3	Input	Input / output Mode select [3]
17	VDDP4	Input	Pad Power
18	I_MODE_4	Input	Input / output Mode select [4]
19	I_MODE_5	Input	Input / output Mode select [5]
20	I_MODE_6	Input	Input / output Mode select [6]
21	VSSP4	Input	Pad Power
22	I_G_OUT_0	Output	output value pin[0]
23	VDDC1	Input	Core Power
24	VDDP0	Input	Pad Power
25	I_OUT_CLK_0	Output	DCO output clock
26	VSSC1	Input	Core Power

27	VSSP0	Input	Pad Power
28	I_G_OUT_1	Output	output value pin[1]
29	I_G_OUT_2	Output	output value pin[2]
30	I_G_OUT_3	Output	output value pin[3]
31	VDDP1	Input	Pad Power
32	I_G_IN_0	Input	Input value pin[3]

In addition, the input Pad I_G_IN_0 to I_G_IN_3 are the coefficient register input pins, and the output Pad I_G_OUT_0 to I_G_OUT_3 are the coefficient register output pins. The input pad I_MODE_0 to I_MODE_6 represents the input mode, and the input mode can be 0 to 127. We use different code of mode[6:0] to input different value through G_IN[3:0]. The G_OUT[3:0] used as a debug register value in different mode.

The Table 5.2 shows the corresponding inputs and outputs in each mode, which including the coefficients of the linear calculator. There are totally 102 modes can be used. The input pad I_EXT_REF_CLK is an external reference clock. The circuit input coefficients required a reference clock. When the coefficients have been input, the circuit starts operation, the input pad I_EXT_REF_CLK is not required.

Table 5.2: The serial pin of mode[6:0] information of CBOCSO.

mode[6:0]	G_IN[3:0]	G_OUT[3:0]
1	G_IN[3:0] input to Coefficient_A_0.900V[11:8]	None
2	G_IN[3:0] input to Coefficient_A_0.900V[7:4]	G_OUT[3:0] print Coefficient_A_0.900V[11:8]
3	G_IN[3:0] input to Coefficient_A_0.900V[3:0]	G_OUT[3:0] print Coefficient_A_0.900V[7:4]
4	G_IN[3:0] input to Coefficient_A_0.925V[11:8]	G_OUT[3:0] print Coefficient_A_0.900V[3:0]
5	G_IN[3:0] input to Coefficient_A_0.925V[7:4]	G_OUT[3:0] print Coefficient_A_0.925V[11:8]
6	G_IN[3:0] input to Coefficient_A_0.925V[3:0]	G_OUT[3:0] print Coefficient_A_0.925V[7:4]

7	G_IN[3:0] input to Coefficient_A_0.950V[11:8]	G_OUT[3:0] print Coefficient_A_0.925V[3:0]
8	G_IN[3:0] input to Coefficient_A_0.950V[7:4]	G_OUT[3:0] print Coefficient_A_0.950V[11:8]
9	G_IN[3:0] input to Coefficient_A_0.950V[3:0]	G_OUT[3:0] print Coefficient_A_0.950V[7:4]
10	G_IN[3:0] input to Coefficient_A_0.975V[11:8]	G_OUT[3:0] print Coefficient_A_0.950V[3:0]
11	G_IN[3:0] input to Coefficient_A_0.975V[7:4]	G_OUT[3:0] print Coefficient_A_0.975V[11:8]
12	G_IN[3:0] input to Coefficient_A_0.975V[3:0]	G_OUT[3:0] print Coefficient_A_0.975V[7:4]
13	G_IN[3:0] input to Coefficient_A_1.000V[11:8]	G_OUT[3:0] print Coefficient_A_0.975V[3:0]
14	G_IN[3:0] input to Coefficient_A_1.000V[7:4]	G_OUT[3:0] print Coefficient_A_1.000V[11:8]
15	G_IN[3:0] input to Coefficient_A_1.000V[3:0]	G_OUT[3:0] print Coefficient_A_1.000V[7:4]
16	G_IN[3:0] input to Coefficient_A_1.025V[11:8]	G_OUT[3:0] print Coefficient_A_1.000V[3:0]
17	G_IN[3:0] input to Coefficient_A_1.025V[7:4]	G_OUT[3:0] print Coefficient_A_1.025V[11:8]
18	G_IN[3:0] input to Coefficient_A_1.025V[3:0]	G_OUT[3:0] print Coefficient_A_1.025V[7:4]
19	G_IN[3:0] input to Coefficient_A_1.050V[11:8]	G_OUT[3:0] print Coefficient_A_1.025V[3:0]
20	G_IN[3:0] input to Coefficient_A_1.050V[7:4]	G_OUT[3:0] print Coefficient_A_1.050V[11:8]
21	G_IN[3:0] input to Coefficient_A_1.050V[3:0]	G_OUT[3:0] print Coefficient_A_1.050V[7:4]
22	G_IN[3:0] input to Coefficient_A_1.075V[11:8]	G_OUT[3:0] print Coefficient_A_1.050V[3:0]
23	G_IN[3:0] input to Coefficient_A_1.075V[7:4]	G_OUT[3:0] print Coefficient_A_1.075V[11:8]
24	G_IN[3:0] input to Coefficient_A_1.075V[3:0]	G_OUT[3:0] print Coefficient_A_1.075V[7:4]
25	G_IN[3:0] input to Coefficient_A_1.100V[11:8]	G_OUT[3:0] print Coefficient_A_1.075V[3:0]
26	G_IN[3:0] input to Coefficient_A_1.100V[7:4]	G_OUT[3:0] print Coefficient_A_1.100V[11:8]
27	G_IN[3:0] input to Coefficient_A_1.100V[3:0]	G_OUT[3:0] print Coefficient_A_1.100V[7:4]
28	G_IN[3:0] input to Coefficient_B_0.900V[11:8]	G_OUT[3:0] print Coefficient_A_1.100V[3:0]
29	G_IN[3:0] input to Coefficient_B_0.900V[7:4]	G_OUT[3:0] print Coefficient_B_0.900V[11:8]
30	G_IN[3:0] input to Coefficient_B_0.900V[3:0]	G_OUT[3:0] print Coefficient_B_0.900V[7:4]
31	G_IN[3:0] input to Coefficient_B_0.925V[11:8]	G_OUT[3:0] print Coefficient_B_0.900V[3:0]

32	G_IN[3:0] input to Coefficient_B_0.925V[7:4]	G_OUT[3:0] print Coefficient_B_0.925V[11:8]
33	G_IN[3:0] input to Coefficient_B_0.925V[3:0]	G_OUT[3:0] print Coefficient_B_0.925V[7:4]
34	G_IN[3:0] input to Coefficient_B_0.950V[11:8]	G_OUT[3:0] print Coefficient_B_0.925V[3:0]
35	G_IN[3:0] input to Coefficient_B_0.950V[7:4]	G_OUT[3:0] print Coefficient_B_0.950V[11:8]
36	G_IN[3:0] input to Coefficient_B_0.950V[3:0]	G_OUT[3:0] print Coefficient_B_0.950V[7:4]
37	G_IN[3:0] input to Coefficient_B_0.975V[11:8]	G_OUT[3:0] print Coefficient_B_0.950V[3:0]
38	G_IN[3:0] input to Coefficient_B_0.975V[7:4]	G_OUT[3:0] print Coefficient_B_0.975V[11:8]
39	G_IN[3:0] input to Coefficient_B_0.975V[3:0]	G_OUT[3:0] print Coefficient_B_0.975V[7:4]
40	G_IN[3:0] input to Coefficient_B_1.000V[11:8]	G_OUT[3:0] print Coefficient_B_0.975V[3:0]
41	G_IN[3:0] input to Coefficient_B_1.000V[7:4]	G_OUT[3:0] print Coefficient_B_1.000V[11:8]
42	G_IN[3:0] input to Coefficient_B_1.000V[3:0]	G_OUT[3:0] print Coefficient_B_1.000V[7:4]
43	G_IN[3:0] input to Coefficient_B_1.025V[11:8]	G_OUT[3:0] print Coefficient_B_1.000V[3:0]
44	G_IN[3:0] input to Coefficient_B_1.025V[7:4]	G_OUT[3:0] print Coefficient_B_1.025V[11:8]
45	G_IN[3:0] input to Coefficient_B_1.025V[3:0]	G_OUT[3:0] print Coefficient_B_1.025V[7:4]
46	G_IN[3:0] input to Coefficient_B_1.050V[11:8]	G_OUT[3:0] print Coefficient_B_1.025V[3:0]
47	G_IN[3:0] input to Coefficient_B_1.050V[7:4]	G_OUT[3:0] print Coefficient_B_1.050V[11:8]
48	G_IN[3:0] input to Coefficient_B_1.050V[3:0]	G_OUT[3:0] print Coefficient_B_1.050V[7:4]
49	G_IN[3:0] input to Coefficient_B_1.075V[11:8]	G_OUT[3:0] print Coefficient_B_1.050V[3:0]
50	G_IN[3:0] input to Coefficient_B_1.075V[7:4]	G_OUT[3:0] print Coefficient_B_1.075V[11:8]
51	G_IN[3:0] input to Coefficient_B_1.075V[3:0]	G_OUT[3:0] print Coefficient_B_1.075V[7:4]
52	G_IN[3:0] input to Coefficient_B_1.100V[11:8]	G_OUT[3:0] print Coefficient_B_1.075V[3:0]
53	G_IN[3:0] input to Coefficient_B_1.100V[7:4]	G_OUT[3:0] print Coefficient_B_1.100V[11:8]
54	G_IN[3:0] input to Coefficient_B_1.100V[3:0]	G_OUT[3:0] print Coefficient_B_1.100V[7:4]
55	G_IN[2:0] input to index_R1_0.900V[10:8]	G_OUT[3:0] print Coefficient_B_1.100V[3:0]
56	G_IN[3:0] input to index_R1_0.900V[7:4]	G_OUT[3:0] print index_R1_0.900V[10:8]

57	G_IN[3:0] input to index_R1_0.900V[3:0]	G_OUT[3:0] print index_R1_0.900V[7:4]
58	G_IN[2:0] input to index_R1_0.925V[10:8]	G_OUT[3:0] print index_R1_0.900V[3:0]
59	G_IN[3:0] input to index_R1_0.925V[7:4]	G_OUT[3:0] print index_R1_0.925V[10:8]
60	G_IN[3:0] input to index_R1_0.925V[3:0]	G_OUT[3:0] print index_R1_0.925V[7:4]
61	G_IN[2:0] input to index_R1_0.950V[10:8]	G_OUT[3:0] print index_R1_0.925V[3:0]
62	G_IN[3:0] input to index_R1_0.950V[7:4]	G_OUT[3:0] print index_R1_0.950V[10:8]
63	G_IN[3:0] input to index_R1_0.950V[3:0]	G_OUT[3:0] print index_R1_0.950V[7:4]
64	G_IN[2:0] input to index_R1_0.975V[10:8]	G_OUT[3:0] print index_R1_0.950V[3:0]
65	G_IN[3:0] input to index_R1_0.975V[7:4]	G_OUT[3:0] print index_R1_0.975V[10:8]
66	G_IN[3:0] input to index_R1_0.975V[3:0]	G_OUT[3:0] print index_R1_0.975V[7:4]
67	G_IN[2:0] input to index_R1_1.000V[10:8]	G_OUT[3:0] print index_R1_0.975V[3:0]
68	G_IN[3:0] input to index_R1_1.000V[7:4]	G_OUT[3:0] print index_R1_1.000V[10:8]
69	G_IN[3:0] input to index_R1_1.000V[3:0]	G_OUT[3:0] print index_R1_1.000V[7:4]
70	G_IN[2:0] input to index_R1_1.025V[10:8]	G_OUT[3:0] print index_R1_1.000V[3:0]
71	G_IN[3:0] input to index_R1_1.025V[7:4]	G_OUT[3:0] print index_R1_1.025V[10:8]
72	G_IN[3:0] input to index_R1_1.025V[3:0]	G_OUT[3:0] print index_R1_1.025V[7:4]
73	G_IN[2:0] input to index_R1_1.050V[10:8]	G_OUT[3:0] print index_R1_1.025V[3:0]
74	G_IN[3:0] input to index_R1_1.050V[7:4]	G_OUT[3:0] print index_R1_1.050V[10:8]
75	G_IN[3:0] input to index_R1_1.050V[3:0]	G_OUT[3:0] print index_R1_1.050V[7:4]
76	G_IN[2:0] input to index_R1_1.075V[10:8]	G_OUT[3:0] print index_R1_1.050V[3:0]
77	G_IN[3:0] input to index_R1_1.075V[7:4]	G_OUT[3:0] print index_R1_1.075V[10:8]
78	G_IN[3:0] input to index_R1_1.075V[3:0]	G_OUT[3:0] print index_R1_1.075V[7:4]
79	G_IN[2:0] input to index_R1_1.100V[10:8]	G_OUT[3:0] print index_R1_1.075V[3:0]
80	G_IN[3:0] input to index_R1_1.100V[7:4]	G_OUT[3:0] print index_R1_1.100V[10:8]
81	G_IN[3:0] input to index_R1_1.100V[3:0]	G_OUT[3:0] print index_R1_1.100V[7:4]

82	G_IN[2:0] input to index_R2_00T[10:8]	G_OUT[3:0] print index_R1_1.100V[3:0]
83	G_IN[3:0] input to index_R2_00T[7:4]	G_OUT[3:0] print index_R2_00T[10:8]
84	G_IN[3:0] input to index_R2_00T[3:0]	G_OUT[3:0] print index_R2_00T[7:4]
85	G_IN[2:0] input to index_R2_25T[10:8]	G_OUT[3:0] print index_R2_00T[3:0]
86	G_IN[3:0] input to index_R2_25T[7:4]	G_OUT[3:0] print index_R2_25T[10:8]
87	G_IN[3:0] input to index_R2_25T[3:0]	G_OUT[3:0] print index_R2_25T[7:4]
88	G_IN[2:0] input to index_R2_50T[10:8]	G_OUT[3:0] print index_R2_25T[3:0]
89	G_IN[3:0] input to index_R2_50T[7:4]	G_OUT[3:0] print index_R2_50T[10:8]
90	G_IN[3:0] input to index_R2_50T[3:0]	G_OUT[3:0] print index_R2_50T[7:4]
91	G_IN[2:0] input to index_R2_75T[10:8]	G_OUT[3:0] print index_R2_50T[3:0]
92	G_IN[3:0] input to index_R2_75T[7:4]	G_OUT[3:0] print index_R2_75T[10:8]
93	G_IN[3:0] input to index_R2_75T[3:0]	G_OUT[3:0] print index_R2_75T[7:4]
94	G_IN[3] input to T75_enable G_IN[2] input to T00_enable G_IN[1] input to Half_enable G_IN[0] input to DRE_enable	G_OUT[3:0] print index_R2_75T[3:0]
95	G_IN[3:0] input to DCO Coarse code	G_OUT[3] print T75_enable G_OUT[2] print T00_enable G_OUT[1] print Half_enable G_OUT[0] print DRE_enable
96	None	G_OUT[3:0] print DCO Coarse code
97	None	G_OUT[2:0] print DRE Estimate R1[10:8]
98	None	G_OUT[3:0] print DRE Estimate R1[7:4]
99	None	G_OUT[3:0] print DRE Estimate R1[3:0]
100	None	G_OUT[2:0] print DRE Estimate R2[10:8]

101	None	G_OUT[3:0] print DRE Estimate R2[7:4]
102	None	G_OUT[3:0] print DRE Estimate R2[3:0]

5.2 Measurement

Fig. 5.3 shows the measurement environment of the CBOCSO test chip. There are a power supply (Agilent E3600), a signal generator (Agilent 81134A), an oscilloscope (Agilent 8000 Series), a seeeduino ADK main board, a chip and a test board. The power supply provides the Core power and Pad power for CBOCSO, and the Core power is 0.90V to 1.10V and the Pad power is 3.3V. The signal generator generates the external input clock for the reference clock. The oscilloscope is used for monitoring the frequency of DCO output clock waveform.

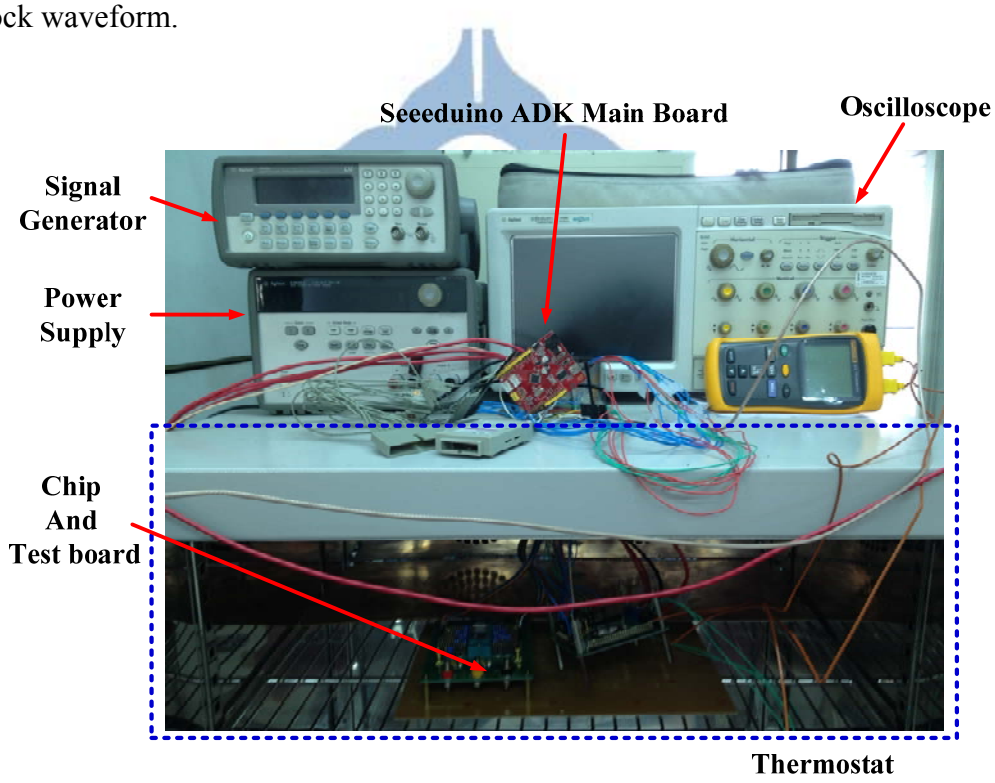


Fig. 5.3: The measurement environment of the CBOCSO.

Fig 5.4 shows the Seeeduino ADK Main Board to communicate with the test board. Seeeduino ADK Main Board is an Android Open Accessory Development Kit(ADK), with general purpose I/O (GPIO) function. The GPIO function can generate digital or analog

pluses. The GPIO function of the seeeduino, which providing 3.3V and 5V mode for users. We can use the GPIO function of the seeduino, produce a continuous input signal through test board and input to our chips. These input data are shown in Table 5.2.

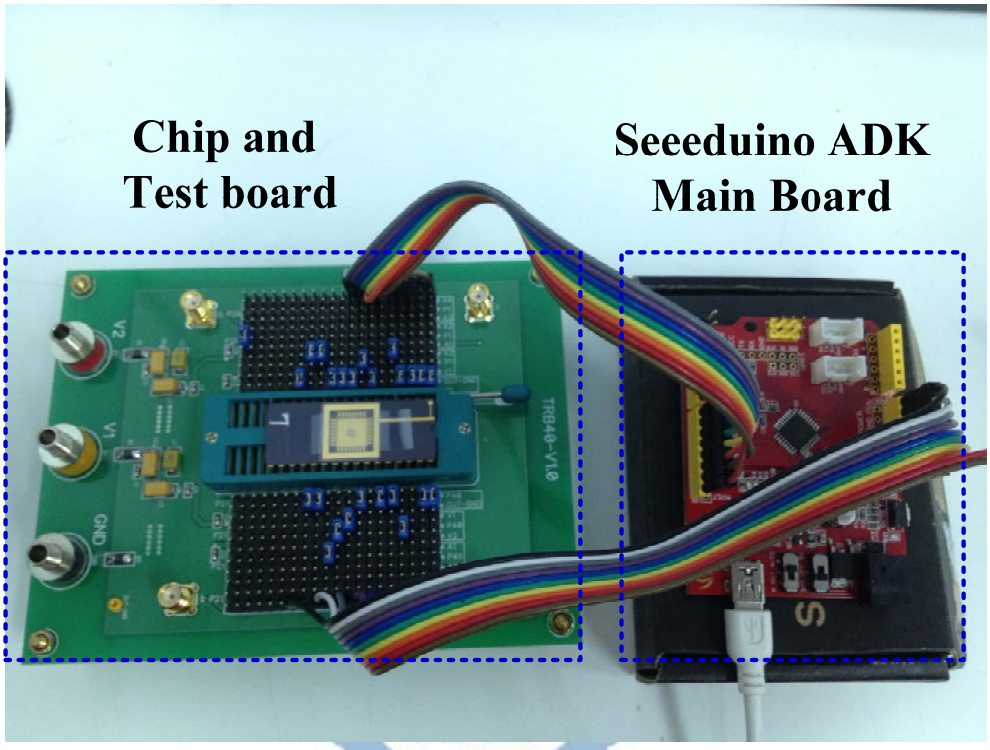


Fig. 5.4: The Seeeduino ADK Main Board to communicate with the chip schematic.

Figs. 5.5 and 5.6 show the measurement results of three chips, the target frequency is 5MHz. After four-point calibration mode, the maximum output frequency error with voltage and temperature variations ranges from -1.47% to +1.31%. The voltage is from 0.90V to 1.10V, which step is 0.25V. The temperature is from 0ºC to 75ºC, which step is 25ºC. The simulation result of output frequency error is -1.36% to +0.91% with PVT variations. We can compare the measurement results and simulation results, there are very close between the two results. Thus, we can prove that the CBOCSO with four-point calibration method is highly effective.

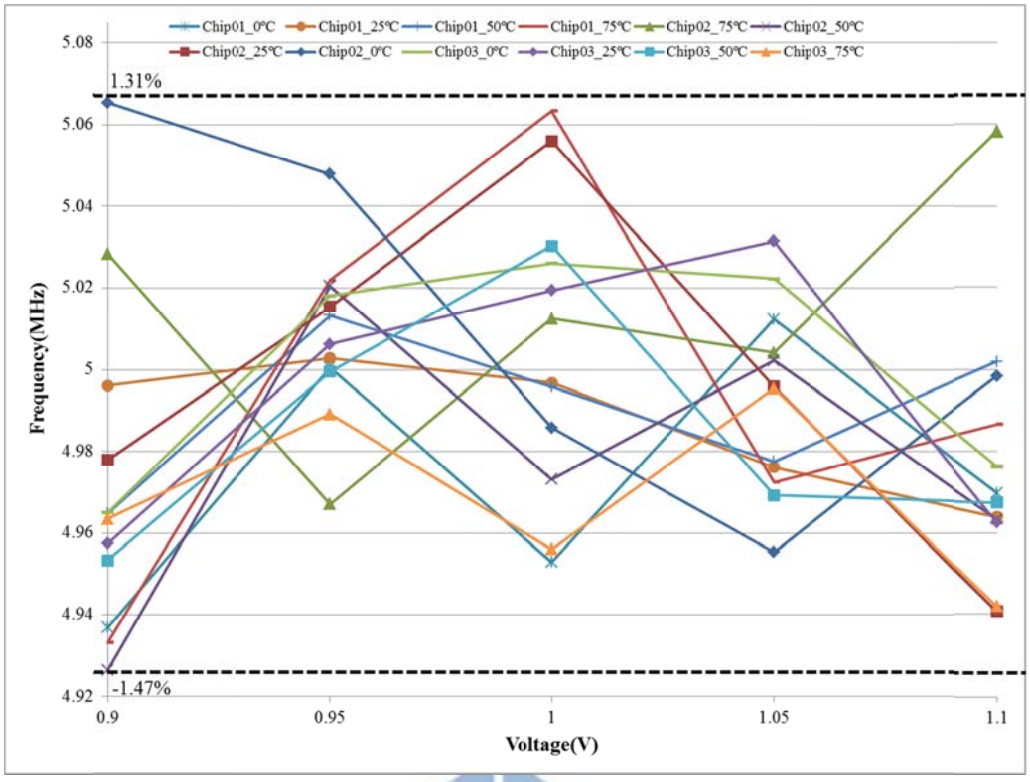


Fig. 5.5: Measurement results of output frequency (x-axis is voltage).

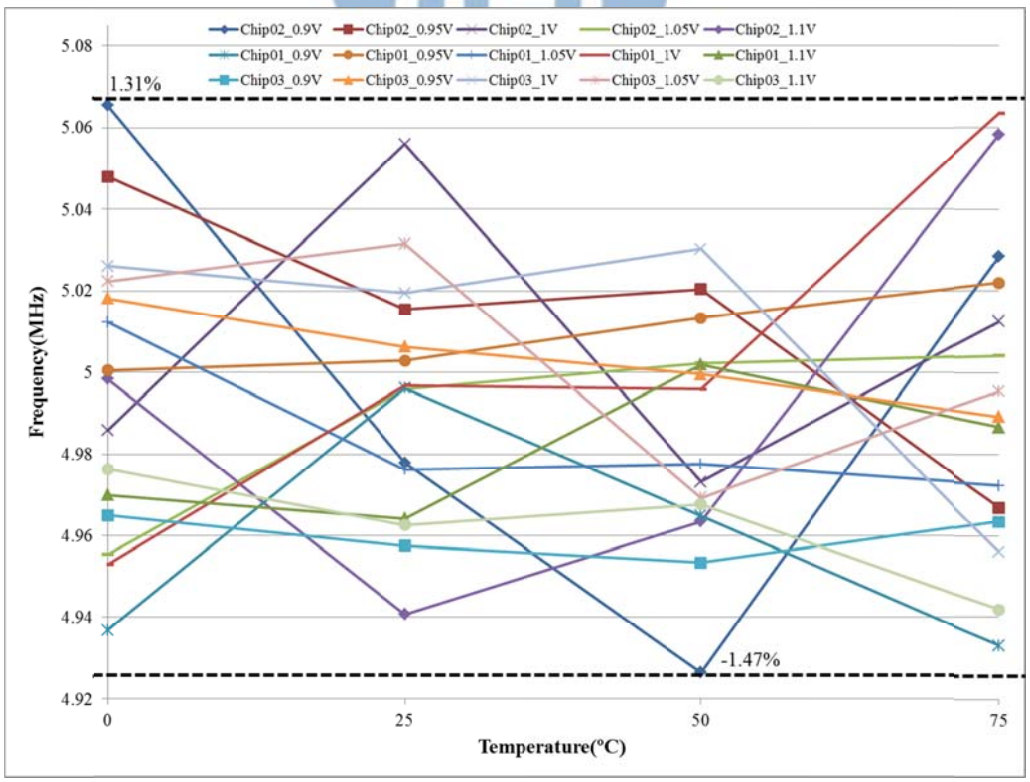
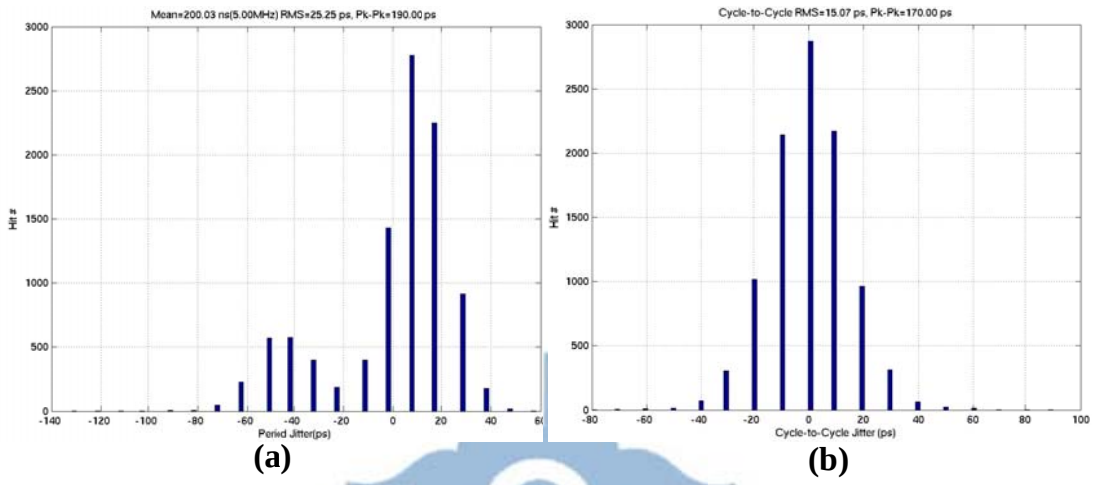


Fig. 5.6: Measurement results of output frequency (x-axis is temperature).

Fig. 5.7(a) shows the simulation period jitter of on-chip oscillator at 1.00V and 25ºC in typical corner. The target frequency of this on-chip oscillator is 5MHz. The Pk-Pk period jitter is 190ps. Fig. 5.7(b) shows the Pk-Pk cycle-to-cycle jitter with the same setting is 170ps. Fig. 5.8 shows the power spectral density with the same setting is -82.20 dBc/Hz at 1MHz distance from the carrier frequency.



(a) **(b)**

Fig. 5.7: The period jitter (a) and cycle-to-cycle jitter (b) of 5MHz target frequency.

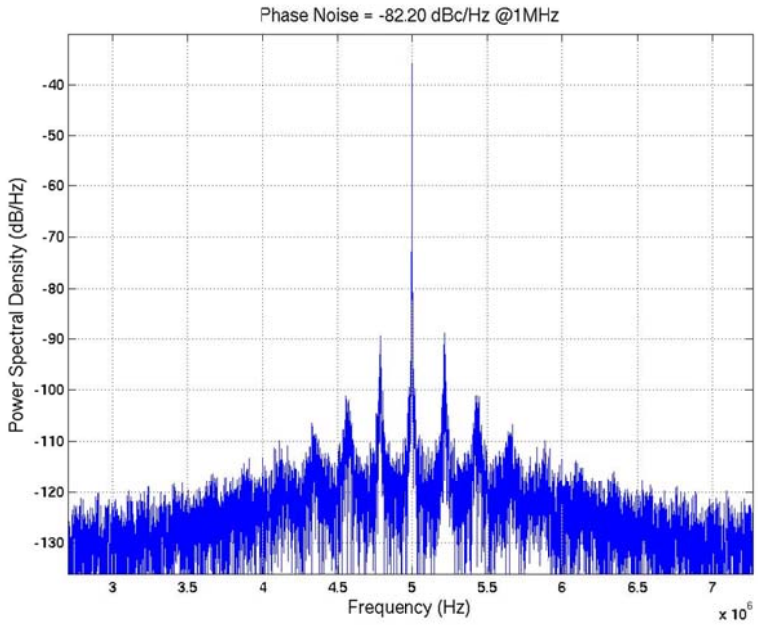


Fig. 5.8: The power spectral density of 5MHz target frequency.

Fig. 5.9 shows the measurement period jitter of on-chip oscillator at 1.00V and 25ºC. The target frequency of this on-chip oscillator is 5MHz. The Pk-Pk period jitter is 153.4ps. Fig. 5.10 shows the Pk-Pk cycle-to-cycle jitter with the same setting is 149.66ps.

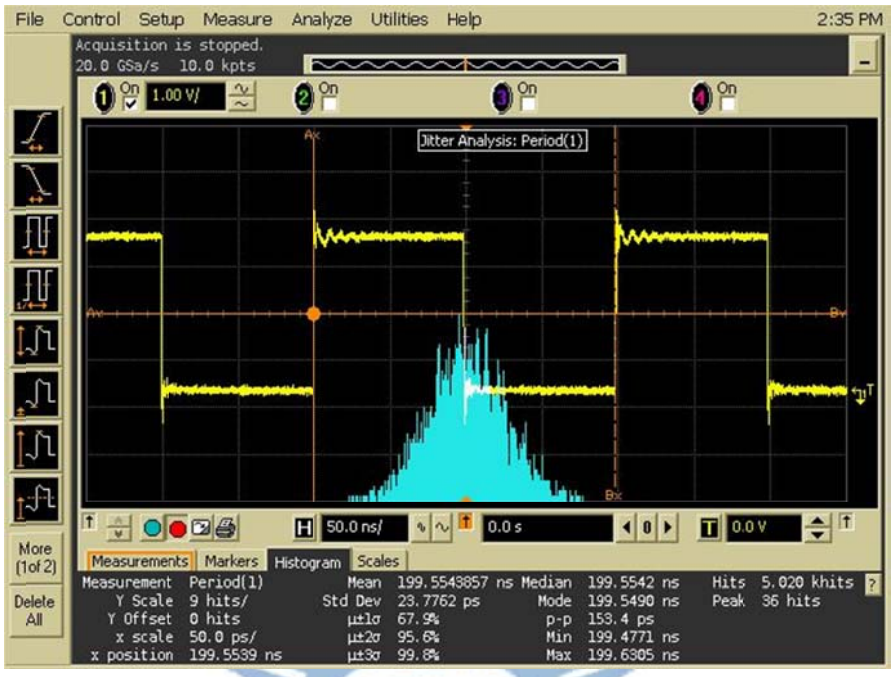


Fig. 5.9: The period jitter (a) and cycle-to-cycle jitter (b) of 5MHz target frequency.

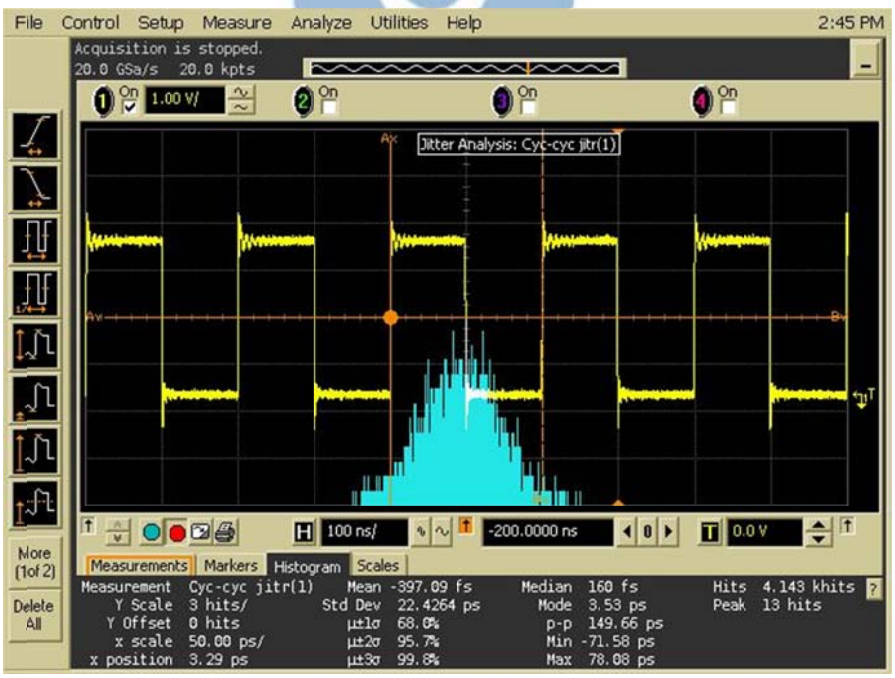


Fig. 5.10: The power spectral density of 5MHz target frequency.

5.3 Comparisons with Recent Research

Table 5.3 shows the comparisons with the state-of-the-art designs. The power consumption when the calibration circuit turns on is 0.61mW. The power consumption of the free running DCO is 0.21mW. The calculation circuit can be turned off after calibration. This circuit only has a free run DCO. Thus, the average power consumption with 10% operation duty cycle can be calculated as 0.61 * 0.1 + 0.21 * 0.9 = 0.25(mW). The measurement frequency error of the proposed on-chip oscillator with temperature variations is 0.60%, which is smaller than [12][16][27]. Although [21][24] has a better accuracy with temperature variation, but [21] and [24] both cannot against process and voltage variations. A full-custom ring oscillator [1] has a very better accuracy, but it requires a band gap voltage reference to against process and voltage variations. Although [24] has a smaller temperature variations, it does not tolerate the voltage variations. The measurement maximum frequency error of the proposed design with voltage variations is 0.72%. Relaxation oscillators [16], can achieve relatively small voltage variations. However, a small voltage variations on the reference voltage (i.e. 2mV) can cause 0.4% frequency error [1][16], and thus, they are sensitive to the supply noise. The measured maximum output frequency error for three chips ranges from -1.47% to +1.31%. In addition, most of the prior researches are analog type design [1][8][12][16][24],which need full-custom design and are not suitable for design automation with poor portability. As compared to [27][46] which requires multi-point calibration, we not only reduce the calibration points, but also reduce the frequency error.

Table 5.3: Performance comparisons of CBOCSO.

Parameter	FPC	[46]ISCAS'13	[21]JSSC'11	[24]JSSC'12	[8]JSSC'09	[12]ESSCIRC'09	[16]JSSC'10	[1]VLSIC'09	[27]TVLSI'12
Osc. Type	ring oscillator	ring oscillator	Mobility ,band gap temp. sensor	Thermal-diffusivity, band gap V reference	RC	VCO	Real. need a current source	ring Osc.,band gap voltage reference	ring oscillator
Technology(nm)	90	90	65	160	65	350	180	180	90
Frequency(MHz)	5	5	0.15	16	6	30	14	10	5
Temp. Range	0 ~ 75	0 ~ 75	-55 ~125	-55 ~ 125	0 ~ 120	-20 ~ 100	-40 ~ 125	-20 ~ 100	0 ~ 75
Vari. with Temp.	0.60%	0.21%	0.50%	0.10%	0.60%	0.70%	0.75%	0.40%	1%
VDD Range	0.9~1.1	0.9~1.1	fixed 1.2v	fixed 1.8v	fixed 1.2v	fixed 1.8v	1.7 ~ 1.9	1.2 ~ 3.0	0.9 ~1.1
Vari. with VDD	0.72%	0.97%	N/A	N/A	N/A	N/A	0.16%	0.05%	1%
Max error %	1.36%	2.83%	N/A	N/A	N/A	N/A	0.91%	0.45%	2.30%
power(mW)	0.25	1.42	0.051	2.1	0.066	0.18	0.045	0.08	0.65
area(mm^2)	0.05	0.0324	N/A	0.5	0.03	0.08	0.04	0.09	0.04
Design Approach	cell-based	cell-based	full-custom	full-custom	full-custom	full-custom	full-custom	full-custom	cell-based

Chapter 6

An Abnormal Temperature Warning Sensor

6.1 Introduction

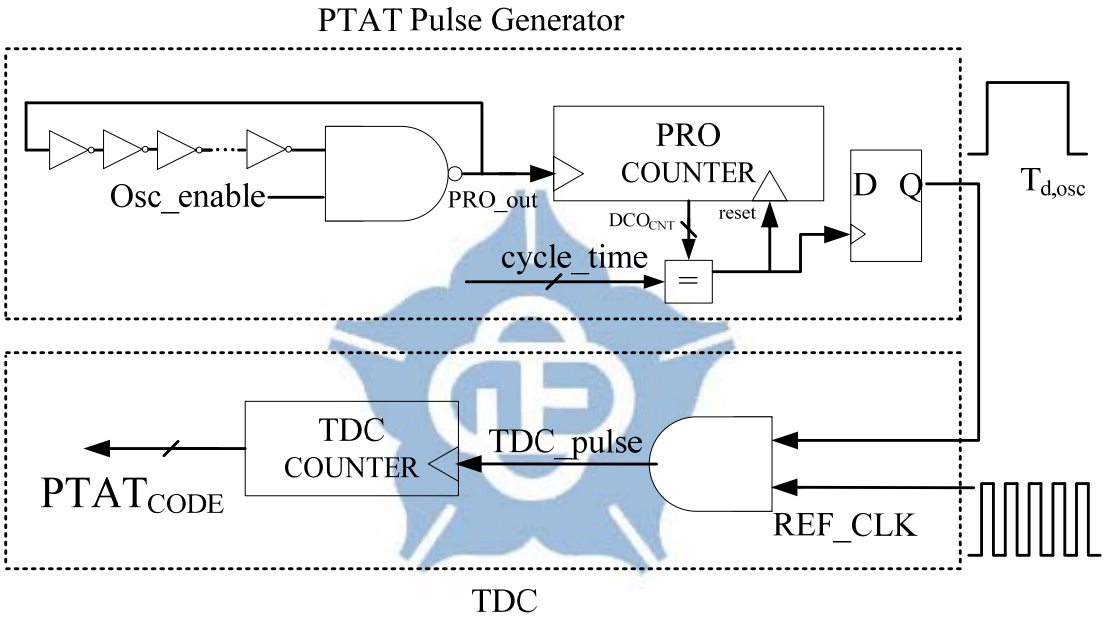


Fig. 6.1: Schematic of the PTAT temperature sensor.

Fig.6.1 shows the block diagram of a proportional to absolute temperature (PTAT) temperature sensor [48]. It is composed of a PTAT pulse generator and a time to digital converter (TDC). When the PTAT ring oscillator generates a pulse (PRO_out), the pulse triggers the PTAT ring oscillator counter (PRO COUNTER). When the output value of the PTAT ring oscillator counter is equal to the input cycle value (cycle_time), the $T_{d,osc}$ pulse is generated. The reference clock and $T_{d,osc}$ pulse connect a AND logic gate to generates a pulse (TDC_pulse), then triggers the TDC counter. In this TDC circuit, the $PTAT_{CODE}$ is the

quantization result of the $T_{d,osc}$ pulse.

Fig. 6.2 shows the simulation results of PTAT temperature sensor with voltage variation at all corners, and this result has two points calibration at 40ºC and 70ºC with 1.00V. The PTAT temperature sensor output can be expressed as Eq.6.1.

$$PTAT_{CODE} = \frac{Period\ of\ logic\ gate(P,V,T)*(2^{14}-1)}{period\ of\ reference\ clk} \qquad \text{(Eq. 6.1)}$$

The PTAT ring oscillator is composed of 20 logic gates (INVX3) in series, where the period of logic gate(P,V,T) is period of the PTAT ring oscillator and, the cycle time is set to 16363 (2^{14}-1), and the period of reference clock is set to 2ns.

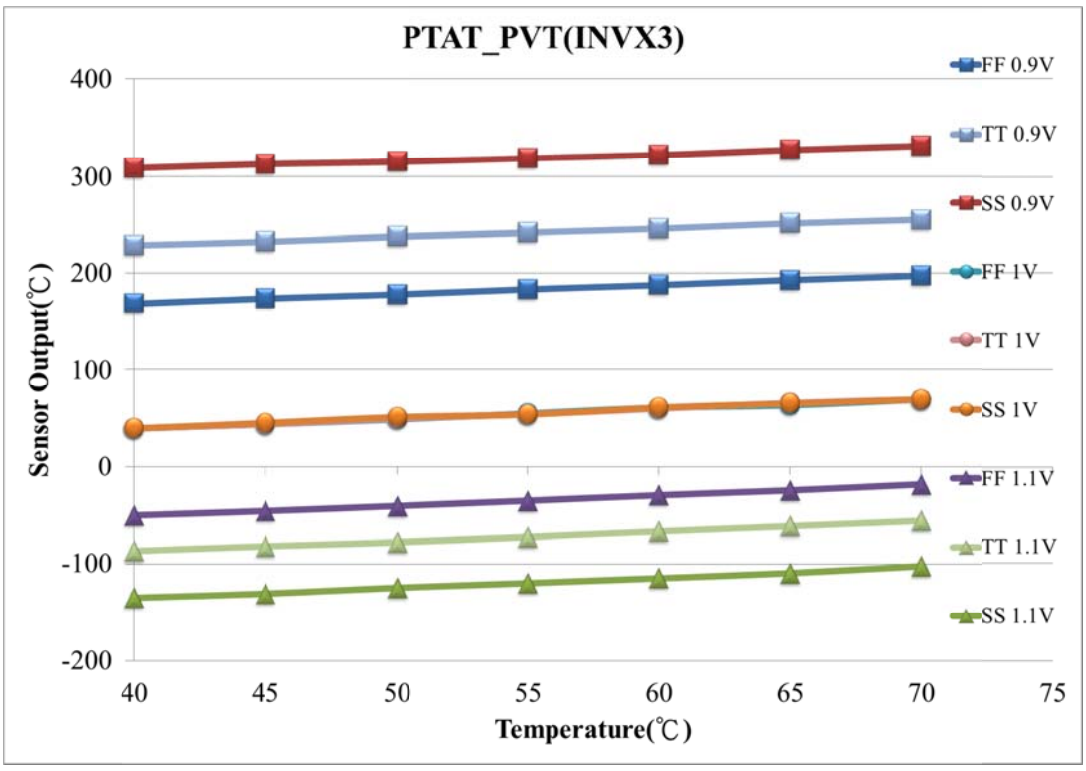


Fig. 6.2: The simulation results of PTAT temperature sensor with voltage variation at all corners.

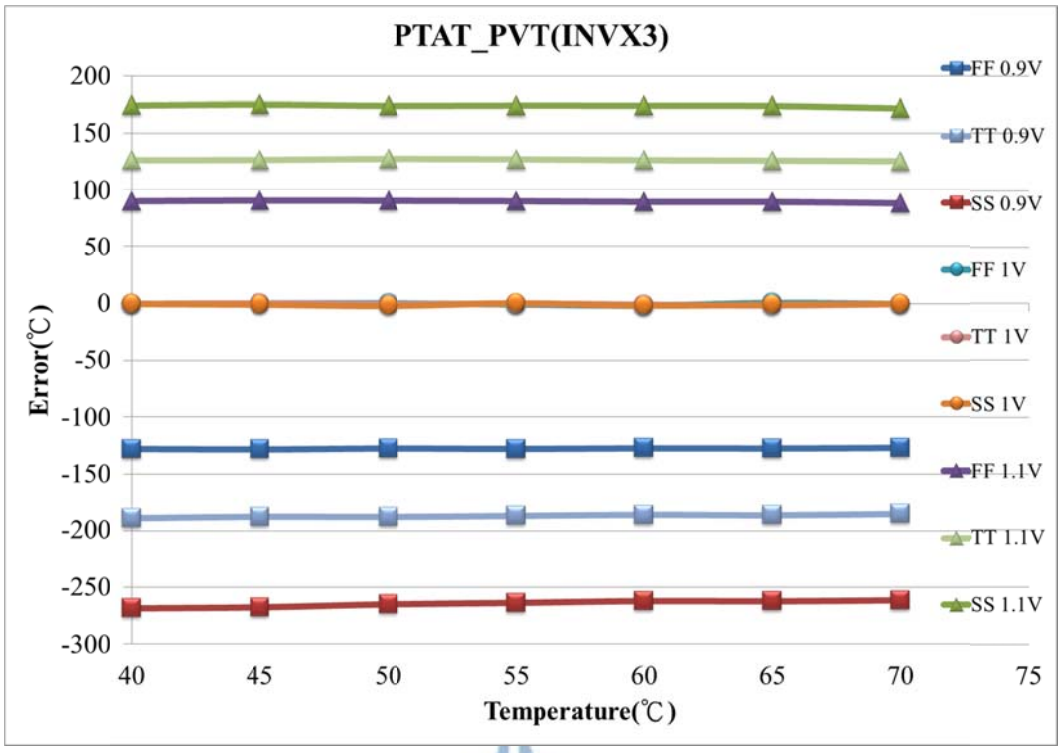


Fig. 6.3: The accuracy of PTAT temperature sensor with voltage variations at all corners.

For this PTAT temperature sensor, we perform two-point calibration with a 1.00V supply in different process corners. The temperature error of the PTAT temperature sensor is from -1.69ºC to +1.00ºC at 1.00V with process variations. However, when the PTAT temperature sensor suffers from voltage variations, the temperature error of the PTAT temperature sensor can be as large as -268.4C to +175.3ºC at all process corners. Therefore, the PTAT has a good resolution and accuracy at a fixed voltage, but its cannot against voltage variations [37][47][48].

In this chapter, we propose an abnormal temperature warning sensor system (ATWS) which can tolerate process and voltage variations. The proposed design also uses the PTAT to build up the temperature sensor. However, a voltage classifier is proposed to estimate supply voltage to improve the accuracy of the temperature sensor with voltage variations.

6.2 System Architecture

The block diagram of the proposed delay ratio estimator (DRE) for temperature sensor application is shown in Fig. 6.4. In section 4.1, the value of N_{TIME} is set to 1023. In this temperature sensor, we require a high resolution for this temperature sensor circuit. Thus, in the DRE circuit, the value of N_{TIME} is changed to 16383, which greatly increases the bit number of the delay ratios R1(P,V,T) and R2(P,V,T). However, the higher N_{TIME} value also means that the temperature sensor calculation time will become longer. Finally, the temperature sensor calculation time is about 200,000 ns to achieve a sampling rate higher than 1k sample/seL.

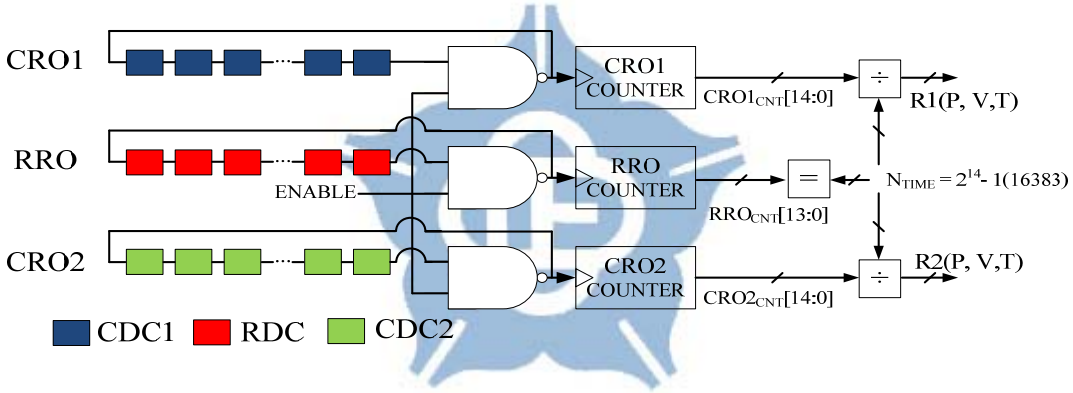


Fig. 6.4: The architecture of the delay ratio estimator.

Fig. 6.5 shows block diagram of the proposed ATWS. It is composed of a delay ratio estimator (DRE), a voltage classifier, and a temperature calculator. The DRE estimates the R1(V,T) and the R2(V,T) at chip run time under voltage and temperature variations. We need to measure the values of R1(V,T), R2(V,T) with two different voltages (V_2 and V_4) and four different temperatures (T_1, T_2, T_6, and T_7). In this chapter, the voltage varies from V_1 to V_5 (V_1=0.900V, V_2=0.950V, and V_3=1.000V, V_4=1.050V, V_5=1.100V), and temperature varies from T_1 to T_7, (T_1=40ºC, T_2=45ºC, T_3=50ºC, T_4=55ºC, T_5=60ºC T_6=65ºC, and T_7=75ºC)

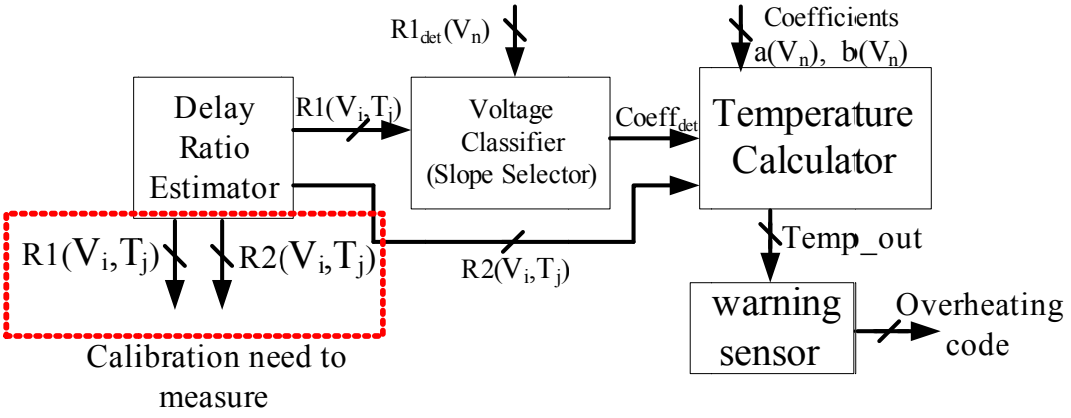


Fig. 6.5: The proposed of the ATWS system architecture.

Fig. 6.6 shows the delay ratios R1(V,T) versus temperature at different voltage in typical process. After calibration mode, we obtain value of R1(V,T) and R2(V,T) at (V_2,T_1), (V_2,T_6), (V_4,T_2), (V_4,T_7) in totally 4 different (V,T) cases, and then the $R1_{det}(V_1)$ to $R1_{det}(V_5)$ can be automatically calculated by interpolation and extrapolation method. This method is the same as we explain in Eq. 4.10 to Eq. 4.18.

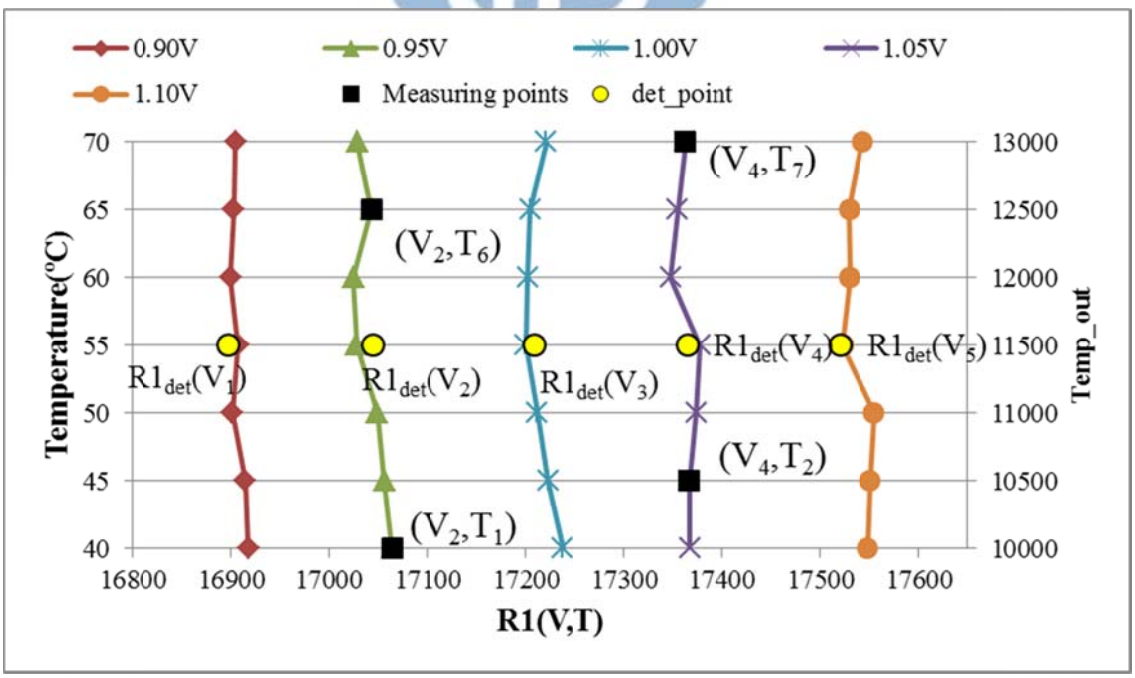


Fig. 6.6: Delay ratios R1(V, T) versus temperature and Temp_out with voltage and temperate variations in typical process corner.

Fig. 6.7 shows the R2(V,T) versus Temp_out with PVT variations. The temperature sensor output (temp_out) can be expressed as Eq. 6.2. In the off-chip process, we perform the two linear regression at the two voltages V_2 and V_4. Firstly, we perform a linear regression of R2(V_2, T_1) and R2(V_2, T_6) versus temp_out to obtain the coefficients a(V_2) and b(V_2). Similarly, we perform a linear regression of R2(V_4, T_2) and R2(V_4, T_7) versus temp_out to obtain the coefficients a(V_4) and b(V_4). After calculation of the coefficients of a(V_2), b(V_2), a(V_4) and b(V_4), the coefficients of a(V_1) to a(V_5) and b(V_5) to b(V_5) can be calculated by interpolation and extrapolation method. This method is the same as we explain Eq. 4.26 to Eq. 4.32.

$$Temp\_out = a(V_n) * R2(V,T) + b(V_n) \qquad \text{(Eq. 6.2)}$$

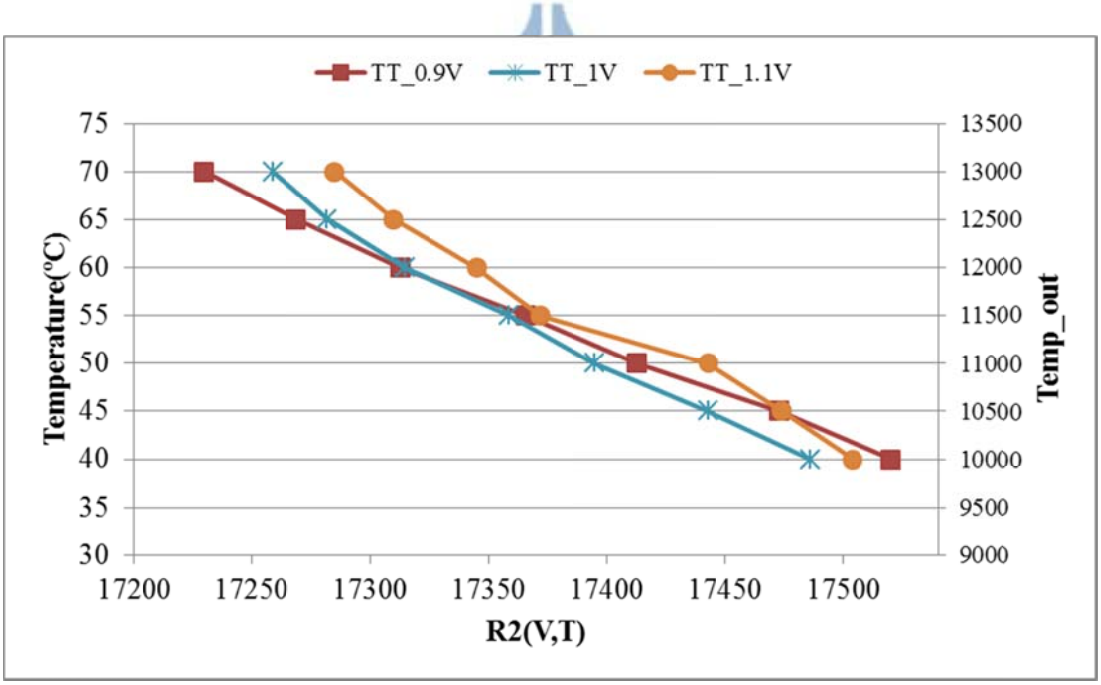


Fig. 6.7: The R2(V,T) versus temperature and Temp_out with VT variations at typical corner.

At chip run time, the DRE estimates R1(V,T) and R2(V,T) with a unknown supply voltage (V) and a operation temperature (T). The voltage classifier uses the $R1_{det}(V_n)$ roughly estimate the unknown supply voltage. When the voltage classifier estimates current

supply voltage, then the temperature calculator uses Eq. 6.2 to calculate temperature sensor output code (temp_out). When the output a code (temp_out) is greater than 40°C, the warning code (overheating code) is output warning message to the system. For example, if the temperature sensor output code (temp_out) is greater than 40°C, the warning code (overheating code) is 3'b001, if the temperature sensor output code (temp_out) is greater than 50°C, the warning code (overheating code) is 3'b011. If the temperature sensor output code (temp_out) is smaller than 40°C, the warning code (overheating code) is 3'b000. Finally, if the temperature sensor output code (temp_out) is latger than 70°C, the warning code (overheating code) is 3'b111.

6.3 Simulation Results

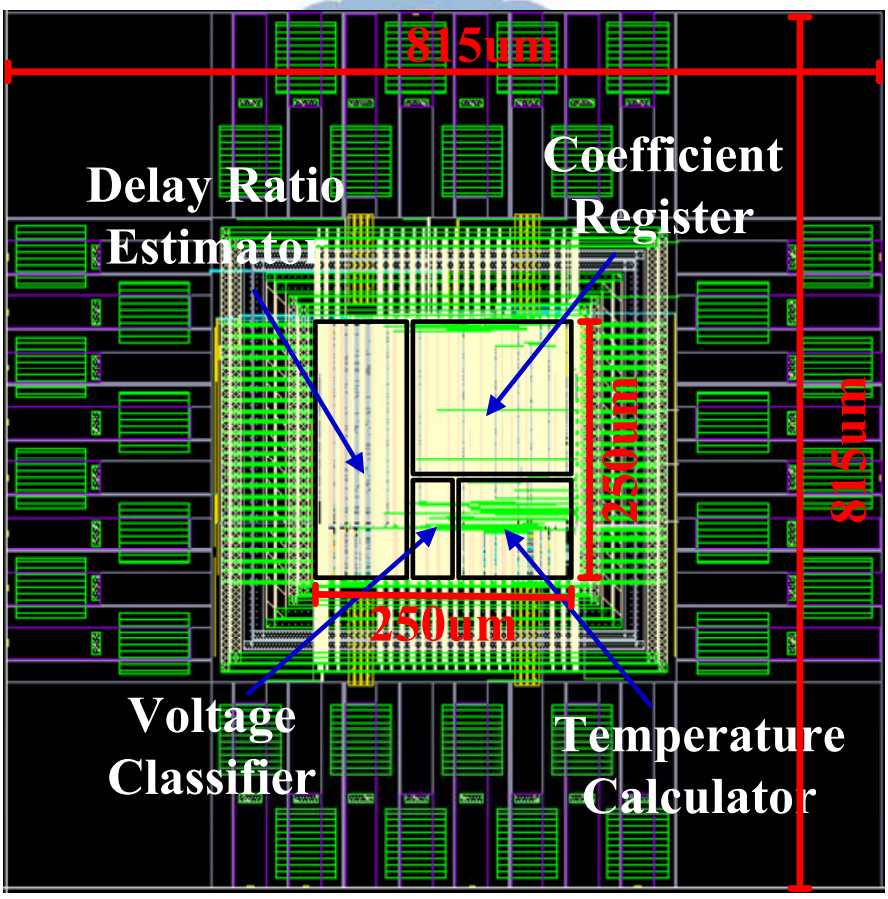


Fig. 6.8: Layout of the ATWS.

The proposed ATWS circuit is implemented in a standard 90nm 1P9M CMOS process. The layout of the ATWS is shown in Fig. 6.8. The ATWS operating voltage ranges from 0.90V to 1.10V, and temperature range is from 0ºC to 70ºC. The chip consists of a coefficient register, a delay ratio estimator (DRE), a voltage classifier, and a temperature calculator. The active area is 250μm×250μm, and the chip area including I/O pads is 815μm×815μm. In addition, the chip area is the larger than the on-chip oscillator in chapter 4, because this temperature sensor requires higher accuracy. Thus, the high bit number in the coefficient register and the DRE make the chip area become larger.

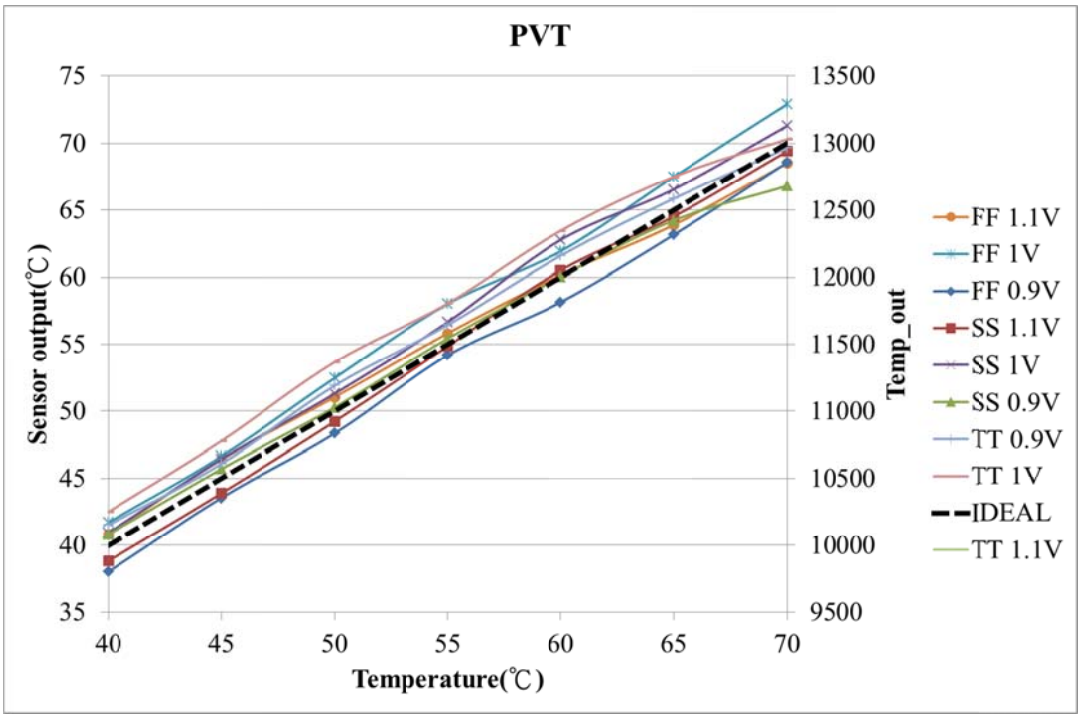


Fig. 6.9: The simulation results of ATWS with process and voltage variations.

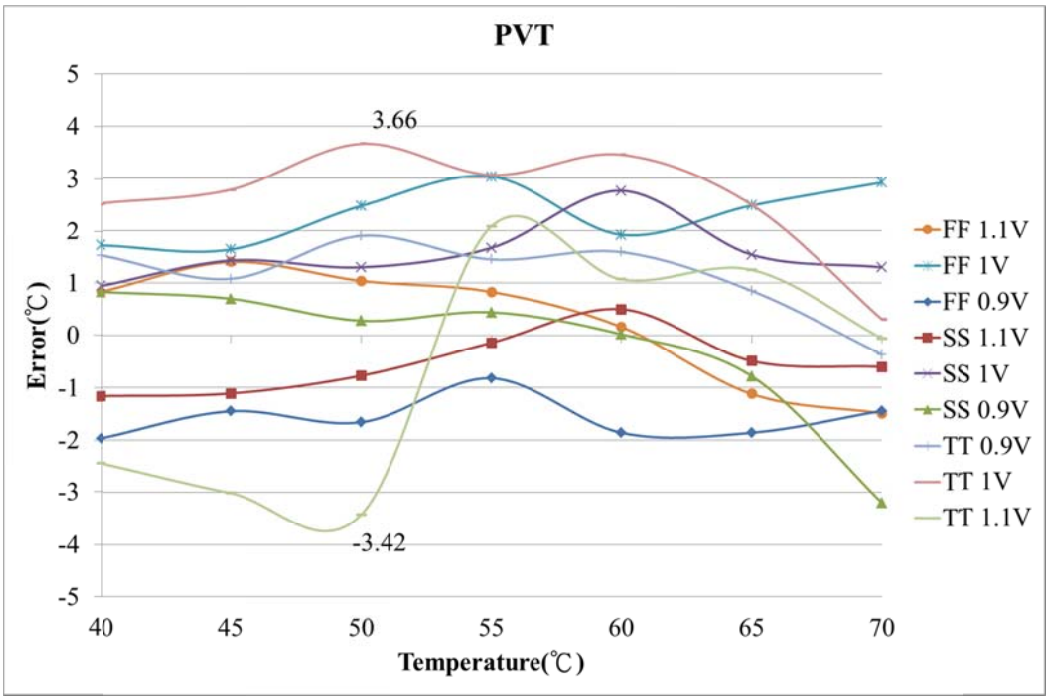


Fig. 6.10: The accuracy of ATWS with process and voltage variations.

After four-point calibration, Fig. 6.9 shows the simulation results of ATWS with process and voltage variations. The y-axis represents the temperature sensor output (ºC) and the corresponding digital code (Temp_out). Thus, we can convert the digital code(Temp_out) into degree Celsius(ºC). In Fig. 6.9, the line IDEL is ideal temperature sensor output. In different process corner and different voltage, the other lines are very close to the ideal line. Fig. 6.10 shows the temperature error of the ATWS with process and voltage variations. The maximum output temperature error with process and voltage variations ranges from -3.42ºC to +3.66ºC. Although each lines have some inaccuracy, proposed ATWS can be used as an abnormal temperature warning sensor for the SoC system. Even with the process and voltage variations, the inaccuracy of the proposed ATWS is still acceptable.

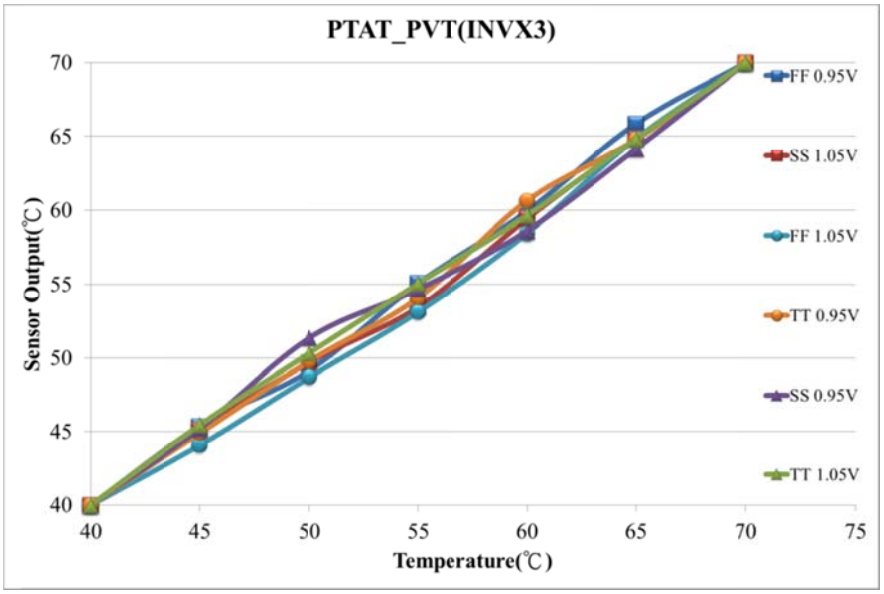


Fig. 6.11: The simulation results of PTAT temperature sensor with four-point calibration at all corner.

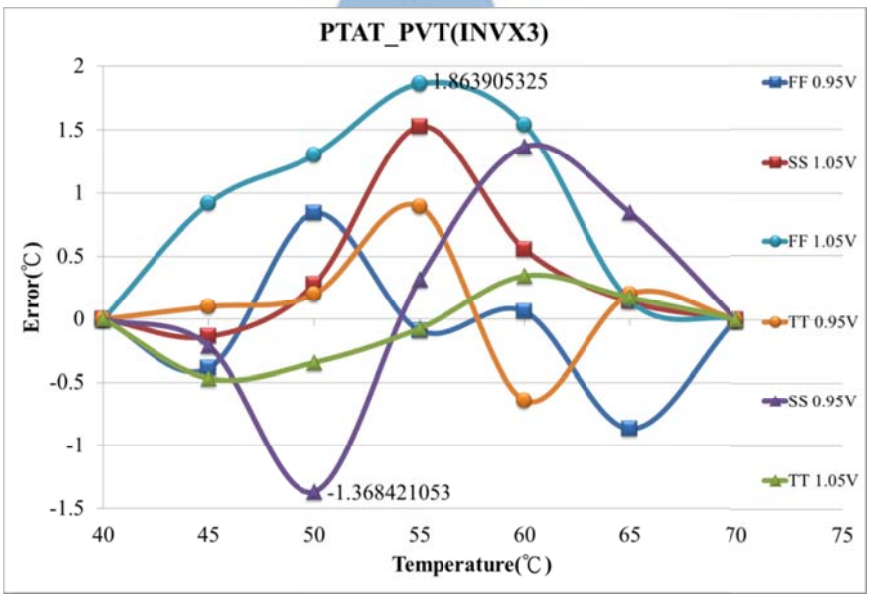


Fig. 6.12: The accuracy of PTAT temperature sensor with four-point calibration at all corner.

We also use four-point calibration method for the PTAT architecture. We have taken 40ºC and 70ºC as calibration points with two voltages, 0.95V and 1.05V, respectively. Fig. 6.11 shows the simulation results of PTAT temperature sensor. Fig. 6.12 shows the accuracy

of PTAT temperature sensor with four-point calibration at all corner. The maximum output temperature error with process and voltage variations ranges from -1.36 ºC to +1.86 ºC if we know the current operating voltage. After calibration at different voltages, the temperature sensor accuracy can be improved. However, we can use the same method with ATWS. In different voltage, we can calculate the slope and intercept by interpolation and extrapolation. Fig. 6.13 shows the simulation results of PTAT temperature sensor. Fig 6.14 shows the accuracy of PTAT temperature sensor with interpolation and extrapolation at all corner. If assume the PTAT can estimate current supply voltage, then we use interpolation and extrapolation get other coefficient a(V_n) to b(V_n) with different voltage. We follow Eq. 6.2 to calculate Temp_out with voltage variations. After calculation, the maximum output temperature error with process and voltage variations ranges from -82ºC to +307 ºC. Therefore, the method of interpolation and extrapolation is not applicable to the PTAT architecture. In the DRE circuit, it is based on relative reference modeling (RRM), the RRM can build up the relationship of these oscillators, since the period of the oscillator is changed with voltage and temperature variations at the same time. When we choose two cells, which their voltage coefficient is very close, and these cells have the characteristics of PTAT.

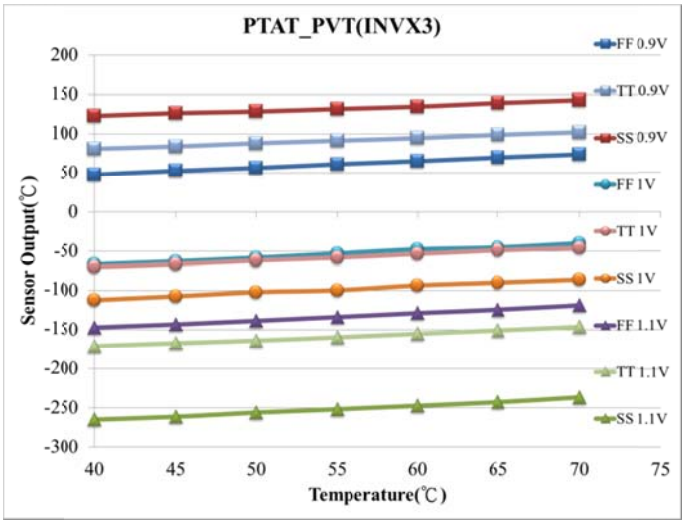


Fig. 6.13: The simulation results of PTAT temperature sensor with interpolation and extrapolation at all corner.

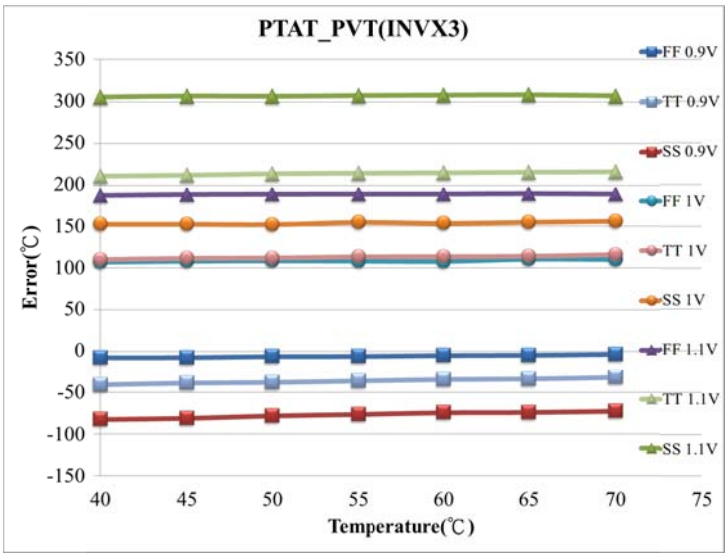


Fig. 6.14: The accuracy of PTAT temperature sensor with interpolation and extrapolation at all corner.

Fig. 6.15 show simulation results of ATWS. Fig. 6.16 shows the accuracy of ATWS with two-points calibration at all corners. In this case, we only have taken 40ºC and 70ºC as calibration points with 1.00V supply. However, the maximum output ATWS error with process and voltage variations ranges from -6.52ºC to +6.55 ºC due to less calibrations points. In addition, in different voltage, the accuracy of ATWS has high accuracy as compared with the PTAT architecture.

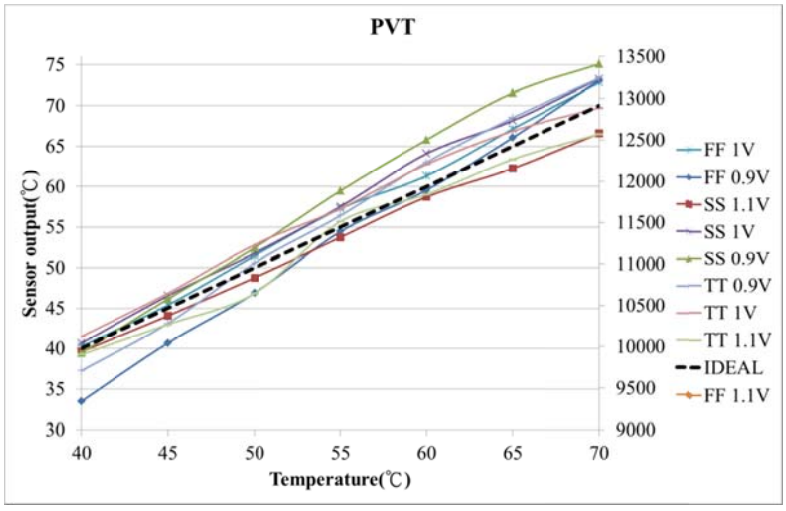


Fig. 6.15: The simulation results of ATWS with two-points calibration at all corners.

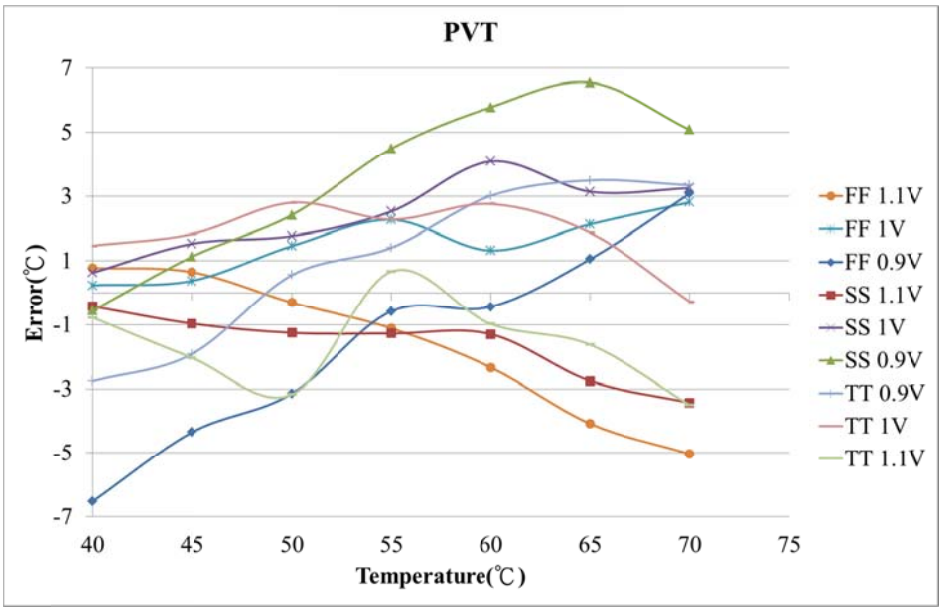


Fig. 6.16: The accuracy of ATWS with two-points calibration at all corners.

6.4 Comparisons Recent Research

Table 6.1 shows the comparisons table of the ATWS with recent smart temperature sensors. The proposed ATWS is not only an all-digital design, but also the only one can against voltages variations. The other recent temperature sensors [38][47][48][50][52] cannot against voltages variations. The temperature error of the proposed ATWS with process and voltage variations is -3.42ºC to +3.66ºC, which is smaller than prior researches [38][47][49][51]. In PTAT architecture [48], their temperature error is very small only with a fixed voltage. If the PTAT architecture [48] operates with voltage variations. Fig. 6.12 shows the accuracy of PTAT temperature sensor with voltage variations, and the temperature error becomes very large with voltage variations. Although the accuracy of dual-DLL-based [52] temperature sensor is very well, and they need only one temperature-point calibration. However, it can only work under a fixed voltage. In addition, the power consumption and chip area are too large in the design. Thus, it is not suitable for system-on-a-chip application.

In addition, in [49] and [51], they have provided the error of temperature sensor with voltage variations. The temperature error of [49] with voltage variations is -90ºC to +90ºC. The temperature error of [51] with voltage variations is -10ºC to +10ºC. With voltage variations, the accuracy of these architectures becomes very worse. Thus, these architectures are not suitable for used as a on-chip temperature sensor with voltage variations.

Table 6.1: Performance comparisons of Temperature Sensors.

Parameter	proposed	[38] TCASII'12	[47] ISCAS'10	[48] TCASI'11	[49] TVLSI'12	[50] VLSI'12	[51] JSSC'10	[52] ISSCC'09
Type	three ring oscillator (all-digital)	PTAT (all-digital)	PTAT (all-digital)	PTAT (FPGA)	Dual DLL (full-custom)	two ring oscillator (full-custom)	two delay line (all-digital)	Dual DLL (all-digital)
Resolution(°C)	0.168	0.139	0.143	0.133	0.78	0.34	0.0918	0.66
Error(°C)	-3.42~3.66 with variation	-5.1~3.4	~10~+10	-0.7~0.6	-4~4	-2.8~2.9	-0.25~0.35	-1.8~2.3
Calibration Point	4	1	2	1	1	1	2	1
Power (uW)	530 uW@ 1.0V	150 uW	55 uW	175 uW	1200 uW	400 uW	36.7 uW	12000 uW
Area(mm^2)	0.0625	0.01	0.01	N/A	0.12	0.0013	0.6	0.16
Conversion Rate(samples/s)	4k	10k	10k	1k	5k	366k	0.002k	5k
Range (°C)	40~70	0~60	0~100	0~100	0~100	-40~110	0~90	0~100
Technology(nm)	90	65	65	220	130	65	350	130
VDD Range	0.9~1.1	fixed 1.0V	fixed 1.0V	fixed 2.5V	fixed 1.2V	fixed 1.2V	fixed 3.3V	fixed 1.2V

6.5 Summary

In this chapter, we propose an abnormal temperature warning sensor system (ATWS) with process and voltage variations. The proposed design can be implemented by standard cells. In addition, we also propose the four-point calibration method to against voltage variations and process variations. The proposed design can operate with a low supply voltage, and is very suitable for low-power and low-cost system-on-a-chip application.

Chapter 7

Conclusion and Future Works

7.1 Conclusion

In this thesis, we propose an efficient method to build up a cell-based on-chip silicon oscillator (CBOCSO) for frequency compensation with PVT variations. We proposed two versions of CBOCSO with multi-points calibration (MPC) and four-point calibration (FPC), respectively.

The proposed two CBOCSOs use a relative modeling and they use the voltage and temperature classifier to roughly estimate the supply voltage and operation temperature at chip run time. The CBOCSO with MPC requires many calibration points, and thus, its testing cost is high. In the CBOCSO with FPC, we make a change on the cell selection rules to choose the cells of the delay ratio estimator. With this method, the CBOCSO with FPC not only can reduce the calibration points but also improves the accuracy of the output frequency.

These two CBOCSOs are both designed with standard cells. Therefore, the proposed CBOCSOs provide a systematic way to automatically generate the on-chip oscillator with PVT variations. The proposed design can operate with a low supply voltage, and is very suitable for low-power and low-cost system-on-a-chip applications.

7.2 Future Works

In this thesis, the CBOCSO with FPC has improved some disadvantages of the CBOCSO with FPC. However, the CBOCSO with FPC still has some drawbacks. In our proposed of delay ratio estimator (DRE) in section 4.1, it is composed of three oscillators. The frequency of these three oscillators will affect the performance of CBOCSO. If the frequency of these three oscillators is faster, the voltage classifier of CBOCSO need to have a higher calculation speed, but the power consumption will become larger. Thus, there exists a tradeoff between the power consumption and the performance. We must consider the power consumption with SoC design. Thus, the frequency of these three oscillators can not be too fast.

When the integrated circuit at the run time, there exists immediate voltage variation, the immediate voltage change is called the dynamic supply noise. However, the proposed CBOCSO requires a longer computation time, and thus, it cannot against dynamic supply noise. If we can provide a faster method of calculating, the issue of dynamic supply noise can be also compensated, and then the CBOCSO will become more stable. In addition, many researches design to against static voltage variations [7][12]-[15][23]. Only the ring VCO oscillator [15] can against dynamic supply noise, however, it only has 1% dynamic supply noise, most of the static voltage variations [7][12]-[15][23] has 5% to 20% drift amount. Thus, in most of research discusses about 5% to 20% drift amount of static voltage variations. Therefore, in this thesis has -10% to +10% drift amount of static voltage variations.

In section 4.8, we summarize the difference between MPC and FPC, although we have reduced the testing costs, however, the FPC is still has too many in off-chip process. The FPC requires calculate two-point linear regression, interpolation, extrapolation, coarse code

and fine code. However, the two-point linear regression, interpolation and extrapolation can be integrated into the circuit automatically calculated. The coarse code and fine code require calculate coarse and fine resolution, these require more decimal arithmetic. Thus, the coarse code and fine code require calculating in off-chip. Therefore, if we want to reduce testing cost, we can only calculate coarse code and fine code in off-chip.

In chapter 6, although the proposed abnormal temperature warning sensor (ATWS) can work with different voltages, but the accuracy of temperature sensor is not good enough. However, the accuracy of the PTAT architecture is good with a fixed voltage. Thus, if we can combine the PTAT architecture and the circuit of voltage classifier, the accuracy of temperature sensor may become better.

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