國 立 中 正 大 學

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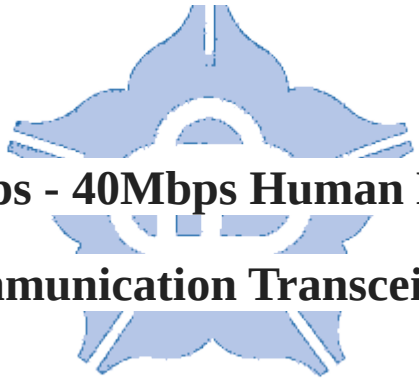
碩 士 論 文

1Mbps - 40Mbps 人體通道傳收器設計



Design of 1Mbps - 40Mbps Human Body Channel Communication Transceiver

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摘要

隨著國民平均年齡的提升，以及行動裝置與半導體科技的進步，有越來越多生物醫學結合半導體科技的研究被發表，人體區域網路就是其中的一項應用。在眾多的人體區域網路的實現與應用中，身體傳輸通道是一項全新的通訊概念。身體傳輸通道是利用人體表皮當作資料與訊號傳輸的媒介。相較於其他傳統的有線或無線傳輸媒介，利用人體傳輸通道有許多優點，例如不需要有線的傳輸、低功率消耗、以及方便安裝與使用。但是由於人體天線效應影響，許多外界的電磁波會干擾到身體傳輸通道的穩定性，進而增加接收端電路在回復資料與時脈的困難度。

本論文提出一個低功率消耗、低硬體成本、高速傳輸速率、與高干擾容忍的人體通道傳收器。在此傳收器的傳送端部分，我們加入了展頻時脈產生器去減少對外部電路的電磁干擾。展頻時脈產生器是在一般的時脈產生器中加入調變，使其產生的時脈訊號頻率會在一個範圍內上下擺動，達成展開頻率的效果。比起其他解決電磁干擾的技術，展頻時脈產生器的成本較低。

在傳收器的接收端前端類比電路部分，我們使用了可調式的放大器架構針對因為不同的傳輸長度而有不同接收電壓大小的訊號進行放大。在數位電路部分，我們採用了 5 倍頻率超取樣時脈與資料回復電路架構，搭配中央取值機制與增減演算法。因此只需要利用到少數量的暫存器成本即可達到高干擾容忍與展頻時脈回復的成果。所以本論文所提出的人體通道傳收器非常適合應用在人體通道傳輸上。

本論文之晶片是以 90 奈米製程的標準元件庫實現，具有很好的製程移轉能力。工作範圍為 1Mb/s 到 40Mb/s，晶片面積為 0.2mm^2，功率消耗在 40Mb/s 為 1.69mW,在 1Mb/s 為 1.61mW.

關鍵字 ： 身體傳輸通道，接收器，高雜訊容忍，高傳輸速率，低功率。

Abstract

In recent years, biomedical applications with semiconductor technologies had become more and more popular. Body area network (BAN) is one of the applications. Traditionally, there are many approaches to implement the BAN and the body channel communication (BCC) is a novel concept of the communication scheme. BCC uses the human body as the signal transmission medium to transmit physiological signals and there are many advantages than wire-less communication, such as low power consumption and easy to use. However, because of the the body antenna effect, there are many external electromagnetic interferences around the human body that will interfere the reliability of the human body channel and increases the design complexity of the clock and data recovery (CDR) circuit.

In this thesis, we propose a low-power consumption, low hardware cost, high-speed and large jitter tolerance wideband signaling (WBS) transceiver for BCC. In the proposed WBS transmitter, we adopts a spread-spectrum clock generator (SSCG) to achieve EMI reduction, because the body antenna effect will radiate the signal power into the air and disturbs the neighbor circuits. The SSCG is modulated with a spreading profile in the traditional clock generator. The output frequency of the SSCG spreads out in a frequency range and achieves spread spectrum. Comparing with other solutions for EMI, the SSCG has lower cost.

In the proposed analog front-end circuit of the WBS receiver, we use a variable gain amplifier to amplify different magnitude of the received signals. In the digital part of the circuit, we adopt the 5X blind oversampling CDR architecture with center-picking method and an Add-Drop FIFO algorithm. Thus, we can use extremely low cost to achieve large jitter tolerance and recover the data with spread spectrum, and it’s very suitable in BCC application.

The chip of this thesis is implemented in TSMC 90nm standard performance CMOS process, and thus it has good portability over different processes. The core area is 0.2mm^2 and the power consumption is 1.69mW at 40 Mb/s and 1.61mW at 1 Mb/s, respectively.

Keyword: BCC, transceiver, high-jitter tolerance, high data rate, low power consumption

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Chapter 1

Introduction

1.1 Human Body Area Network Overview

In recent years, biomedical applications with semiconductor technologies had become more and more popular. The aging of the population also drives for personal healthcare applications. Traditionally, the medical healthcare devices such as electrocardiography (ECG), electromyography (EMG), thermometer, and sphygmomanometer needs occupying bulky volume and space, and more importance is that these devices sensor all needs a wireline connection to transfer the physiological signals and that will cause great inconvenience for the patients in daily life.

As modern mobile communication devices has become an integral part of human life, there is a new type of communication generally knows as body area network (BAN) which was introduced and organized by IEEE 802.15 Task Group 6 (TG6) to standardize the frequency band and the protocols of medical and multimedia communication around the human body [1]. The BAN can provide connectivity between each wearable or implantable device, which is distributed on the human body, within the communication range, corresponding to 1-2 m. For the BAN devices, there are some features must be satisfied, such as lightweight, small-size, and low-power consumption [2]. With the help of the BAN, the wearable devices such as earphones, video eyeglasses, and head-mounted displays can offer more wide range of applications from healthcare to ambient intelligence and multimedia [3]. Fig. 1.1 shows the various applications based on the BAN.

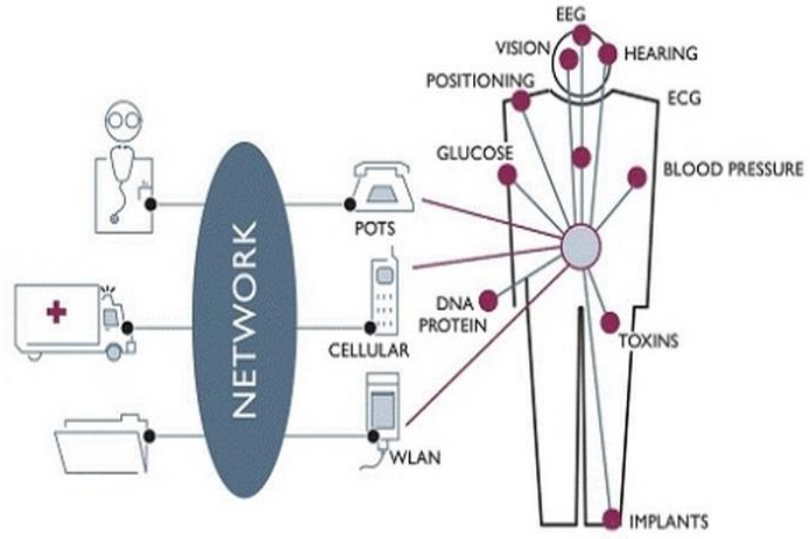


Fig. 1.1: Various applications based on BAN; this photo is captured from the WIFINODES website of http://www.wifinotes.com/computer-networks/body-area-network.html.

Traditionally, there are many approaches to implement the BAN. These approaches are mainly grouped into two categories. The first class uses external mediums such as a wire and the air to transmit data and the other uses the human body as the transmission medium.

In first class, the radio-frequency (RF) applied to the BAN uses the 2.4-GHz ISM band for Bluetooth and Zigbee [4]-[6]. Fig. 1.2 shows a typical RF transceiver. The transceiver is composed of an antenna, a TX/RX switch, a power amplifier, a pulse generator, a low-noise amplifier, a variable gain amplifier (VGA), a band-pass filter, and an analog-to-digital converter (ADC). Although RF scheme can provides more practical usability for short range communication. However, it has potential problems such as low data rate, high power consumption, and vulnerability to interference by external user who uses the nearby frequency bands at the 2.4-GHz.

The recent investigations found that the Bluetooth techniques using 2.4-GHz band is not appropriate for BAN because of the large path loss affected by the body shadowing

effect [4]. Besides, the RF scheme must use the antenna to transmit and receive signal, and the antenna occupies lots of space and it also causes high power consumption with the power amplifier. Even the Zero-G receiver [5] for achieving significant power saving, the Bluetooth radio still consumes too much power, and it is not suitable for long-term personal healthcare applications.

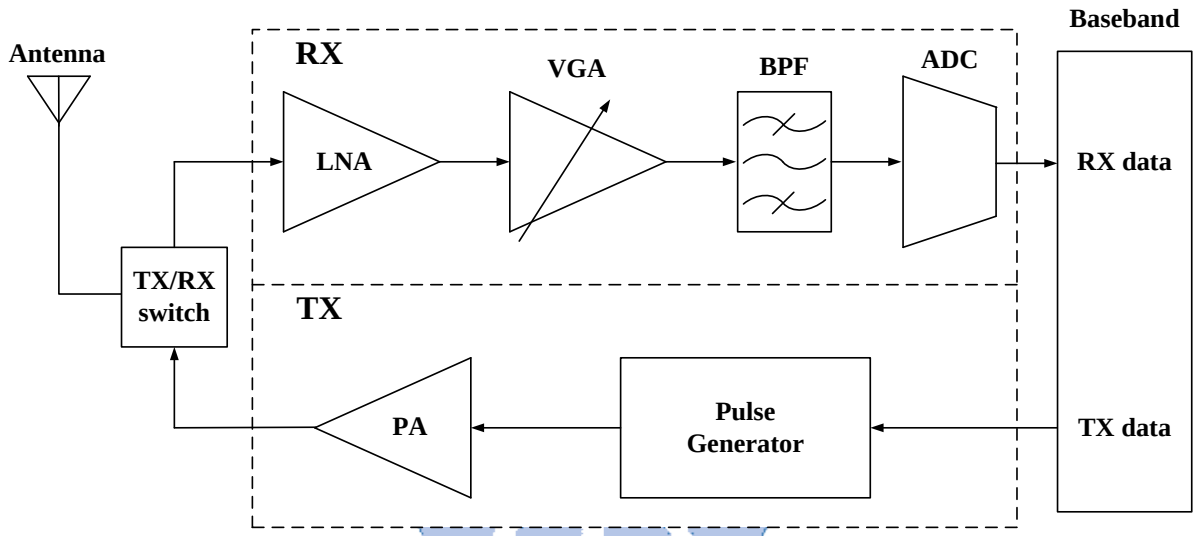


Fig. 1.2: Typical RF transceiver.

Thus, in the second class, a promising new method, body channel communication (BCC), was introduced to solve these problems. The concept of the BCC was first introduced by Zimmerman [7]. BCC does not use the wireline as the transmission medium [8] but uses the human body as a signal transmission medium to transmit physiological signals to a central device such as a personal digital assistant (PDA) or a cellular phone. After receiving the signals, the mobile device analyzes these physiological signals immediately or directly transfers the data to the medical center to achieve healthcare purposed.

Fig. 1.3 shows the concept of the human body channel communication [9]. The communication channel is formed by attaching two Ag/Agcl or metal electrodes to the

human skin. One of the wearable electrode as the transmitter port, another electrode as the receiver port, and the human body is the transmission medium. The communication distance is from 10 cm to 120 cm, depending on the devices and the sensors location on the body. The communication frequency is dependent on the transmission schemes, ranges from several kHz to several MHz. Using the human body as a signal transmission medium has many advantages. Firstly, the body channel shows less path loss than the air-channel because of the high conductivity of the human body channel as compared with the air. Secondly, since this technique is based on near-field coupling, thus, the signal radiated from human body decays rapidly, less interfering with adjacent electronic devices. Finally, because the physiological signal and data can be directly transmitted into human body channel with electrode as the interface, there is no needs to use external antenna. Thus, the power consumption can be greatly reduced.

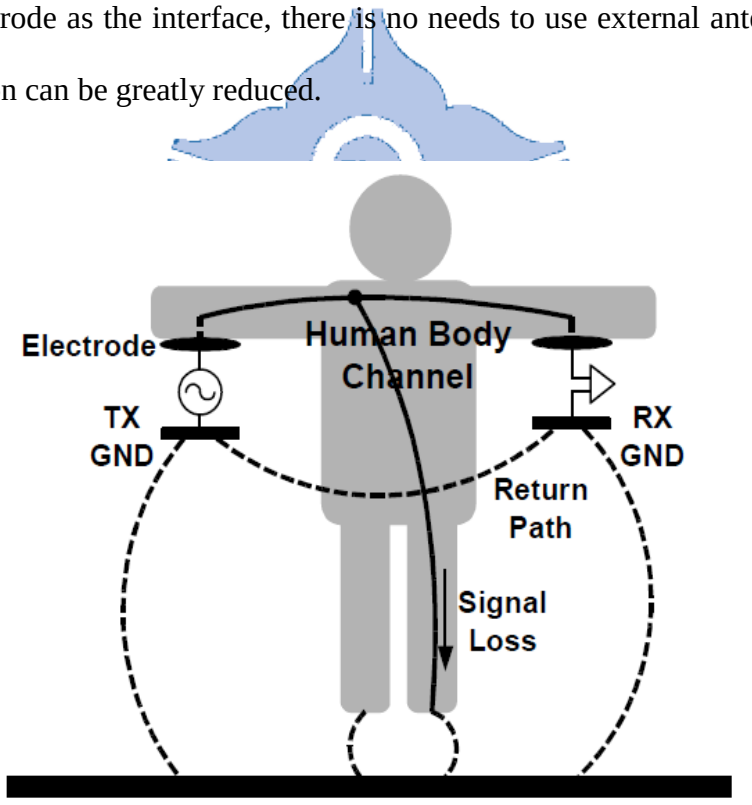


Fig. 1.3: Concept of the human body channel communication.

1.2 Characteristics of Human Body Channel

In order to utilize the human body as the communication medium, we need to know the characteristics of human body channel. Nowadays, the characteristics of human body channel had been studied and investigated in [7], [10], [11], [12]. These studies have indicated that at different transmission distance and frequency, the human body channel can be represented as a discrete RC model.

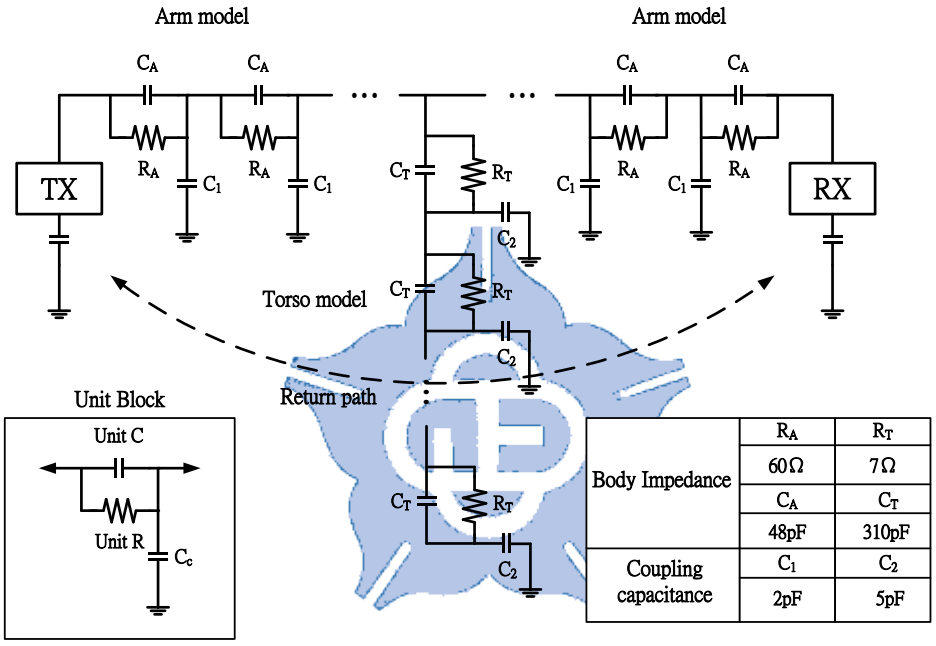


Fig. 1.4: Near-field coupling RC model of the human body.

Fig. 1.4 shows a near-field coupling RC model of human body [10]. In order to represent the truly shape of the human body, the human body model is consists of three cylinders to model the body torso and two arms. Each cylinders consists of different numbers of unit blocks. For each unit block, the complex impedance and the coupling capacitance to the external ground is calculated by Gabriel's experimental results [11] and Zimmerman's method [7], individually. The R and C values in the discrete RC model are

calculated from the electrical properties in 10-60 MHz. Since each RC unit block represents for the 10-cm long of body tissues, thus, we can simulate the N x 10 cm body channel length by cascading the N-stage unit blocks. In the RC circuit model, the return path is formed the electrical coupling between the transmitter and receiver grounds through the external ground.

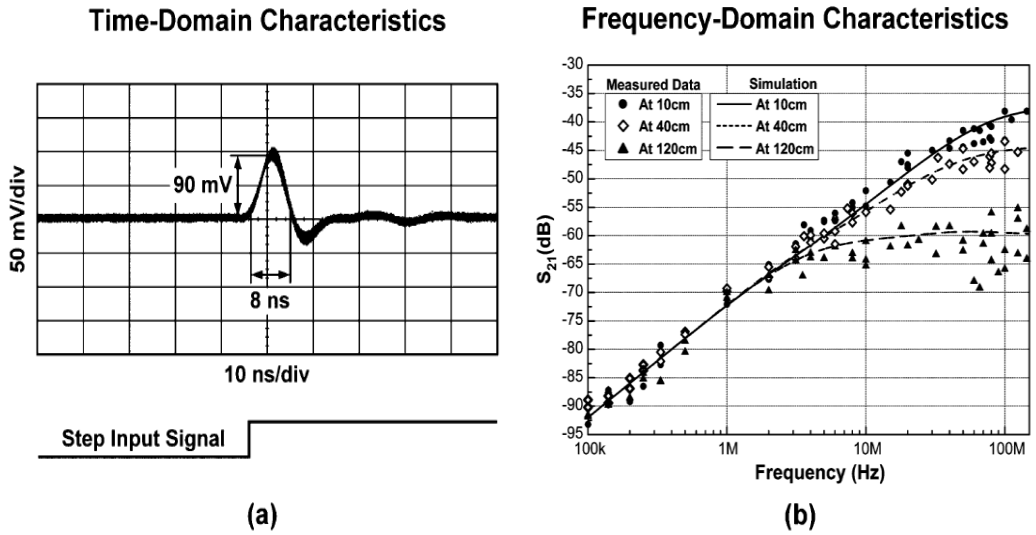


Fig. 1.5: Characteristics of human body channel [10]. (a) In the time-domain (b) In the frequency-domain

The characteristics of human body channel are investigated in both the time-domain and frequency-domain [10]. Fig. 1.5 (a) shows the measured output waveform for the time-domain. The input signal is 2 MHz square wave with 1-V amplitude, the channel output signals are measured to be the positive and negative small pulse signals with no DC offset. When the channel distance on the body increases, the peak of the pulse is lowered and its width becomes wider. For the frequency domain analysis, the S_{21} parameter of the body channel is measured. Fig.1.5 (b) shows the measurement of S_{21} parameter with frequency ranges from 100 kHz to 150 MHz. When the frequency is below than 10 MHz,

the channel distance has a slight effect on the receiver power, however, beyond 10 MHz, the channel distance can have a great impact on the receiver power.

The investigation result shows that the human body behaves as a bandpass filter with a bandwidth of about 100 MHz and the range of 10 kHz to 100 MHz is founded as the suitable frequency band for human body channel communication.

According to the investigation of previous studies, we build up a simple discrete RC model by simplifying the previous complex discrete RC model to simulate the human body channel. We also discuss the characteristics of the simple discrete RC model in the time-domain and the frequency-domain. Fig. 1.6 shows the simplified RC model. The simple RC model consists of only two resistors and three capacitors. We can adjust the ratio between capacitors and resistors to simulate different frequency signals waveform transmitted through the human body channel.

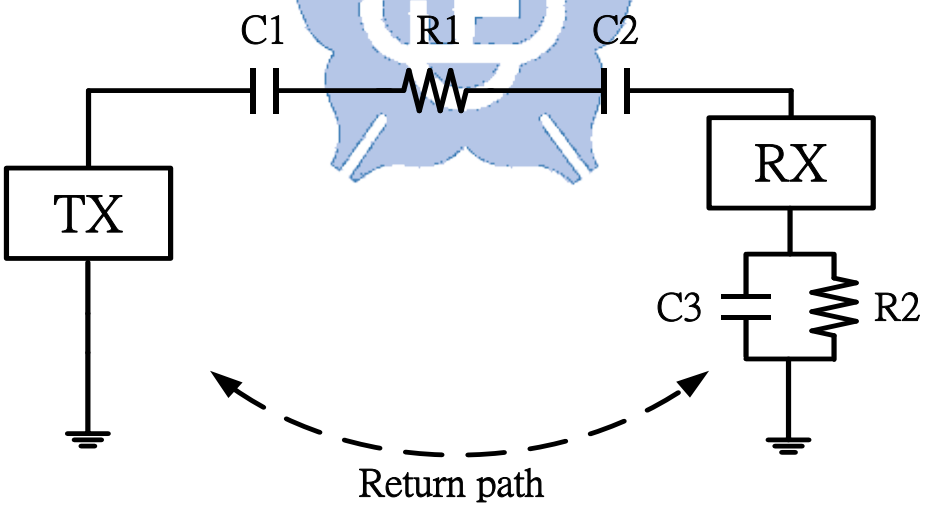


Fig. 1.6: Simple discrete RC model

Fig.1.7 shows the measurement setup for the human body channel. The distance between the transmitter and the receiver is 10cm. The transmitter is a square wave signal generator. The amplitude of the square waveform is 1 V and the frequency range from 1 MHz to 8 MHz. The transmission signal is transferred to the HBC by electrode. Another electrode of the receiver is connected to a digital oscilloscope and the ground between the transmitter and the receiver are floated.

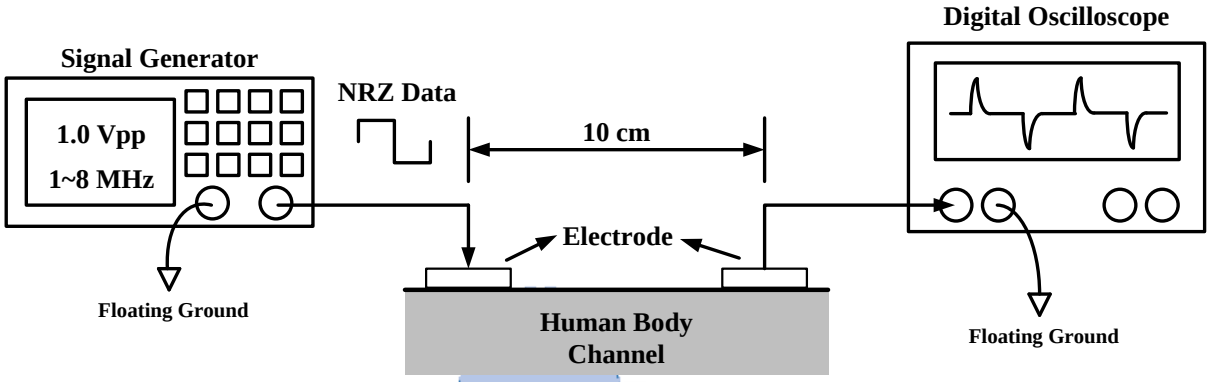


Fig. 1.7: Measurement setup for the investigation of the HBC.

Fig. 1.8 and Fig. 1.9 shows the characteristics of time-domain between the real measurement results and the simulation of the simple discrete RC model. The input signal is a square wave with 1-V amplitude and the frequency ranges from 1 MHz to 8MHz at 10-cm distance.

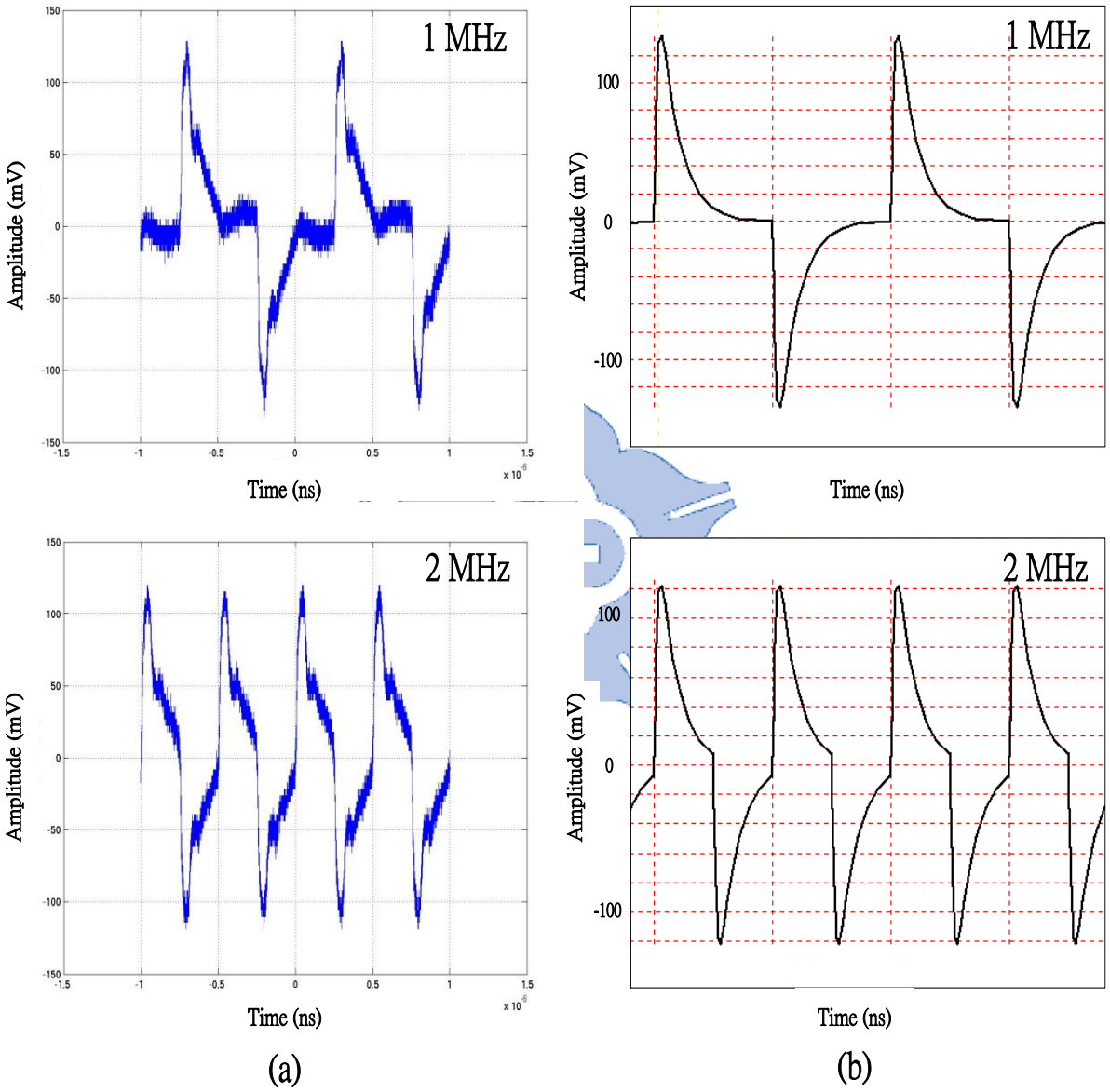


Fig. 1.8: Transient channel response from 1 MHz to 2 MHz. (a) Measured step response. (b) Simulation step response.

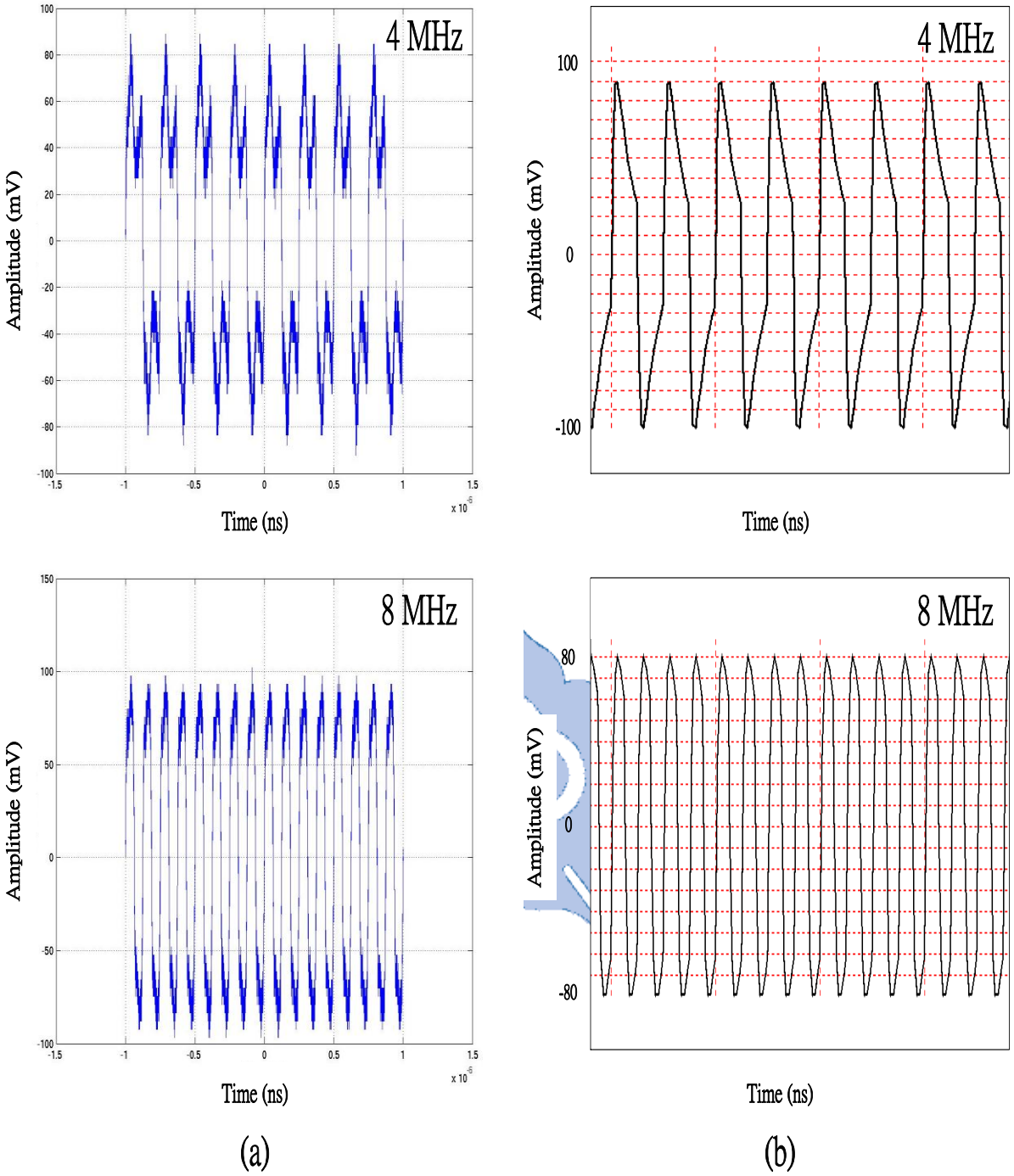


Fig. 1.9: Transient channel response from 4 MHz to 8 MHz. (a) Measured step response. (b) Simulation step response.

The simulation results of the simple RC discrete model show the characteristics of human body channel. The output waveform has positive and negative small pulses with no DC offset. As the transmission frequency increases, the peak value of the pulse is lower, and the shape of the output waveform is more like a sin wave. However, due to the real measurement environmental impacts, there are still different between the real waveform and simulation results.

Fig. 1.10 shows the characteristics of frequency-domain in simple RC discrete model. For the frequency-domain analysis, S_{21} parameter of the simple RC discrete model is measured. The simulation result is relative similar to the pervious investigation as shown in Fig. 1.5(b). The simulation result shows that below 4 MHz, the body channel model is relatively deterministic, with at most 7 dB of derivation regardless of the distance. However, beyond 10 MHz, the length of transmission distance has great impact on the received power.

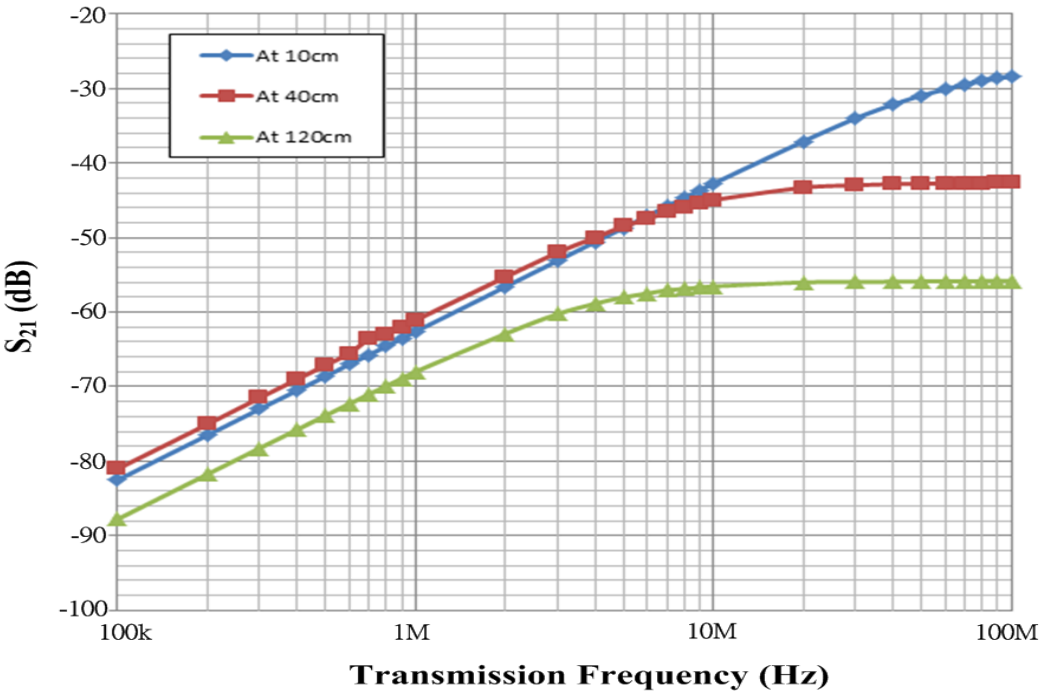


Fig. 1.10: Characteristics of simple discrete RC model in frequency-domain.

1.3 Human Body Antenna Effect

Communication reliability is also an important issue must be considered when we use the human body as the transmission medium. In addition to the characteristics of human body channel, there are many researches had indicated that the body antenna effect also cause great impact to the human body channel communication [10], [13], [14].

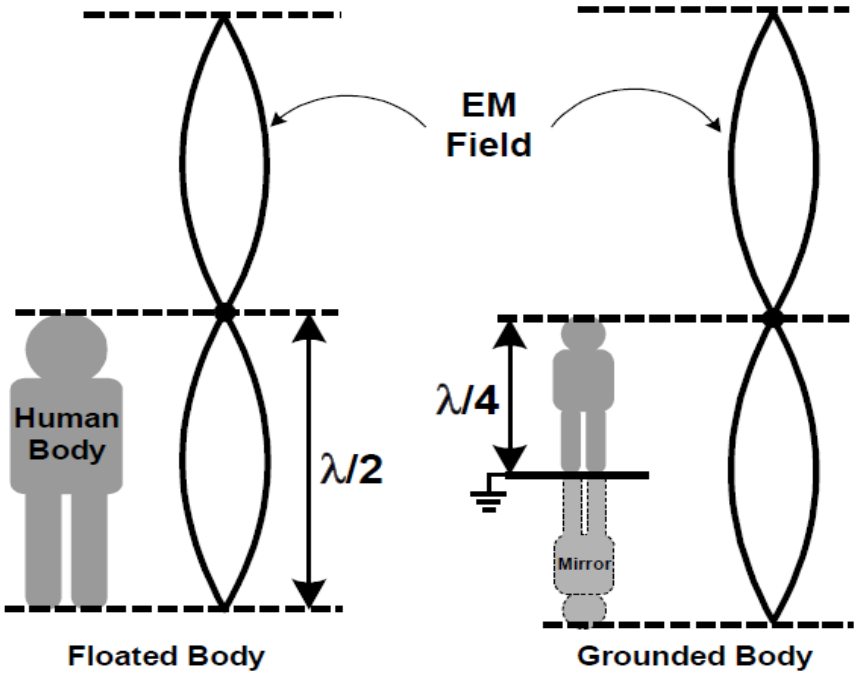


Fig. 1.11: Human body antenna effect [13].

Fig. 1.11 shows that the human body under external electromagnetic fields behaves as an antenna [13]. The resonance frequency of the human body determined by the wavelength (λ) which is equal to twice of the human height. Besides, if the human body is grounded, the resonance wavelength (λ) is equal to four times of the human height because of the mirror effect [14]. Since the human body is a lossy conductor with its conductance value of < 0.1 S/m and has a complex shape, the peaking of resonance is not sharp but broadly distributed. Therefore, the human body operates as a wideband antenna in 30-400 MHz

frequency range, which overlaps the suitable frequency band for human body channel communication range from 10 kHz to 100 MHz [10], [12].

Due to the human body antenna effects, the human body will absorb external electromagnetic interferences or radio signals into the human body channel, and that will degrades the signal to interference ratio (SIR) and corrupts the transmission signal significantly. In order to measure the strength of the interferences, a spectrum analyzer is connected to the right hand of a 1.78m human subject using a metal electrode and coaxial. Fig. 1.12 shows the NCTU Si2 LAB prototype platform of the measurement.

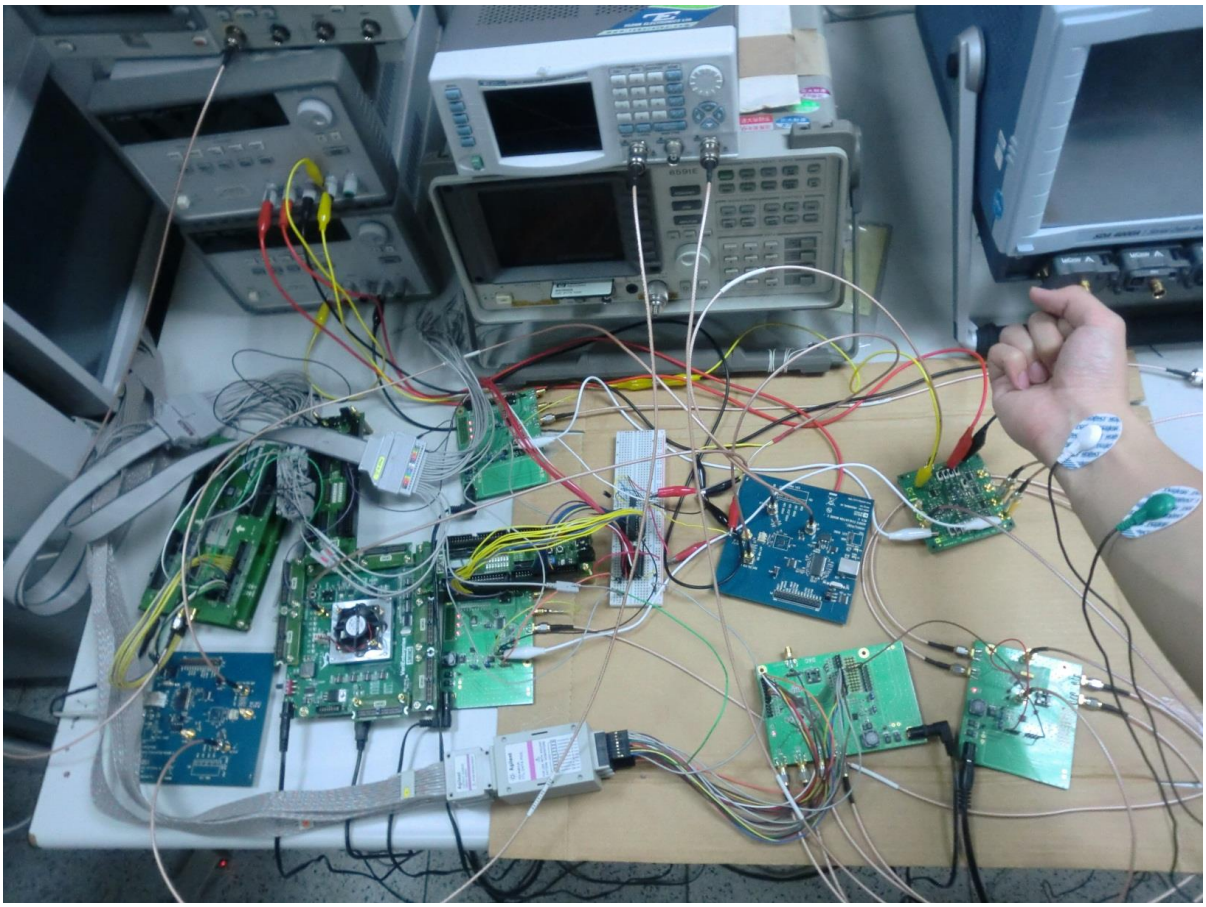


Fig. 1.12: NCTU Si2 LAB prototype of measurement platform.

During the measurement, one of setting step is required consideration. All of measurement instruments, such as the signal generator and the spectrum analyzer are powered by uninterruptible power supply (UPS) in order to float the ground. Because the common ground will cause a return path from transmitter to receiver and that will influence the measurement results.

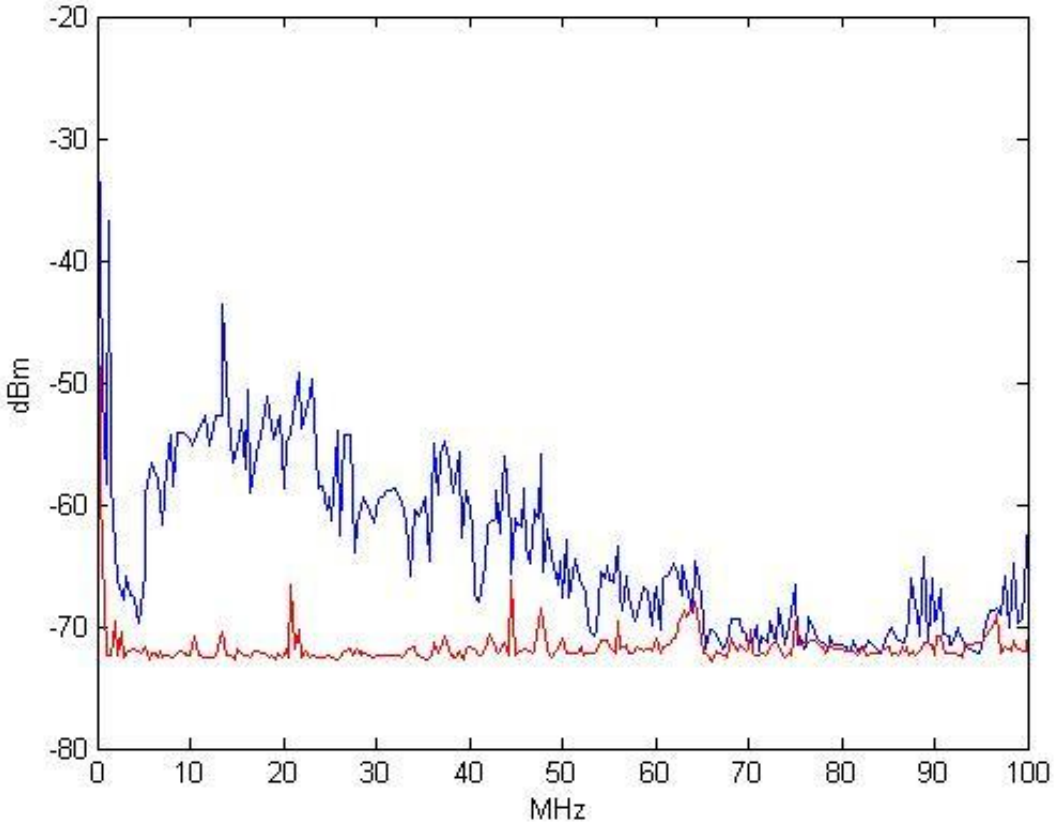


Fig. 1.13: Measured in-band interferences to the body channel receiver.

Fig. 1.13 shows the measured in-band interferences coupled to the receiver from wireless sources nearby. The red line represents the power spectrum of TX electrode and RX electrode which didn't attach to the human body skin. Therefore, there is only air coupling between the TX electrode and RX electrode. The blue line represents the power spectrum of TX electrode and RX electrode attached to the right hand of the human subject.

We can find that there are various interferences, such as cordless phone, FM radio broadcasting tower, and other electric devices, within the 100 MHz frequency band of human body channel.

The human body not only absorbs the external electromagnetic interferences but also radiates electromagnetic emission outside of the human body, which can influence the operation of neighboring electronic devices. The human body channel communication with high frequencies is beneficial to achieve high signal to noise ratio (SNR) and data rate. However, the fast change of the electric field induces electromagnetic emission outside of the human body. At high frequencies, the human body operates as an antenna which radiates the signal power into the air. To investigate the body antenna effect to the nearby electric devices, the electric-field (E-field) strength is measured around human body. Fig. 1.14 shows the measured E-field strength around the human body [10]. This experiment result shows that the E-field magnitude increases with the transmitting frequency and the maximum radiated power is 30 times larger than that of the minimum power at 4 MHz. The measured E-field is not regular and its directivity at different frequency is unpredictable. That is because there are many factors that affect the measurement, such as complex shape of a human body, height differences of each person, and different pose of the person.

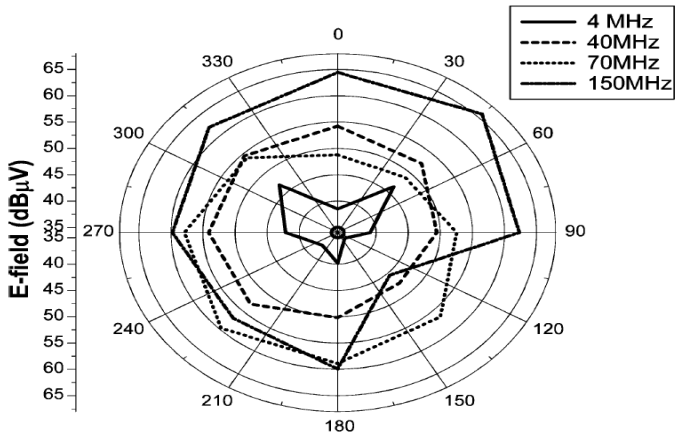


Fig. 1.14: E-field pattern around a person [10].

Because of the body antenna effect, the human body not only injects various external radio interferences into the human body channel, but also radiates the signal power into the air. Then, it not only causes enormous jitter to the receiver circuit but also causes electromagnetic interferences to the nearby electronic devices, and that will be a design challenge for the transmitter and the receiver circuit.

1.4 Introduction to Spread Spectrum Clock Generator

Because of the body antenna effects [10], the human body not only absorbs the external interferences but also induces electromagnetic emission outside the human body which can influence the operation of neighboring electronic devices. In order to reduce the electromagnetic interference (EMI), there are several techniques proposed to prevent the circuits from interfering. These techniques are metal shielding, pulse shaping filter, slew rate control, differential clocking, and spread-spectrum clocking. However, these techniques all have some drawbacks. One of the most serious drawback is the cost is too expensive. Therefore, spread-spectrum clock generator (SSCG) [15] is proposed to reduce the EMI with lower cost and simpler design complexity.

The spread-spectrum clock generator is widely adopted in many data transfer devices, such as USB 3.0, SATA 3.0, PCI-E 3.0, and DisplayPort. Spread-spectrum clock generator is a phase-locked loop (PLL)-based circuit and the spread-spectrum is realized with frequency modulation technique to disperse the energy of carrier frequency.

Fig. 1.15 shows the frequency modulation profile of center-spread SSCG. The spreading ratio is α, the baseline frequency is F_{center}, and the modulation frequency is f_m. The average frequency (baseline frequency) in the center-spread modulation should be equal to the non-spread clock frequency. In addition, the spreading ratio determines the maximum and minimum output frequencies of SSCG. For example, if F_{center} is 100 MHz, and the spreading ratio (α) is 10 %, the output clock frequency ranges from 95 MHz to 105 MHz.

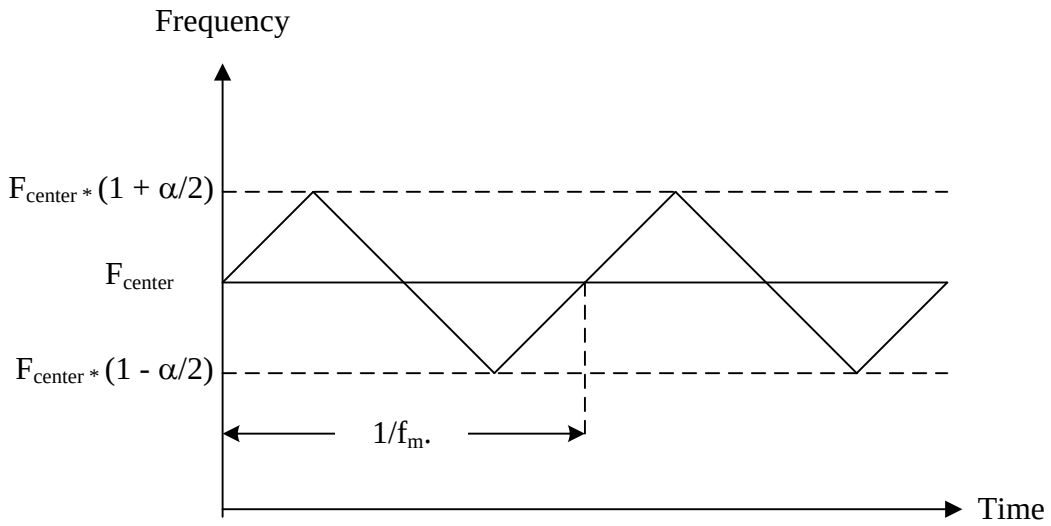


Fig. 1.15: Spread spectrum clock generation.

Fig. 1.16 shows the example of the EMI reduction before and after spread spectrum. The red section is spread-spectrum off stage, and the black section is spread-spectrum turn on stage. We can see that before the spread-spectrum turn on, the peak power of the clock is very high. After the spread-spectrum turn on, the peak power has been reduced to a lower magnitude. This phenomenon indicates the EMI reduction, and it makes the nearby electric devices operating profitably.

Comparing to conventional EMI reduction approaches, spread-spectrum clock generator has many advantages such as low cost, easy for integration, low design complex, and excellent EMI reduction performance. Hence, this scheme is widely adopted in SoC applications.

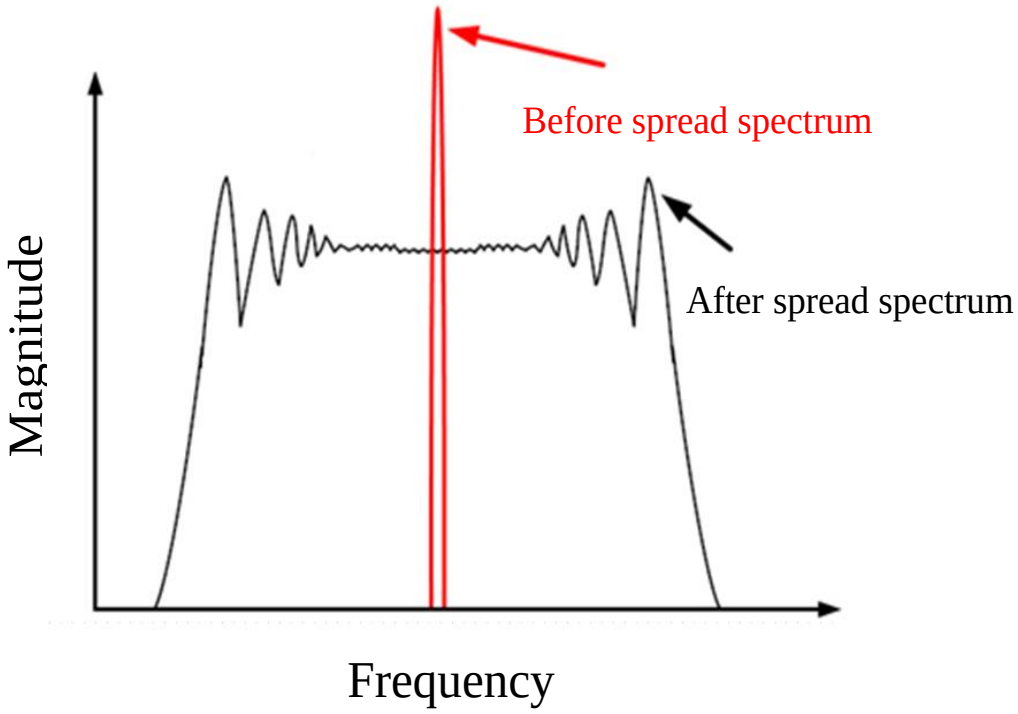
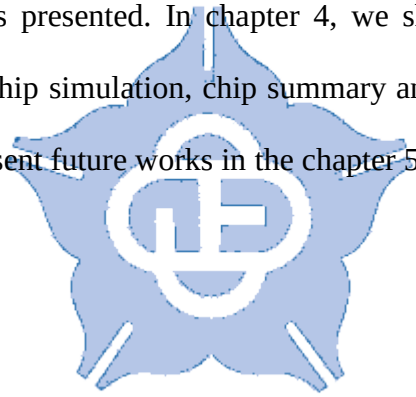


Fig. 1.16: Reduce peak power with spread-spectrum technique

1.5 Thesis Overview

In this thesis, we discuss a wideband signaling (WBS) transceiver with a direct-coupled interface (DCI) as the transmission method. The WBS transmitter is adopted a spread spectrum clock generator (SSCG) as the clock generator. The WBS receiver is a 5X blind oversampling clock and data recovery (CDR) circuit with an add-drop FIFO scheme.

In chapter 2, we discuss the basic concept of the transceiver circuit and survey of proposed body channel communication scheme. Besides, we also survey the conventional CDR circuit. In chapter 3, the proposed WBS transceiver with DCI for body channel communication applications is presented. In chapter 4, we show the simulations results, including chip test plan, full chip simulation, chip summary and comparison table. Finally, we make a conclusion and present future works in the chapter 5.



Chapter 2

Survey of Body Channel Communication Transceiver

2.1 Basic Components of BCC Transceiver

2.1.1 Transmitter

Fig. 2.1 shows the block diagram of BCC transmitter. The transmitter is composed of a encoder, a modulator, a driver, and a transmitter (TX) electrode. After the sensor node senses the physiological signals or multimedia data, the transmission data are sent to the encoder to encode the data. Then the encoded data sent to the modulator to modulate the data. After the data is modulated, the data pattern is sent to the human body channel through the driver and TX electrode.

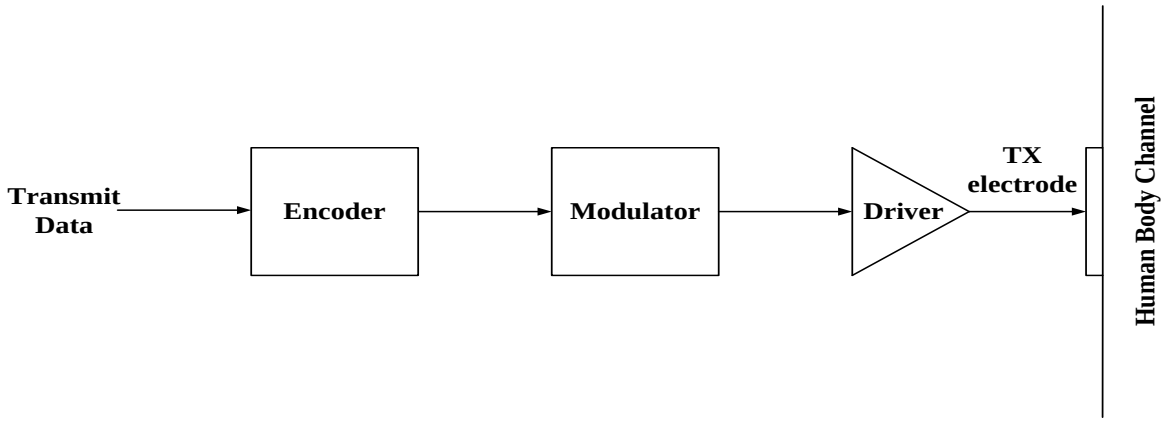


Fig. 2.1: Block diagram of BCC transmitter.

2.1.2 Receiver

Fig. 2.2 shows the block diagram of the BCC receiver. The receiver is composed of a receiver (RX) electrode, an amplifier, a clock and data recovery (CDR) circuit, a demodulator, and a decoder. After the receiver electrode receives the weak signal, which is corrupted by human body channel, the signal is amplified by the amplifier and then sends to the CDR circuit. The CDR circuit has to extract the original clock from the incoming data pattern and retimes the incoming data to perform clock and data recovery. Then the receiver demodulates and decodes the received data and completes the data transmission.

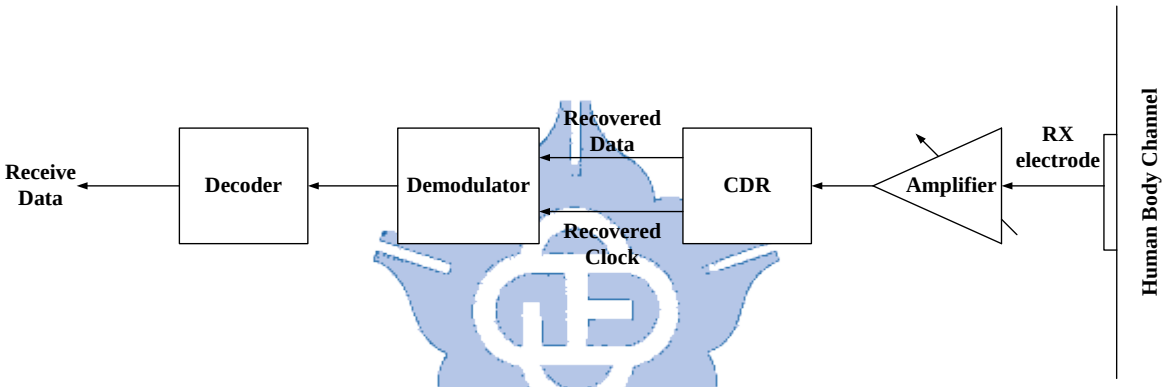


Fig. 2.2: Block diagram of BCC receiver.

2.2 Conventional BCC Transceiver

2.2.1 Near-Field Electrostatic Coupling Scheme

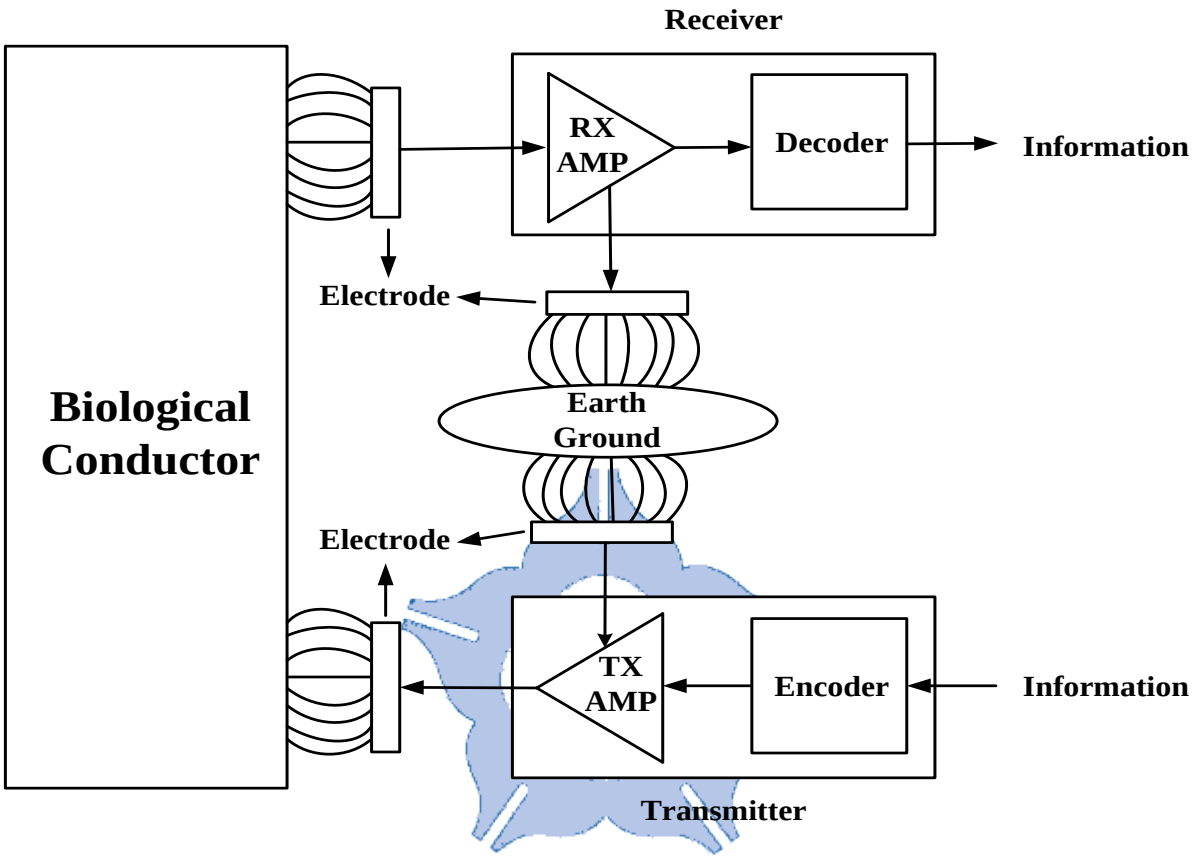


Fig. 2.3: Block diagram of near-field electrostatic coupling transceiver.

The near-field electrostatic coupling scheme using a narrowband low-frequency signal was first introduced by Zimmerman [7]. Fig. 2.3 shows the basic near-field electrostatic coupling transceiver. The transceiver is composed of an encoder, a TX amplifier, a RX amplifier, a decoder, and two pairs of electrodes. The transmitter capacitive couples a modulating pico-ampere displacement current through the human body to the receiver. The return path is provided by the earth ground, which includes all conductors and dielectrics in

the environment that are in the nearby of the BCC devices. In order to prevent the shorting of the electrostatic coupling transceiver, the earth ground needs to be electrically isolated from the body.

This type of transceiver, which using the human body as transmission medium, does not need to use the antenna to send and receive signals, thus, the size of near-field electrostatic coupling transceiver is smaller than RF type transceiver. In addition, the power consummation is also less than RF type transceiver.

However, the near-field electrostatic coupling scheme still has some drawbacks. Firstly, the surrounding environment, such as earth ground, plays an important role when the transceiver is in operation. The experiment reveals that body capacitance to the environment degrades the BCC communication quality. Since the electric potential, which the transmitter is trying to impose on the body, will be grounded by human body. Secondly, the use of narrowband transmission [16], [17], 400 kHz, the near-field electrostatic coupling scheme has limited data rate of 2.4 kb/s. The data rate of this approach for some of the basic biomedical applications may be sufficient. However, for the other advanced multimedia applications, such a low data rate is not sufficient.

2.2.2 Electromagnetic Wave Scheme

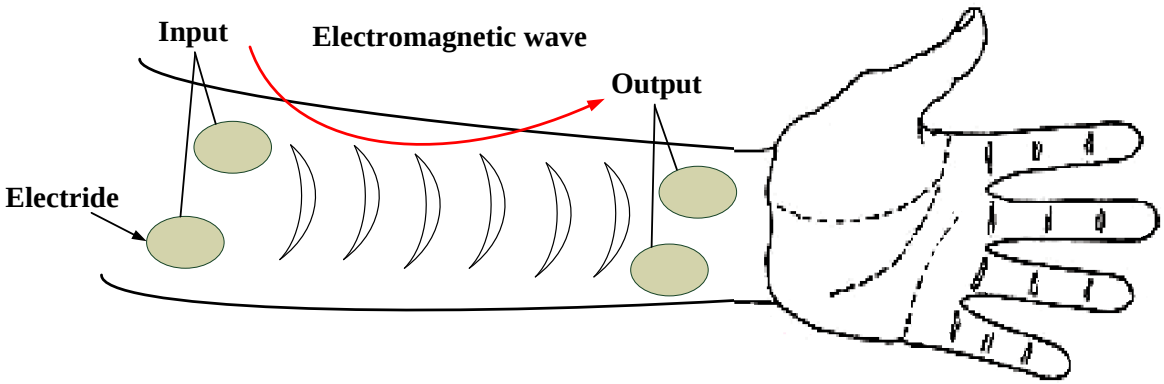


Fig. 2.4: Electromagnetic wave scheme.

Fig. 2.4 shows the concept of electromagnetic wave scheme [18]. The completely detailed analysis of intra-body communication is shown in [5]. Like the near-field electrostatic coupling scheme, the electromagnetic wave scheme also needs two pairs of electrodes to transfer data. In their experiments [5], two pairs of electrodes are attached to the upper arm and the wrist. The input signals are sin waves and the frequency range is form 1 MHz to 40 MHz (1 V peak-to-peak). The output signals are measured by oscilloscope.

The intra-body communication methods with signals transmitted by high-frequency carrier wave of 10 MHz also suffers from the bandwidth limitation in FM and FSK modulation. In addition, electromagnetic wave scheme is also vulnerable to external electromagnetic interferences.

2.2.3 Galvanic Coupling Scheme

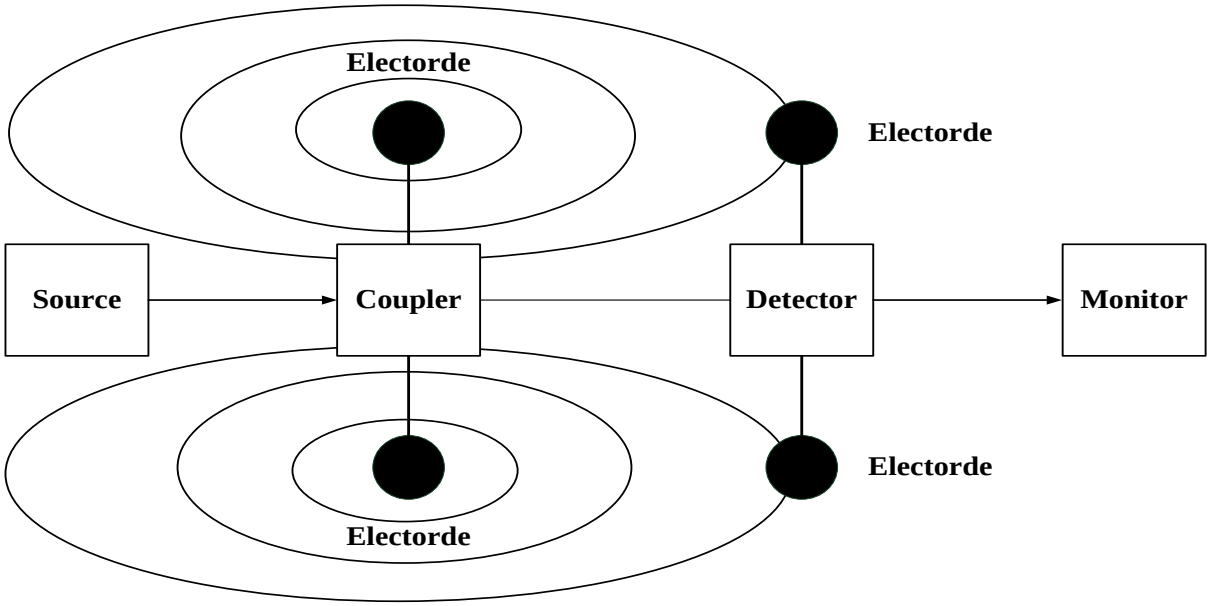


Fig. 2.5: Concept of galvanic coupling scheme.

Galvanic coupling was investigated by Oberle [19]. Fig. 2.5 shows the concept of galvanic coupling scheme [20], [21]. The signal transfer is established between transmitter coupler and receiver detector by coupling signal currents galvanically into the human body. The galvanic coupling scheme also needs two pairs of electrodes to transfer data. The transfer data is applied differential over two coupler electrodes and received the differential signal by the two detector electrodes. The galvanic coupling communication scheme has the frequency range from 10 kHz to 1 MHz and the applied current has amplitude of 1 mA.

Since galvanic coupling scheme uses the current to transmit signals, thus, safety requirements have to be fulfilled. Moreover, the coupler and detector are bulky and heavy, that is not convenient to use in long-term continuous monitoring applications.

2.2.4 Wideband Signaling with Direct-Coupled interface Scheme

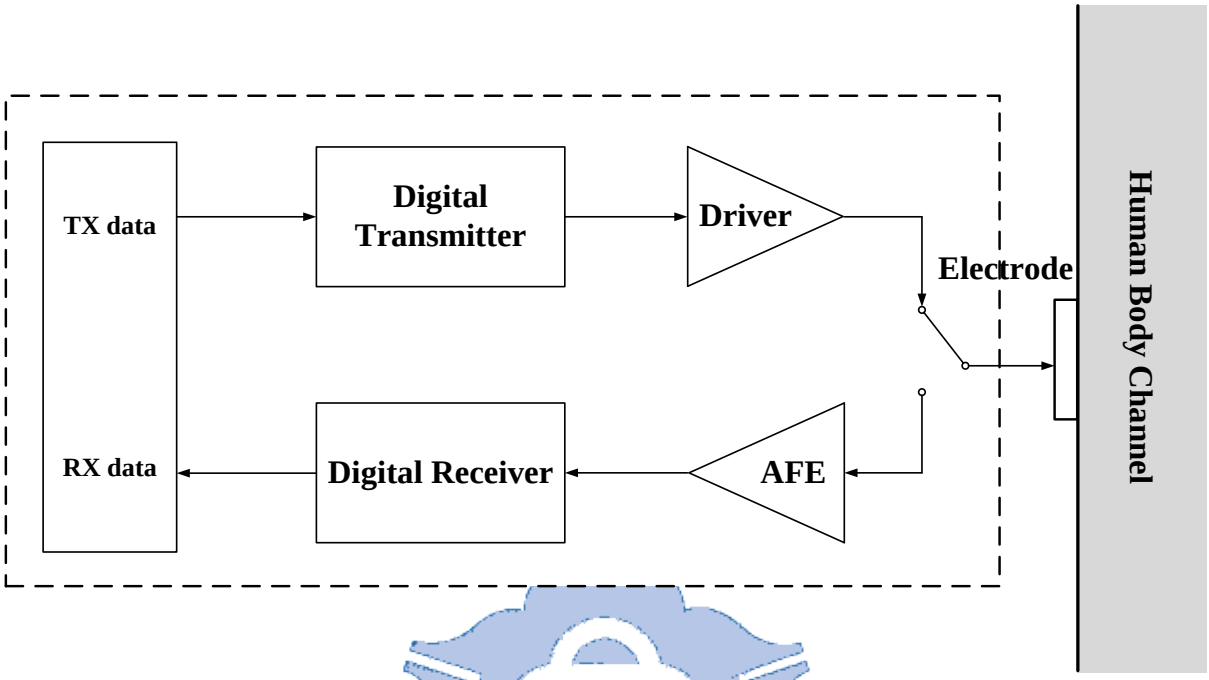


Fig. 2.6: Concept of human body communication with direct-coupled interface.

The wideband signaling (WBS) with direct-coupled interface (DCI) scheme is proposed by [22]. Fig. 2.6 shows the concept of the human body communication transceiver with a DCI. The transceiver is composed of a single electrode, a digital transmitter, a driver, an analog front-end (AFE) amplifier, and a digital receiver. The DCI is an interface scheme which connected to the silicon chip with the human body directly. Compared with other BCC transceiver, the WBS transceiver uses only a single electrode for data transmission without using any additional off-chip sensor to detect the weak electric field and the earth ground path. Thus, it can fully integrate all function blocks into a silicon chip and it can also reduce the physical size and achieve low cost.

The WBS transceiver uses a wide bandwidth to increase the data rate. The transmitter directly transmits binary digital signal through the electrode into the human body, and then recovers the corrupt binary data at the receiver. The WBS transmission scheme with DCI has some advantages. Firstly, the WBS transceiver uses only a single electrode for data transmission and that simplify the interface of communication. Secondly, the WBS scheme can provides higher data rate than other BAN schemes.

According to the investigation of human body channel [10], the body antenna effect will absorb external electromagnetic interferences into human body channel. Then, it causes enormous jitter performance to the receiver circuit and that will be a design challenge for the receiver circuit design.

2.2.5 Summary

Table 2.1 summarizes the prior body channel communication transceiver schemes. These schemes all have some advantages and disadvantages. In this thesis, we adopted the wideband signaling transceiver with direct-coupled interface to increase the data rate. Therefore, the application for the BAN can be greatly extended.

Table 2.1: Conventional BCC transceiver comparison.

BCC transceiver scheme	**Advantages**	**Disadvantages**
Near-Field Electrostatic Coupling [7]	Low power consumption than RF Small transceiver size than RF	Devices need to be grounded Vulnerability to interference Low data rate
Electromagnetic Wave [18]	Devices no need to be grounded	Vulnerability to interference Low data rate Bulky device
Galvanic Coupling [20]	Devices no need to be grounded	Vulnerability to interference Low data rate Bulky device
Wideband Signaling with Direct-Coupled Interface [22]	High data rate Sample interface Low power consumption Highly integration	Complexity of CDR circuit design

2.3 Conventional CDR Circuit Survey

2.3.1 PLL-based CDR Circuit

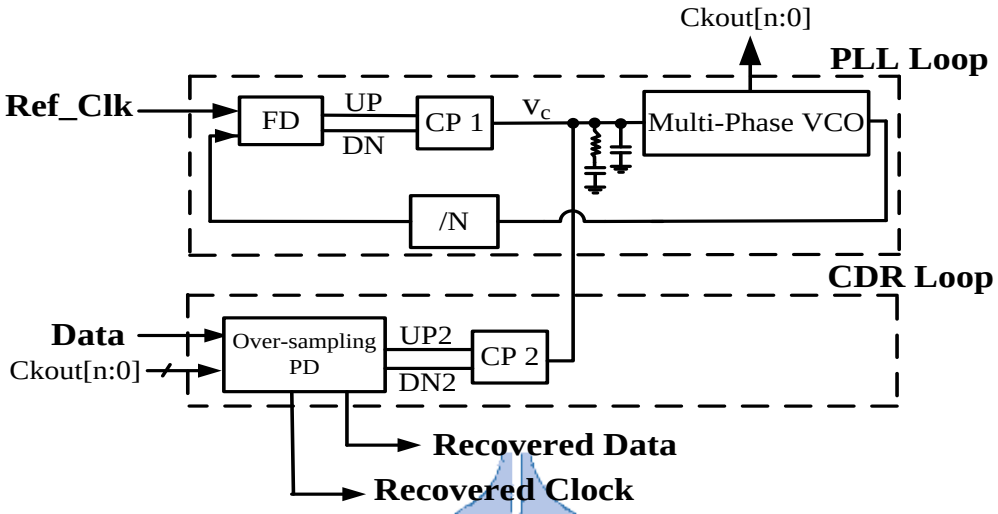


Fig. 2.7: Architecture of the PLL-based CDR circuit.

Fig. 2.7 shows an example of the PLL-based CDR circuit [23], [24]. This architecture is composed of a multi-phase PLL loop and a CDR loop. In the PLL loop, there is a multi-phase voltage control oscillator (VCO) uses an external reference clock to generate the reduced clock rate multi-phase signals, Ckout[n:0], which is usually a half or quarter rate than the data rate to reduce the power consumption of the VCO. The CDR loop uses these multi-phase clocks, Ckout[n:0], to trigger the oversampling PD and generates the up/down pulse to charge/discharge the charge pump to adjust the multi-phase VCO output clock frequency and then outputs recovered clock and data.

The advantage of this architecture is that the power consumption from VCO can be decreased due to the VCO clock rate is reduced to a half or quarter of the data rate. However, there are some disadvantages such as transistor leakage current problem in

advance CMOS process (< 90 nm) and design complexity will be increased because of multi-phase clock generation and the over-sampling circuit.

2.3.2 Continuous Rate CDR Circuit

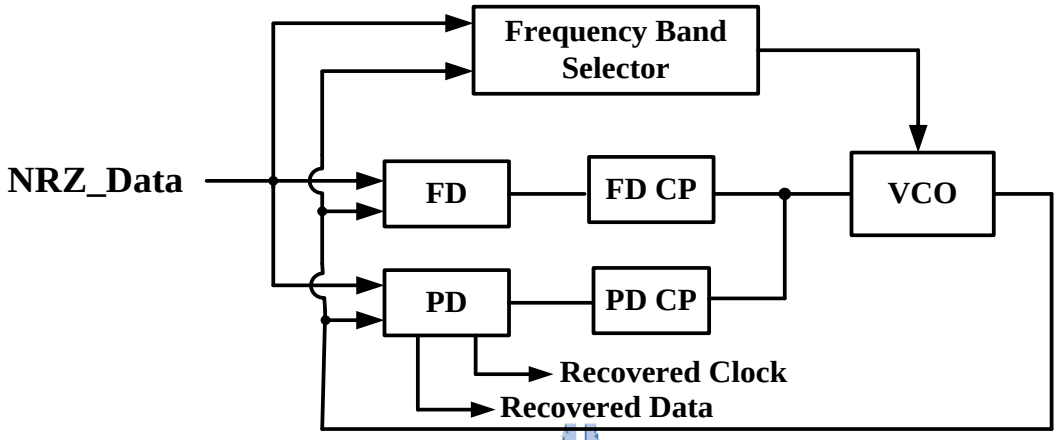


Fig. 2.8: Architecture of continuous rate CDR circuit

Fig. 2.8 shows the architecture of the continuous rate CDR circuit. It is widely used in CDR circuit which can continuous track the input data rate [25]-[27]. The continuous rate CDR circuit is composed of a frequency band selector, a frequency detector (FD), a phase detector (PD) and a VCO.

The frequency band selector selects the VCO frequency band which is close to the input data rate in order to speed up the frequency acquisition. Then, the FD compares the VCO clock and the input data rate to adjust the FD charge pump. Thus, the frequency of the VCO can quickly be converged to the data rate. The PD compares the phase information between the VCO phase and the input data transition phase. The information of lead or lag will control the PD charge pump to maintain the phase of the recovery clock.

2.3.3 Phase Interpolator Based CDR

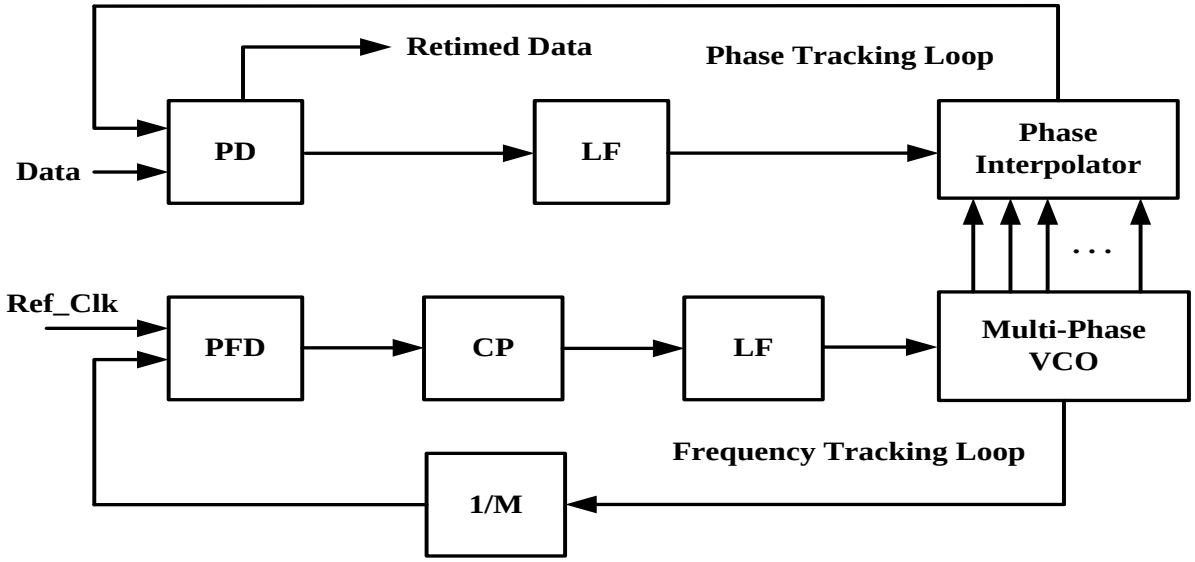


Fig. 2.9: Architecture of phase interpolator based CDR.

Fig. 2.9 shows the architecture of the phase interpolator based CDR. The phase interpolator based CDR is widely used in SATA applications [28], [29]. The phase interpolator based CDR usually has a frequency tracking loop and a phase tracking loop. In frequency tracking loop, it uses the reference clock, Ref_Clk, to generate the high speed multi-phase signals. Then, the high-speed multi-phase signals are used by the phase tracking loop.

The phase interpolator is driven by the loop filter, and it adjusts the phase by choosing multi-phase signals and performs interpolation. The phase interpolator based architecture is suitable for multichannel transmission because each channel can share these multi-phase signals.

However, the phase interpolator based CDR still needs an external reference clock to generate high speed multi-phase signals and that will increase the complexity of the design.

2.3.4 Blind Oversampling Type CDR

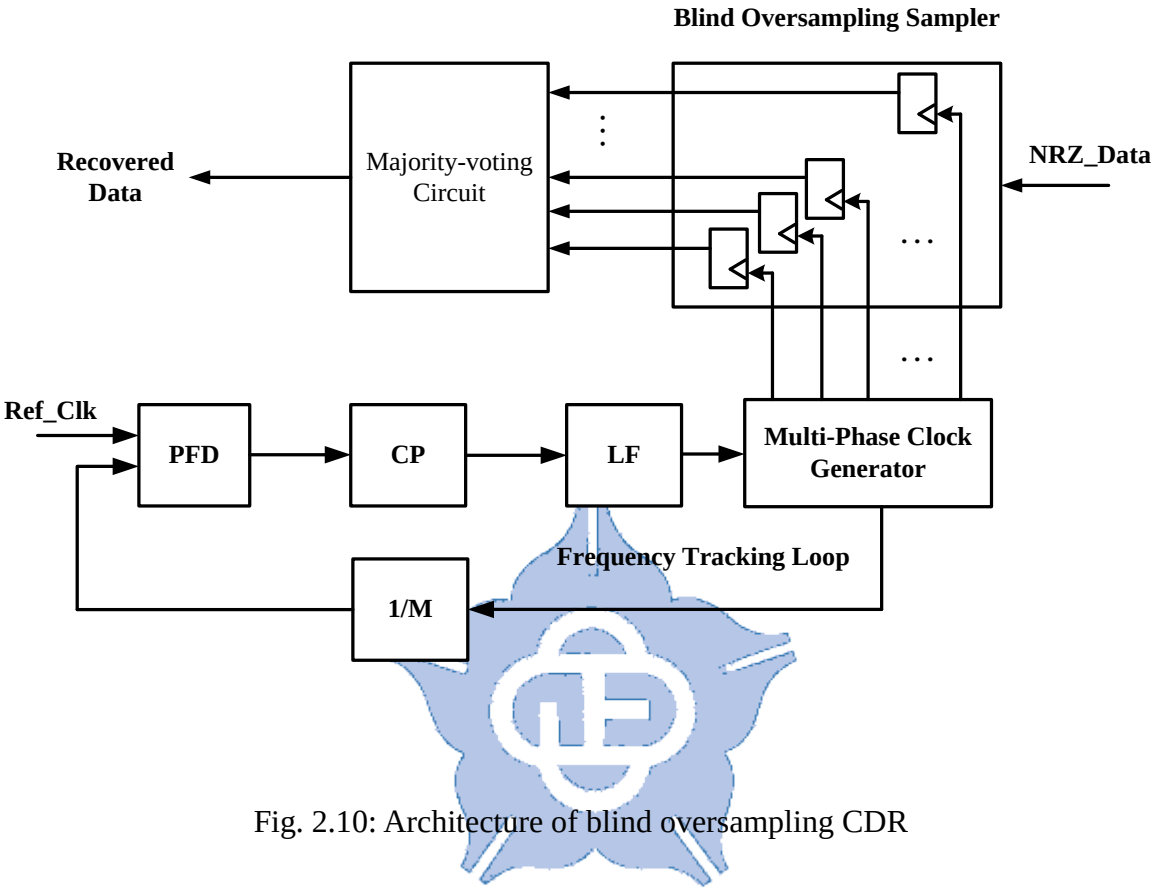


Fig. 2.10: Architecture of blind oversampling CDR

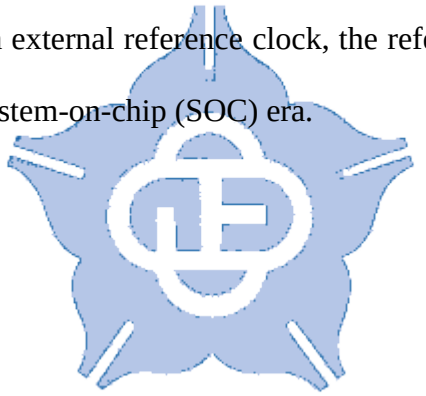
Fig. 2.10 shows the block diagram of the blind oversampling circuit [30]-[32]. This architecture is composed of a frequency tracking loop to generate multi-phase clocks, a blind oversampling sampler, and a majority-voting circuit. The frequency tracking loop uses the external reference clock, Ref_clk, to generate the multi-phase clocks. The multi-phase clocks trigger the blind oversampling sampler to sample the input data, NRZ_Data. Then, these sampled data are sent to decision circuit, majority-voting circuit, to decide the right data to be recovered.

The blind oversampling architecture has no feedback loop to track the phase and has fast acquisition ability, but it still needs an external reference clock and multi-phase clock generator which will cause extra power consumption.

The multi-phase clock sample rate usually is 2X, 3X or 4X higher than the data rate. Basically, the higher sampling clock rate can achieve better bit error rate (BER) performance. However, the higher sampling clock rate also results in higher power consumption. Thus, it requires to trade off the BER performance with power consumption.

2.3.5 Referenceless Issue of CDR Circuit

An external reference clock is often required in a phase-locked loop (PLL). Therefore, many PLL based CDR circuits need an external reference clock to generate multi-phase clocks. However, the external reference clock is often provided by extra crystal oscillator. The extra crystal oscillator not only has high cost, but also has high power consumption. To overcome the problem with an external reference clock, the referenceless CDR architecture is more attractive in today's system-on-chip (SOC) era.



2.3.6 Summary

Table 2.2: CDR architecture comparison.

CDR Architecture	Advantages	Disadvantages
PLL-based [23]	Ability of input frequency tracking Input jitter rejection	Long lock-in time Large loop filter area External reference clock needed Multiphase clocks needed
Continuous rate [25]	Ability of input frequency tracking Input jitter rejection No need external frequency	Long lock-in time Complexity of frequency band selector
Phase interpolator [28]	Multichannel can share input clock	External Reference clock needed Multiphase clocks needed
Blind oversampling [30]	Fast lock-in Fast acquisition	External Reference clock needed Multiphase clocks needed Large FIFO size

Table 2.2 summarizes conventional CDR architectures. They all have some disadvantages such as long-lock time, external reference clock needed, multi-phase clocks needed and high hardware design complexity.

In order to tolerate large jitter effects, we propose an all-digital 5X blind oversampling CDR circuit with fast lock-in time, no multi-phase clock generator needed. We adopted the center-picking method instead of majority voting to recover data. The center-picking method is always chooses the middle of the data points as recover data. Besides, we also propose an add-drop FIFO algorithm to achieve high jitter tolerance. As a result, we can

easily recover the transmission data which is suffered from serious attenuation by the human body channel.

Chapter 3

The Proposed Wideband Signaling Transceiver

3.1 The Proposed Wideband Signaling Transceiver Overview

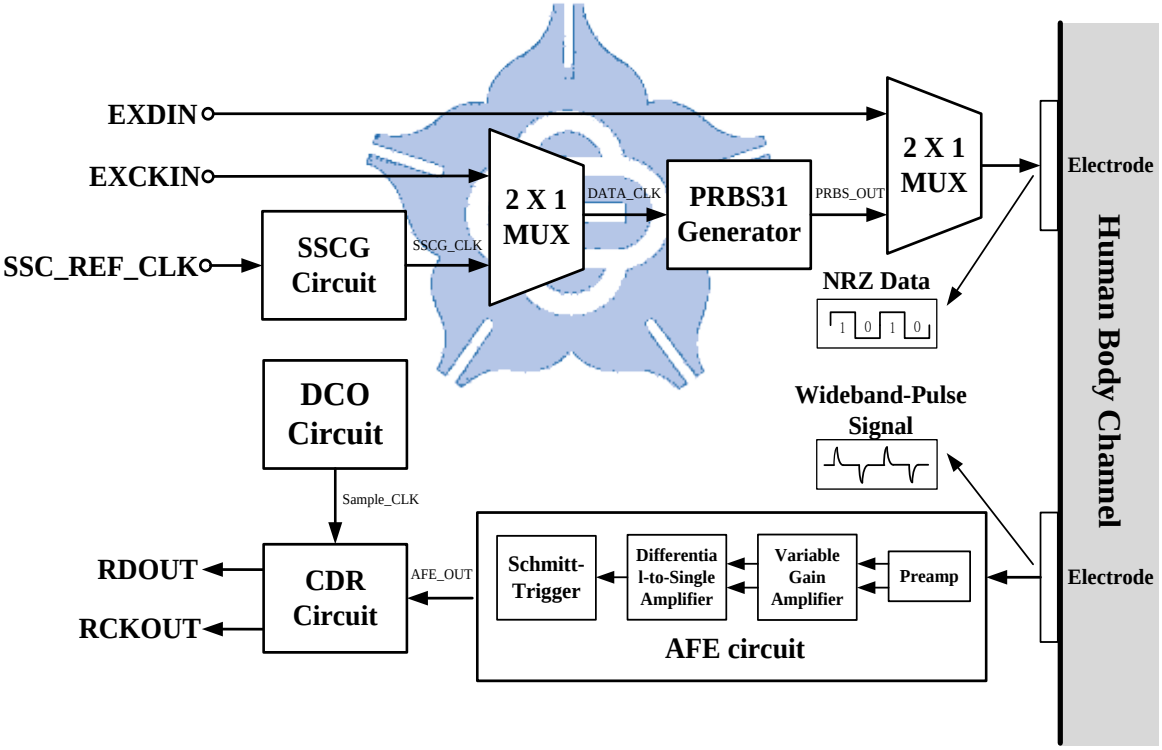


Fig. 3.1: Proposed wideband signaling transceiver architecture.

Fig. 3.1 shows the block diagram of the proposed wideband signaling (WBS) transceiver. The proposed WBS transceiver is composed of a spread spectrum clock generator (SSCG) based transmitter, an analog front-end (AFE) circuit, and a 5X blind oversampling clock and data (CDR) circuit. The proposed SSCG-based transmitter directly transmits digital binary data to the human body channel. Then the wideband pulse signal is amplified by the analog front-end circuit and recovered by the oversampling receiver circuit.

There are three advantages of WBS scheme: simple interface, the capability of high data rate and low power consumption. The WBS transceiver is connected to the human body skin with a single metal electrode. Since there is no ground electrode to establish return path, thus, there is only the parasitic ground exists to provide the return path. In addition, since the WBS scheme is independent of the surrounding environment, the data transmission is slightly impacted by the condition of the surrounding environment, such as earth ground. However, the body antenna effect still causes a great impact to the human body channel communication.

According to the investigation of human body channel, binary digital data show the characteristics of attenuation in different transmission distance and frequency. Comparing with other body channel communication schemes [33]-[36], adopting NRZ binary data to transmission not only reduces the complexity of the transceiver design but also reduce the power consumption.

3.2 Spread Spectrum Clock Generator based Transceiver

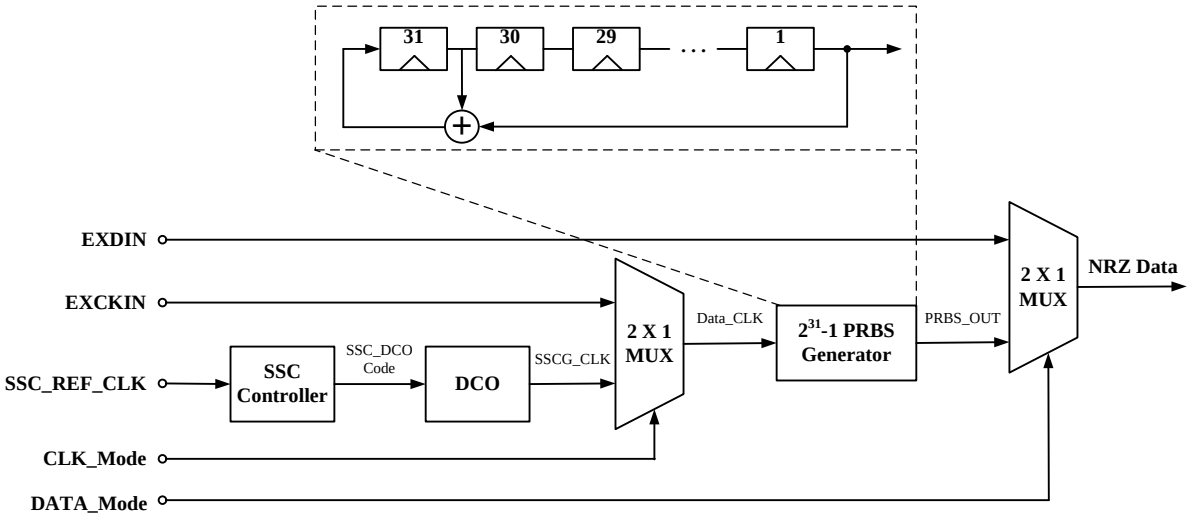


Fig. 3.2: Block diagram of SSCG-based WBS transmitter.

Fig. 3.2 shows the block diagram of the proposed SSCG-based transmitter. The SSCG-based transmitter is composed of a spread spectrum clock (SSC) controller, a digital control oscillator (DCO), two 2-to-1 multiplexers (MUXs), and a pseudo-random binary sequence (PRBS) generator. The SSCG-based transmitter can directly transmit digital binary data to the human body by exploiting WBS scheme.

The transmission clock is generated by the DCO, which is controlled by the SSC controller to generate a spread-spectrum clock, or by an external clock input (EXCKIN). The spreading ratio of SSCG determines the amount of EMI reduction. In conventional SSCG, the spreading ratio is chosen to be smaller than 5000ppm [37] and the modulation frequency is chosen as 30~33 kHz. However, if the spreading ratio can as high as 10%, there will be more EMI reduction. In the proposed SSCG-based transmitter, because the capability of the 5X blind oversampling CDR, the maximum spreading ratio (α) can be up

to 10%. Thus, we set the spreading ratio (α) to 10%, and the center-spread modulation frequency is 30 kHz. The SSCG clock output frequency ranges from 38 MHz to 42 MHz for the high speed mode and ranges from 0.9 MHz to 1.1 MHz for the low speed mode.

Fig. 3.3 shows the simulation of power spectrum density of the SSCG_CLK at 40MHz. Before spread spectrum operation, the peak power of the 40 MHz is -44.29 dB. After spread spectrum operation, the peak power can be reduced to -62.21 dB. Thus, the EMI reduction is 22.08dB.

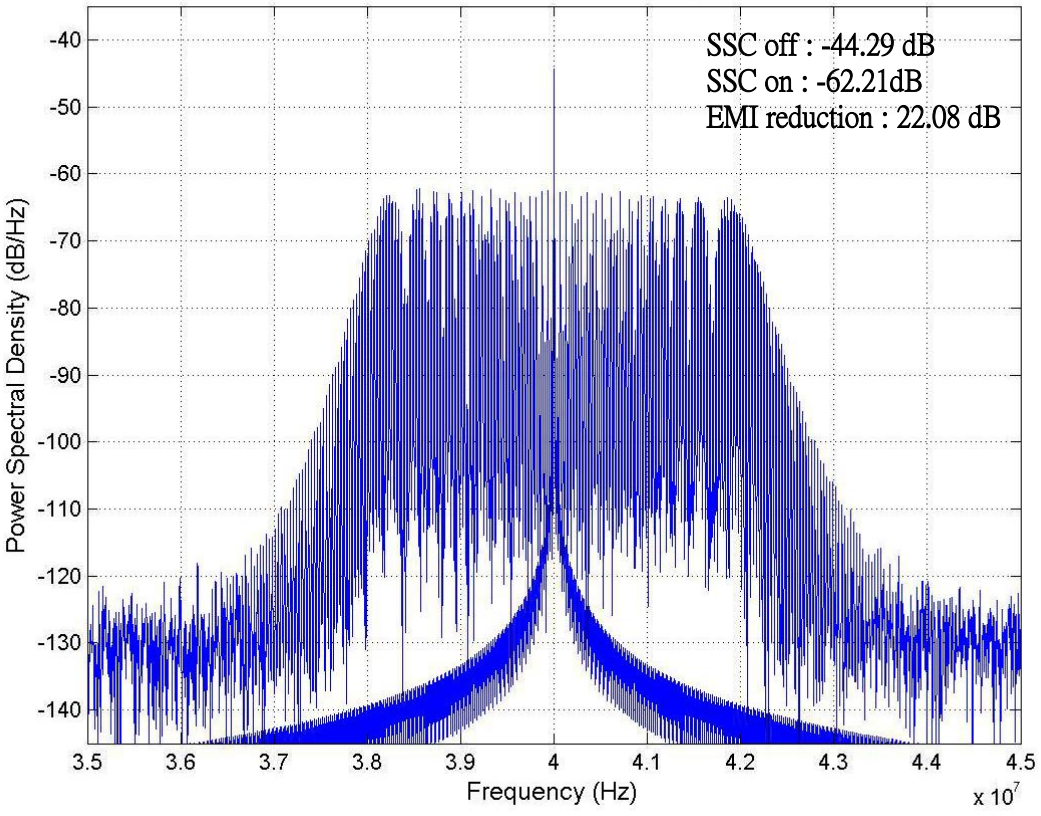


Fig. 3.3: Simulated power spectrum density at 40MHz with 10% spreading ratio.

Linear feedback shift register (LFSR) is a critical portion of any digital system that relies on a PRBS generator, with applications ranging from cryptography and bit-error-rate measurements, to wireless communication systems employing spread spectrum or CDMA techniques. The PRBS generator is activated by SSCG_CLK or EXCKIN to generate 2^{31}-1 PRBS data. The PRBS generator as a binary data source is based on polynomial of $x^{31} + x^{30} + 1$ to generate random data. After the PRBS generator generates the binary data, the data is transfer to a 2-to-1 MUX and the MUX will select one of these two kinds of data, an external data input (EXDIN) or a PRBS_OUT, as the output NRZ data. Then, the NRZ data are transmitted to the human body channel through the TX electrode.

3.3 Wideband Signaling Receiver

3.3.1 Analog Front-End Circuit

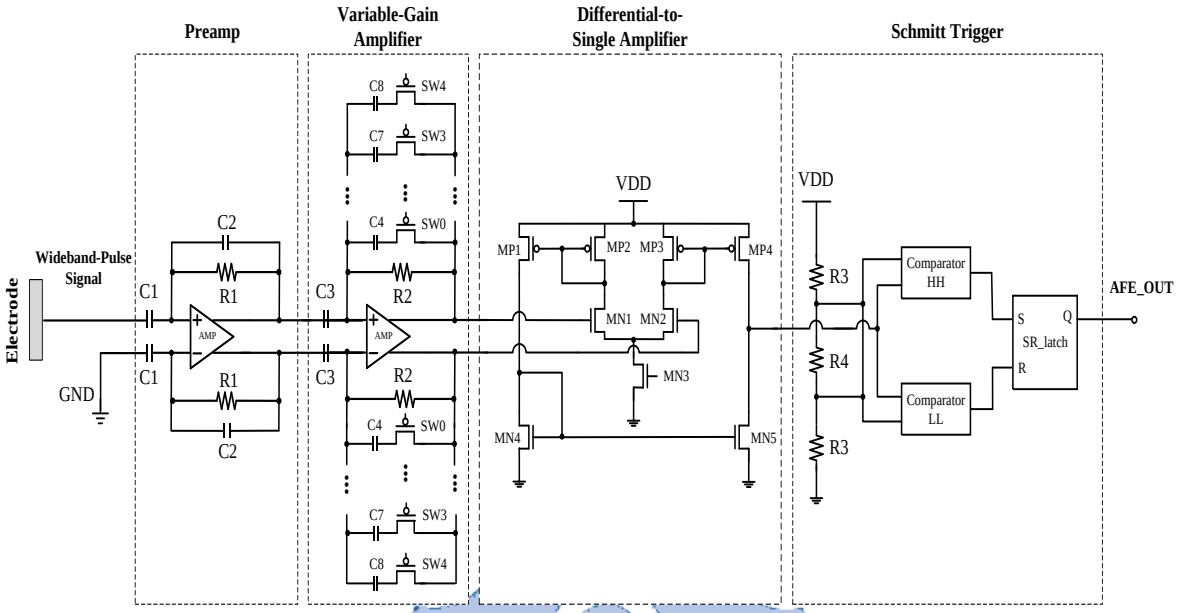


Fig. 3.4: Architecture of the analog frontend circuit.

Fig. 3.4 shows the architecture of the analog front-end (AFE) circuit. The frequency range of the input wideband-pulse signal starts from 1 MHz to 40MHz. In order to achieve the specifications to enlarge the signal with the amplitude of 50mV to 125mV and filter out the noise about 15mV to 25mV at the same time, the proposed analog frontend circuit is composed of a pre-amplifier, a variable gain amplifier (VGA), a differential-to-single amplifier and a Schmitt trigger.

A DC-blocking capacitor is used to reduce the DC offset from electrodes. Furthermore, the amplitude of the signal is 50mV to 125mV. In order to accomplish adjustable magnification, the VGA is implemented in a standard performance 90nm CMOS process with a 1.0V power supply. In the proposed architecture, the VGA achieves a gain tuning

range from 5dB to 28dB and a bandwidth of 100MHz. In this work, different switch pairs, EN0-EN4, with capacitor load, C4-C8, are selected for the variable-gain stage by changing the ratio of capacitors. In addition, a capacitor C3 is added to suppress the high frequency interference. The poles of the VGA are

$$f_{p1} = \frac{1}{2\pi (R_2 C_3)}$$

$$f_{p2} = \frac{1}{2\pi (R_2 C_3 + R_2 C_4 + \ldots)}$$

Because the transmission distance of the body channel ranges from 10 cm to 120 cm, the peak value of the received signal decreases as the transmission distance increases. Thus, we need a VGA to amplify the different magnitude of the received signals. Fig. 3.5 shows the VGA's control bit versus gain amplitude. The output gain amplitude ranges from 5 dBm to 28 dBm with the different control bits, and the output gain is sufficient for BCC application.

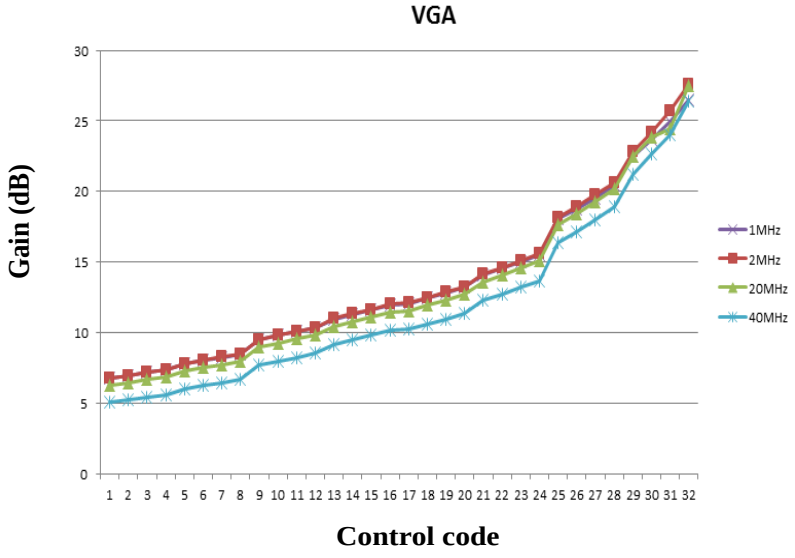


Fig. 3.5: VGA amplified gain

The differential-to-single amplifier converts differential input signals to a single-end output. The Schmitt trigger is composed of two comparators and a SR latch. The comparator is a device that compares two voltages or currents and switches its output to indicate which one is larger. They are commonly used in devices such as analog-to-digital converters (ADCs). By means of the characteristics, we can enlarge the signal to the high electric potential “1” or degrade it to the low electric potential “0” by adjusting appropriate magnification. Finally the SR latch maintains the level at the previous potential until the next state charge. The AFE circuit can provide maximum 38dB magnification, and the power consumption is only 1.35mW.

Fig. 3.6 shows the simulation result of the AFE circuit. The input data are generated by simple RC model with interferences. The input data rate is 1 Mb/s and the amplitude is about 100 mV. After amplification by AFE circuit, the attenuated signal can be amplified to 1 V and passed to the CDR circuit.

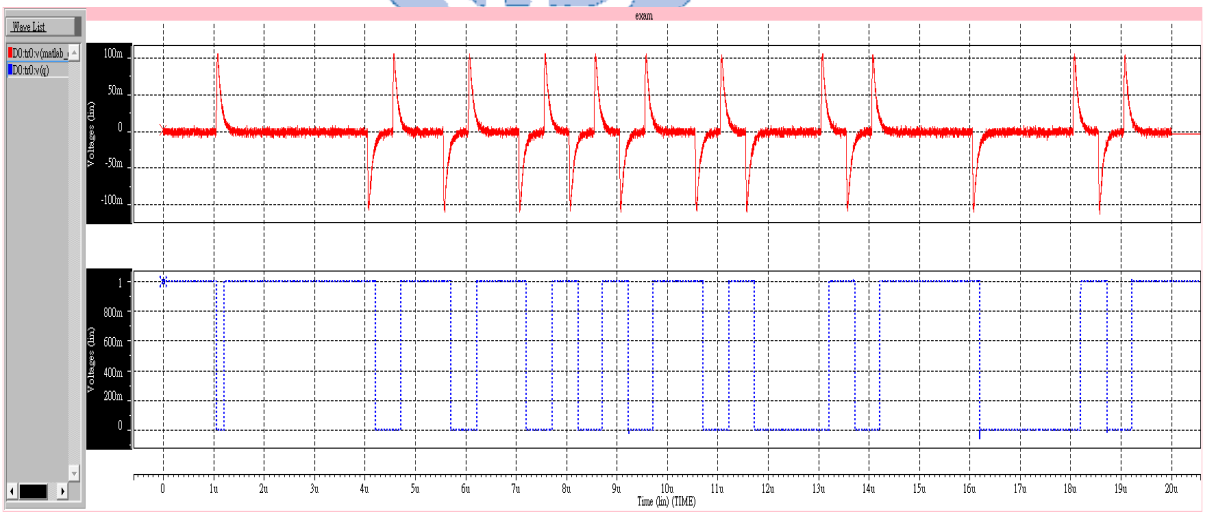


Fig. 3.6 Simulation result of AFE circuit.

3.3.2 5X Blind Oversampling CDR

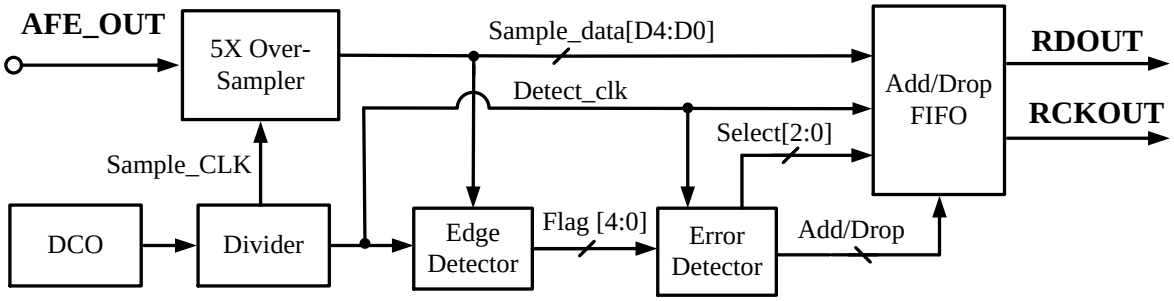


Fig. 3.7: Block diagram of the proposed 5X oversampling CDR circuit.

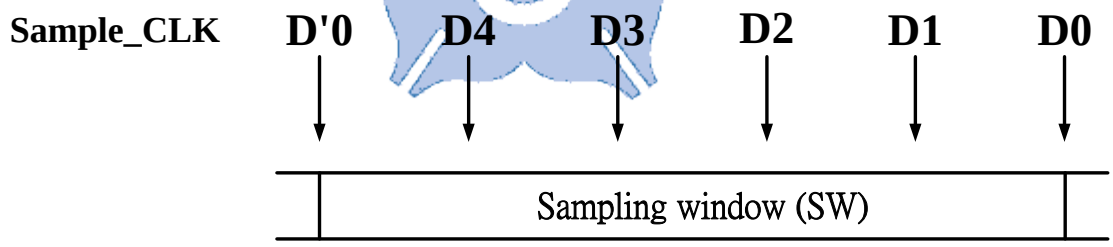
Fig. 3.7 shows the block diagram of the proposed 5X blind oversampling CDR circuit. The CDR circuit is consisted of a 5X over-sampler, a monotonic low-power DCO, a divider, an edge detector, an error detector, and an add-drop FIFO. The main reference of add-drop method is [31] and we have improved this method.

When the AFE_OUT data, which is amplified by analog front-end circuit, transfers into the CDR, the 5X over-sampler uses the sampling clock (Sample_CLK), the sampling clock rate is 200 MHz and provides by the DCO, to sample five points in one symbol period. Then, these sampled data (D4 to D0) are sends to the edge detector and the add-drop FIFO. The edge detector finds the data transition by exclusive-or the two adjacent sampling data and adopts the center-picking method to determine the middle of sampling phase and output 5-bit data transition information (Flag) to the error detector. The error detector uses the 5-bit flag information to generate the 3-bit Select signal and it also compares the current and previous values of the 5-bit flag information to generate the Add/Drop signals to the add-drop FIFO. The add-drop FIFO determines which sampled data output as recover data (RDOUT) by Add/Drop and 3-bit Select signals.

The DCO is a ring type DCO constructed by a coarse-tuning delay line and fine-tuning delay line to provide the sampling clock and it can be controlled by external control pins to adjust the frequency.

3.3.2.1 Center-Picking Method

Fig. 3.8 shows the center picking method within a single sampling window. This method is used by the edge detector to determine the phase information from the 5-bit sampled data (D4 to D0). These 5-bit sampled data which sampled by 5X over-sampler are sent to the edge detector. The center-picking method using the current 5-bit sampled data and previous 1-bit sampled data (D'0) to select the middle of the data. The sampling window (SW) is defined to be a time interval starting from one rising edge of D0 to the next rising edge of D0. According to the sampled data, there are five cases of input transition position (Case 1 to Case 5) within a sampling window.



	Case 1	Case 2	Case 3	Case 4	Case 5
Input transition position	**D'0-D4**	**D4-D3**	**D3-D2**	**D2-D1**	**D1-D0**
Selected sampled data	**D2**	**D1**	**D0**	**D4**	**D3**

Fig. 3.8: Center picking method.

For example, in Fig. 3.9 (a), data transitions are located D4 of SW2 and D4 of SW3. Thus, in sample window SW2 and SW3, the sampled data D2 will be selected to save to the

add-drop FIFO. Similarly, in Fig. 3.9 (b), data transitions are located at D3 of SW2 and D3 of SW3. Thus, in sample window SW2 and SW3, the sampled data D1 will be selected to save to the add-drop FIFO. Besides, if there is no any data transition within a sampling window, which indicates that the 5-bit sampled data are '00000' or '11111', it will maintains the previous sampling data position.

At every sampling window, the center point of the input data (data eye point) is always selected as sampled data, thus, this scheme is called center picking method within a single sampling window.

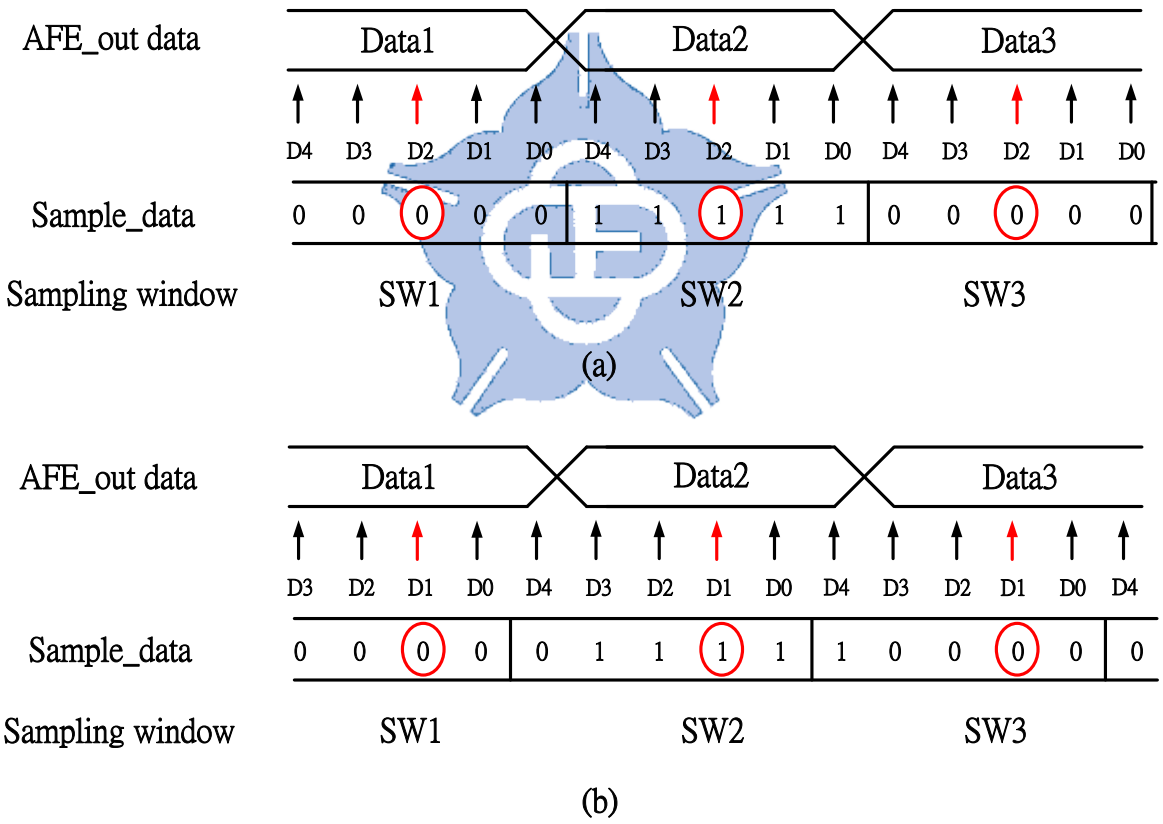


Fig. 3.9: Example of center picking method. (a) Case 1. (b) Case 2.

3.3.2.2 Add-Drop FIFO Algorithm

Due to the human body antenna effects [10], interferences in the environment, such as cordless phones, frequency modulation (FM) radios, and walkie-talkies, may cause enormous jitter to the received data. For long time data transmission, it may cause frequency offset between the transmitter and the receiver. Therefore, it causes symbol boundary variations. Then the CDR circuit may miss one bit or duplicate one bit, as illustrated in Figs. 3.10(a) and 3.10(b). For example, in Fig. 3.10(a), the data transition is located D1 of SW2, thus, in sample window SW2, the sampled data D4 will be selected. However, due to the effect of interferences, the data transition is move forward, thus, the data transition is located D2 of SW3 and sampled data D0 will be selected. Consequently, the Date2 isn't to be sampled and it causes the missing data case. In Fig. 3.10(b), the data transition is located D2 of SW2, in sample window SW2, the sampled data D0 will be selected. However, due to the effect of interferences, the data transition is move backward, thus, the data transition is located at D1 of SW3 and sampled data D4 will be selected. Consequently, the Data2 is sampled two times and cause duplicate data case.

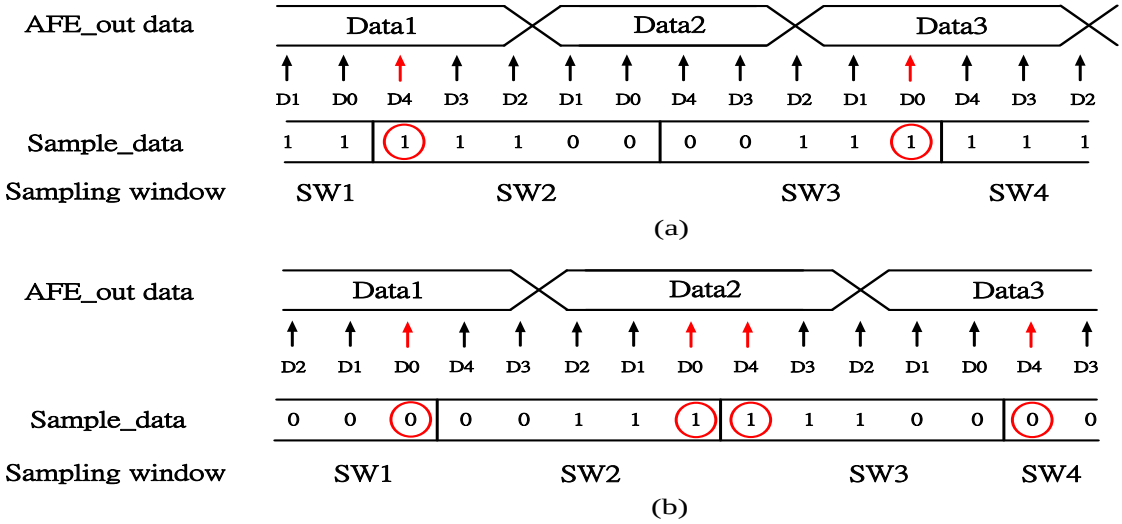


Fig. 3.10: (a) Missing data case. (b) Duplicated data case.

The Add/Drop signals are generated by the error detector. If the selected sample_data is changed from D4 to D0, as shown in Fig. 3.10(a), the “Add” signal will be activated. Oppositely, if the selected sampled data is changed from D0 to D4, the “Drop” signal will be activated. The error detector generates the Add/Drop and the Select signals to add-drop FIFO. The add-drop FIFO determines which 5-bit sampled data will be selected as the recovery data according to the Add/Drop and the Select signals.

Fig. 3.11 shows the operation of the proposed add-drop FIFO. In this figure, we take a 7-bit add-drop FIFO as an example. The add-drop FIFO operates the basic function of FIFO, however, it can add or drop a bit data from the FIFO queue. In each sampling window, the add-drop FIFO will shift to left by one bit, and save the current selected sampled data to the least significant bit. Then it outputs the data as pointed by the “Index” register. In addition, in the beginning, the “Index” register is pointed to the middle of the add-drop FIFO. If “Add” signal is activated, the missing data will be added to the add-drop FIFO, and the value of “Index” register is added by one. Oppositely, if “Drop” signal is activated, the add-drop FIFO stalls one cycle to drop the duplicated data, and the value of “Index” register is subtracted by one.

For example, in Fig. 3.11(a), data transition are located D1 from SW1 to SW5, thus, the sampled data D4 will be selected to save to the add-drop FIFO’s least significant bit. At SW6, the data transition is moved forward to D2, thus, sampled data D0 will be selected and the original sampled data D4 is missing. At the same time, the add signal is activated by the error detector and the add-drop FIFO will obtain the missing data from the 5-bit Sample_Data.

In Fig. 3.11(b), data transition are located at D2 from SW1 to SW5, thus, the sampled data D0 will be selected to save to the add-drop FIFO’s least significant bit. At SW6, the data transition is move backward to D1, and thus, sampled data D4 will be selected and the

original sampled data D0 is duplicated. At the same time, the drop signal is activated by error detector and the add-drop FIFO will discard the duplicated data by stalling the FIFO.

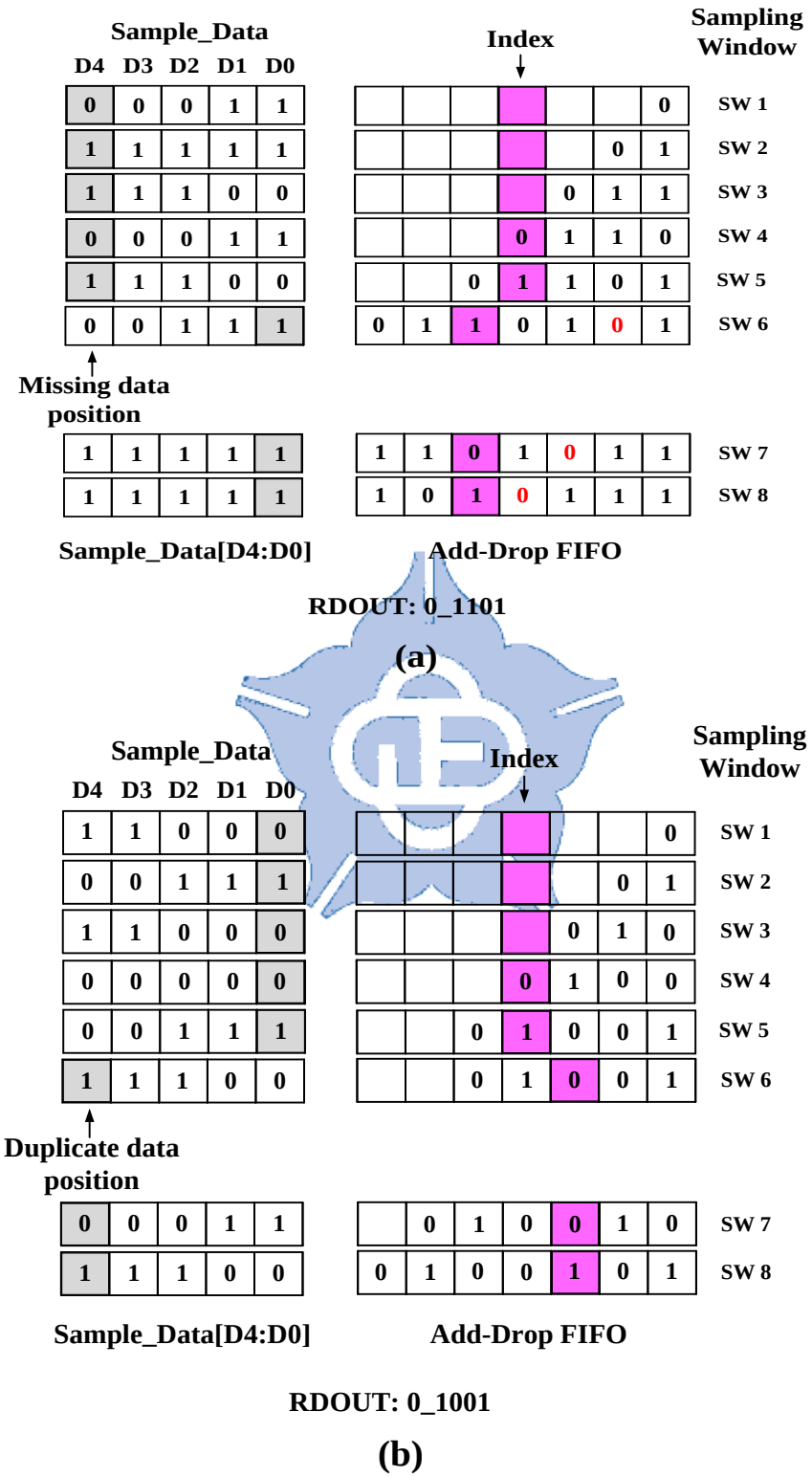


Fig. 3.11: (a) Algorithm of add operation. (b) Algorithm of drop operation.

Comparing with the traditional PLL-based CDR [38], the proposed 5X blind oversampling CDR have some advantages. Firstly, the PLL-based CDR requires constant to track the current transmission frequency depending on the input data. If the transmission environment has larger noise interference, the transmission data will cause large jitter in a short period. The PLL-based CDR needs extra clock cycles to relock the transmission frequency and that will cause poor BER.

On the contrary, there is no need for the proposed 5X blind oversampling CDR to track the transmission frequency. The jitter phenomenon causes the missing or duplicated data will recover by the Add-Drop FIFO. Therefore, this method can achieve better BER.

3.3.2.3 Digital Control Oscillator

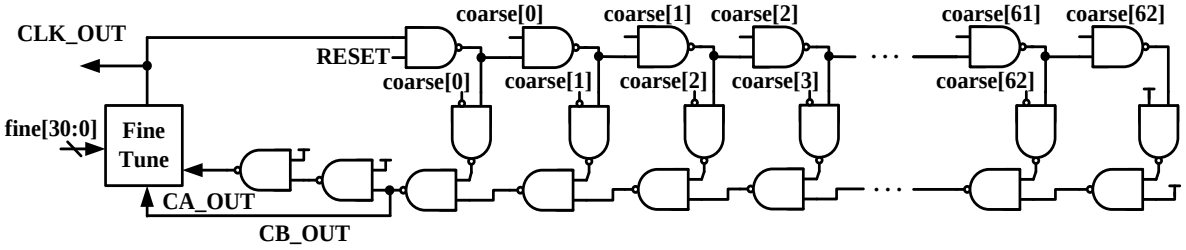


Fig. 3.12: Coarse tuning stage of DCO.

As shown in Fig. 3.12, the ring type DCO architecture is constructed by a coarse-tuning delay line and the fine-tuning delay line [39]. The coarse-tuning delay line is composed with 64 coarse-delay cells (CDC). The CDC is composed with three NAND-gates, and controlled by the coarse-tuning code to disabled redundant power consumption. The coarse code is used to select the delay path to control the DCO output clock. Besides, in order to enhance the resolution of DCO, there are two signals CA_OUT and CB_OUT are fed into the fine-tuning circuit to perform interpolation.

Fig. 3.13 shows the fine-tuning stage architecture. This fine-tuning circuit is designed with interpolating scheme [40]. The fine-tuning circuit is composed of two parallel tri-state buffer arrays, and sets different states to interpolate an appropriate output clock phase. The fine-tuning circuit divides one coarse-tuning delay time into 32 parts and controlled by the fine-tuning code. Because the delay difference of CA_OUT and CB_OUT is equal to one CDC delay time, when we turn on more tri-state buffers in the left hand side array, the output clock (CLK_OUT) is more closed to CA_OUT. Oppositely, if we turn on more tri-state buffers in the right hand size array, the output clock is more closed to CB_OUT.

This architecture of the fine-tuning circuit can provide high resolution sampling clock to the sampler, the more accurate sample clock can reduce the frequency drift problem between the transmitter and the receiver.

Fig. 3.14 shows the simulation result of the DCO control code versus period with PVT variations, and the range and step of each stage is shown in Table 3.1.

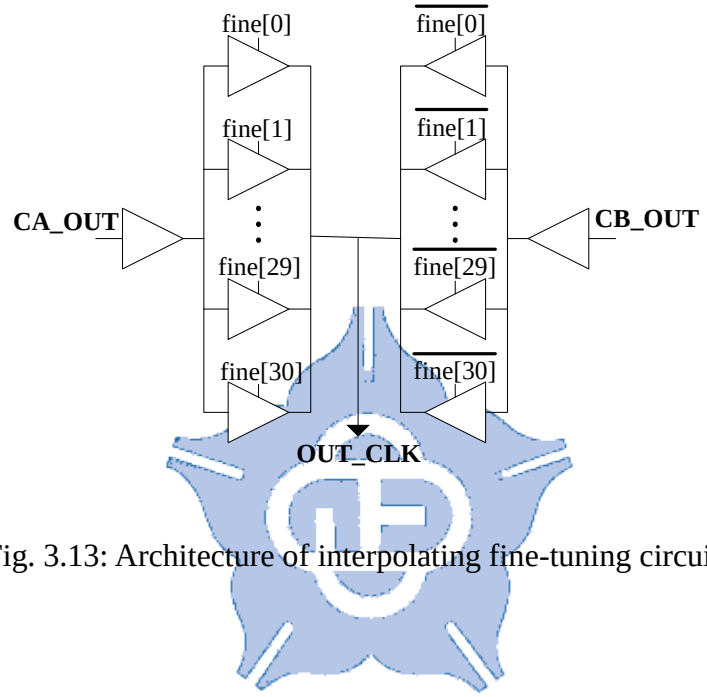


Fig. 3.13: Architecture of interpolating fine-tuning circuit.

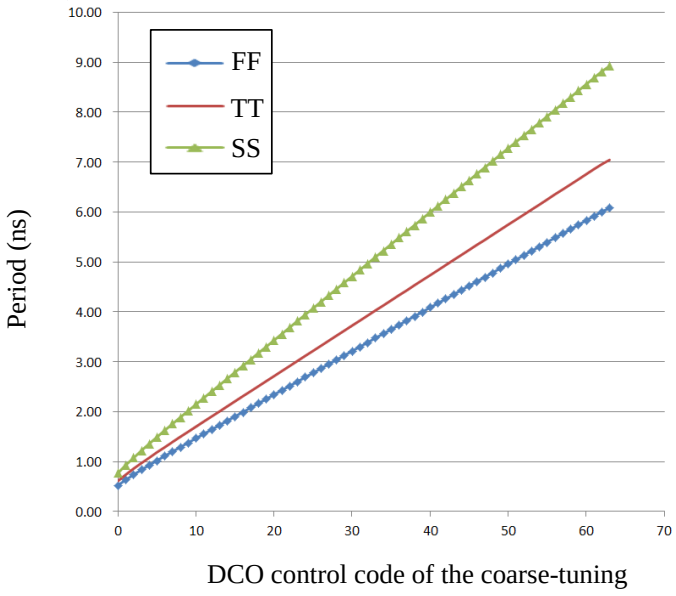


Fig. 3.14: DCO delay line simulation with PVT variations.

Table 3.1: Coarse/Fine step in PVT variations

PVT corner	Slow Case	Typical Case	Fast Case
	Step	Step	Step
Coarse tune stage	129.4 ps	102 ps	88.1 ps
Fine tune stage	4.04 ps	3.18 ps	2.75 ps
Output frequency	77MHz~1300MHz	141MHz~1632MHz	164MHz~1903MHz

Chapter 4

Experimental Results

4.1 Test Chip Implementation

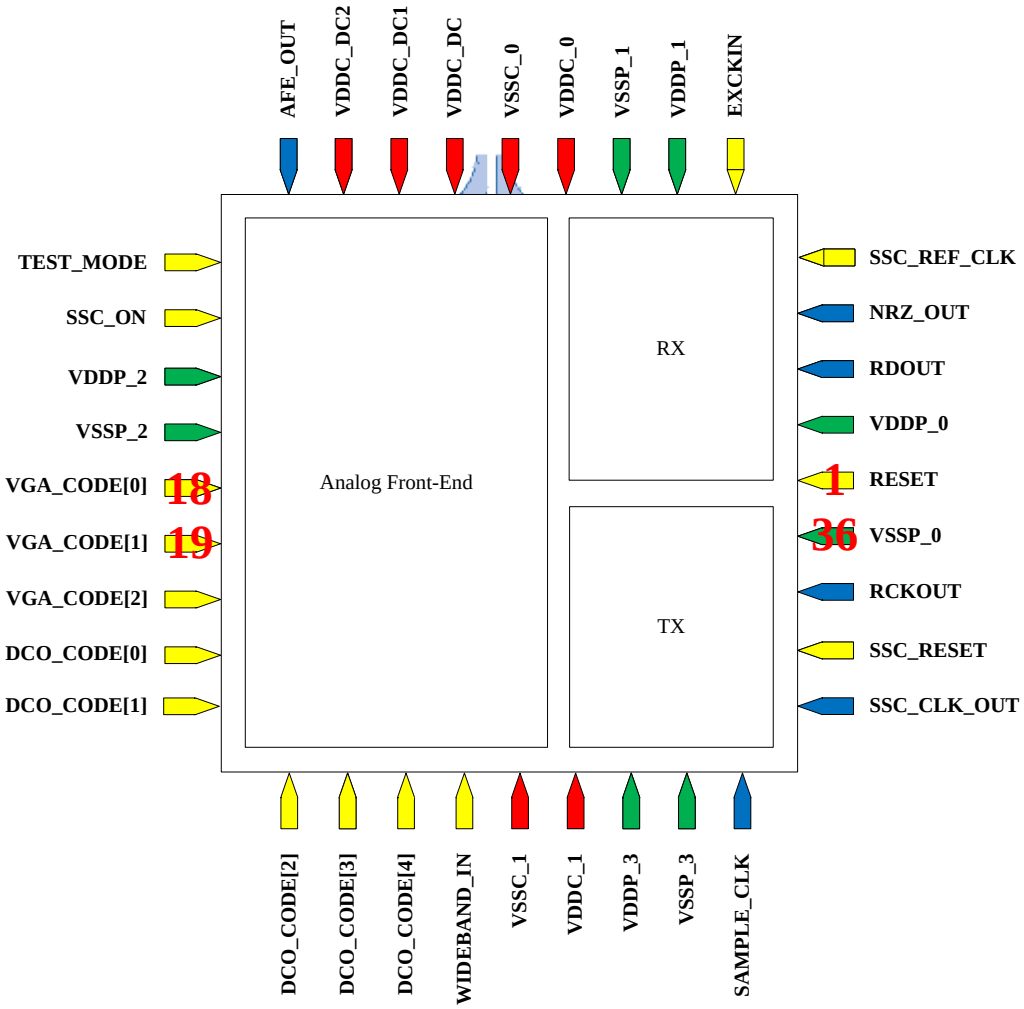


Fig. 4.1: Test chip floor planning and I/O planning.

Fig. 4.1 shows the proposed wideband signaling transceiver's floor planning and I/O planning. There are 21 I/O PADs and 15 power PADs. The detail I/O description is shown in Table 4.1. The test chip is composed of the proposed WBS transmitter, the WBS analog front-end circuit and the WBS receiver. The WBS transmitter is composed of a on-chip spread spectrum clock generator (SSCG) and pseudo-random binary sequence (PRBS) generator. The SSCG generates spread spectrum clock which has the range of 1 MHz to 40 MHz to trigger the PRBS generator. The PRBS generator generates the data pattern and adopts the linear feedback shift register (LFSR) for random bits generation.

Table 4.1 I/O PADs description

Output	Bit	Function
SSC_CLK_OUT	1	SSCG clock
NRZ_OUT	1	Random data pattern
AFE_OUT	1	Signals amplified by analog front-end
SAMPLE_CLK	1	5X sample clock
RDOUT	1	CDR circuit recovery data
RCKOUT	1	CDR circuit recovery clock
Input	**Bit**	**Function**
RESET	1	System reset
SSC_RESET	1	SSCG reset
SSC_ON	1	SSCG on
EXCKIN	1	External input data clock
SSC_REF_CLK	1	SSCG reference clock

TEST_MODE	1	0	TX data to CDR
		1	AFE_out to CDR
WIDEBAND_IN	1	Human body channel input data (Analog input pin)	
VGA_CODE	3	Variable gain amplifier ratio	
DCO_CODE	5	DCO control code	
Analog Power Pins			
VDC	Analog power pins 0.4V		
VDC1	Analog power pins 0.5V		
VDC2	Analog power pins 0.6V		

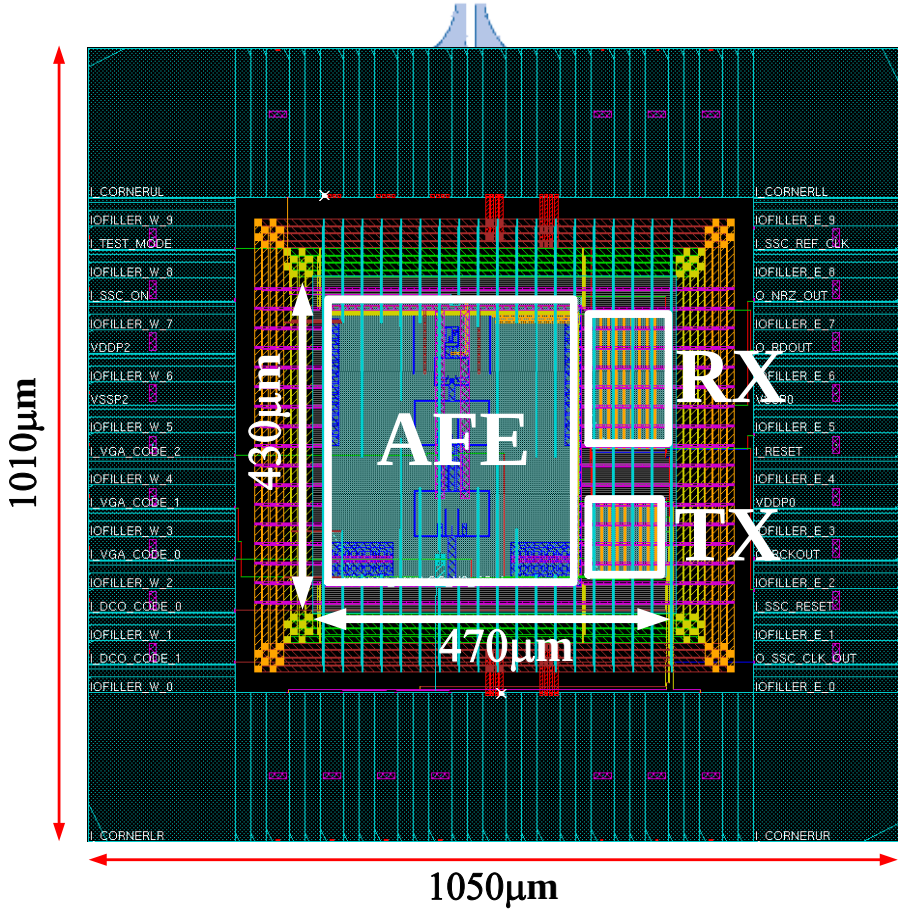
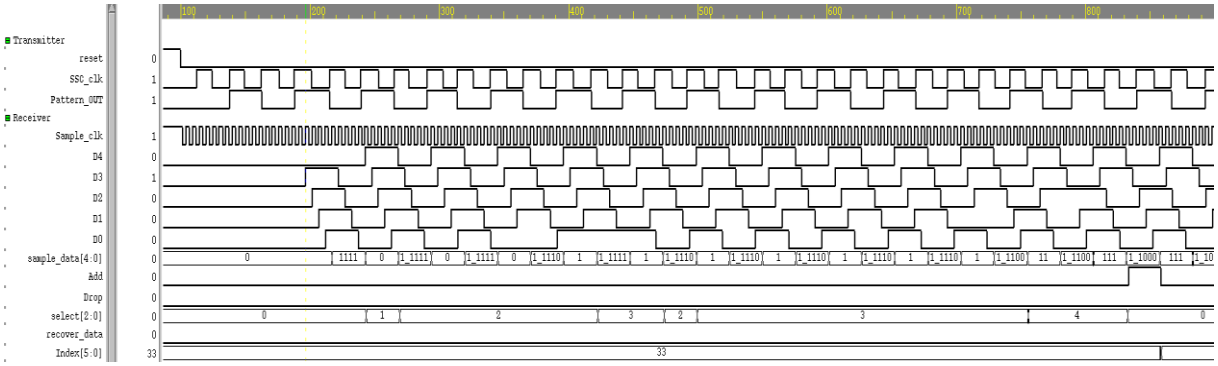


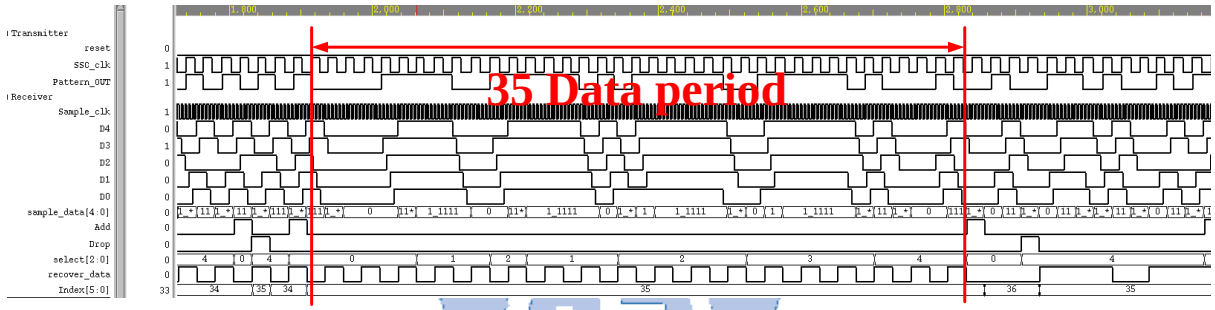
Fig. 4.2: Layout of the test chip.

Fig. 4.2 shows the layout of the test chip. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The chip size is 1.03 mm^2 and the core size is 430*470 μm^2. The test chip is composed of the digital part of the WBS transceiver. The proposed WBS transmitter (TX) block contains the SSCG and PRBS generator. The proposed WBS receiver (RX) block contains a 5X over-sampler, an Edge detector, an Error detector, 64-bit Add-Drop FIFO and the AFE circuit.

4.2 Full Chip Simulation



(a)



(b)

Fig. 4.3: System simulation of proposed WBS transceiver in 40 MHz.

Fig. 4.3(a) shows the post layout simulation of the proposed digital CDR in 40 MHz. The PRBS generator is activated by SSCG, which can perform the 10% center-spread modulation with a 30 kHz modulation frequency, or external clock.

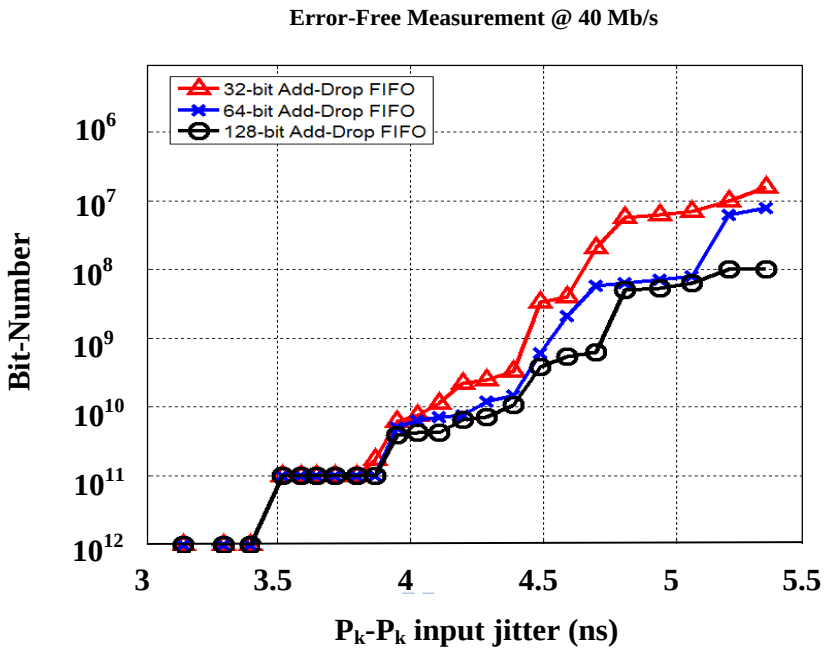
In the first fixed ‘10’ data pattern, the 5X over-sampler will sample the input data to determines the input data rate. After determining the transmission data rate, the 5X over-sampler uses the sample clock, which is 5 times faster than input data rate, to sample the input data.

After receiving the sample data, the edge detector finds the data transition by exclusive-or the two adjacent sampling data and adopts the center-picking method to determine the middle of sampling phase and output 5-bit data transition information to the error detector. The error detector uses the 5-bit flag information to generate the 3-bit Select signal and it also compares the current and previous values of the 5-bit flag information to generate the Add/Drop signals to the add-drop FIFO.

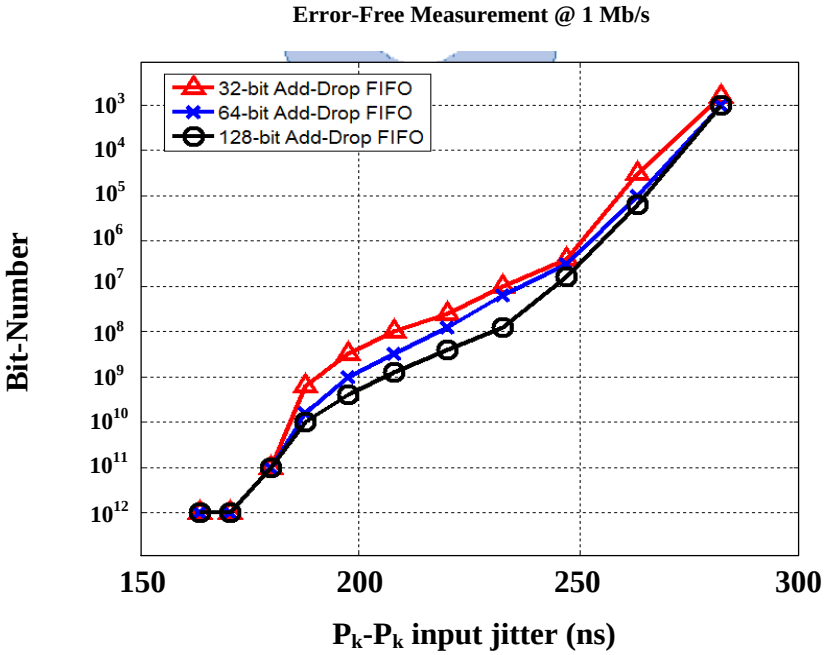
Because the add-drop FIFO is a 64 bit FIFO, in the beginning, the Index value of the add-drop FIFO is set to 33, in the middle of the FIFO, and the Index value added or subtracted by one according to the Add/Drop signals.

In Fig. 4.3(b) shows the first output correct data. Because the index value is 33, and there are two fixed ‘10’ pattern in the beginning of the transmission data, thus, the first output correct data will be delay 35 data period compared with the input data.

4.3 Error Free Measurement in RTL Simulation



(a) 40 Mb/s NON-SSC



(b) 1 Mb/s NON-SSC

Fig. 4.4: Error-free CDR simulation results. (a) 40 Mb/s. (b) 1 Mb/s.

Fig. 4.4 shows the error-free simulation results at 40 Mb/s and 1 Mb/s, respectively. The model of the jitter pattern has a normal distribution. In Fig. 4.4(a), when the proposed 5X oversampling CDR circuit operates in 40Mb/s, if the P_k-P_k received random data jitter is small than 4ns, the proposed CDR circuit can achieve a bit-error-rate (BER) < 10^{-10}. In Fig. 4.4(b), when the proposed 5X oversampling CDR circuit operates in 1Mb/s, if the P_k-P_k received random data jitter is small than 175ns, the BER is < 10^{-12}.

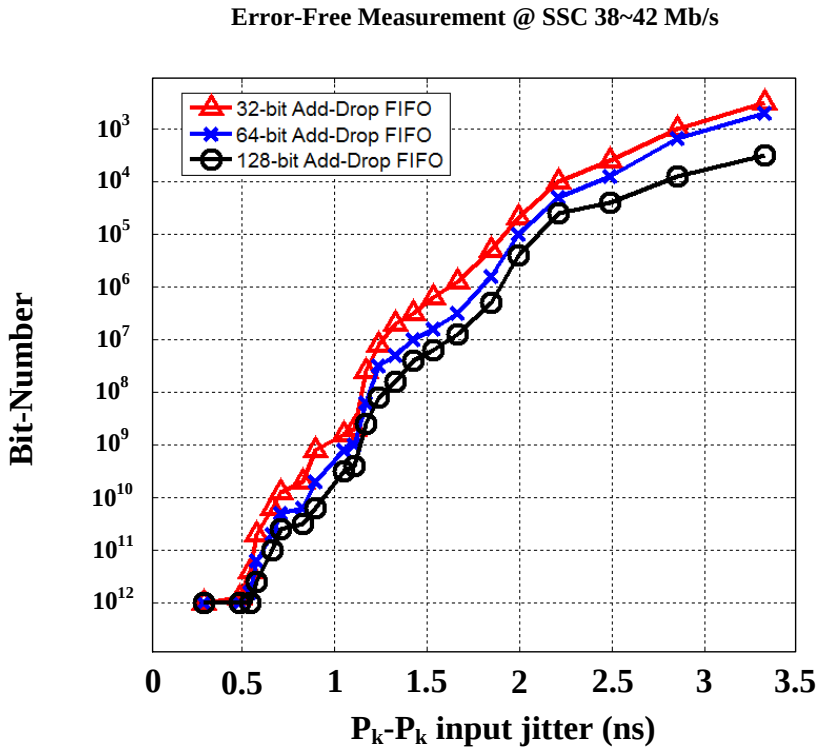


Fig. 4.5: SSCG with random jitter error-free simulation results.

In Fig. 4.5, when the data is transmitted with 10% center-spread modulation and the data rate range is from 38 Mb/s to 42 Mb/s, if the P_k-P_k received random data jitter is small than 1ns, the BER is < 10^{-9}.

4.4 Chip Summary and Comparison Table

Process	90nm CMOS
Operating Range	1 Mb/s ~ 40 Mb/s
Supply Voltage	1.0V
Core Area	0.2 mm^2
Power Consumption	1.69 mW (40Mb/s) 1.61 mW (1Mb/s)
Front-End Voltage Gain	38 dB
Sensitivity	-36 dBm
BER	10^{-10} (40 Mb/s) 10^{-12} (1 Mb/s)
Energy/bit	0.042 nJ/b (40 Mb/s) 0.161 nJ/b (1 Mb/s)

Table 4.2: Chip summary

The chip summary is shown in Table 4.2. The chip is implemented in TSMC 90nm standard performance CMOS process and 1.0V supply. The core area is 0.2mm^2. The frequency range of the proposed WBS transceiver ranges from 1Mb/s to 40Mb/s. The power consumption is 1.69mW at 40MHz and 1.61mW at 1Mb/s, respectively. The sensitivity of the analog front-end circuit is -38dBm. The bit error rate (BER) is 10^{-10} at 40 Mb/s and BER is 10^{-12} at 1 Mb/s. The energy consumption per bit at 40 Mb/s and 1 Mb/s is 0.042 nJ/b and 0.161 nJ/b, respectively.

The performance of proposed WBS transceiver and the comparison with related works are shown in Table 4.3.

Table 4.3: Comparison table

	[7] Zimmerman'96	[33] Shinagawa'04	[22] JSSC'07	[34] JSSC'09	[35] ISSCC' 09	[36] ISSCC'12	Proposed
Communication Mwthod	Narrowband Modulation	Electrooptic Conversion	Wideband Signaling	FSK	Body-couple	FSK	Wideband Signaling
Process	N/A	N/A	0.25-μm	0.18-μm	0.13-μm	0.18-μm	90 nm
Data Rate	2.4 kb/s	10 Mb/s	2 Mb/s	60 kb/s ~ 10 Mb/s	8.5 Mb/s	1 kb/s ~ 10 Mb/s	1 Mb/s ~ 40 Mb/s
Modulation	OOK/DSSS	No	No	Adaptive Frequency Hopping FSK	Correlation Direct Digital	Double FSK	No
Supply	9 V	5 V	1 V	1 V	1.2 V	1 V	1 V
Sensitivity	N/A	N/A	-35 dBm	-65 dBm	-60 dBm	-66 dBm	-36 dBm
Power Consumption	400 mW	650 mW	5 mW	4.6 mW	2.75 mW	2.4 mW	1.69 mW
Area	N/A	N/A	0.85 mm^2	2.30 mm^2	0.19 mm^2	12.5 mm^2 (with I/O pad)	0.2 mm^2
BER	N/A	$4.7*10^{-8}$	$1.1*10^{-7}$	10^{-5} (10Mb/s) $<10^{-9}$ (60kb/s)	10^{-3}	10^{-5}@10Mb/s/ 10^{-12}@10kb/s	10^{-10}@40Mb/s 10^{-12}@1Mb/s
Energy/bit	170 μJ/b	65 nJ/b	2.5 nJ/b	0.37 nJ/b	0.32 nJ/b	0.24 nJ/b	0.042 nJ/b

Chapter 5

Conclusion and Future Works

5.1 Conclusion

In this thesis, a low-power, low-hardware cost, high-speed and large jitter tolerance WBS transceiver for the body channel communication is presented.

In the proposed SSCG-based transmitter, the spread-spectrum clock generator is adopted to achieve EMI reduction, because the body antenna effect will radiates the signal power into the air and disturbs the neighbor circuits.

The proposed WBC receiver uses the 5X over-sampling CDR circuit which adopts the center-picking method to select the middle of the data points, and an add-drop FIFO algorithm which no needs a large FIFO to correct the selected data to increase the jitter tolerance.

With the direct-coupled interface, the NRZ binary data can be directly transmitted into the human body channel and it can not only reduces the complexity of the transceiver design but also reduce the power consumption. Thus, it can fully integrate all function blocks into a silicon chip and it can also reduce the physical size and achieve low cost.

The test chip is implemented in TSMC 90nm standard performance CMOS process, and thus it has good portability over different processes. The core area is 0.2 mm^2 and the power consumption is 1.69mW at 40 Mb/s and 1.61mW at 1 Mb/s, respectively.

5.2 Future Works

Because the BCC is using the human body as the transmission medium, the jitter phenomenon which caused by the body antenna effect still plays a critical rule when the transmission is in progress.

Although in our proposed WBS receiver, we can adopt the appropriate scheme and algorithm with very low hardware cost to recover the enormous interfered data. However, we still need a more reliable correction mechanism to ensure that there is no frequency offset between transmitter and receiver in long-term personal healthcare applications. Besides, we also need to standard the cyclic redundancy check (CRC) mechanism to ensure the correction of the package transmission.

With these schemes, we can make the entire BCC transmission mechanism is more complete and reliable, so that the BCC transmission can be used in more applications.

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