A Wide-Range Low-Cost All-Digital Duty-Cycle Corrector

Ching-Che Chung, *Member, IEEE*, Duo Sheng, *Member, IEEE*, and Chang-Jun Li

Abstract—A system clock with a 50% duty cycle is demanded in high-speed data communication applications, such as double data rate memories and double sampling analog-to-digital converters. In this paper, a wide-range low-cost all-digital duty-cycle corrector (ADDCC) is presented. The proposed ADDCC uses a delay-recycled half-cycle time delay line to reduce the required length of the delay line to half of the input clock period. Thus, it can extend the operating frequency toward a lower frequency with small area cost as compared with the conventional design. The proposed design is implemented in a standard performance 90-nm CMOS process, and the active area is 170 × 170 μm^2. The input frequency of the proposed ADDCC ranges from 75 to 734 MHz, and the input duty-cycle ranges from 9% to 86%. The measured output duty-cycle error is less than 1.78%. The proposed ADDCC consumes 4.59 mW at 734 MHz and 0.9 mW at 75 MHz with a 1.0-V power supply.

Index Terms—All-digital duty-cycle corrector (ADDCC), delay-locked loop (DLL), digitally controlled delay line, phase alignment, wide-range.

I. INTRODUCTION

A S THE operating frequencies of electronic systems continue to increase, double edge sampling techniques are increasingly used in high-performance systems. For example, double data rate memories and double sampling analog-to-digital converters require sampling the input data via the positive and negative edges of the reference clock. However, the duty-cycle error of the clock signal may be as high as ±20% when the clock signal is distributed to other module blocks through clock buffers [1]. The duty-cycle error of the clock signal causes unbalanced calculation times for sequential circuits. Accordingly, a system clock with a 50% duty cycle is demanded. Therefore, a duty-cycle corrector (DCC) is used in a system-on-a-chip (SoC) to correct distortions in the clock signal owing to process, voltage, and temperature (PVT) variations. Furthermore, the corrected clock signal should be phase aligned with the input clock to avoid inserting an additional clock skew by the DCC circuit.

In recent years, many DCCs have been proposed and can be classified into two categories: analog DCCs [2] and

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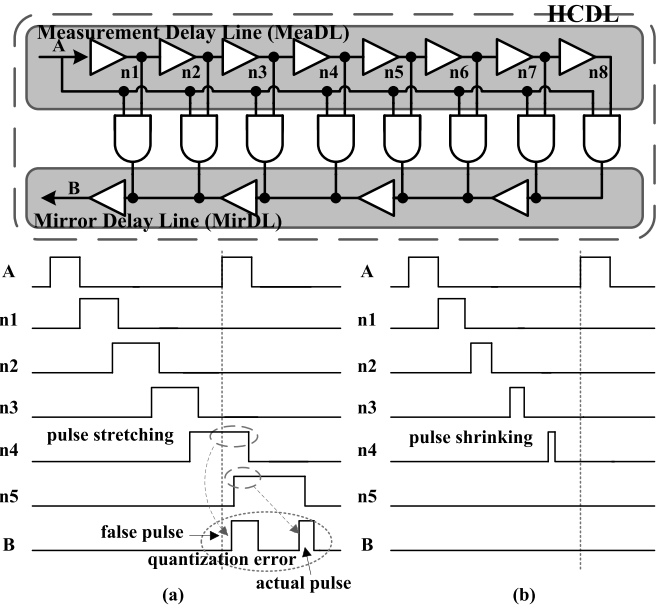
Fig. 1. Operation of the SMD-based DCC at unbalanced process corners. (a) Pulse stretching. (b) Pulse shrinking.

digital DCCs [3]–[15]. Analog DCCs use a pulsewidth control loop (PWCL) to correct the input clock by continuously adjusting the feedback voltage of the control stage [2]. However, PWCL-based DCC requires a relatively long settling time and uses several large on-chip capacitors for filtering control voltage ripples. Thus, PWCL-based DCC often occupies a relatively large chip area. Furthermore, PWCL-based DCC has a serious charge pump mismatch problem at unbalanced process corners (i.e., slow-fast or fast-slow), and this problem will affect the output duty-cycle error. In addition, the leakage current of transistors in advanced CMOS process also causes ripples on the control voltage and affects the stability of the output clock. Moreover, the output clock is not phase aligned with the input clock in PWCL-based DCC [2].

In contrast to analog DCCs, all-digital DCCs (ADDCCs) utilize no passive components facilitating their integration with other digital circuits. There are two major ADDCC architectures: the synchronous-mirror-delay (SMD) type and the time-to-digital converter (TDC) type. The SMD-based ADDCC [4] uses a half-cycle delay line (HCDL) to measure the period of the input clock. However, when short pulses pass through the HCDL, the pulses can be stretched or shrank due to the duty distortion caused by the delay line at unbalanced process corners. As shown in Fig. 1(a), when a false pulse
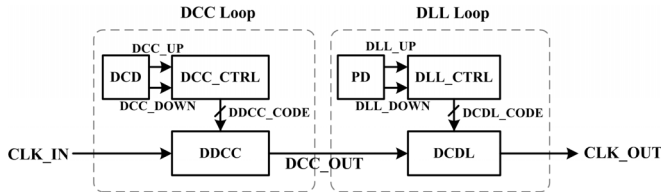
Fig. 2.   Dual-loop ADDCC architecture.

is generated at node B due to pulse stretching, the output duty-cycle error is increased. On the other hand, as shown in Fig. 1(b), when the pulse at node B disappears due to pulse shrinking, the SMD-based ADDCC suffers a malfunction.

The TDC is widely used in ADDCCs [5]–[9] to reduce the lock-in time. The TDC can obtain input clock period information, and therefore, the lock-in time can be greatly reduced as compared with the DCC [11] using the successive approximation register controlled or pulse shrinking/stretching approaches [12]–[15]. However, in ADDCCs [5], [6], the TDC has an extra area cost, and a delay mismatch problem also exists between the TDC and the delay line. To reduce the chip area and delay mismatch problem, ADDCCs [7]–[9] integrate the TDC into the delay line. However, in ADDCCs [7]–[9], since the fine-tuning delay stage is not added in the delay line, the duty-cycle error of these ADDCCs is dependent on the coarse-tuning delay stage resolution.

As compared with TDC-based ADDCCs, delay-recycled ADDCCs [8]–[10] have fewer delay cells in the delay line and flip-flops in the TDC. Thus, the operating frequency range can be extended to a lower frequency with less area cost and lower power consumption. However, the binary-weighted delay line in ADDCCs [8], [9] has a nonlinearity problem with on-chip variations. To improve the resolution of the delay line, fine-tuning delay cells are added in the ADDCC [10] to achieve a relatively small duty-cycle error. However, the cascaded delay line architecture usually needs to overlap the coarse-tuning step by 20%–30% in design of the fine-tuning delay stage to ensure that the controllable delay range of the fine-tuning delay stage is larger than one coarse-tuning step with PVT variations. However, the delay time versus control code becomes a nonmonotonic response in [10], and there will have a large cycle-to-cycle jitter when the DCC controller switches coarse-tuning control code.

A dual-loop-based ADDCC [14], [15] that employs a DCC and a delay-locked loop (DLL) is shown in Fig. 2. The dual-loop-based ADDCC has high duty-cycle correction accuracy while maintaining phase alignment between the input and the output clocks. However, the dual-loop-based ADDCC requires a relatively long lock-in time due to the dual-loop operation. In addition, since the DLL is used to generate two complementary duty-cycle signals, the duty-cycle error caused by the delay line of the DLL cannot be corrected by the DCC loop. Therefore, the duty-cycle error caused by the digitally controlled delay line will directly affect the duty-cycle error of the output clock (CLK_OUT).

In this paper, an ADDCC that can achieve a high duty-cycle correction resolution and have a wide operating frequency range (734/75 MHz = 9.78) while maintaining

phase alignment and low area cost is presented. The rest of this paper is organized as follows. The architecture of the proposed ADDCC is presented in Section II. Section III describes the circuit implementation of the proposed design. Section IV discusses the theoretical performance of the ADDCC. Section V shows the experimental results of the proposed design. Finally, the conclusion is given in Section VI.

II. PROPOSED ADDCC ARCHITECTURE

A block diagram of the proposed ADDCC is shown in Fig. 3. The ADDCC is composed of a multiplexer (MUX), a pulse generator (PG), an AND gate, a HCDL, a phase detector (PD) [16], an ADDCC controller, a TDC encoder, and a D-type flip-flop (DFF). The PG transforms the input clock (CLK_IN) and the feedback clock (CLK_FB or CLK_OUT) into narrow pulses (in_pulse and fb_pulse). The signal tdc_start selects CLK_FB or CLK_OUT to generate fb_pulse. The AND gate before the pulse signal will be pulled down to avoid unnecessary pulses triggering the DFF until the reset signal (RESET) is pulled low. Once the reset signal (RESET) is pulled low, the AND gate before the pulse signal allows the short pulses to propagate through the HCDL.

The proposed TDC-embedded HCDL is composed of a 6-bit TDC-embedded coarse-tuning delay line (CDL) and a 5-bit fine-tuning delay line (FDL) [19], as shown in Fig. 4. The proposed CDL is composed of 63 lattice delay units [20] and embedded with a TDC. The dummy cells are added to balance the capacitance loading of the NAND gates. Every two NAND gates have a DFF for quantizing the period of the input clock and output as tdc_data [63:0], and the resolution of the CDL is the propagation delay of the two NAND gates. To improve the delay line resolution, the FDL is added. The FDL [19] is composed of two parallel connected tristate buffer arrays operating as an interpolator circuit. In the proposed ADDCC, the delay-recycled architecture reduces the required length of the delay line to half of the input clock period. As a result, the operating frequency range can be extended to a lower frequency with less area cost and lower power consumption.

Fig. 5 shows the overall timing diagram of the proposed ADDCC. After the ADDCC is reset, the control code (ctrl_code [10:0]) of the HCDL is set to the maximum value (i.e., 11'd2047) that sets the HCDL to provide a maximum delay time, and tdc_start is pulled high in the beginning. Subsequently, the narrow pulses propagate through the HCDL. At the next rising edge of the input clock (CLK_IN), the TDC captures the propagated pulse signals and stores them as tdc_data [63:0]. The TDC encoder searches for the bit location of the first 1 in tdc_data [63:0], from the most-significant bit (MSB) to the least-significant bit (LSB). Then, the TDC encoder outputs the initial delay control code (tdc_code [5:0]) for the ADDCC to achieve fast lock-in.

After setting the initial control code, the input (CLK_IN) and output (CLK_OUT) clocks still have a residual phase error due to the finite TDC resolution. Hence, the proposed ADDCC increases or decreases the delay-line control code (ctrl_code [10:0]) according to the outputs of the PD.
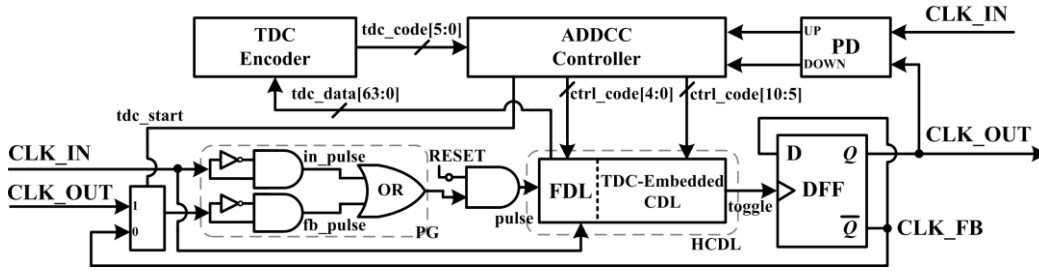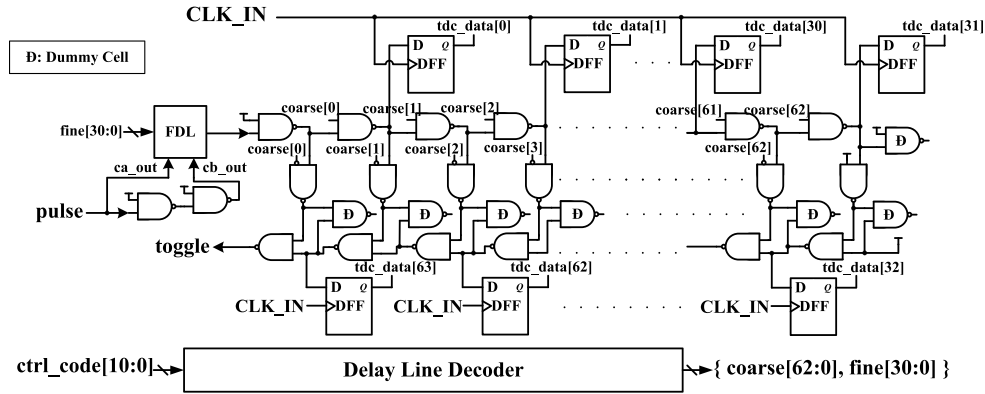
Fig. 3. Proposed ADDCC.
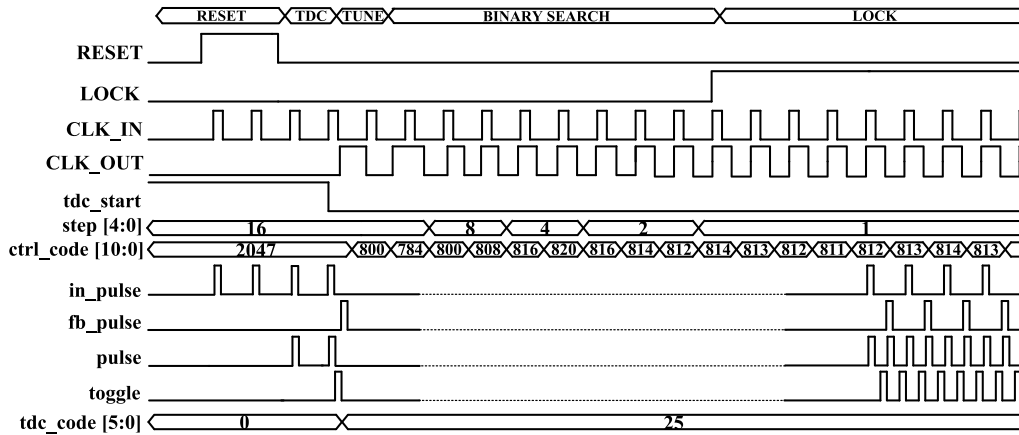

Fig. 4. TDC-embedded HCDL.

Fig. 5. Overall timing diagram of the proposed ADDCC.

A binary search scheme is adopted in the ADDCC controller to accelerate the fine-tuning process. Whenever the PDs output is changed from UP to DOWN or vice versa, the search step (step [4:0]) is divided by 2 until the step is reduced to one. Once the step is equal to one, the ADDCC is locked, and the output clock (CLK_OUT) is phase aligned with the input clock (CLK_IN). In the proposed ADDCC, the required delay time of the HCDL is reduced to one half of the input clock period. Thus, for wide-range operation, chip area and power consumption of the ADDCC can be reduced as compared with other ADDCCs [5]–[7].

The detail timing diagrams of the TDC with a low-frequency input clock and a high-frequency input clock are shown in Figs. 6 and 7, respectively. In Fig. 6, after the ADDCC

is reset, the first rising edge transition of the toggle signal triggers the DFF to pull up the output clock (CLK_OUT) to logic 1 state, indicating that the period of the input clock (CLK_IN) is longer than the maximum delay time of the HCDL. Then, the PG generates the feedback pulse (fb_pulse) from CLK_OUT. Subsequently, the combined pulse signal propagates through the HCDL and produces the next rising transition of the toggle signal. The first 1 bit location of tdc_data [63:0] from the MSB to the LSB is 16. However, the logic 1 state of CLK_OUT indicates that the pulse signal has already propagated through the HCDL and looped back to the HCDL again. Therefore, the period of the input clock (CLK_IN) is quantized as 80 (= 16 + 64) coarse-tuning delay unit's delay time. For the proposed ADDCC, the
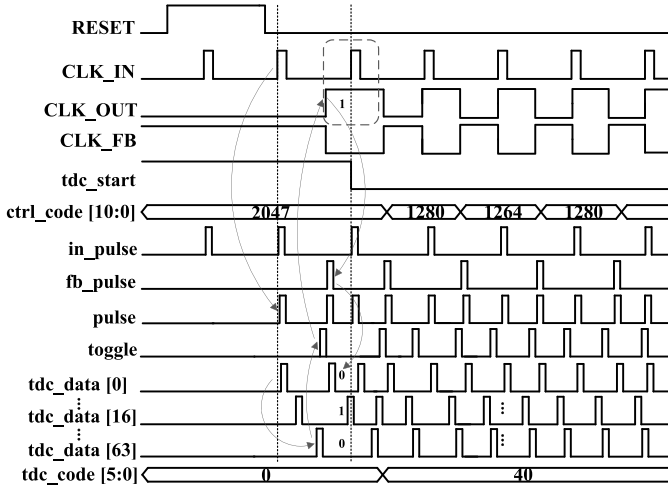
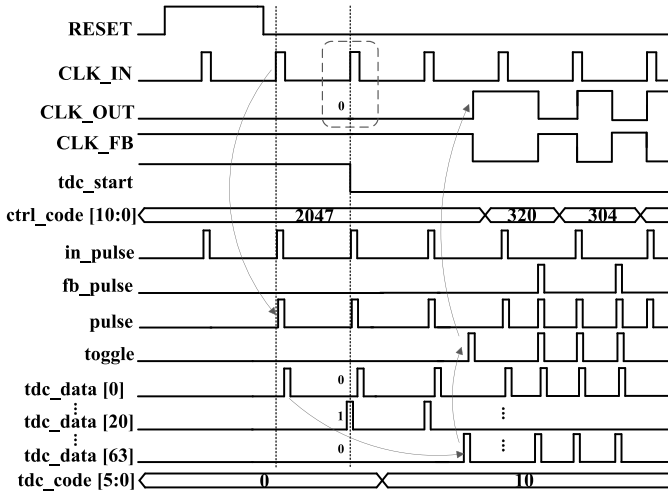Fig. 6.　Timing diagram of the TDC with a low-frequency input.

Fig. 7.　Timing diagram of the TDC with a high-frequency input.

HCDL needs to provide a half-cycle delay time of the input clock such that tdc_code [5:0] output by the TDC encoder is 40 (=80/2).

When the period of the input clock (CLK_IN) is smaller than the maximum delay time of the HCDL, the short pulses require more than one input clock cycle to pass through the full delay line, as shown in Fig. 7. Thus, at the next rising edge of the input clock (CLK_IN), the output clock (CLK_OUT) does not have a rising transition in this case. In Fig. 7, the first 1 bit location of tdc_data [63:0] from the MSB to the LSB is 20. Therefore, tdc_code [5:0] should be 10 (=20/2). With the TDC, the proposed ADDCC can achieve fast lock-in time within 15 input clock cycles.

III. CIRCUIT IMPLEMENTATION

Fig. 8 shows the block and timing diagrams of the PG. The PG generates narrow pulses to propagate through the HCDL at rising transitions of the input clocks (CLK_A and CLK_B). The OR gate outputs the short pulses (PG_OUT) to the HCDL from signals a_pulse and b_pulse. Fig. 8 also shows that the PG can generate pulses with a
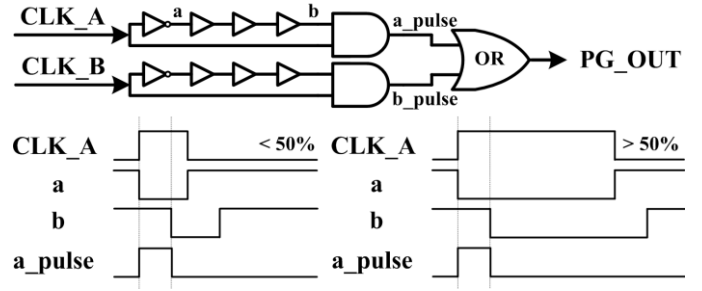
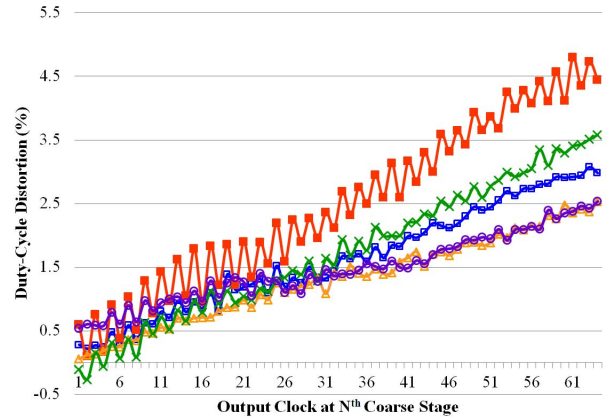

Fig. 8.　Block diagram and timing diagram of the PG.

Fig. 9.　Duty-cycle distortion caused by the TDC-embedded CDL.

fixed pulsewidth when the duty cycle of the input clock (CLK_A or CLK_B) is greater than or smaller than 50%. When the pulsewidth of the input clock is longer than the buffer chain delay, the PG generates pulses whose pulsewidth is equal to the buffer chain delay. Oppositely, when the pulsewidth of the input clock is shorter than the buffer chain delay, the PG generates pulses whose pulsewidth is equal to the input clock. Hence, once the pulsewidth is too small and cannot trigger the DFF, the proposed ADDCC will not work correctly.

After integrating the DFFs of the TDC into the CDL, the capacitance loadings of the individual NAND gates are not equal. Fig. 9 shows the duty-cycle output of the TDC-embedded CDL at the Nth coarse-tuning stage with a 50% duty-cycle input clock. The maximum duty-cycle distortion caused by the CDL is 4.8% at all process corners. Since the proposed PG generates pulses with a fixed pulsewidth, and the CDL increases the pulsewidth at all process corners, the toggle signal can always trigger the DFF at all process corners. As a result, the input duty-cycle range will not be affected by the duty-cycle distortion caused by the HCDL.

Cascaded delay line architectures [10], [12], [14]–[18], [20], [21] not only increases the area cost and power consumption of the chip but also causes a large cycle-to-cycle jitter when the coarse-tuning control code is switching. Therefore, the interpolator-based FDL [19] is used to enhance the resolution of the HCDL and guarantees that the controllable delay range of the FDL is equal to one coarse-tuning step with PVT variations.
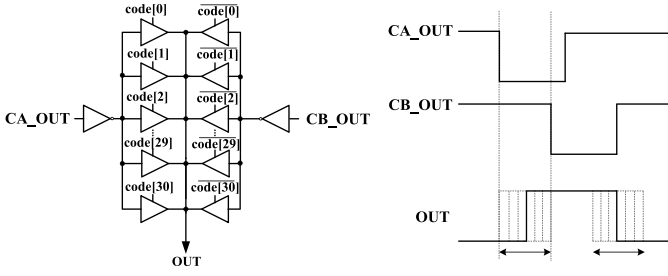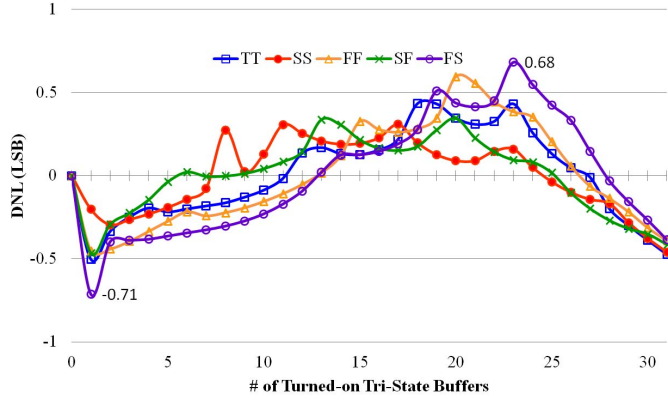
Fig. 10. Proposed FDL.

Fig. 11. DNL of the proposed FDL.

Fig. 12. Microphotograph of the proposed ADDCC.

Fig. 10 shows the architecture and the timing diagram of the proposed FDL. The propagation delay of the FDL is controlled by the driving strength of two parallel connected tristate buffer arrays. The rising edge of the output clock (OUT) will be close to CA_OUT when the fine-tuning control code (code [30:0]) sets to the maximum value (i.e., 31'h7FFF_FFFF). In contrast, the output clock (OUT) will be close to CB_OUT when the fine-tuning control code sets to the minimum value (i.e., 31'h0). By adjusting the number of turned-ON tristate buffers in the arrays, the resolution of the FDL can be enhanced to be 1/31 that of the coarse-tuning step. Therefore, the output duty-cycle error of the proposed ADDCC can be further reduced. The proposed FDL has a maximum differential nonlinearity (DNL) of −0.71 LSB, as shown in Fig. 11. DNL is a term describing the deviation between two delay values corresponding to adjacent input digital control codes. DNL of the proposed FDL is higher than −1.0 LSB, and this indicates that the proposed FDL has a monotonic response at all process corners.

IV. PERFORMANCE ANALYSIS

A bang-bang PD [16] is used in the proposed ADDCC to compare the phase relationship between the input clock and the output clock. When the ADDCC is locked, the following equation should be satisfied:

$$
\begin{aligned}
T_{\text{CLK\_OUT}} &= T_{\text{CLK\_IN}} \\
&= 2(T_{\text{PG}} + T_{\text{AND}} + \underline{T_{\text{HCDL}}} + T_{\text{DFF}}) \\
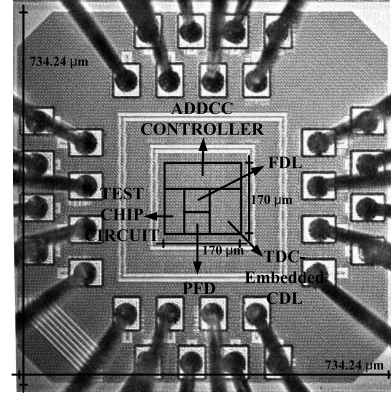&= 2(T_{\text{PG}} + T_{\text{AND}} + \underline{T_{\text{FDL}} + T_{\text{CDL}}} + T_{\text{DFF}}) \quad (1)
\end{aligned}
$$

where $T_{\text{CLK\_IN}}$ is the period of the input clock, $T_{\text{CLK\_OUT}}$ is the period of the output clock, T_{PG} is the delay time of the PG, T_{AND} is the delay time of the AND gate, T_{HCDL} is the delay time of the HCDL that includes the delay time of the FDL (T_{FDL}) and the delay time of the CDL (T_{CDL}), and T_{DFF} is the clock-to-q delay of the DFF.

The maximum operating frequency of the proposed ADDCC is determined by the total intrinsic delay from the input clock (CLK_IN) to the output clock (CLK_OUT), as shown in (2). In (2), $T_{\text{HCD}L\text{min}}$ is the intrinsic delay of the HCDL. Oppositely, the minimum operating frequency of the proposed ADDCC is given by (3). In (3), $T_{\text{HCD}L\text{max}}$ is the maximum delay time of the HCDL. In our design, the CDL is composed of 63 coarse delay units to extend the operating frequency range to a lower frequency

$$
T_{\text{CLK\_IN}_{\text{min}}} = 2(T_{\text{PG}} + T_{\text{AND}} + T_{\text{HCD}L\text{min}} + T_{\text{DFF}}) \quad (2)
$$
$$
T_{\text{CLK\_IN}_{\text{max}}} = 2(T_{\text{PG}} + T_{\text{AND}} + T_{\text{HCD}L\text{max}} + T_{\text{DFF}}). \quad (3)
$$

When PVT variations are considered, the input frequency range at all PVT corners is shown in (4) and (5). The slow-slow corner and fast-fast corner dominate the maximum and minimum input operating frequencies, respectively

$$
\begin{aligned}
T_{\text{CLK\_IN}_{\text{min}}} = 2(&T_{\text{PG,SS}} + T_{\text{AND,SS}} \\
&+ T_{\text{HCD}L\text{min,SS}} + T_{\text{DFF,SS}}) \quad (4)
\end{aligned}
$$
$$
\begin{aligned}
T_{\text{CLK\_IN}_{\text{max}}} = 2(&T_{\text{PG,FF}} + T_{\text{AND,FF}} \\
&+ T_{\text{HCD}L\text{max,FF}} + T_{\text{DFF,FF}}). \quad (5)
\end{aligned}
$$

The proposed TDC quantizes the input clock period into digital codes. If the ADDCC is in high-frequency operation, as shown in Fig. 7, the input clock period in high-frequency operation ($T_{\text{CLK\_IN},H}$) after TDC operation can be expressed by (6), where T_{CDU} is the delay time of the coarse delay unit. After TDC operation, the CDL turns ON $(n/2)$ CDUs to provide a delay time close to half of the input clock period. However, the output clock period in high-frequency operation ($T_{\text{CLK\_OUT},H}$) has a quantization error Δ_H. This error can be further compensated by the ADDCC controller after TDC operation, but this quantization error will increase
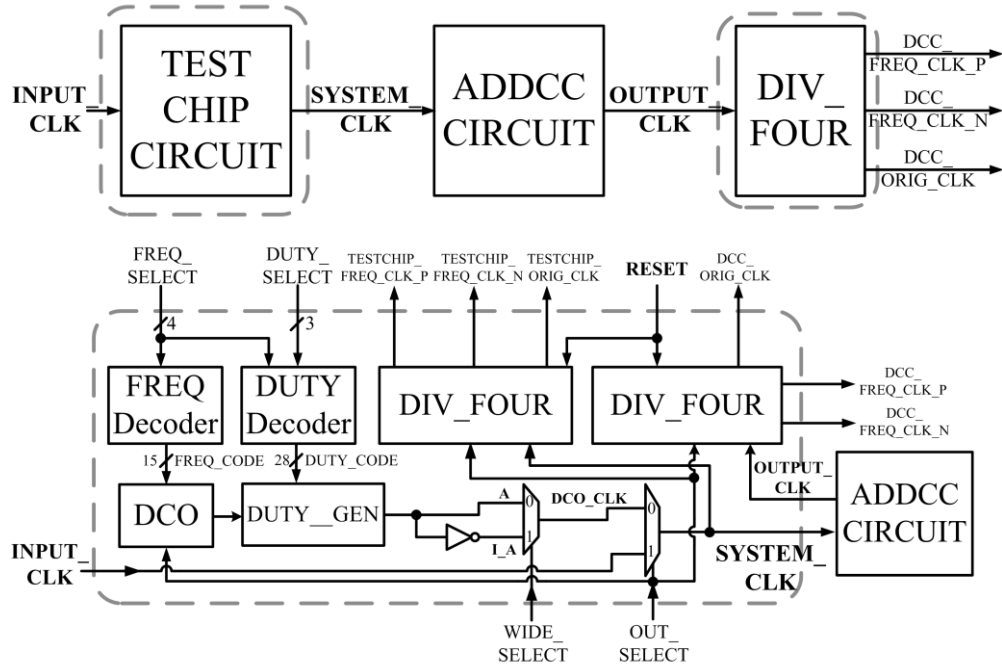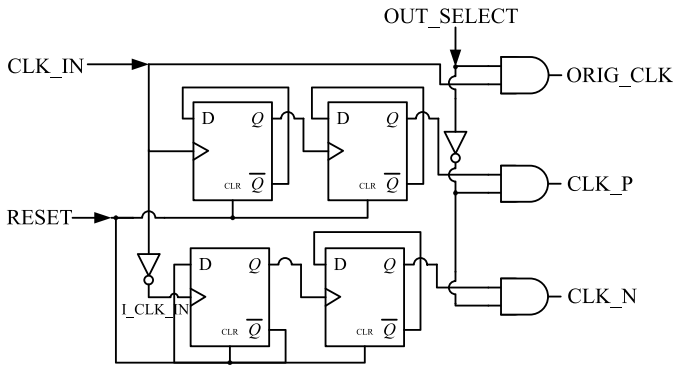
Fig. 13.	Block diagram of the test chip.

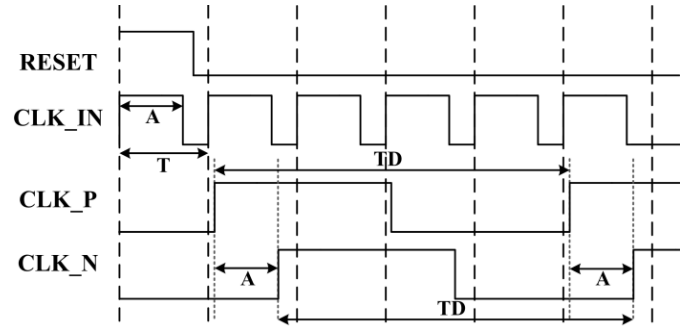Fig. 14.	Block diagram of the DIV_FOUR circuit.

Fig. 15.	Timing diagram of the DIV_FOUR circuit.

the lock-in time of the ADDCC

$$T_{\text{CLK\_IN},H} = T_{\text{PG}} + T_{\text{AND}} + T_{\text{FDL}} + nT_{\text{CDU}}$$

$$T_{\text{CDL}} = \frac{1}{2}(nT_{\text{CDU}})$$

$$= \frac{1}{2}(T_{\text{CLK\_IN},H} - T_{\text{PG}} - T_{\text{AND}} - T_{\text{FDL}})$$

$$T_{\text{CLK\_OUT},H} = 2(T_{\text{PG}} + T_{\text{AND}} + T_{\text{FDL}} + T_{\text{CDL}} + T_{\text{DFF}})$$

$$= T_{\text{CLK\_IN},H} + \underline{T_{\text{PG}} + T_{\text{AND}} + T_{\text{FDL}} + 2T_{\text{DFF}}}$$

$$= T_{\text{CLK\_IN},H} + \triangle_H \qquad (6)$$

$$T_{\text{CLK\_IN},L} = 2(T_{\text{PG}} + T_{\text{AND}} + T_{\text{FDL}}) + T_{\text{DFF}} + nT_{\text{CDU}}$$

$$T_{\text{CDL}} = \frac{1}{2}(nT_{\text{CDU}})$$

$$= \frac{1}{2}[T_{\text{CLK\_IN},L} - 2$$

$$\times (T_{\text{PG}} + T_{\text{AND}} + T_{\text{FDL}}) - T_{\text{DFF}}]$$

$$T_{\text{CLK\_OUT},L} = 2(T_{\text{PG}} + T_{\text{AND}} + T_{\text{FDL}} + T_{\text{CDL}} + T_{\text{DFF}})$$

$$= T_{\text{CLK\_IN},L} + \underline{T_{\text{DFF}}}$$
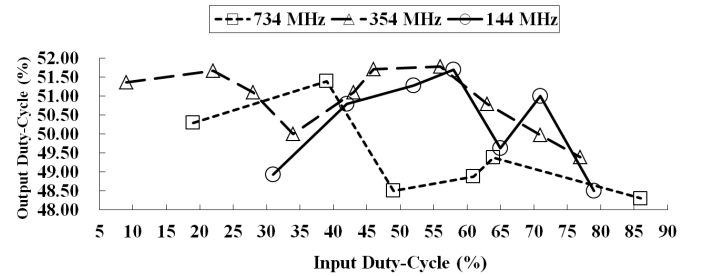
$$= T_{\text{CLK\_IN},L} + \triangle_L. \qquad (7)$$

Fig. 16.	Measured output duty cycle with various input frequencies and duty cycles.

When the proposed ADDCC is in low-frequency operation, as shown in Fig. 6, the input clock period at low-frequency operation ($T_{\text{CLK\_IN},L}$) after TDC operation can be expressed by (7). The output clock period in low-frequency operation ($T_{\text{CLK\_OUT},L}$) has a small quantization error Δ_L. This error can also be compensated by the ADDCC controller after TDC operation.
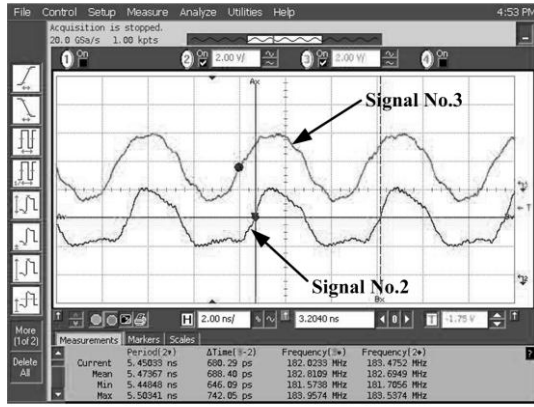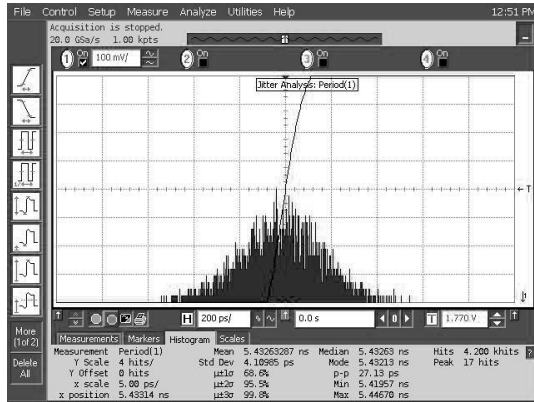
Fig. 17. Output clock at 734 MHz. (a) Duty-cycle measurement. (b) Jitter histogram.

Fig. 18. Output clock at 144 MHz. (a) Duty-cycle measurement. (b) Jitter histogram.

The TDC quantization errors will be at least one DFFs propagation delay time. After TDC operation, the ADDCC controller with the proposed PD can reduce the residual duty-cycle error caused by the finite TDC resolution.

V. EXPERIMENTAL RESULTS

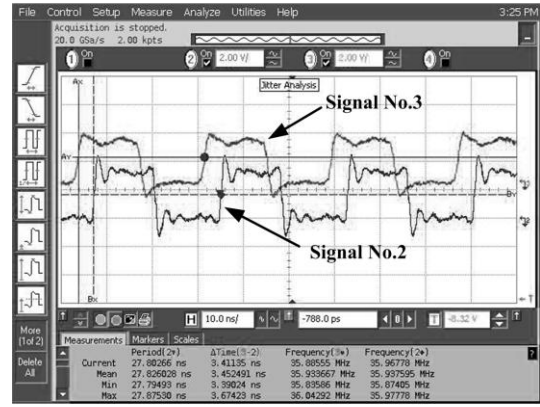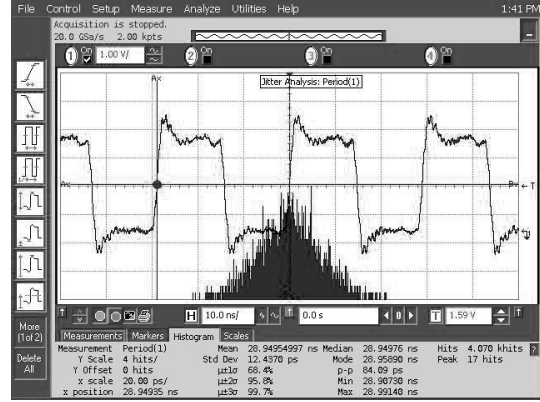The proposed ADDCC is fabricated using a 90-nm standard performance CMOS process, and the microphotograph of the ADDCC is shown in Fig. 12. The core area is $170 \times 170 \ \mu m^2$, and the chip area including I/O pads is $734.24 \times 734.24 \ \mu m^2$.

The chip consists of an ADDCC and a test chip circuit. Due to the speed limitations of the I/O pads, signals with a frequency higher than 300 MHz are not able to transmit through the I/O pads. Hence, we use a digitally controlled oscillator (DCO) and a duty-cycle generator (DUTY_GEN) to generate an on-chip high-speed clock (DCO_CLK) with various frequencies and duty cycles for testing the proposed ADDCC, as shown in Fig. 13. The DCO is designed as a MUX-type DCO, and its operating frequency ranges from 144 to 734 MHz. The DUTY_GEN sets the output duty cycle from the duty selection bits (DUTY_SELECT). The DCO and the DUTY_GEN can only generate an output clock (*A*) with a duty cycle higher than 50%. Thus, a clock with a duty cycle smaller than 50% can be provided by

an inversed signal (I_A). The system clock selection bits (OUT_SELECT) select the on-chip clock (DCO_CLK) or the external clock (INPUT_CLK) to be the ADDCCs input clock (SYSTEM_CLK).

The divide-by-four (DIV_FOUR) circuit is designed to divide the high-frequency signal to a lower frequency for measurement considerations, as shown in Fig. 14. DFFs triggered by the positive and negative edges of the CLK_IN signal are used to divide the CLK_IN frequency by four. After frequency division, the low-frequency signals (CLK_P and CLK_N) are able to be sent to the output pads. When the CLK_IN frequency is low, we can directly send the input clock to the I/O pads without frequency division.

The timing diagram of the DIV_FOUR circuit is shown in Fig. 15. If the period of the CLK_IN is T and its pulsewidth is A, the duty cycle of the CLK_IN is A/T. After frequency division, the period of CLK_P and CLK_N becomes TD $(= 4 \times T)$. Since the phase difference between the rising edges of CLK_P and CLK_N is still A, the duty cycle of the input clock (CLK_IN) can be computed as $(4 \times A)/$TD.

Fig. 16 summarizes the measurement results of the proposed ADDCC. As shown in Fig. 16, the input frequency ranges from 144 to 734 MHz, and the input duty-cycle ranges from 9% to 86%. The maximum output duty-cycle error is 1.78%. In addition, the core power is 1.0 V and the pad power is 3.3 V.

TABLE I
PERFORMANCE COMPARISONS

Parameter	Proposed	JSSC'08 [2]	TVLSI'13 [21]	TVLSI'13 [15]	TVLSI'12 [3]	TCAS-II'06 [5]	JSSC'09 [6]	ISSCC'08 [22]
Phase Alignment	Yes	No	Yes	Yes	No	Yes	Yes	Yes
Type	TDC/ HCDL	Analog PWCL	TDC/ HCDL/ Interpolator	Sequential Search/ HCDL	TDC/ HCDL	TDC	DCC/DLL	DCC/DLL
Process	90 nm	0.18 μm	0.18 μm	65 nm	0.18 μm	0.18 μm	0.18 μm	66 nm
Supply Voltage (V)	1.0	1.8	1.8	1.0	1.8	1.8	1.8	1.5
Frequency (MHz)	$75 \sim 734$	$50 \sim 1100$	$250 \sim 625$	$262 \sim 1020$	$400 \sim 2000$	$800 \sim 1200$	$440 \sim 1500$	$100 \sim 1000$
Input Duty-Cycle Range (%)	$9 \sim 86$	$30 \sim 70$	$30 \sim 70$	$14 \sim 86$	$20 \sim 80$	$40 \sim 60$	$40 \sim 60$	$40 \sim 60$
Maximum Output Duty-Cycle Error (%)	1.78	1.0	1.6	1.4	3.5	1.5	1.8	1.0
Lock-in Time (Cycle)	< 15	< 138	< 36	N/A	< 3.5	< 10	< 15	N/A
RMS Jitter	4.11ps @734MHz	1.95ps @1.3GHz	2.56ps @625MHz	3.23ps @1.02GHz	3.55ps @1GHz	1.5ps @1GHz	0.9ps @1.5GHz	5.26ps @1GHz
Power Consumption	0.9mW @75MHz 4.59mW @734MHz	4.8mW @1.3GHz	8.4mW @250MHz 10.8mW @625MHz	1.96mW @262MHz 6.5mW @1.02GHz	1.76mW @400MHz 3.6mW @2GHz	15mW @1GHz	43mW @1.5GHz	4.2mW @100MHz 20mW @1GHz
Area (mm²)	0.0289	0.2068	0.09	0.01	0.025	0.23	0.053	0.111
PBR (mW)	0.47	0.02	0.78	1.66	N/A	0.94	0.95	0.89

The proposed ADDCC consumes 4.59 mW at 734 MHz, and 0.9 mW at 75 MHz.

Fig. 17 shows the duty-cycle measurement and the jitter histogram at 734 MHz. Signal No.3 is CLK_P and Signal No.2 is CLK_N, as shown in Fig. 15. As shown in Fig. 17(a), the frequency of the ADDCC output clock (OUTPUT_CLK) should be four times faster than Signal No.3. Hence, the frequency of the output clock (OUTPUT_CLK) is 734 MHz (=182.8109 × 4). The phase difference between two rising edges of Signal No.3 and Signal No.2 is 688.4 ps. Therefore, the duty cycle of the output clock (OUTPUT_CLK) is 50.3% (= 4 × 0.6884/5.47367). As shown in Fig. 17(b), the peak-to-peak (P_K-P_K) jitter and the root-mean-square (rms) jitter are 27.13 and 4.1 ps at 734 MHz, respectively.

Fig. 18 shows the duty-cycle measurement and the jitter histogram at 144 MHz. As shown in Fig. 18(a), the frequency of the output clock (OUTPUT_CLK) is 144 MHz (= 35.933667 × 4). The phase difference between the two rising edges of Signal No.3 and Signal No.2 is 3.45 ns. Therefore, the duty cycle of the output clock (OUTPUT_ CLK) is 49.63% (= 4 × 3.452491/27.826028). As shown in Fig. 18(b), the P_K-P_K jitter and the rms jitter are 84.09 and 12.44 ps at 144 MHz, respectively.

Fig. 19 shows the duty-cycle measurement of the proposed ADDCC from an external 75 MHz clock input. Signal No.2 is

the input clock, and Signal No.3 is the output clock. In Fig. 19, these two signals are phase aligned. Hence, the proposed ADDCC does not insert an extra skew between the input clock and the output clock.

Table I lists the performance comparisons of the proposed ADDCC with current DCCs. A power bandwidth ratio (PBR) [8] is adopted to provide a fair performance comparison, as expressed in (8). The proposed ADDCC has the lowest PBR as compared with current ADDCCs. Although analog PWCL-based DCC has a small PBR, it occupies a relative large chip area as compared with other DCCs due to the on-chip loop filter. In addition, the output clock is not phase aligned with the input clock in the analog PWCL-based DCC [2].

The HCDL of the ADDCC [3] has only coarse-tuning delay units, and thus the duty-cycle error is higher than that of the other ADDCCs at high-frequency operation. Therefore, we did not include the ADDCC [3] in PBR comparisons. Furthermore, DCCs [2], [15], [21] are easily affected by unbalanced process variations, and thus, their architectures are not suitable for mass production. As compared with current DCCs, the proposed ADDCC not only has a relatively wide frequency range but also has a relatively wide input duty-cycle range with small area cost and low-power consumption. Thus, the proposed ADDCC is suitable for high-speed on-chip
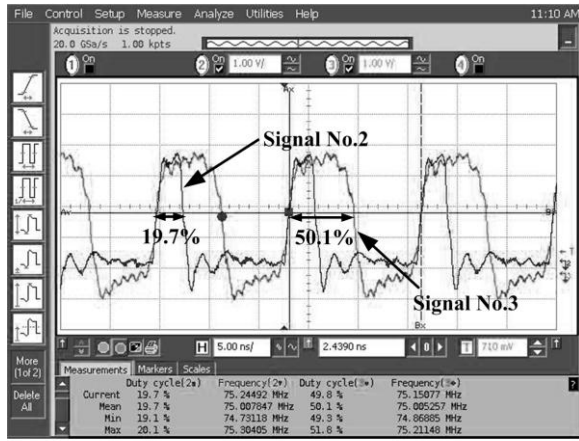
(a)
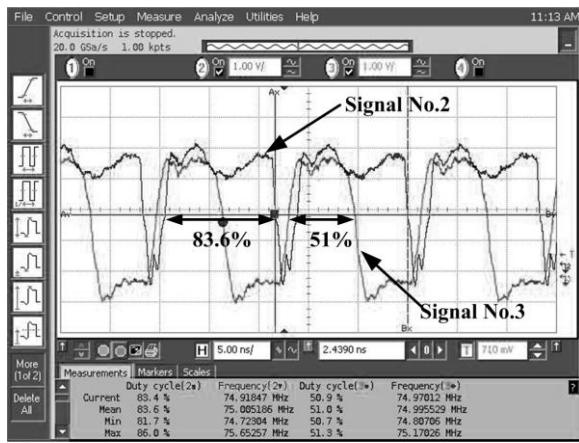
(b)

Fig. 19. Phase alignment measurement at 75 MHz with (a) 19.7% and (b) 83.6% input duty cycles.

duty-cycle correction applications

NF: Normalized Frequency $= F \times \dfrac{\text{Technology}}{0.09}$

NP: Normalized Power

$$= P \times \left(\frac{0.09}{\text{Technology}}\right) \times \left(\frac{1.0}{VDD}\right) \times \frac{734}{F_{\max}}$$

PBR: Power Bandwidth Ratio $= \text{NP} \div \left(\dfrac{\text{NF}_{\max}}{\text{NF}_{\min}}\right). \qquad (8)$

VI. CONCLUSION

A wide-range and low-cost ADDCC is presented in this paper. The proposed ADDCC uses delay-recycled architecture to reduce the delay line length to half of the reference clock period. Thus, the area cost is lower than other DCCs. In addition, the proposed ADDCC can achieve a wide-range operation with an input frequency ranging from 75 to 734 MHz and the input duty-cycle ranges from 9% to 86%, so it can be integrated into the SoC to correct duty-cycle error. Furthermore, the proposed ADDCC still works at unbalanced process corners, and it is therefore suitable for SoC applications.

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