A Low-Cost Low-Power All-Digital Spread-Spectrum Clock Generator

Ching-Che Chung, Duo Sheng, and Wei-Da Ho

***Abstract*— In this brief, a low-cost low-power all-digital spread-spectrum clock generator (ADSSCG) is presented. The proposed ADSSCG can provide an accurate programmable spreading ratio with process, voltage, and temperature variations. To maintain the frequency stability while performing triangular modulation, the fast-relocked mechanism is proposed. The proposed fast-relocked ADSSCG is implemented in a standard performance 90-nm CMOS process, and the active area is 200 μm × 200 μm. The experimental results show that the electromagnetic interference reduction is 14.61 dB with a 0.5% spreading ratio and 19.69 dB with a 2% spreading ratio at 270 MHz. The power consumption is 443 μW at 270 MHz with a 1.0 V power supply.**

***Index Terms*— All-digital phase-locked loops (ADPLLs), electromagnetic interference (EMI) reduction, oscillators, spread-spectrum clock generator (SSCG).**

I. Introduction

The problem of electromagnetic interference (EMI) has become increasingly important in the recent years. A high-speed data transmission usually causes severe EMI, and this influences the operation of neighboring circuits. Hence, to overcome these noises, spread-spectrum clock generators (SSCGs) [1], [3]–[14] are proposed to reduce the EMI at a relatively low cost and a relatively simple design. There are several devices that have the defined specifications to restrict the EMI with a SSCG, such as DisplayPort [2], [3], which is a digital display interface and serial advanced technology attachment, which is a storage interface.

There are several modulation methods of SSCGs. Some SSCGs directly modulate the voltage controlled oscillator (VCO) [4] or the digitally controlled oscillator (DCO) [5] to achieve a spread spectrum. This modulation method can provide better EMI reduction performance, and it is a relatively simple modulation method to implement a SSCG. However, this approach usually requires a very large on-chip capacitor as a loop filter and occupies a relatively large chip area [6].

Although an all-digital SSCG (ADSSCG) with DCO modulation and a frequency maintenance mechanism is proposed in [7], this approach causes large cycle-to-cycle jitters due to the rescheduling division triangular modulation. The other digital approach uses a digitally controlled delay-line (DCDL) cascaded with the all-digital phase-locked loop (ADPLL) to realize the ADSSCG [8]. Nevertheless, the operation of DCDL is set at a high frequency, and thus, this architecture consumes more power.

To perform spread spectrum at a high frequency and keep the entire operation stable, most prior researches adopt a dual-modulus frequency divider with the spread-spectrum controller in SSCG [9], [12]. This modulation method occupies a smaller area and its cost is comparable with that of the other modulation methods. However, since the PLL still tracks the phase and frequency of the reference clock during the triangular profile generation the generated modulation profile is probably flatter than the ideal triangular modulation profile [12]. This phenomenon may decrease the EMI reduction effect. In addition, the bit number of the triangular profile generator, the bit number of the accumulator of the delta–sigma modulator (DSM), and the division ratio of the PLL, also cause the error in the spreading ratio.

The spreading ratio is a key point to decide the EMI reduction performance. The programmable spreading ratio can make a SSCG relatively flexible. With various spreading ratios, the SSCG can change conditions to achieve the required EMI reduction with process, voltage, and temperature (PVT) variations. For a given spreading ratio, the energy spreading can be optimized with different modulation frequencies. It is shown that the optimal results can be achieved with a modulation frequency close to the resolution bandwidth (RBW) used to evaluate the spectrum [11].

For directly controls the oscillator method [5], irrespective of whether this method controls the DCO by changing the control code ratio or it controls the VCO by changing the voltage control gain to achieve the programmable spreading ratio, its implementation is relatively simple. However, it cannot maintain the same spreading ratio if there exist PVT variations.

In this brief, an ADSSCG is presented with a direct modulation on DCO. The proposed ADSSCG with the fast-relocked scheme can avoid the nominal frequency drift in the spread-spectrum state, and realize an accurate triangular modulation profile. A digital loop filter (DLF) is proposed to enhance the lock-in time and shorten the relock time in the spread-spectrum state. To achieve the correct programmable spreading ratio with PVT variations, we propose a truly programmable spreading ratio decision method to determine the corresponding spreading range (SR). A DSM with the DCO can enhance the DCO resolution, and thus, the direct modulation on the DCO can generate a smooth triangular modulation on the output frequency. In addition, most ladder-shaped DCOs have nonmonotonic problems, and these may induce a relatively poor EMI reduction performance because of the overlapped subfrequency bands. Therefore, a low-power monotonic DCO [16] is used. Finally, the proposed ADSSCG is designed using standard cells. Hence, it is very suitable for system-on-a-chip (SoC) applications.

The rest of this brief is organized as follows. The architecture of the proposed ADSSCG is introduced in Section II. The experimental results are reported in Section III. Finally, Section IV presents the conclusion.

II. Proposed ADSSCG

The block diagram of the proposed ADSSCG is shown in Fig. 1. This ADSSCG is composed of a phase and frequency detector (PFD), a spread-spectrum clock (SSC) controller, a spreading ratio detector, a DLF, a DSM, a low-power monotonic DCO, and a frequency divider. The proposed ADSSCG uses the modulation method on DCO. Therefore, the SSC controller directly controls the DCO control code (control_code) to perform the center-spread triangular modulation on

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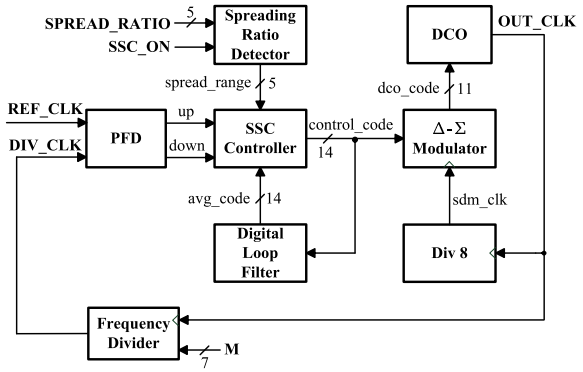

Fig. 1. Block diagram of proposed ADSSCG.

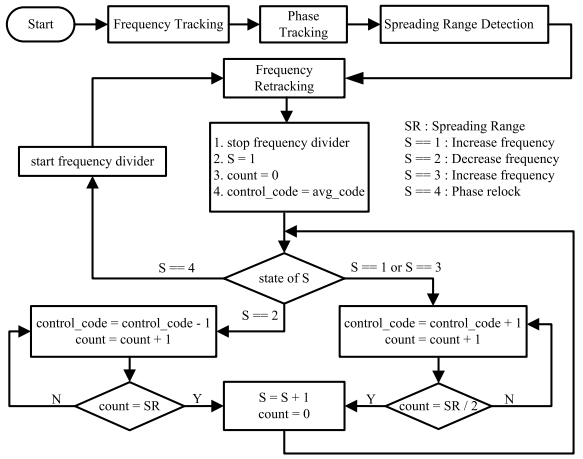

Fig. 2. Flowchart of the proposed ADSSCG.

the output frequency. According to the SR (spread_range), which is calculated from spreading ratio detector, the SSC controller modulates the output frequency to achieve the corresponding spreading ratio. The proposed spreading ratio detector is for finding the SR with the proposed truly programmable spreading ratio decision method.

To generate a smooth triangular modulation profile, the DCO resolution is further enhanced by employing a DCO dithering scheme through a 3-bit first-order DSM. The integer part of the DCO control code has 11-bit, and the fractional part of the DCO control code has 3 bit. The DLF is applied in the ADSSCG to generate a stable average frequency to eliminate the jitter effects of the reference clock. The DLF can generate a 14-bit baseline DCO control code (avg_code) for the SSC controller. Thus, the SSC controller can keep updating the triangular modulation profile with PVT variations. The monotonic DCO [16] is applied to overcome the nonmonotonic phenomenon when the spread-spectrum function is active.

The flowchart of the proposed ADSSCG is shown in Fig. 2. After the system is reset, the SSC controller starts the frequency tracking. To increase the frequency tracking speed, this state is searched by only adjusting the coarse-tuning code until the coarse step is converged into one coarse-tuning code. After the frequency tracking is complete, the phase tracking is started. The phase tracking searches for the correct frequency with fine-tuning code adjustment. When the fine-tuning step is converged into one fine-tuning code, the DSM is started. Because the DSM is used for enhancing the DCO resolution to the third digit after the decimal point, the baseline DCO control code which is provided from DLF, is important in this state for enhancing the lock-in speed.

When the frequency tracking and the phase tracking are complete, the spread-spectrum function is turned ON, and the detection of the SR is started by the spreading ratio detector, which will be described later. The modulation type of the proposed ADSSCG is center-spread, and the modulation frequency ($f_{\rm m}$) of the proposed ADSSCG is related to the frequency of the reference clock and the SR. There are four stages in the spread-spectrum state. Before starting the first stage (S == 1), the frequency divider is stopped, and then, the other parameters are initialized. The first stage (S == 1) is spread up the frequency with the (SR/2) control codes. The second stage (S == 2) is spread down the frequency with the SR control codes. The third stage (S == 3) is spread up the frequency with the (SR/2) control codes again. Finally, the fourth stage (S == 4) enables the frequency divider and starts performing the fast-relock mechanism. After the fourth stage is finished, the new triangular modulation cycle is continued.

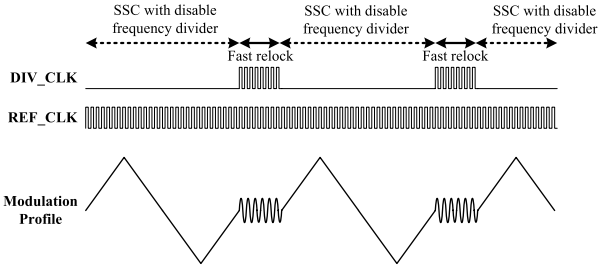

Fig. 3. Modulation profile with fast-relocked mechanism.

A. Spread Spectrum With Fast-Relocked Mechanism

When SSCG is in the spread-spectrum state, it does not have external information to maintain the average frequency. This may influence the nominal frequency, especially for the modulation method on DCO/VCO. The SSCG probably faces PVT variations in the spread-spectrum state, and the nominal frequency may be changed if there is no mechanism to retrack the frequency.

One of the possible approaches to avoid the frequency drift is to retrack the correct nominal frequency. Fig. 3 shows the proposed method, which disables the frequency divider during the triangular modulation and enables it at the beginning of the frequency retracking. We can see that the frequency divider is disabled when the ADSSCG starts to perform the spread-spectrum generation. Subsequently, at the end of one modulation cycle, the frequency divider is triggered by the reference clock for the enabled operation. Then, the frequency divider starts up the divided clock immediately. Therefore, the phase error between the reference clock and divided clock is cancelled. After the frequency relock is complete, the frequency divider is disabled again and the new modulation cycle is continued.

B. Digital Loop Filter

For an ADPLL, the frequency and phase tracking is realized by adjusting the DCO control code by the controller. After ADPLL is locked, the baseline control code can prevent the frequency drift if there is a sever jitter on the reference clock suddenly. As a result, it is very important to acquire the correct baseline control code as fast as possible. Hence, we propose a DLF [15] to maintain the baseline control code. The detailed operation of baseline control code maintenance is described in the flowchart shown in Fig. 4.

There are six registers of T0, T1, T2, T3, T4, and T5 in the proposed DLF to store the DCO control codes. In Fig. 4, the first two states save two current DCO control codes to T4 and T5 in two cycles. In the third state, the maximum and minimum DCO control codes in T0–T5 are removed, and then, the other codes are saved

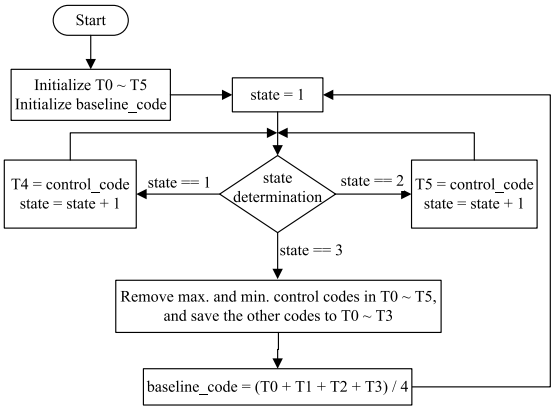

Fig. 4. Flowchart of baseline control code maintenance.

to the T0–T3. Then, the average DCO control code of T0–T3 is calculated and outputted as the baseline control code.

By obtaining the baseline control code, the ADSSCG cannot only shorten the duration of frequency and phase tracking but also reduce the reference clock jitter effects. The DCO control code (control_code [13:0]) will make a pullback if the up–down polarity of the PFD occurs in the frequency and phase tracking state. Therefore, this technique can reduce the lock-in time, and make the frequency tracking more stable.

C. Truly Programmable Spreading-Ratio Decision Method

For the modulation method on DCO, the spreading ratio (S_{ratio}) of the ADSSCG depends on the SR (S_{range}), the DCO fine-tuning resolution (R_{f}), and T_{target}, where T_{target} is the clock period of the target frequency. Among these parameters, DCO resolution is the most important parameter for determining the spreading ratio, and it is sensitive to the PVT variations. This is why most SSCGs cannot provide a correct spreading ratio with PVT variations.

Therefore, we propose a novel method to decide the correct SR with a corresponding spreading ratio. The proposed truly programmable spreading ratio decision method adopts the cycle count difference to determine the current DCO resolution. After R_{f} is decided, the correct spreading ratio can be realized with an appropriate SR. For example, the correct SR can be calculated (1) if the DCO resolution is 2.5 ps and the spreading ratio is set to 1%

$$\begin{aligned} S_{\text{range}} &= \frac{S_{\text{ratio}} \times T_{\text{target}}}{R_{\text{f}}} \\ &= \frac{1\% \times \frac{1}{270\ \text{MHz}}}{2.5\ \text{ps}} \\ &= \frac{1\% \times 3703\ \text{ps}}{2.5\ \text{ps}} \\ &= 14.812. \end{aligned} \tag{1}$$

The SR calculated from (1) is 14.812. To avoid over spreading, a floor function is added to this equation. Therefore, the calculated SR is 14 DCO control codes with the conditions of 1% spreading ratio, 2.5 ps DCO resolution, and 270 MHz output frequency.

The timing diagram of the proposed spreading ratio decision method is shown in Fig. 5. In the proposed ADSSCG, the DCO is composed of a coarse-tuning stage and a fine-tuning stage [16]. In addition, one coarse-tuning resolution (R_{c}) is equal to 32 times the fine-tuning resolution (R_{f}). In Fig. 5, after phase tracking, we add 256 (={6'h1, 5'h0, 3'h0}) to the DCO control code to represent the addition of one coarse-tuning code. After the cycle

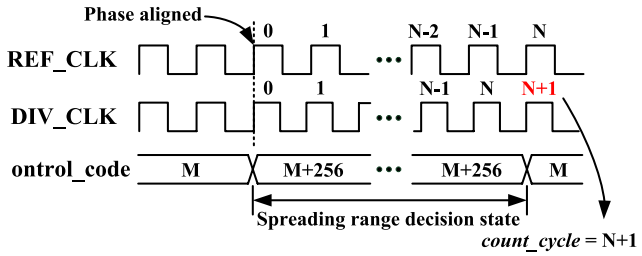

Fig. 5. Timing waveform for the calculation of the SR.

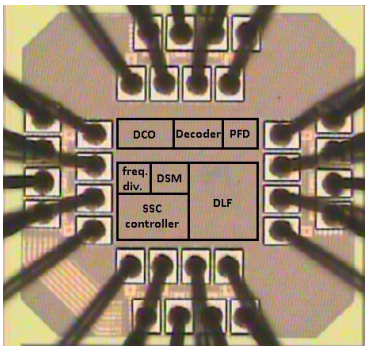

Fig. 6. Microphotograph of the proposed ADSSCG.

count difference between REF_CLK and DIV_CLK is more than one cycle, we obtain the accumulated cycle count (count_cycle). With the count_cycle, the current coarse-tuning resolution can be calculated.

For instance, if we obtain the number of count_cycle, then the percentage of the coarse-tuning resolution (R_{c}) for the clock period (T_{target}) is calculated using $R_{\text{c}}/T_{\text{target}} = 1/\text{count\_cycle}$. The percentage of the fine-tuning resolution (R_{f}) for the clock period (T_{target}) can be calculated using $R_{\text{f}}/T_{\text{target}} = 1/(32 \times \text{count\_cycle})$. Then, the spreading range can be calculated using $S_{\text{range}} = S_{\text{ratio}} \times (T_{\text{target}}/R_{\text{f}}) = 32\times\ \text{count\_cycle} \times S_{\text{ratio}}$. The numerator and the denominator can both be multiplied by ratio_code to obtain (2), where ratio_code is the input spreading ratio code. We set the product of S_{ratio}/ratio_code and the number 32 to be a new constant const and derive (3) from (2). The value of const is determined by S_{ratio}/ratio_code, which is the percentage of one spreading ratio code for the spreading ratio. To simplify (3), we set const to be 1/16. Therefore, the value of the S_{ratio}/ratio_code is $1/(16 \times 32) = 0.1953125\%$, and this number is close to 0.2%

$$S_{\text{range}} = 32 \times \frac{S_{\text{ratio}}}{\text{ratio\_code}} \times \text{ratio\_code} \times \text{count\_cycle} \tag{2}$$

$$S_{\text{range}} = \text{const} \times \text{ratio\_code} \times \text{count\_cycle}. \tag{3}$$

Equation (3) is available for up-spread or down-spread. However, the proposed ADSSCG performs the spread spectrum with the center-spread. The spreading range should be an even number for the center-spread. Hence, the spreading range calculated from (3) should be divided by 2. Then, a floor function should be added, and the SR is multiplied by 2 to obtain an even number, as shown in

$$S_{\text{range}} = \left\lfloor (\text{ratio\_code} \times \text{count\_cycle}) \times \frac{1}{32} \right\rfloor \times 2. \tag{4}$$

Equation (4) is the final equation, and this equation can be implemented at a relatively low-circuit cost. For example, if the cycle count (count_cycle) is 39 and the required spreading ratio is 1.953125%, which means the ratio_code should be set to 10. Then, the SR is

TABLE I
PERFORMANCE COMPARISONS

	2011 TCAS2 [3]	2008 TCAS1 [6]	2003 JSSC [4]	2010 JSSC [11]	2009 JSSC [12]	This work
Process	0.18μm	0.35μm	0.35μm	65nm	0.18μm	90nm
Modulation profile	Triangular	Triangular	Triangular	Arbitrary	Triangular	Triangular
Modulation method	VCO modulation	VCO modulation	VCO modulation	Digital delay-line	ΔΣ ADPLL	DCO modulation
Compensation for spreading ratio error	Yes	No	No	No	No	Yes
EMI reduction (dB)	8.75dB (0.5%) @270MHz	16.3dB (1.5%) @400MHz	11dB (2.5%) @266MHz	20.5dB (6%) @750MHz	10.48dB (0.5%) @1500MHz	14.61dB (0.5%) @270MHz 19.69dB (2%) @270MHz
Output frequency (MHz)	162~270	400	266	180~1270	1500	270
Maximum f_m	33kHz	40kHz	40kHz	5MHz	31kHz	70kHz
Chip area (mm^2)	1.8	0.656	2	0.044*	0.2	0.04
Power consumption (mW)	19 @ 270MHz	27.5 @ 400MHz	300 @ 266MHz	44 @ 1270MHz*	15 @ 1500MHz	0.443 @270MHz
Rms jitter (ps)	4.7	10.2	19.0	12.8	4.0	17.4

*: without PLL

calculated using

$$S_{\text{range}} = \left\lfloor (10 \times 39) \times \frac{1}{32} \right\rfloor \times 2 = 24. \quad (5)$$

From (5), the SR is calculated as 24. This implies that we should spread 24 DCO codes to achieve the 1.953125% spreading ratio with the current DCO resolution. Therefore, for the center-spread spread-spectrum operation, the SR shown in Fig. 2 should be set to 24 to achieve the required spreading ratio.

Equation (4) looks like it requires three multiplications and one division to get the result. This equation will not require any multiplication and division operation. First, the division of 1/32 and multiplication of 2 can be realized with a shifting operation. The product of ratio_code × count_cycle can be calculated by accumulating ratio_code in count_cycle cycles; thus, this operation can be implemented with addition operations. With the proposed truly programmable spreading ratio decision method, we achieve the spread spectrum with the correct spreading ratio with PVT variations. Moreover, the complex calculation is simplified to save the circuit area cost.

III. EXPERIMENTAL RESULT

The microphotograph of the proposed ADSSCG is shown in Fig. 6. This ADSSCG is designed using standard cells in a standard 90-nm CMOS technology. The core area is 200 μm^2 × 200 μm^2, and the measured power dissipation is 443 μW at 270 MHz. The measured power spectrum density (PSD) of the proposed ADSSCG without spread spectrum at 270 MHz output frequency with a 1.0 V power supply is shown in Fig. 7(a). In Fig. 7, the RBW is set to 100 kHz, and the video bandwidth is also 100 kHz. The peak power is −2.47 dBm at 270 MHz without spread spectrum.

After the proposed ADSSCG is locked, the peak power of the output clock can be reduced. In Fig. 7(b), it shows the EMI reduction with a 2.0% spreading ratio is 19.69 dB. When the spreading ratio is set to 0.5%, the EMI reduction is 14.61 dB, as shown in Fig. 7(c). Because the proposed fast-relocked mechanism can keep tracking the reference clock, there is no frequency drift in these figures.

Fig. 7(c) shows the power spectral density with a 0.5% spreading ratio and a 1.0 V power supply at 270 MHz. Because the truly programmable spreading ratio decision method is adopted, the power spectral density looks very similar in Fig. 7(d) with a 0.9 V power supply and Fig. 7(e) with a 1.1 V power supply. Therefore, the proposed ADSSCG can tolerate PVT variations and produces the output frequency with the desired spreading ratio under PVT variations. The root-mean-square jitter and peak-to-peak (P_K–P_K) jitter at 270 MHz without spread-spectrum operation is 17.4 and 128.4ps, respectively.

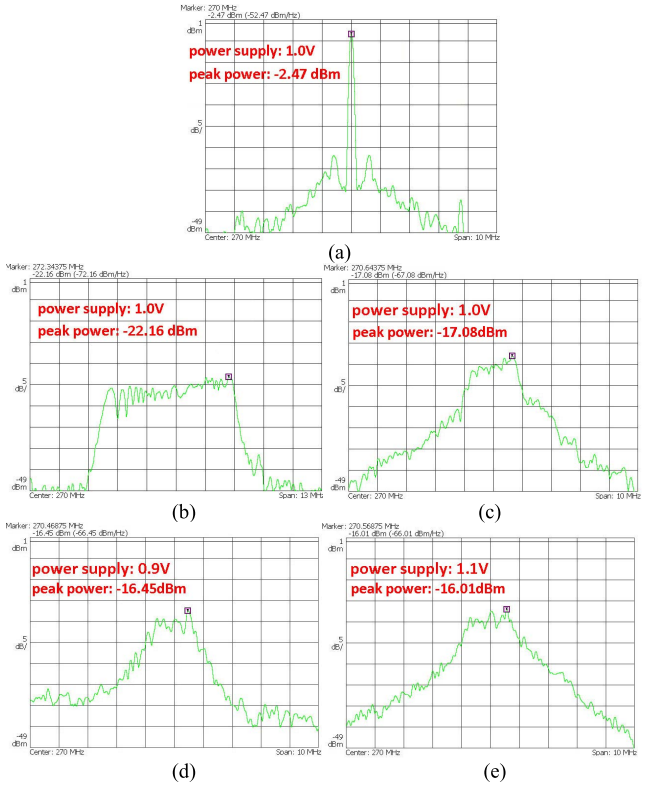

Fig. 7. PSD of (a) spread-spectrum OFF, (b) 2.0% spreading ratio, (c) 0.5% spreading ratio with a 1.0 V power supply, (d) 0.5% spreading ratio with a 0.9 V power supply, and (e) 0.5% spreading ratio with a 1.1 V power supply.

To highlight the characteristics of the proposed ADSSCG, we present a comparison table, as shown in Table I. From this comparison table, we see that the proposed ADSSCG consumes the lowest power

consumption. Moreover, because of the all-digital approach, our core area occupies the smallest area. Further, even for the EMI reduction with a 0.5% spreading ratio, the proposed ADSSCG shows the best performance. In addition, the proposed truly programmable spreading ratio decision method can calculate the current DCO resolution with PVT variations and then compensate for the spreading ratio error.

IV. Conclusion

In this brief, we presented several solutions to build an ADSSCG to maintain frequency stability while performing the spread-spectrum operation. The proposed fast-relocked ADSSCG can provide an accurate triangular modulation profile and achieve a high EMI reduction performance. Moreover, the proposed ADSSCG can provide an accurate programmable spreading ratio under different PVT variations. Therefore, the proposed ADSSCG is suitable for SoC applications.

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