Built-in Self-Calibration Circuit for Monotonic Digitally Controlled Oscillator Design in 65-nm CMOS Technology

Ching-Che Chung, *Member, IEEE*, Chiun-Yao Ko, and Sung-En Shen

***Abstract*—This brief presents a built-in self-calibration (BISC) circuit to correct nonmonotonic responses in a digitally controlled oscillator (DCO) with a cascading structure. Generally speaking, a cascading DCO structure has the advantages of low power consumption and a small chip area. Nevertheless, when a subfrequency band is changed, an overlap region between subfrequency bands causes a large phase error and cycle-to-cycle jitter in an output clock. The proposed BISC circuit can reduce this problem; thus, it is very suitable for a low-power all-digital phase-locked loop design in system-on-a-chip applications. The proposed DCO, implemented with a standard performance 65-nm complementary metal–oxide–semiconductor process, can output frequency ranges from 47.8 to 538.7 MHz. The total power consumption of the DCO with a calibration circuit is 0.142 mW at 58.7 MHz and 0.205 mW at 481.6 MHz.**

***Index Terms*—Calibration, clocks, delay lines, digital phase-locked loops (PLLs), jitter, oscillators.**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in many communication systems such as on-chip clock generators, clock and data recovery circuits, and frequency synthesizers. Traditionally, PLLs are often designed with charge pump-based architecture [1], [2]. However, charge-pump-based PLLs suffer from a serious leakage current problem in a 65-nm complementary metal–oxide–semiconductor (CMOS) process. Thus, jitter performance becomes unacceptable due to ripples in control voltage. Hence, all-digital PLLs [3]–[6], [10], which use robust digital control codes to control digitally controlled oscillators (DCOs), can avoid the leakage current problem, and they have become more and more popular now.

A DCO is the most critical component in an all-digital phase-locked loop (ADPLL). Almost 50% of the area and power consumption of an ADPLL is occupied by a DCO. Therefore, determining how to design DCOs with low power consumption, a small chip area, and sufficient frequency resolution is very important. In order to achieve both a wide frequency range and high resolution with a smaller chip area and lower power consumption, a cascading structure is often used in designing DCOs [3], [5], [7]–[9]. In these DCOs, a coarse-tuning stage, which uses large delay cells to achieve wide-range delay control, is accompanied with a fine-tuning stage to improve the resolution of the DCOs, as shown in Fig. 1(a).

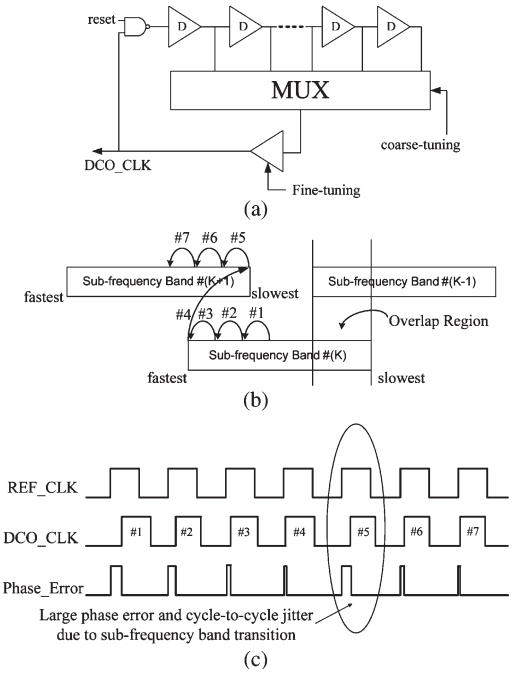

Fig. 1. (a) Cascading structure DCO. (b) Frequency allocation of the DCO. (c) Transition between subfrequency bands.

Frequency allocation of a DCO is illustrated in Fig. 1(b). In the cascading architecture, there are overlap regions between subfrequency bands to make sure that there will not be any frequency dead zones in the DCO with process, voltage, and temperature (PVT) variations. The overlap region makes DCO's output frequencies nonmonotonic with DCO control codes. Fig. 1(c) shows an example for phase tracking with the cascading DCO structure. In the beginning, the subfrequency band #(K) is selected, and an ADPLL controller keeps increasing the output frequency of the DCO to reduce the phase error between REF_CLK and DCO_CLK. In the fourth DCO_CLK cycle, output frequency reaches the fastest frequency output of the subfrequency band #(K). Thus, the output frequency jumps to the slowest frequency output of the subfrequency band $\#(\mathrm{K}+1)$. However, when the subfrequency band is changed, the phase error and the cycle-to-cycle jitter at that cycle become very large due to the DCO's nonmonotonic response.

Manuscript received September 5, 2010; revised November 11, 2010; accepted January 16, 2011. Date of current version March 16, 2011. This work was supported in part by the National Science Council of Taiwan under Grant NSC97-2218-E-194 -009-MY2. This paper was recommended by Associate Editor A. Liscidini.

The authors are with the Department of Computer Science and Information Engineering, National Chung Cheng University, Chiayi, Taiwan (e-mail: wildwolf@cs.ccu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2011.2110370

To reduce phase errors and cycle-to-cycle jitter in cascading structure DCOs, a coarse-tuning DCO control code should be determined in a frequency search step and fixed after the frequency search is done. Then, the ADPLL controller only adjusts a fine-tuning DCO control code to fine-tune the output frequency and keeps tracking the phase of the reference clock in a selected subfrequency band. In most applications, if there is an enough fine-tuning controllable range, the ADPLL works fine with this two-step DCO control code selection process. However, in spread spectrum clock generator (SSCG) applications [5], [6], triangular modulation on a DCO control code often makes it necessary to change the coarse-tuning DCO control code after the frequency search has been done. In addition, if the reference clock is very noisy, the ADPLL also needs to change the coarse-tuning DCO control code to track the phase of the reference clock.

Therefore, an SSCG [6] uses a single-stage DCO to avoid this problem. However, power consumption and chip area have become very large due to the single-stage architecture. A phase selection DCO [4] is another solution, using a free-running multiphase DCO to achieve wide-range operation without cascading DCO architecture. Nevertheless, a high-speed asynchronous control block in the phase selection DCO consumes a large amount of power and requires a large chip area. In [10] and [11], a DCO, which uses interpolators to generate a fine-tuning delay between two coarse-tuning delays, is presented to remove the overlapped region between subfrequency bands. However, a short-circuit current of an interpolator greatly increases the power consumption of the DCO. To achieve better portability over different processes and for low-power applications without steady power consumption, the cascading DCO architecture is still a better choice.

In this brief, a cell-based DCO with a built-in self-calibration (BISC) circuit to overcome the nonmonotonic response problem in the cascading DCO structure is presented. The mechanism of self-calibration decides the compensation code for DCO fine-tuning control codes when coarse-tuning control codes are changed. The proposed self-calibration method can guarantee a monotonic response for the DCO, and therefore, the advantages of using the cascading DCO structure can be retained.

This brief is organized as follows. The proposed DCO with a BISC circuit is discussed in Section II. The implementation of the proposed design using a standard performance (SP) 65-nm CMOS process is presented in Section III. Section IV shows the experimental results of the test chip. Finally, Section V concludes with a summary.

II. BISC Circuit

In cascading structure DCOs [3], [5], [7]–[9], a DCO has an overlap region between subfrequency bands. Fig. 2 shows a transition between subfrequency bands in the cascading DCO structure. In Fig. 2, the DCO control code is noted as (coarse-tuning code, fine-tuning code). Since the fine-tuning code has N bits, the highest possible value for the fine-tuning code is $(2^N - 1)$. If the current coarse-tuning code is (K) and the fine-tuning control code reaches the maximum value $(2^N - 1)$, the output frequency will be at the fastest frequency output of the subfrequency band #(K). However, if the ADPLL controller still needs to increase the output frequency, the coarse-tuning code is changed to $(\mathrm{K} + 1)$, which means that the subfrequency band is changed to $\#(\mathrm{K} + 1)$, and the fine-tuning code is reset to zero to provide the slowest frequency output of the subfrequency band $\#(\mathrm{K} + 1)$.

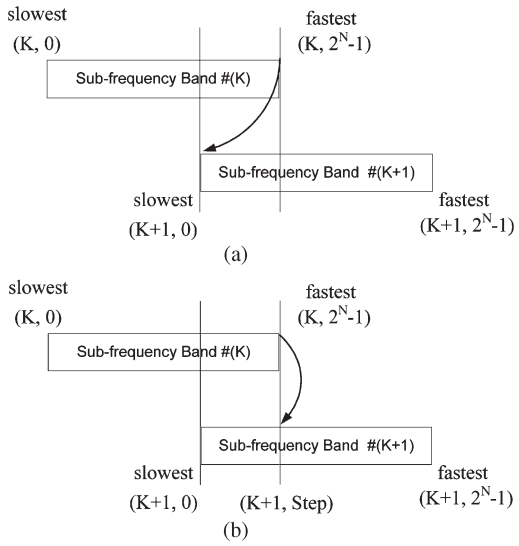

Fig. 2. Subfrequency band transition (a) without a compensation code and (b) with a compensation code.

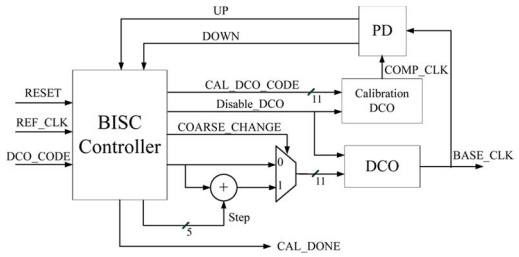

Fig. 3. Proposed DCO with the BISC circuit.

The slowest frequency output of the subfrequency band $\#(\mathrm{K} + 1)$ is slower than the fastest frequency output of the subfrequency band #(K). The nonmonotonic increasing characteristic of the cascading DCO structure causes a large phase error and cycle-to-cycle jitter during subfrequency band transitions. To avoid this problem, compensation codes should be added to the fine-tuning control code if there are changes in the coarse-tuning control code. In Fig. 2(b), a compensation code (Step[4:0]) is added to the fine-tuning control code so that the monotonic increasing characteristic can still be retained. Therefore, the DCO control code is changed from $(\mathrm{K}, 2^N - 1)$ to $(\mathrm{K} + 1, \mathrm{Step})$ to provide an output frequency that is faster than the frequency output with the DCO control code $(\mathrm{K}, 2^N - 1)$.

The compensation code (Step[4:0]) can be determined by circuit simulation. However, a fixed compensation code is not suitable for an ADPLL with different PVT variations. Therefore, in this brief, a BISC circuit is proposed to calculate the compensation code for current operation conditions. Fig. 3 shows the overall architecture of the proposed DCO with a BISC circuit. The BISC circuit is composed of a phase detector (PD), a "calibration DCO," and a BISC controller.

The "calibration DCO" is the same as the DCO. Thus, the BISC controller can use these two DCOs to calculate the

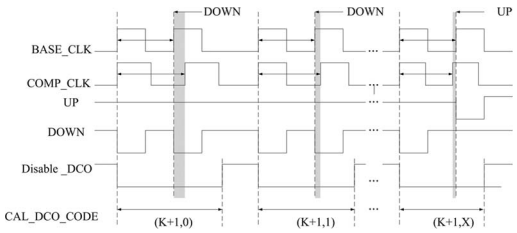

Fig. 4. Timing diagram of the BISC circuit.

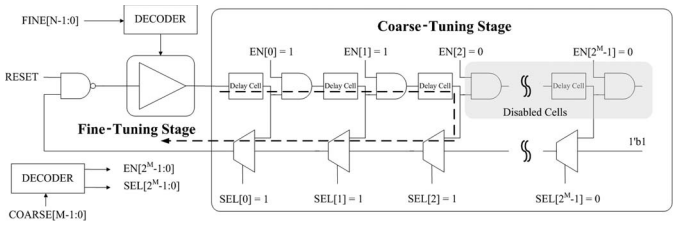

Fig. 5. Coarse-tuning stage of the proposed DCO.

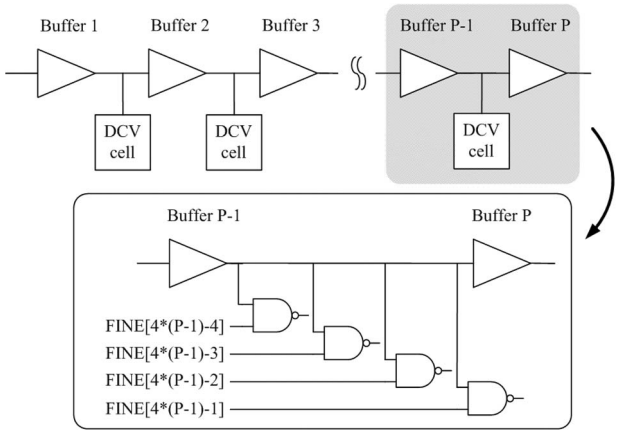

Fig. 6. Fine-tuning stage of the proposed DCO.

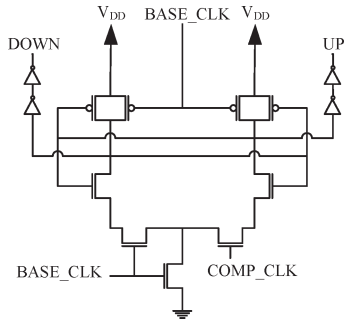

Fig. 7. PD in the calibration circuit.

compensation code. The calibration circuit starts to work when the system is reset. After calibration is finished, the compensation code is determined, and then, the ADPLL starts its normal operation. Furthermore, if operating voltage or chip's temperature changes after the initial calibration, the BISC circuit can be restarted to calculate the compensation code for current operation conditions.

After the calibration is done, the "calibration DCO" and the PD are disabled, and the DCO control code DCO_CODE, which inputs to the DCO, is sent to the BISC controller to detect if there has been any changes in the coarse-tuning control code. Then, the compensation code (Step[4:0]) for the DCO fine-tuning control code is added to the current input DCO control code to ensure the monotonic response of the DCO during subfrequency band transitions. If the coarse-tuning control code is not changed, the DCO control code (DCO_CODE) is bypassed to the DCO.

The operation of the proposed BISC circuit is illustrated in Fig. 4. The DCO's output clock BASE_CLK and the calibration DCO's output clock COMP_CLK are compared with the PD. In the beginning of the calibration process, DCO_CODE: $(\mathrm{K}, 2^N - 1)$ is applied to the DCO, and CAL_DCO_CODE: $(\mathrm{K}+1, 0)$ is applied to the "calibration DCO."

Since there are overlapped regions between the subfrequency bands, the output frequency of the "calibration DCO" is always slower than the DCO in the beginning of the calibration process, and COMP_CLK lags behind BASE_CLK. The signal "Disable_DCO" is used to reset the two DCOs after each phase comparison, thus allowing the PD to be used to detect the frequency error between the two DCOs. The PD outputs UP and DOWN signals to indicate that the frequency output of the DCO is faster or slower than the frequency output of the "calibration DCO." The BISC controller keeps increasing the fine-tuning DCO control code of the "calibration DCO" until COMP_CLK leads BASE_CLK. Then, the compensation code for the current operation conditions can be determined, and value X, shown in Fig. 4, is saved as the fine-tuning compensation code (Step[4:0]); therefore, the calibration process is completed.

III. Test Chip Architecture

Fig. 5 shows the architecture of the proposed DCO in a test chip. The DCO is composed of coarse-tuning and fine-tuning stages. The coarse-tuning stage, which has $(2^M - 1)$ delay cells with $(2^M - 1)$ multiplexers, can provide 2^M different delays. In order to generate a sufficient delay time in a 65-nm CMOS process, the delay cells in the cell library are used to build up the coarse-tuning stage. In addition, two-input AND gates are added to each delay cell's output to disable unused cells and save power consumption.

Fig. 6 shows the DCO's fine-tuning stage. To achieve better DCO resolution, digital-controlled varactors [3], [5], [7]–[9] are used in the fine-tuning stage. The fine-tuning stage has P buffers, and in each buffer, it connects to four NAND gates. When the fine-tuning control code $(\mathrm{FINE}[4^*(P-1)-1:0])$ is changed, capacitance in the buffer's output node is also changed. Therefore, a high-resolution fine-tuning delay stage with good linearity can be created.

Since in the proposed DCO, the coarse-tuning stage has a very regular structure with good linearity in the output delay control, the overlap regions in different subfrequency bands are almost the same. As a result, we can create the "calibration DCO" with a fixed coarse-tuning control code K. Thus, the unused delay cells and two-to-one multiplexers can be eliminated to reduce the area cost of the "calibration DCO." In the calibration process, the BISC controller only detects the compensation code between subfrequency bands #(K) and $\#(\mathrm{K}+1)$, and the compensation code for other subfrequency bands uses the same compensation code to reduce calibration cost.

Fig. 7 shows the schematic of the PD [3] used in the calibration circuit. The principle of the PD is to determine which of

TABLE I
PROPERTIES OF THE DCO

	Chip Meas.	PostSim TT	PostSim FF	PostSim SS
Coarse-Tuning Step (ps)	292	289	209	466
Fine-Tuning Range (ps)	558	566	439	833
Average Resolution (ps)	17.4	18	14	27
Max. Frequency (MHz)	538.7	610.1	839.1	383.6
Min. Frequency (MHz)	47.8	49.0	67.5	30.5
Compensation code	20	17	18	15

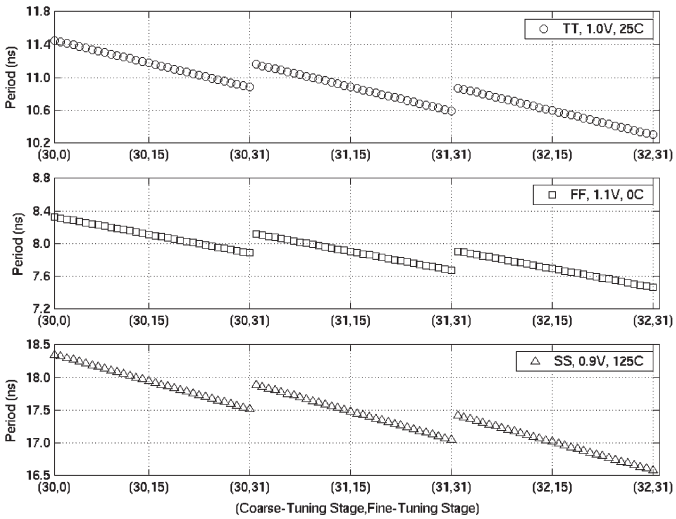

Fig. 8. Output period of the noncalibrated DCO.

the rising edges (the one in the BASE_CLK or the one in the COMP_CLK) occurs later. This PD has a dead zone about 1 ps in 65-nm CMOS process. This is sufficient to detect a tiny phase difference in the phase comparison. In this brief, two additional inverters are added at the output ports of the PD to increase driving capacity.

The other circuits such as the BISC controller are written with hardware description language, and then, the cell-based design flow is used to implement the full test chip.

IV. EXPERIMENTAL RESULTS

The test chip is implemented with a SP 65-nm CMOS process. The design parameters of this test chip are determined as follows: $M = 6$, $N = 5$ and $P = 9$. This means that the proposed DCO has 64 coarse-tuning steps in the coarse-tuning stage and 32 fine-tuning steps in the fine-tuning stage.

Table I shows the properties of the proposed DCO in chip measurement and in postlayout simulation with PVT variations. The compensation code, which is calculated by the proposed BISC circuit, varies with different PVT conditions. In addition, the fine-tuning range is always larger than the coarse-tuning step with different PVT conditions. The measurement results show that the DCO can output frequency ranges from 47.8 to 538.7 MHz. In addition, the resolution in the proposed DCO is about 17.4 ps, determined from our chip measurement results.

Fig. 8 shows the simulation results of the DCO's output period versus the DCO control code in the noncalibrated DCO with PVT variations. Because the subfrequency bands are overlapped, the DCO output clock period does not monotonically

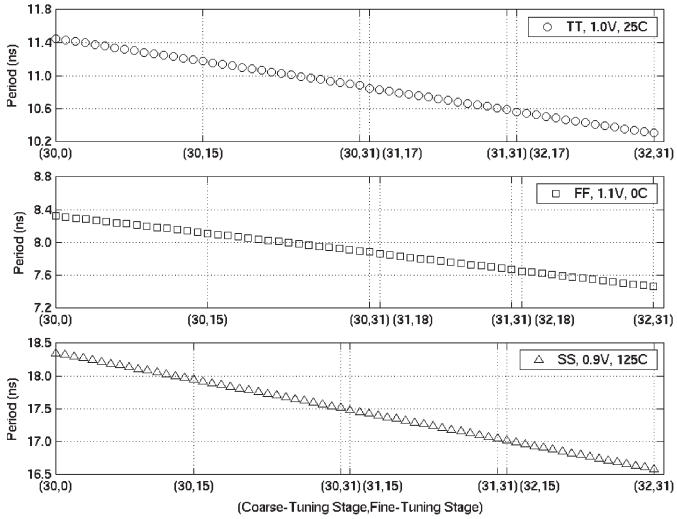

Fig. 9. Output period of the calibrated DCO.

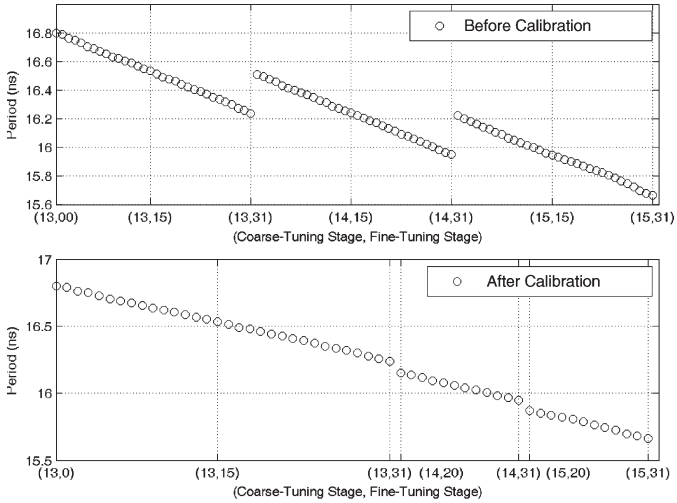

Fig. 10. Measurement results of the DCO.

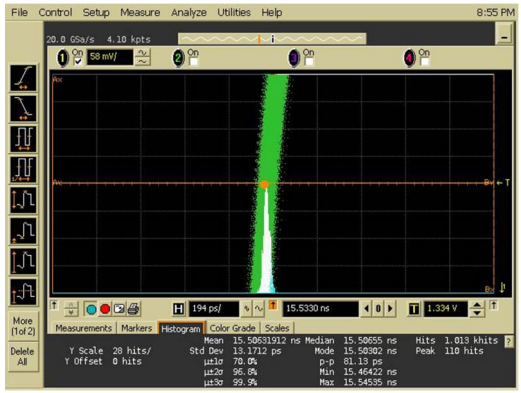

Fig. 11. Measured period jitter histogram operates at 64.489 MHz.

decrease, whereas the DCO control code increases. After the calibration process is done, the output period monotonically decreases, whereas the DCO control code increases. Hence, the proposed self-calibration circuit can ensure a DCO monotonic response during DCO coarse-tuning control code transitions, as shown in Fig. 9.

TABLE II
PERFORMANCE SUMMARY

	This work	[11]	[10]	[5]	[9]	[6]
Process	65nm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	90nm CMOS	0.18μm CMOS
Design Approach	Cell-Based	All-Digital	All-Digital	Cell-Based	Cell-Based	All-Digital
DCO Type	Cascading	Interpolating	Interpolating	Cascading	Cascading	Single Stage
Supply (V)	1.0	1.8	1.28	1.8	1.0	1.8
Frequency Range (MHz)	47.8 - 538.7	33 - 1040	300 - 1300	27 - 54	191 - 952	1100 - 2200
rms Jitter (ps)	13.2 (DCO) (@64.49MHz)	13.8 (PLL) (@950MHz)	10.4 (DCO) (@950MHz)	94 (PLL) (@54MHz)	8.24 (DCO) (@952MHz)	4.0 (DCO) (@1500MHz)
p-p Jitter (ps)	81.1 (DCO) (@64.49MHz)	86.7 (PLL) (@950MHz)	59.0 (DCO) (@950MHz)	X	49.95 (DCO) (@952MHz)	28.4 (DCO) (@1500MHz)
LSB Resolution (ps)	17.4	X	5.9	1.1	1.47	1.0
Chip Area (mm^2)	0.01 (DCO)	0.06 (DCO)	0.0075 (DCO)	0.156 (PLL)	X	0.20 (PLL)
Power (mW)	0.142(@ 58.7MHz) 0.205(@481.6MHz)	7.85* (@1.04GHz)	4.48 (@ 950MHz)	0.6* (@54MHz)	0.14 (@200MHz)	7.5* (@1500MHz)

X: Not mentioned.
*Power Consumption calculated from 50% of ADPLL.

Fig. 10 shows measurement results of the DCO output period. After the calibration process is done, the output clock period monotonically decreases, whereas the DCO control code increases, and the BISC controller adds the compensation code (Step[4:0]): 20 to the DCO control code if there are changes in the coarse-tuning control code. If the compensation code is not added, the cycle-to-cycle jitter during subfrequency band transitions is 266 ps. After the calibration process is done, the cycle-to-cycle jitter during subfrequency band transitions is reduced to 83 ps. The jitter effects of the DCO's output clock may influence the performance of the proposed BISC circuit. Thus, the best compensation code determined from the chip measurement is 16, and the BISC circuit outputs 20.

Fig. 11 shows the period jitter measurement results of the DCO output clock. The root mean square jitter and peak-to-peak jitter at 64.49 MHz is 13.2 and 81.1 ps, respectively. Table II summarizes test chip performance and compares it with other DCOs. In Table II, the interpolated DCO [10], [11] consumes large power consumption due to the short-circuit current in the interpolator circuit. Thus, it is not suitable for low-power ADPLL applications. In addition, the single-stage DCO [6] has very large power consumption and requires a large chip area compared with the cascading structure DCOs. In summary, the proposed DCO with the BISC circuit has a smaller area and lower power consumption and is very suitable for ADPLL design.

V. CONCLUSION

In this brief, a monotonic DCO with a BISC circuit in 65-nm CMOS technology is presented. The proposed DCO can output frequency ranges from 47.8 to 538.7 MHz with low power consumption. The proposed calibration circuit can solve the nonmonotonic problem in DCOs with cascading architecture when the coarse-tuning control code is changed. Thus, it is very suitable for ADPLL design in system-on-a-chip applications.

ACKNOWLEDGMENT

The authors would like to thank their colleagues in the Silicon Sensor and System Laboratory of National Chung Cheng University for the many fruitful discussions. The shuttle program supported by the United Microelectronics Corporation is acknowledged as well.

REFERENCES

[1] A. Arakali, S. Gondi, and P. K. Hanumolu, "Low power supply regulation techniques for ring oscillators in phase-locked loops using a split-tuned architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2169–2181, Aug. 2009.

[2] C.-C. Hung and S.-I. Liu, "A leakage-compensated PLL in 65-nm CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 7, pp. 525–529, Jul. 2009.

[3] H.-J. Hsu, C.-C. Tu, and S.-Y. Huang, "A high-resolution all-digital phase-locked loop with its application to built-in speed grading for memory," in *Proc. IEEE VLSI-DAT*, Apr. 2008, pp. 267–270.

[4] P.-H. Hsieh, J. Maxey, and C.-K. K. Yang, "A phase-selecting digital phase-locked loop with bandwidth tracking in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 781–792, Apr. 2010.

[5] D. Sheng, C.-C. Chung, and C.-Y. Lee, "A low-power and portable spread spectrum clock generator for SoC applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, Mar. 2010.

[6] S.-Y. Lin and S.-I. Liu, "A 1.5 GHz all-digital spread spectrum clock generator," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3111–3119, Nov. 2009.

[7] R. B. Staszewski, C.-M. Hung, D. Leipold, and P. T. Balsara, "A first multi-gigahertz digitally controlled oscillator for wireless applications," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 11, pp. 2154–2164, Nov. 2003.

[8] P.-L. Chen, C.-C. Chung, and C.-Y. Lee, "A portable digitally controlled oscillator using novel varactors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 5, pp. 233–237, May 2005.

[9] D. Sheng, C.-C. Chung, and C.-Y. Lee, "An ultra-low-power and portable digitally controlled oscillator for SoC applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 11, pp. 954–958, Nov. 2007.

[10] B.-M. Moon, Y.-J. Park, and D.-K. Jeong, "Monotonic wide-range digitally controlled oscillator compensated for supply voltage variation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 10, pp. 1036–1040, Oct. 2008.

[11] K.-H. Choi, J.-B. Shin, J.-Y. Sim, and H.-J. Park, "An interpolating digitally controlled oscillator for a wide-range all-digital PLL," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 9, pp. 2055–2063, Sep. 2009.