An Autocalibrated All-Digital Temperature Sensor for On-Chip Thermal Monitoring

Ching-Che Chung, *Member, IEEE*, and Cheng-Ruei Yang

***Abstract*—This brief presents an autocalibrated all-digital temperature sensor circuit for use with on-chip thermal sensing applications. The proposed temperature sensor eliminates the need for two-temperature-point calibration in prior temperature sensors. Therefore, temperature sensor calibration efforts in high-volume production can be significantly reduced. The proposed design uses reference clock period information to perform self-calibration, and thus, effects of process variation can be removed. Subsequently, the accuracy of the proposed temperature sensor can be improved with very small area cost and low power consumption. The temperature sensor is implemented with a standard performance 65-nm complementary metal–oxide–semiconductor technology. The core area is 0.01 mm^2, and the power consumption of the proposed circuit is 150 μW with a 1-V supply. Since the proposed temperature sensor can be easily calibrated with a reference clock, the proposed design is very suitable for dynamic thermal management applications in a system-on-a-chip era.**

***Index Terms*—Calibration, circuit reliability, delay circuits, delay lines, digital circuits, sensors.**

I. Introduction

In RECENT years, the advanced CMOS process makes it possible to integrate many designs into a single chip. The number of central processing units on a single embedded system chip is now extended to 64 cores or more [1]. When multiple chips are integrated and fabricated on a single chip, the power density is significantly increased. As a result, certain areas of the chip involving high switching activities can generate a localized high-temperature area called a "hotspot." Furthermore, in system-in-a-package design with 3-D integrated-circuit technology or stacked dies, the situation will become worse than before.

Hotspots cause unusual temperature gradients across the chip, and this proves a significant threat to both reliability and robustness of the product. Therefore, in modern microprocessor designs, on-chip thermal sensing and dynamic thermal management are very important for system reliability [2]–[5]. However, low-power schemes such as a power shutdown or clock gating cause these hotspots to change dynamically. For this reason, in POWER7 microprocessors [2], the design includes 40 temperature sensors implemented at different locations for on-chip thermal monitoring. Subsequently, the chip can manage these localized hotspots through adaptive systems and cooling management solutions.

State-of-the-art CMOS temperature sensors [6] are typically implemented as chopper-stabilized amplifiers measuring current from substrate p-n-p bipolar transistors. This type of a temperature sensor, although it has a high level of accuracy, requires significant design effort and a large area as well as extra postsilicon transistor trimming costs. In addition, the analog circuits used in this design are inconvenient for use in a 65-nm CMOS technology with a supply voltage of 1 V or lower. For these reasons, all-digital sensors are desired.

Temperature sensing based on temperature-dependent delays of inverters [7]–[10] could be suited for microprocessor applications as this leads to digital implementation. An all-digital time-domain temperature sensor that uses a time-to-digital converter (TDC) to quantize a delay pulse into temperature information is proposed in [7]–[9]. Notably, an all-digital architecture can be easily ported to different processes in a short time. In addition, it also allows for easy integration with digital systems.

However, prior temperature sensors [7]–[9] need to perform two-temperature-point calibration with a fixed direct-current (dc) power supply before the temperature sensors can be used. Otherwise, the effect of process variation can strongly influence the accuracy of temperature measurement. Since there will be many temperature sensors on the chip, the temperature sensors [7]–[9], which need to perform calibration on every sensor with an external thermometer, are not suitable for on-chip thermal sensing applications. Furthermore, the proposed low thermal sensitivity delay line [7], [9], with three diode-connected transistors between the supply rails, is difficult to be implemented in a 65-nm CMOS technology with a low supply voltage of 1 V.

A dual-delay-locked-loop (DLL)-based all-digital temperature sensor (ADTS) [10] is proposed to remove the effects of process variation via calibration at only one temperature point. A reference clock with a multiphase delay line can generate a fixed delay to calibrate the temperature errors. Thus, calibration cost in high-volume production can be reduced. Additionally, the use of DLLs simplifies sensor operation and yields a high measurement bandwidth (at 5 kS/s). However, the temperature sensor with dual DLLs occupies too large chip areas with a high level of power consumption at a milliwatt level.

In summary, a temperature sensor should occupy a low chip area allowing multiple sensors to be placed on-chip for localized temperature measurement processes. In addition, the sensor should have low power consumption at a submilliwatt level as this reduces errors due to self-heating. A temperature sensor should be easily calibrated without using any external

Manuscript received August 13, 2010; revised October 22, 2010 and November 26, 2010; accepted December 6, 2010. Date of publication February 14, 2011; date of current version February 24, 2011. This work was supported in part by the National Science Council of Taiwan under Grant NSC99-2220-E-194-011. This paper was recommended by Associate Editor P. Mohseni.

The authors are with the Department of Computer Science and Information Engineering, National Chung Cheng University, Minhsiung 62102, Taiwan (e-mail: wildwolf@cs.ccu.edu.w).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2010.2104016

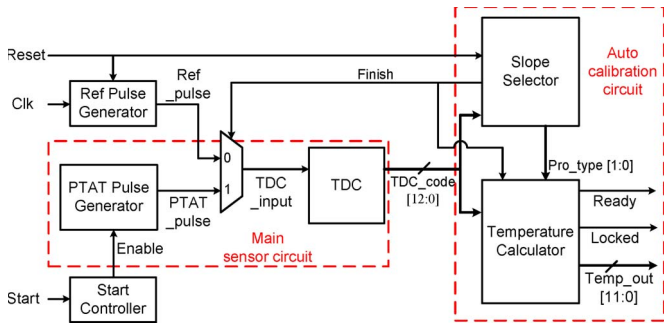

Fig. 1. Proposed ADTS.

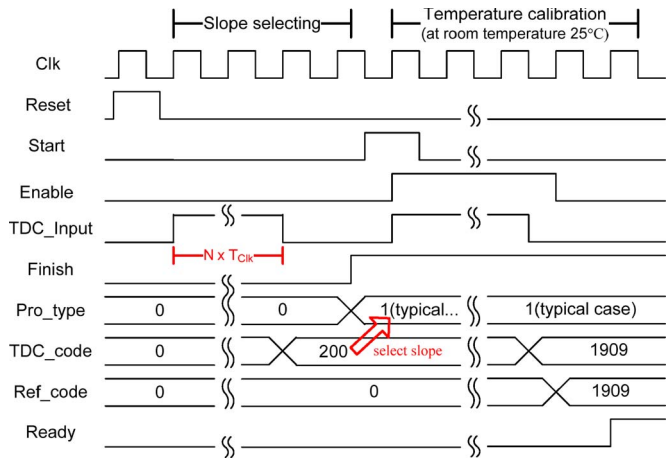

Fig. 2. Timing diagram of the autocalibration circuit.

current or voltage references. A sensor that fulfills all of these requirements will be reliable and easy to be used for on-chip thermal sensing.

In this brief, an autocalibrated ADTS in a 65-nm technology is presented. The proposed temperature sensor can perform autocalibration at a known equilibrium temperature value when the system is reset to eliminate two-temperature-point calibration in prior temperature sensors [7]–[9]. The proposed design uses reference clock period information to perform self-calibration, and then, the effects of process variation can be removed. Thus, the accuracy of temperature measurement can be improved with very small area cost and low power consumption. Since the proposed temperature sensor can be easily calibrated with a reference clock, it is very suitable for current dynamic thermal management applications in a system-on-a-chip era.

The rest of this brief is organized as follows. Section II describes the architecture of the proposed temperature sensor. The implementation of the proposed design is discussed in Section III. Section IV shows the experimental results of the chip. Finally, Section V concludes with a summary.

II. Architecture of Temperature Sensor

Fig. 1 shows the block diagram of the proposed autocalibrated ADTS. The whole circuit can be simply divided into three components: a reference pulse generator, a main sensor circuit and an autocalibration circuit. The propotional-to-the-absolute-temperature (PTAT) pulse generator can generate a pulse with a width PTAT. Subsequently, the proposed TDC can quantize this pulse into digital codes (TDC_code[12:0]). After temperature calculation, the absolute temperature value in degree Celsius (°C) can be outputted as Temp_out[11:0].

The TDC's output (TDC_code[12:0]) is a linear function of the localized temperature value near the sensor. Thus, if the slope and the intercept of the line are known, the absolute temperature value in degree Celsius (°C) can be easily calculated. However, the slope and the intercept of the line are changed with process and voltage variations. As a result, in prior temperature sensors [7]–[9], two-temperature-point calibration using an external thermometer with a fixed dc power supply is required to obtain the slope and the intercept before the temperature sensors can be used. Additionally, if the dc power supply value is changed, sensor calibration must be performed again.

Since for on-chip thermal sensing applications, there are many temperature sensors placed on a chip. Thus, it is not possible to perform two-temperature-point calibration for every sensor. Furthermore, a sensor, which is placed in a different chip location, will have a different linear function due to on-chip variations in a 65-nm CMOS technology.

In the proposed temperature sensor, the process variation is removed by the autocalibration circuit. The timing diagram of the autocalibration circuit is illustrated in Fig. 2. First, after a system is shut down for a long time, when the system is reset, the whole-chip temperature is now at its equilibrium temperature. The reference pulse generator uses the reference clock to generate a pulse (TDC_Input) whose width is always fixed under the process, voltage, and temperature variations. Then, this pulse is fed to the TDC to obtain a process testing code (TDC_code). Note that in this section, the equilibrium temperature is assumed to a known value at a room temperature of 25 °C, and the dc power supply is 1 V.

The process variation affects TDC's resolution. Thus, a slope selector compares the process testing code (TDC_code) with circuit simulation results at different process corners to choose a suitable slope for the sensor. For example, in Fig. 2, because the process testing code (TDC_code: 200) is close to the simulation result at a typical process corner, thus, the slope in a typical process corner is used for further temperature calculation. In the slope selector, it stores two threshold values to determine whether the process corner is at the typical, the best, or the worst corner. Then, the signal "Finish" is pulled high to change the input of the TDC from the reference pulse generator to the PTAT pulse generator.

After slope selection, a start controller triggers the main sensor circuit to produce a reference code at equilibrium temperature. For example, in Fig. 2, the TDC output is stored as a reference code (Ref_code: 1909) for further temperature calculation. Subsequently, the signal "Ready" is pulled high, and the proposed temperature sensor becomes ready for temperature measurement.

The timing diagram of the proposed temperature sensor is shown in Fig. 3. After calibration is complete, when the signal "Start" is enabled, the start controller sends the signal "Enable" to trigger the main sensor circuit. The main sensor circuit measures the current temperature information and outputs a digital code (TDC_code) to the temperature calculator to compute the temperature value (Temp_out) in degree Celsius (°C). Then, the signal "Locked" is pulled high to indicate that the temperature value is ready for output.

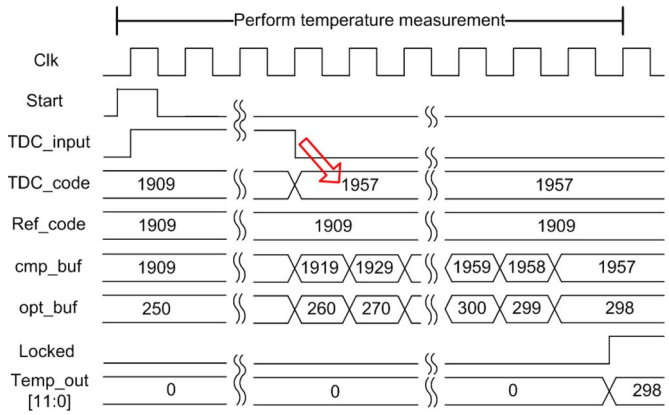

Fig. 3. Timing diagram of the temperature sensor.

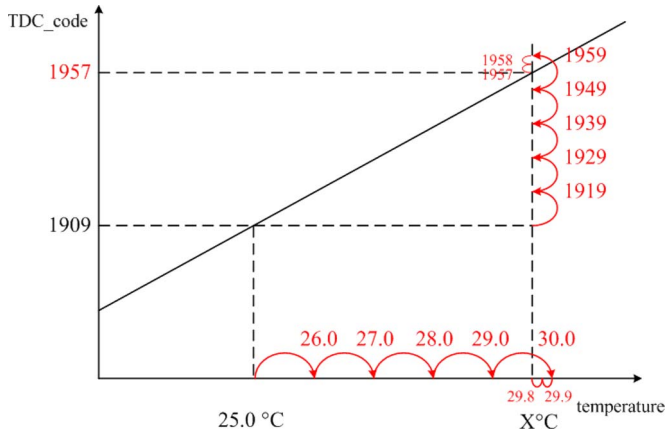

Fig. 4. Example of temperature calculation.

The temperature calculation is illustrated in Fig. 4. When the on-chip temperature near the temperature sensor is changed, the new temperature value in degree Celsius (°C) can be calculated from the difference between the reference and current TDC codes. Assume a situation where the current TDC code is 1957 and the reference code at a room temperature of 25 °C is 1909. In this example, the slope is assumed to be 10 TDC_code/°C for illustrating purposes. Then the reference code is copied to "cmp_buf," and the initial value of "opt_buf" is set to 250 (i.e., 25 °C) in the beginning of temperature calculation.

The temperature calculator continues adding the slope value to "cmp_buf" until the value of "cmp_buf" is higher than the current TDC code. Every time when the value of "cmp_buf" is increased by 10, the value of "opt_buf" should be increased by 10, which adds 1 °C to the output temperature value. Then, the temperature calculator continues subtracting one tenth of the slope value to "cmp_buf" until the value of "cmp_buf" is equal to the current TDC code (i.e., 1957). In addition, when the value of "cmp_buf" is lowered by 1, the value of "opt_buf" should be lowered by 1, which subtracts 0.1 °C from the output temperature value. Finally, the value of "opt_buf" is 298, meaning that the current temperature value is 29.8 °C.

The proposed temperature calculator only uses an adder and a subtractor to compute the temperature value. Although it takes several clock cycles to compute the results, the area of the sensor can be kept as low as possible.

After a system is reset, if the whole-chip equilibrium temperature value is not known, the temperature calculator will not work correctly. As a result, before the temperature sensors can be used, one of the on-chip temperature sensors should perform autocalibration at a known equilibrium temperature. After that, this sensor can provide the required equilibrium temperature for other sensors to perform the autocalibration. In the proposed temperature sensor, calibration efforts are significantly reduced by the autocalibration circuit. Thus, calibration cost in high-volume production can be reduced as well.

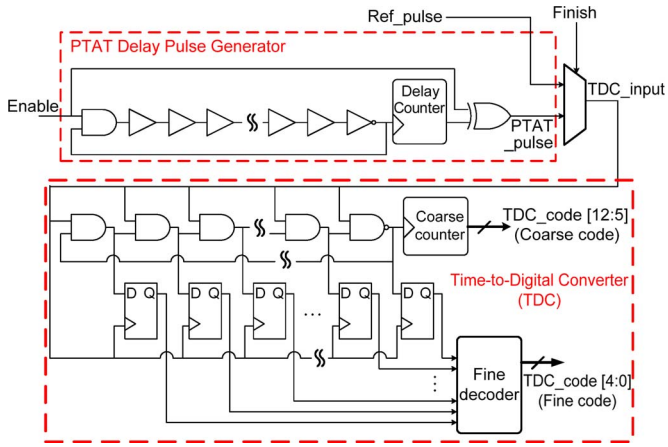

Fig. 5. Main sensor circuit.

III. Circuit Implementation

Fig. 5 shows the detail circuit of the proposed main sensor circuit. It is composed of the PTAT delay pulse generator and the TDC. To reduce the area of the sensor, the delay line used in the PTAT delay pulse generator is a cyclic delay line [11]. The cyclic delay line is composed of a two-input AND gate, 50 delay cells, and an inverter. When the signal "Enable" is pulled high, the cyclic delay line begins to oscillate. The delay counter counts up until the specified value is reached. Then, the PTAT pulse generator generates a pulse with a width PTAT. The PTAT pulse generator should produce a pulse, which width is wide enough for the next-stage TDC to quantize it into a digital code. The proposed cyclic delay line architecture can avoid the need for a very high resolution TDC; thus, the design complexity of the sensor circuit can be greatly reduced.

The cyclic TDC architecture [12] is used to quantize the pulsewidth into a digital code. The proposed TDC uses a coarse counter and a fine decoder to achieve two-step quantization over the wide range of the input pulsewidth. In the proposed cyclic TDC, 32 TDC cells are used to compose the TDC delay line. When the signal "TDC_Input" is pulled high, the TDC coarse counter counts the arrival positive edges of the oscillation to generate the TDC coarse code. Subsequently, when the signal "TDC_Input" is pulled low, residual pulsewidth information in the TDC delay line can be quantized by D flip-flops and a fine code decoder. In addition, the output of the TDC coarse counter and the fine code decoder are combined as TDC_code[12:0]. The resolution of the proposed TDC is 90 ps, and the input pulsewidth can be as wide as 737 ns in a typical case.

The main sensor circuit is implemented with standard cells. In addition, the reference pulse generator, the start controller, and the autocalibration circuit are written with hardware description language, and a cell-based design flow is used to implement the full chip. The proposed temperature sensor can

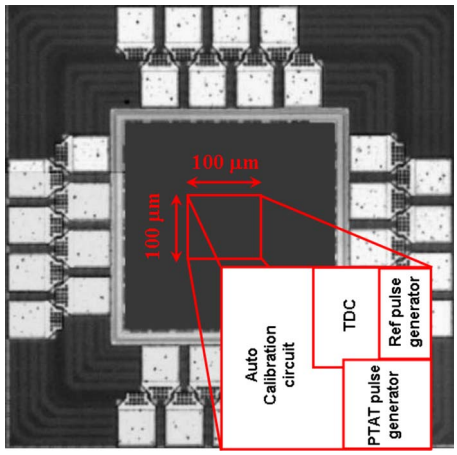

Fig. 6. Microphotograph of the temperature sensor test chip.

be implemented with standard cells; thus, it is easily ported to different processes in a short time.

IV. Experimental Results

The proposed autocalibrated ADTS is fabricated on a standard performance 65-nm CMOS technology. Fig. 6 shows a microphotograph of the temperature sensor, and the core area is 0.01 mm^2. In this test chip, only one temperature sensor is implemented. Thus, this sensor requires performing autocalibration at a known equilibrium temperature. However, if there are many sensors placed on-chip, only one temperature sensor is needed to perform autocalibration with an external thermometer. The other sensors can obtain the whole-chip equilibrium temperature from the calibrated sensor.

In Fig. 4, the TDC_code is assumed to have a linear function of the temperature value. However, there are some temperature measurement errors in the real sensor circuit, which mainly come from the nonlinearity of the PTAT pulse generator. Therefore, in the proposed temperature sensor, the line for temperature calculation is split up into two line segments. We use two different slopes in the temperature calculation between 0 °C to 25 °C and 25 °C to 60 °C. Fig. 7 shows the circuit simulation result of the proposed temperature sensor with single [13] and dual slopes in temperature calculation. In addition, if the proposed sensor uses the conventional two-temperature-point calibration, the measurement errors are also shown in Fig. 7. The simulation results show that the maximum temperature measurement error can be reduced to −1.2 °C to 2.2 °C by the dual-slope temperature calculation method in a typical process corner. The temperature error of the proposed temperature sensor is very close to the sensor with two-temperature-point calibration.

Fig. 8 shows the measurement results of the proposed autocalibrated ADTS. Because the printed circuit board and data pods of the logic analyzer are not heat resistant, the measured temperature ranges from 0 °C to 60 °C. The line "predict temperature," as shown in Fig. 8, indicates the ideal temperature sensor output. The other lines indicate the measured output of three test chips. In the proposed temperature sensor, the slope selector only stores the slopes in typical, best, and worst process corners. Thus, when the fabricated chip is not exactly at these three process corners, there will be measurement errors in the

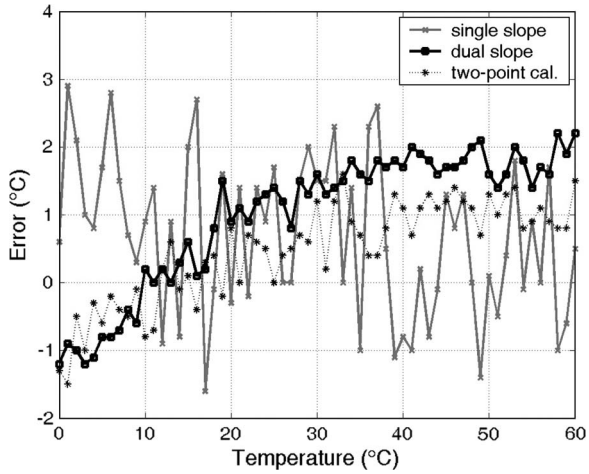

Fig. 7. Simulation result of the proposed temperature sensor.

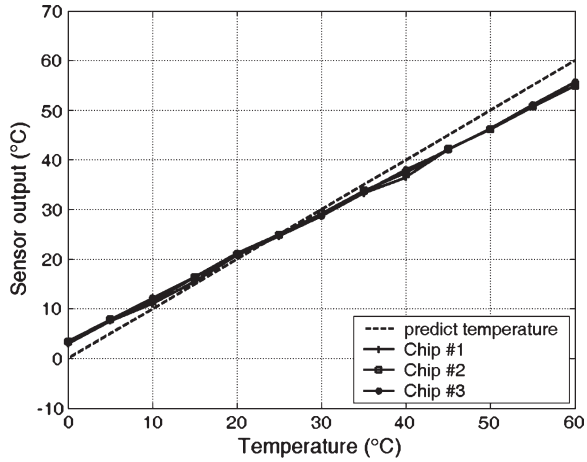

Fig. 8. Measurement results of the three chips.

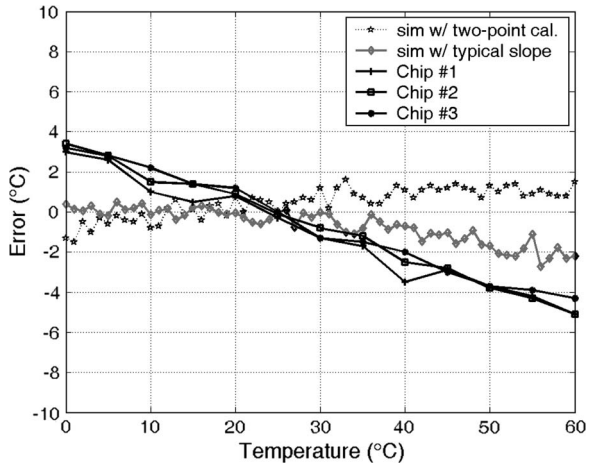

Fig. 9. Temperature errors of the three chips.

proposed temperature sensor. In Fig. 8, these three test chips are close to a typical process corner but are a little worse than the chip, which is exactly at a typical process corner.

Fig. 9 shows the measured temperature error of the three test chips. In Fig. 9, the line "sim w/ typical slope" is used to simulate the effect when process is at the worst process corner, but the slope in the typical process corner is used to calculate the temperature value. In addition, the line "sim

TABLE I
COMPARISONS OF RECENT SMART TEMPERATURE SENSORS

Sensor	Resolution (°C)	Error (°C)	Calibration	Power	Area (mm^2)	Conversion Rate (samples/s)	Temperature Range (°C)	CMOS Technology
[6]	0.01	±0.1 (3σ)	One-point with Post-silicon Trimming	247 μW@ 3.3V	4.5	10	-55 ~ 125	0.7μm
[7]	0.16	-0.7 ~ +0.9	Two-points	0.49 mW@ 3.3V	0.175	1000	0 ~ 100	0.35μm
[8]	0.058	-1.5 ~ +0.8	Two-points	8.4 μW @ 2.5V	N/A	2	0 ~ 75	FPGA
[9]	0.0918	-0.25 ~ +0.35	Two-points	36.7 μW@3.3V	0.6	2	0 ~ 90	0.35μm
[10]	0.66	-1.8 ~ +2.3	One-point with Dual DLLs	12 mW@ 1.2V	0.16	5,000	0 ~ 100	0.13μm
Proposed	0.139	-5.1 ~ +3.4	Auto Calibration*	150 μW@1.0V	0.01	10,000	0 ~ 60	65nm

*: one of the on-chip temperature sensors requires one-point calibration.

w/ two-point cal." is the simulation results for the sensor with two-temperature-point calibration in the typical process corner. From the measurement results, the trend of temperature errors is similar to the simulation result shown in the line "sim w/ typical slope." The temperature error of the proposed temperature sensor is from -5.1 °C to $+3.4$ °C, and the accuracy of the proposed temperature sensor is sufficient for dynamic thermal management applications.

Table I lists the comparisons of recent smart temperature sensors. Although the temperature error is very small in [6], the temperature sensor using a substrate p-n-p bipolar transistor is not suitable for dynamic thermal management applications. In all-digital smart temperature sensors [7]–[9], the two-temperature-point calibration is required in every sensors; thus, calibration cost is very large in on-chip thermal sensing applications with many sensors. Additionally, the conversion rate of the temperature sensor [7]–[9] is very slow. The dual-DLL-based temperature sensor [10] only needs one-temperature-point calibration, but it has high power consumption and a large chip area, making it unsuitable for on-chip thermal sensing applications.

V. CONCLUSION

An autocalibrated all-digital smart temperature sensor has been developed with 65-nm CMOS technology. It has a small chip area and low power consumption, making the proposed sensor very suitable for current on-chip dynamic thermal management applications. The proposed temperature sensor eliminates the need for two-temperature-point calibration in prior temperature sensors. Therefore, temperature sensor calibration efforts can be significantly reduced.

ACKNOWLEDGMENT

The authors would like to thank their colleagues in the Scalable Sensing Service (S3) Laboratory of National Chung Cheng University for many fruitful discussions. The shuttle program supported by United Microelectronics Corporation is acknowledged as well.

REFERENCES

[1] S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung, J. MacKay, M. Reif, L. Bao, J. Brown, M. Mattina, C.-C. Miao, C. Ramey, D. Wentzlaff, W. Anderson, E. Berger, N. Fairbanks, D. Khan, F. Montenegro, J. Stickney, and J. Zook, "TILE64—Processor: A 64-Core SoC with mesh interconnect," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 88–598.

[2] M. Ware, K. Rajamani, M. Floyd, B. Brock, J. C. Rubio, F. Rawson, and J. B. Carter, "Architecture for power management: The IBM Power7 approach," in *Proc. IEEE Int. Symp. HPCA*, Jan. 2010, pp. 1–11.

[3] R. Mukherjee and S. O. Memik, "Systematic temperature sensor allocation and placement for microprocessors," in *Proc. ACM/IEEE Design Autom. Conf.*, Jul. 2006, pp. 542–547.

[4] D. Brooks and M. Martonosi, "Dynamic thermal management for high-performance microprocessors," in *Proc. IEEE Int. Symp. HPCA*, Feb. 2001, pp. 171–182.

[5] K. Skadron, T. Abdelzaher, and M. R. Stan, "Control theoretic techniques and thermal-RC modeling for accurate and localized dynamic thermal management," in *Proc. IEEE Int. Symp. HPCA*, Feb. 2002, pp. 17–28.

[6] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.1 °C from -55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[7] P. Chen, C.-C. Chen, C.-C. Tsai, and W.-F. Lu, "A time-to-digital-converter-based CMOS smart temperature sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1642–1648, Aug. 2005.

[8] P. Chen, M.-C. Shie, Z.-Y. Zheng, Z.-F. Zheng, and C.-Y. Chu, "A fully digital time-domain smart temperature sensor realized with 140 FPGA logic elements," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 12, pp. 2661–2668, Dec. 2007.

[9] P. Chen, C.-C. Chen, Y.-H. Peng, K.-M. Wang, and Y.-S. Wang, "A time-domain SAR smart temperature sensor with curvature compensation and a 3σ inaccuracy of -0.4 °C $\sim +0.6$ °C over a 0 °C to 90 °C range," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 600–609, Mar. 2010.

[10] K. Woo, S. Meninger, T. Xanthopoulos, E. Crain, D. Ha, and D. Ham, "Dual-DLL-based CMOS all-digital temperature sensor for microprocessor thermal monitoring," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 68–69a.

[11] P. Chen, S.-I. Liu, and J. Wu, "A CMOS pulse-shrinking delay element for time interval measurement," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 9, pp. 954–958, Sep. 2000.

[12] C.-C. Chen, P. Chen, C.-S. Hwang, and W. Chang, "A precise cyclic CMOS time-to-digital converter with low thermal sensitivity," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 4, pp. 834–838, Aug. 2005.

[13] C.-C. Chung and C.-R. Yang, "An all-digital smart temperature sensor with auto-calibration in 65 nm CMOS Technology," in *Proc. IEEE ISCAS*, May 2010, pp. 4089–4092.