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Design of a human body channel communication transceiver using convolutional codes

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ABSTRACT

This paper presents a wideband signaling body channel communication (BCC) transceiver that uses the convolutional encoding method. The proposed transmitter uses the convolutional encoding method to increase the data reliability, and the modulated data are transmitted directly to a human body through a SMA cable and an electrode. In the receiver side, the oversampling phase detection clock and data recovery circuit with convolutional encoding method recovers the clock and data and increases 1.8x random data jitter tolerance (i.e., 50ns–90ns) at 10^{-9} BER. The proposed BCC transceiver, except for the pre-amplifier of the RX, can be realized as a synthesizable digital IP. Thus, the proposed design can be ported to different processes in a short time. The feasibility of the proposed transceiver architecture was verified by the FPGA, and no bit errors occurred over 10^8 bits received at data rate 3.125 Mbps in transmission distance under 140 cm, which indicates the transceiver is very suitable for high-performance BCC applications.

1. Introduction

As wearable devices are widely applied in the healthcare and entertainment industries, many studies have focused on the design of body area networks. The wireless body area network (WBAN) is a network composed of sensor nodes, whereby the body sensor nodes are connected to each other and to a central hub. For the healthcare aspect, the body states of people who live with chronic diseases, such as asthma, diabetes, and heart attacks, need to be carefully controlled. The WBAN applications can alert the hospital before a patient has a heart attack. Furthermore, on-body syringe can automatically inject insulin for diabetes patients.

The IEEE 802.15.6 standard for WBANs supports the following three physical layers: ultra-wideband (UWB), narrow-band (NB), and body channel communication (BCC). The WBAN is characterized by three major issues. First, the operating time of the battery-powered sensor devices is limited by battery life. The energy efficiency of the radio frequency (RF) communication methods, such as Zigbee and Bluetooth, is poor. Although some studies claim that Zigbee has an operating time of three years [1], it has a low data rate under 250 kb/s. Second, the high-frequency bands of UWB and NB suffer from huge signal attenuation inside the human body channel due to the body shadowing effects [2–7]. Third, the other RF wireless products may operate at the same frequency band and result in an interruption.

In BCC, the human body is utilized as a communication medium to enable a set of on-body sensor nodes to communicate with a coordinator; thus, it is different from the RF propagating method. As shown in Fig. 1, the coordinator, such a smartwatch, collects all the information through the human body. Subsequently, the information collected by the body sensors can be delivered to the user smartphone or a remote server for further processing. Using BCC offers some advantages. First, because its operation involves a frequency range below 100 MHz, the BCC technique has a relatively high data rate with minimum energy per bit, compared to Zigbee, Bluetooth, and ultra-wideband. Second, the path loss of the signal for BCC is less than that when the RF propagation method is used. Moreover, the BCC is almost insensitive to the motion of the human body [8].

In addition to the development of RF communication, several low-power RF techniques have been proposed, such as low-power Bluetooth and near-field communication (NFC). Near-field communication is developed for short-term communication. Its power consumption is similar to that of low-energy Bluetooth, and its setup time is shorter than that of the general Bluetooth. The low-energy Bluetooth has lower power consumption than the general Bluetooth. However, Bluetooth and NFC

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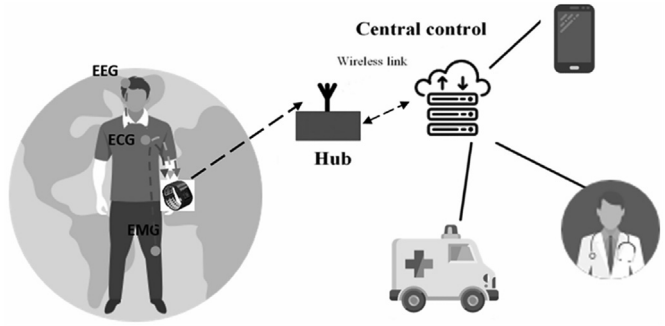

Fig. 1. A simple demonstration of the body channel communication.

are characterized by several security issues. Security issues are relatively fewer in BCC because the signal is largely attenuated when emitted from the human body [9]. Moreover, the security on BCC can be more prompted by using human physiological measurements to establish a customized secret key among network nodes [10]. Lastly, with the coordinator being a portable device on the body, the energy efficiency of BCC is better than those of Bluetooth and NFC.

The path loss and time-domain characteristics of capacitive BCC are measured and modeled in Ref. [13,24], and the magnetic BCC [22] offers relatively low path loss as compared to the capacitive BCC. However, the coil resonance variations due to the motion of the human body and the use of coil limits the on-chip integration are the design challenges for magnetic BCC [23]. The frequency shift keying (FSK) or the on-off-keying (OOK) modulation schemes had been applied in BCC [15,22]. An adaptive frequency hopping (AFH) technique is proposed in Refs. [15]; with AFH, every channel status is uninterruptedly monitored and the clean channel will be chosen for the adaptive frequency hopping. There is more than 10 dB improvement for interference resistance which is achieved by the four channels AFH approach. However, two frequency synthesizers are required for reducing the hopping time of the AFH. Also, the phase discontinuity and the timing mismatch are the design challenges for the BCC receiver with two phase-locked loops (PLLs).

The orthogonal frequency division multiplexing modulation (OFDM) BCC transceiver [17,18,23,25] modulates data on the multiple sub-carrier frequency bands, and OFDM BCC transceiver can achieve relatively high data rate with high spectrum efficiency properties (10 MHz bandwidth for 29.1 Mbps) [17]. However, the complicated design mainly increases the power consumption and chip area. The frequency selective digital transmission (FSDT) BCC modulates the data with a coding gain and is presented in Ref. [11,16,21]. The code length of the encoded data is larger than the original data to provide good data reliability. Nonetheless, the code rate is low with respect to using redundant bits to protect the original data. Moreover, except for the pre-amplifier of the RX, most of the previously published BCC transceiver [15–18,21–23,25] cannot be realized as a synthesizable digital intellectual property (IP).

In this paper, a wideband signaling (WBS) transceiver for BCC is proposed. In the transmitter part, the data are encoded with a convolutional encoding method, and then, the encoded data are modulated by a non-return-to-zero, inverted (NRZI) encoder with a bit stuffer. The data are transmitted in a packet format. In the receiver part, the proposed oversampling phase detector (OSPD) clock and data recovery (CDR) circuit recover the clock and data. The proposed BCC transceiver with the convolutional encoding method enhances the data reliability. Other coding methods, such as low-density parity-check (LDPC) coding and Turbo coding, have much more operations and higher design complexity than the convolutional encoding method used in the BCC transceiver, as discussed in Ref. [20]. The proposed BCC transceiver, except for the pre-amplifier of the RX, can be realized as a synthesizable digital IP. Thus, the proposed design can be ported to different process or FPGA in a short time.

The architecture of the proposed WBS transceiver is presented in Section 2. Section 3 describes the convolutional encoding method of the proposed design. Section 4 presents the experimental results. Finally, the conclusion is given in Section 5.

2. The proposed WBS transceiver architecture

Fig. 2 illustrates the overall BCC transceiver architecture. The personal computer (PC) #1 transmits data to a field-programmable gate array (FPGA)-based BCC transmitter. The transmitter encodes and modulates the input data before sending them to the human body. Because the signal is attenuated when going through the human body, an analog front end (AFE) board with a variable gain amplifier (VGA) and a Schmitt trigger is used to pre-process the received signal. The gain setting for the VGA and the offset voltage for the Schmitt trigger should be adjusted for different transmission distances. After the attenuated signal is restored to digital waveforms, the data are sent to the BCC receiver for clock and data recovery. The recovered data are demodulated and decoded by the receiver. Finally, the decoded data are sent to PC #2.

2.1. Transmitter

Fig. 3 shows the block diagram of the proposed BCC transmitter. The clock divider divides the system clock of the FPGA board and triggers all blocks. The user can choose to send the multimedia images stored in the memory block or send the random data generated from the linear

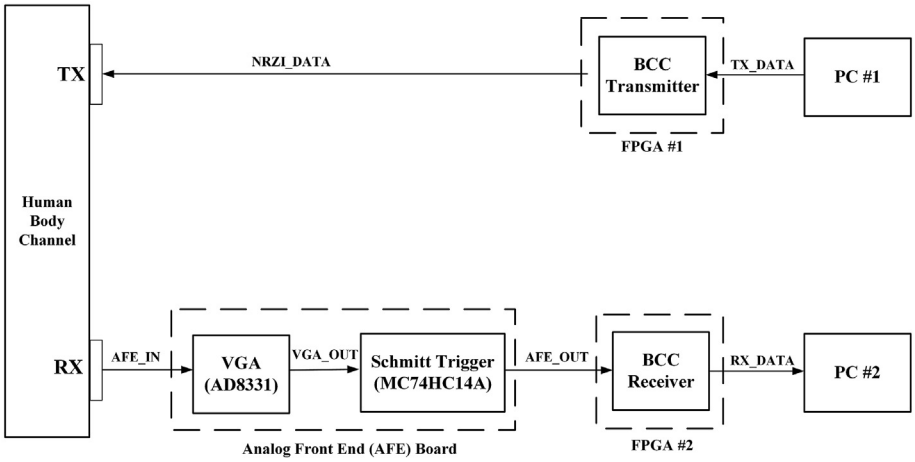

Fig. 2. The overall architecture of the proposed BCC transceiver.

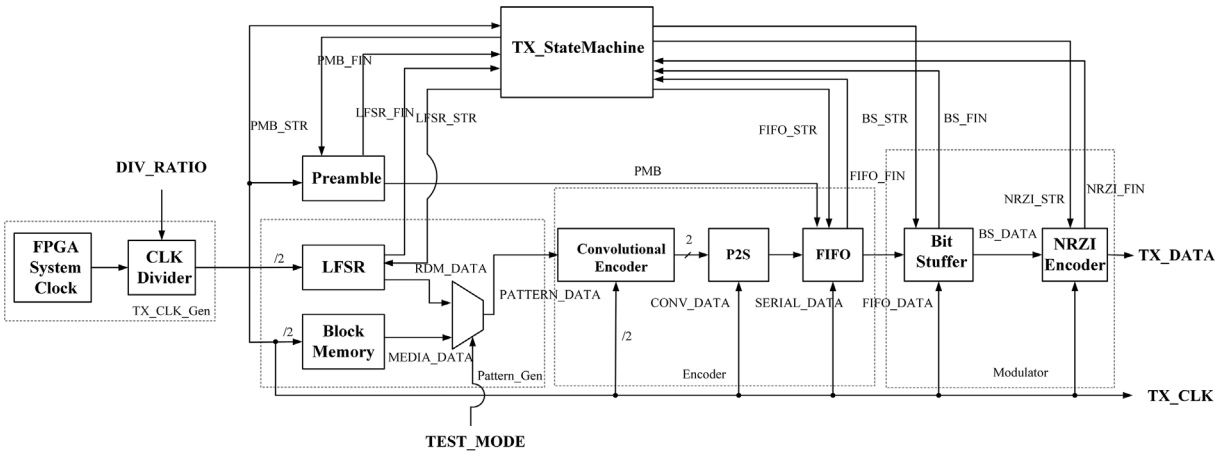

Fig. 3. Block diagram of the proposed BCC transmitter.

feedback shift register (LFSR) pattern generator. The convolutional encoder uses encoded format (2, 1, 7) to encode data in order to increase data reliability. The first and second parameters in the encoding format mean the encoder outputs two bits when one-bit data is inputted, while the last parameter means six registers store the input values and the newest input data does exclusive-or (XOR) according to the polynomial-generated matrix. The first-in-first-out (FIFO) puts packet header and then encodes data in order. The modulator consists of a bit stuffer to limit the maximum length of the consecutive identical digits (CID), and then, the NRZI output waveform will have more data transition.

The packet format is shown in Fig. 4. The preamble block generates the regular sequence and the start frame delimiter (SFD) to be the packet header. The guard bits are inserted to let the Viterbi decoder of the receiver decoding the data correctly. The number of guard bits is determined by the number of constraint lengths of the convolutional encoding method used in our design.

Fig. 5 shows the flowchart of the proposed BCC transmitter. First, the TX_INNER_RESET signal resets the transmitter. Then, the preamble is generated to the FIFO. The convolutional encoder encodes the LFSR random data or binary data in the FPGA memory block, depending on the TEST_MODE signal. After the data are encoded, the preamble and encoded data are transmitted in NRZI format. Because the latency of the decoded time of Viterbi decoder (shown in Fig. 6) needs about 246 cycles, the transmitter waits for 250 cycles and then transmits the next packet.

2.2. Receiver

The block diagram of the proposed BCC receiver is shown in Fig. 6. The AFE_IN (shown in Fig. 2) is pre-amplified and triggered by an AFE board then outputs as AFE_OUT. According to AFE_OUT, the OSPD produces the recovery clock and the recovery data. An NRZI decoder and bit-unstuffer are contained in the demodulator, which demodulates RCY_DATA based on RCY_CLK. When the demodulated data is ready, the RX_StateMachine enables the Viterbi decoder to decode the demodulated data. Lastly, if the TEST_MODE is high, the LFSR_Checker will compare the decoded data with the local random data patterns which are the same as the transmitter side. Any unmatched data will trigger the bit error rate

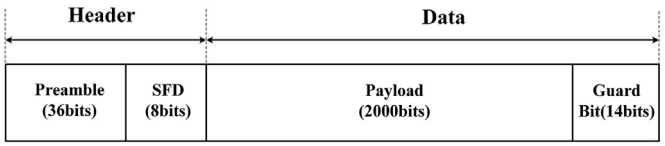

Fig. 4. The packet format of the WBS transceiver.

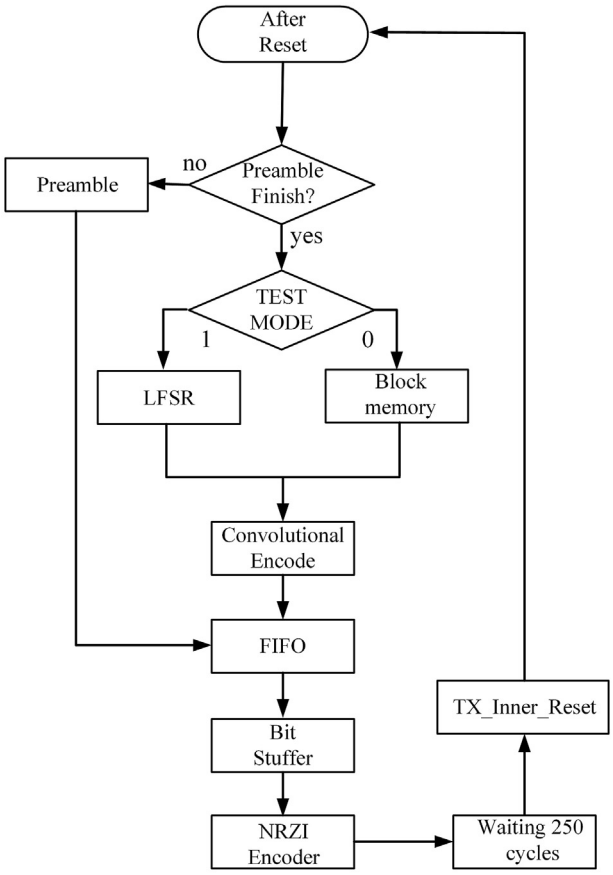

Fig. 5. Flowchart of the proposed transmitter.

(BER) flag signal.

Fig. 7 shows the flowchart of the proposed BCC receiver. In the first, the OSPD recovers data and clock. The NRZI decoder continuously demodulates the RCY_DATA. After detecting the SFD sequence, the un-bitstuffer begins to remove the redundant data bits until the number of un-bitstuffing data bits is 2000. Based on the un-bitstuffing data, the Viterbi decoder decodes data and sends the decoded data to the LFSR checker for pattern matching.

The RX_INNER_RESET has pulled high for soft-resetting the Viterbi decoder when the number of compared data bits is 1000. If there are any mismatching data, the COMP_FLAG will be pulled high correspondingly.

The block diagram of OSPD is shown in Fig. 8. The FPGA system clock

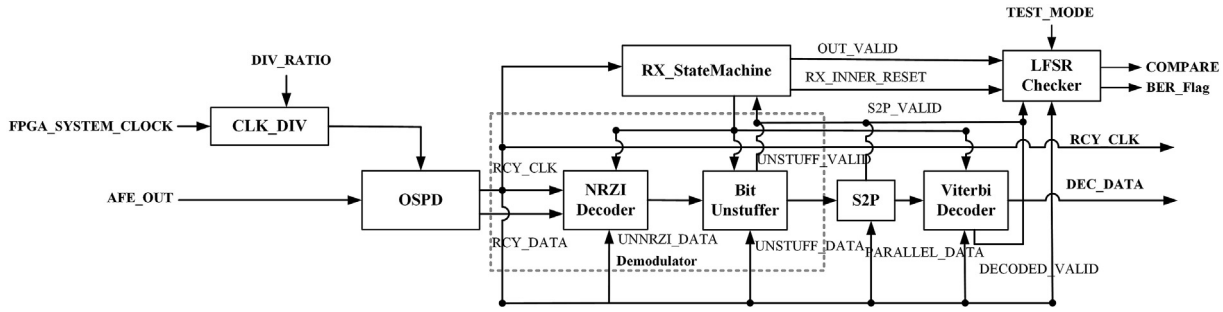

Fig. 6. Block diagram of the proposed BCC receiver.

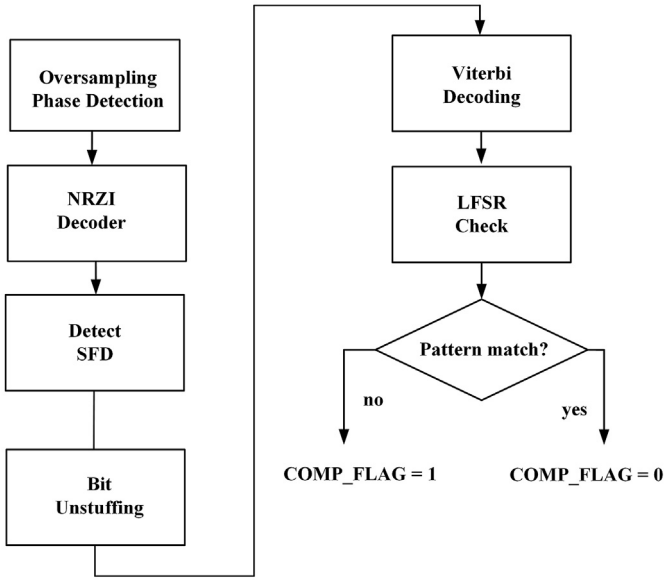

Fig. 7. Flowchart of the proposed BCC receiver.

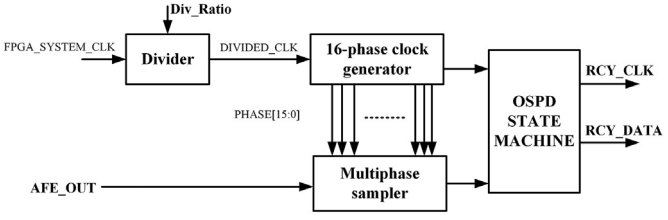

Fig. 8. Block diagram of oversampling phase detection.

is divided by a frequency divider. A 16-phase clock generator uses the divided clock to generate 16 phases. A multiphase sampler samples input data and saves the value in multiple phases. Based on the 16 phases, an OSPD state machine recovers RCY_CLK and RCY_DATA.

The 16-phase clock generator block uses the Divided_CLK and a phase counter to generate 16 multiple phases in one symbol period of the AFE_OUT. Fig. 9 shows the timing diagram of the oversampling phase detection without phase error. The divided clock oversamples 16 times at one input data symbol. Meanwhile, 16 phases are aligned to the sampling value. When the phase counter is equal to N, the OSPD state machine will compare the sampled value of phase (N−1) and the value of AFE_OUT. If the comparison result shows a difference, a data transition edge is detected. At the same time, the value of Edge registers is refreshed to (N−1). The value in Edge registers remains the same when there is no phase error caused by jitter noise.

Fig. 10 shows the timing diagram of the OSPD with phase error and one CID situation. A TRANSITION_EDGE signal is pulled high when a rising edge or a falling edge occurs. Then, the TRANSITION_EDGE_FLAG is pulled high for waiting RCY_CLK is pulled high. The RCY_CLK will be pulled high when the difference between the phase counter and the Edge register is equal to eight while the TRANSITION_EDGE_FLAG is high.

The flow of the OSPD state machine is shown in Fig. 11. For the 1st transition edge in Fig. 10, the value of the phase counter is 10. The XOR of the AFE_OUT sampled by FCLK and the value sampled by the positive edge of PHASE 9 is 1. Therefore, a data transition is detected. The value of Edge is set to 9, and the TRANSITION_EDGE is pulled high. Moreover, CID_COUNTER is set to 0 when the TRANSITION_EDGE is pulled high. Because the edge transition occurs, the RCY_DATA will change the value to the sample value of PHASE 10. An edge transition will lead to the pulling high of TRANSITION_EDGE_FLAG for waiting for the absolute value of the phase counter minus the value of EDGE is 8. For example, when the phase counter value is 1, the EDGE value (9) minus the phase counter (1) is 8, and then, RCY_CLK is pulled high for one FCLK cycle and the CID_COUNTER is set to 0. When the RCY_CLK is high, the TRANSITION_EDGE_FLAG is pulled down. Otherwise, with the value of an internal CID counter being 17, the RCY_CLK will also be pulled high for one FCLK cycle when no data transition occurs. When RCY_CLK is pulled high, the CID counter will be reinitialized as zero.

3. Convolutional encoding method

To increase the data reliability, a convolutional encoding method that belongs to channel code is adopted. Compared to Walsh code modulation in Ref. [11], the code rate (1/2) of the adopted convolutional encoding is 1.6 times higher than the code rate of the Walsh code (5/16). As shown in Fig. 12, the convolutional encoder uses six registers to save the input data. The output data are generated by the XOR values in the registers and the current input data. The convolutional encoded format (2, 1, 7), which is used in IEEE standard 802.11a/g, means that two output data bits are produced by one input data bit XOR six registers [12]. The output is alternately generated according to two generator polynomials shown in Eqs. (1) and (2). The digit "1" in polynomials in binary format means that the value of the register is involved in XOR calculation and vice versa.

$$g^{(0)} = (1011011) \quad or \quad (91)_{10} \tag{1}$$

$$g^{(1)} = (1111001) \quad or \quad (121)_{10} \tag{2}$$

4. Experimental results

The proposed BCC transceiver was implemented using FPGAs. Table 1 shows the resource utilization of the proposed BCC transceiver. For the TX FPGA, the drive strength of the output pad is set to 12 mA to drive the maximum transmission distance 140 cm. The overview of the FPGA board with AFE circuits is shown in Fig. 13. The power of the FPGA can

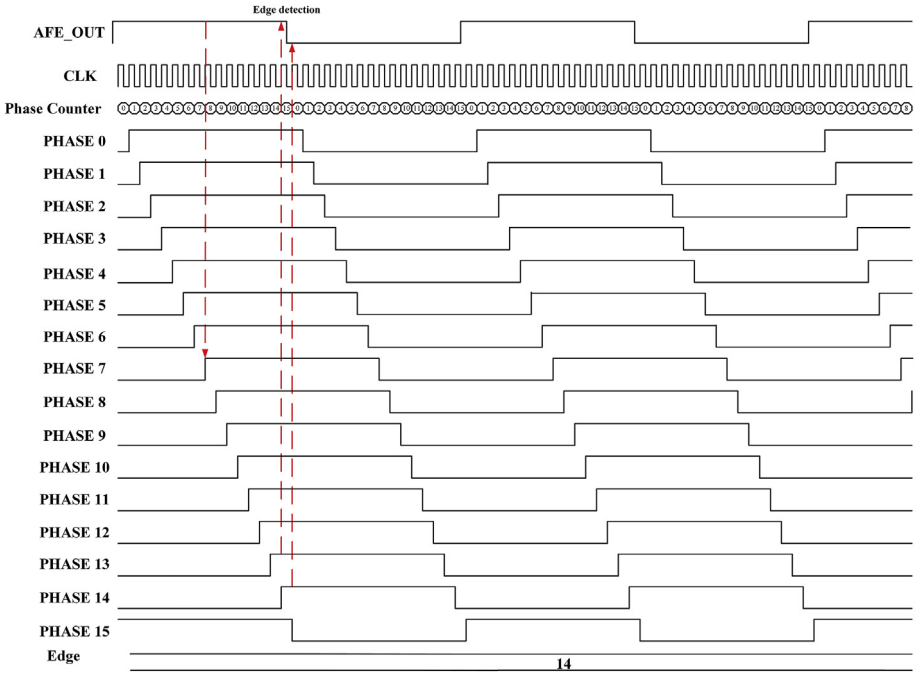

Fig. 9. The timing diagram of the OSPD in no phase error case.

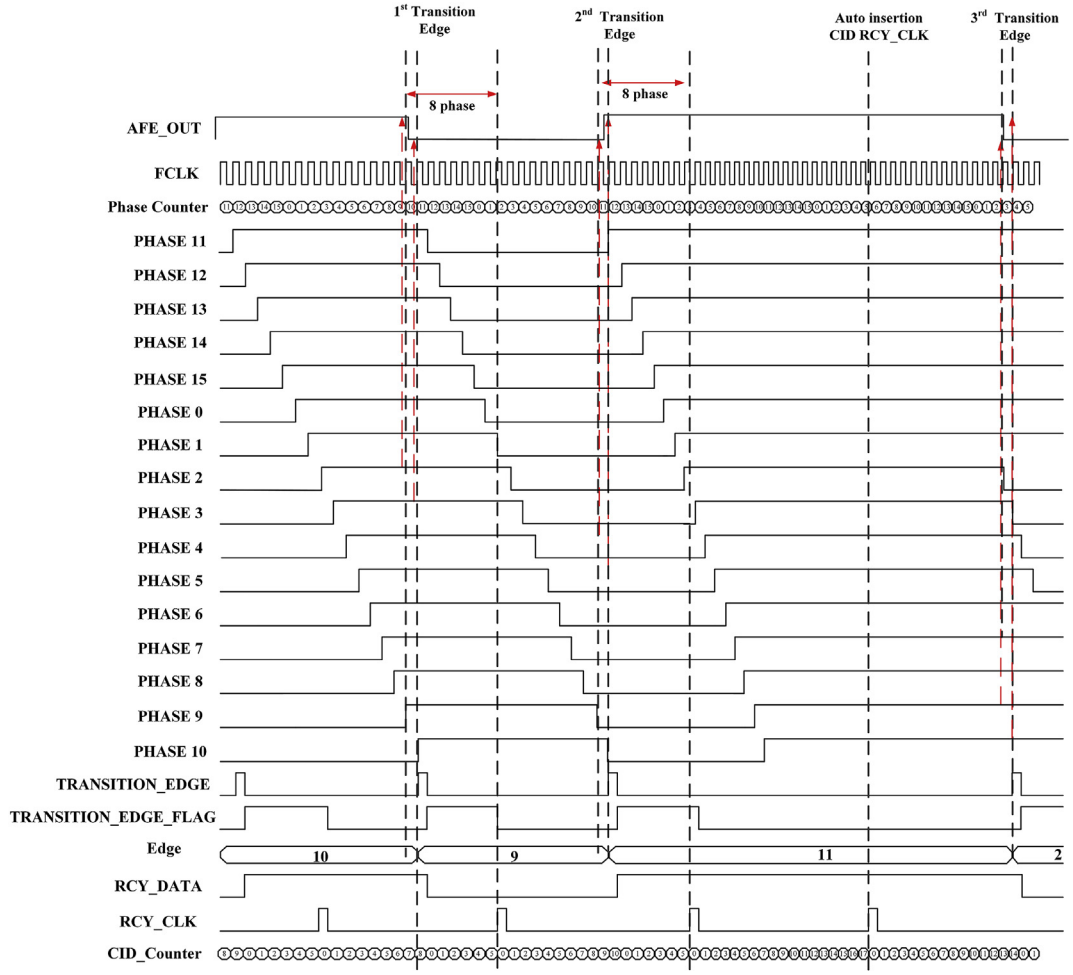

Fig. 10. The timing diagram of the OSPD diagram with the phase error.

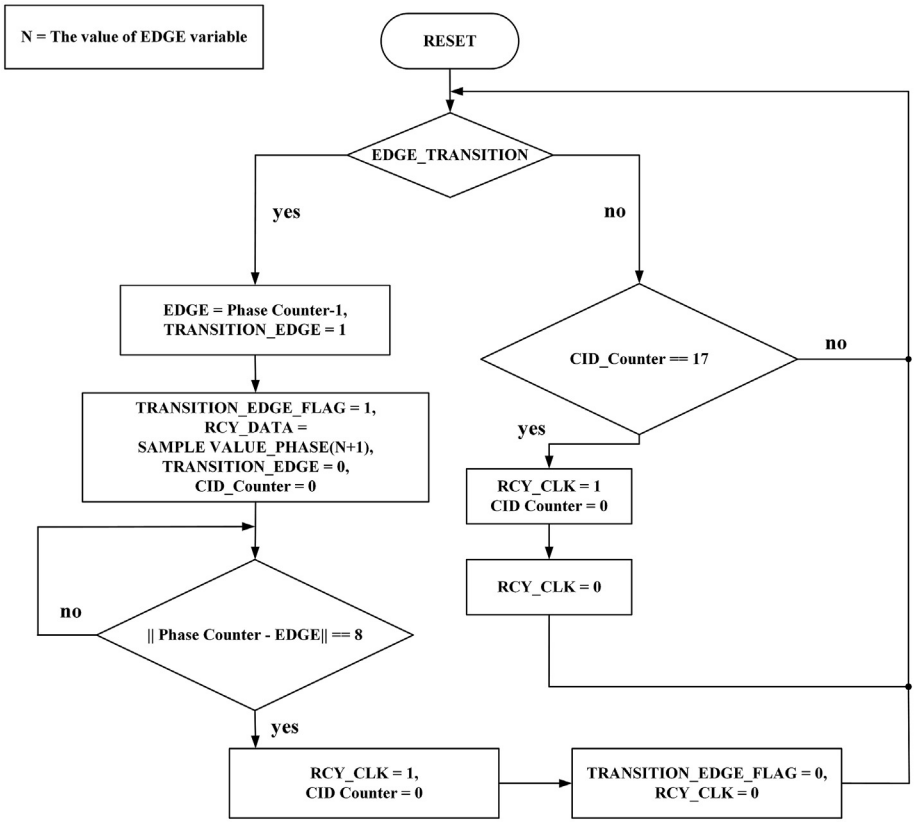

Fig. 11. Flowchart of the OSPD operation.

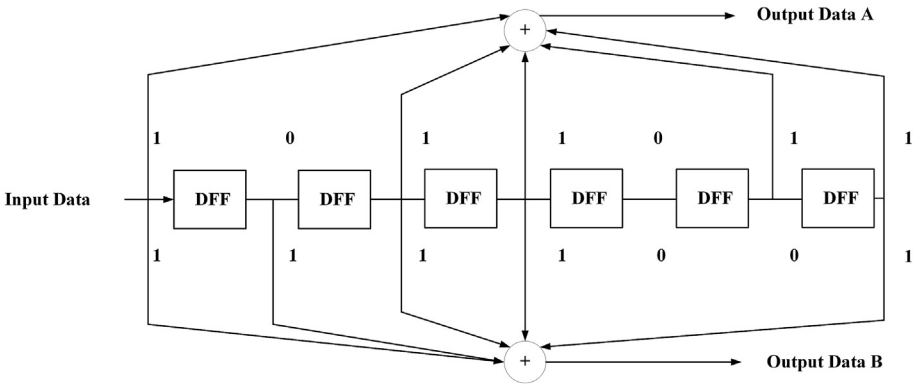

Fig. 12. Convolutional encoder (2, 1, 7).

Table 1
Resource utilization of the proposed BCC transceiver.

Slice Logic Utilization	Used	Available	Utilization
BCC Transmitter			
Number of Slice Registers	2934	20,800	14.11%
Number of Slice LUTs	1320	10,400	12.69%
Number of Occupied Slices	816	8150	10%
Number used as Memory	0	9600	0%
BCC Receiver			
Number of Slice Registers	3715	20,800	17.86%
Number of Slice LUTs	3952	10,400	38%
Number of Occupied Slices	1182	8150	15%
Number used as Memory	0	9600	0%

be supplied by a 9 V battery or a 5 V micro USB cable. The gain control voltage for the variable gain amplifier (VGA) shown in Fig. 2 can be measured from TP2, and the DC level of the Schmitt trigger shown in Fig. 2 can be measured from TP1 with a multi-meter. The VGA switches are used to control the function of the VGA. These AFE circuits are used to pre-process the received signal. After the attenuated signal is restored to digital waveforms, the data are sent to the FPGA-based BCC receiver for clock and data recovery. The FPGA chip is mounted on the backside of the board. In Fig. 13, the AFE_IN signal (shown in Fig. 2) is connected to the INPUT PORT and the output of the FPGA outputs to the OUTPUT PORT. VGA_VOL and VGA_VOH are the digital waveforms output by the AFE circuits.

Fig. 14 shows the verification environment of the proposed BCC transceiver. In the transmitter side, the TX FPGA and TX PC #1 (shown in Fig. 2) are supplied by an uninterruptible power system (UPS). The RX FPGA and RX PC #2 (shown in Fig. 2) are supplied directly by the power outlet. This step makes sure that the grounds of TX and RX are air-coupled. Because there is not enough control I/O pins on the FPGA

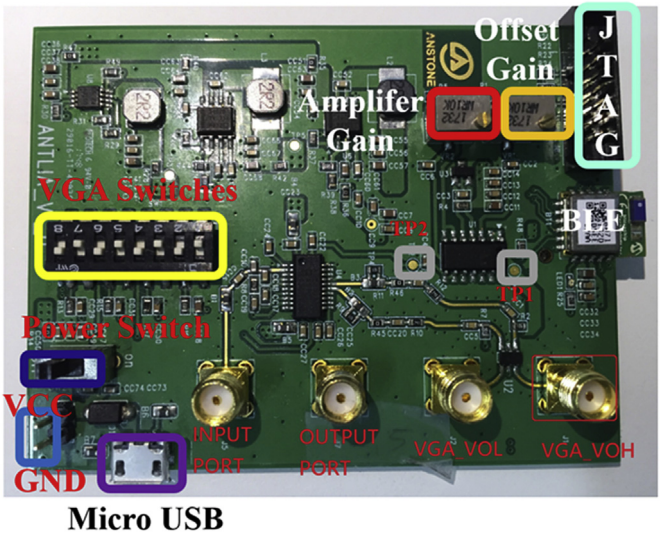

Fig. 13. Overview of the FPGA board with AFE circuits.

Fig. 14. The measurement environment of the proposed BCC transceiver.

board, a virtual input/output (VIO) IP is used in the FPGA and a JTAG cable connects the PC and the FPGA. After that, the TX FPGA transmits data through an SMA cable and an electrode to the human body. The RX PC #2 (shown in Fig. 2) can probe RX FPGA internal signals by using an integrated logic analyzer (ILA) IP integrated on RX FPGA.

Fig. 15 shows the simulation results of the proposed BCC transceiver with the proposed OSPD CDR but without using the convolutional encoding method. The higher number of CID means less data transition of transmitted data. When the consecutive identical digits were reduced, the OSPD CDR achieved a better BER performance at the same peak-to-peak (P_k-P_k) data jitter.

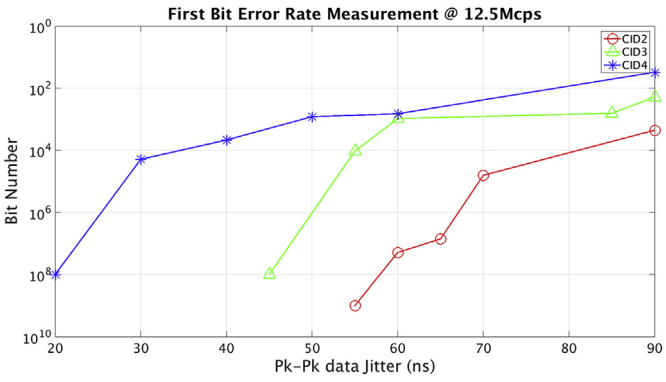

Fig. 15. Performance of the proposed BCC transceiver without using the convolutional encoding method.

Fig. 16 shows the simulation results of applying different constraint lengths of the convolutional encoding method to the proposed design with a CID of 2. The longer the constraint length, the more data reliability the proposed design could achieve. In Fig. 16, the x-axis means the amount of P_k-P_k data jitter added in the simulation. The y-axis means that a first-bit error occurred at the number of the received bits.

Fig. 17 shows the simulation results of the proposed BCC transceiver compared with other BCC architectures. In Ref. [11], a sampler and a vote integrator were used to recover clock and data, and the Walsh code method with code rate 1/8 is used. We use the same voltage integrator [11] with a convolutional encoding method and could achieve a better BER performance than the design in Refs. [11]. The proposed OSPD CDR with a convolutional encoding method shows the best BER performance in Fig. 17. Also, no bit error occurred with 90ns data jitter at 12.5 Mcps. Also, the proposed OSPD CDR with a convolutional encoding method can increase 1.8x random data jitter tolerance (i.e., 50ns–90ns) at 10^{-9} BER.

Table 2 presents the summary of the measurement results of the proposed BCC transceiver using the convolutional encoding method and oversampling phase-detection CDR. The range of the data rate is from

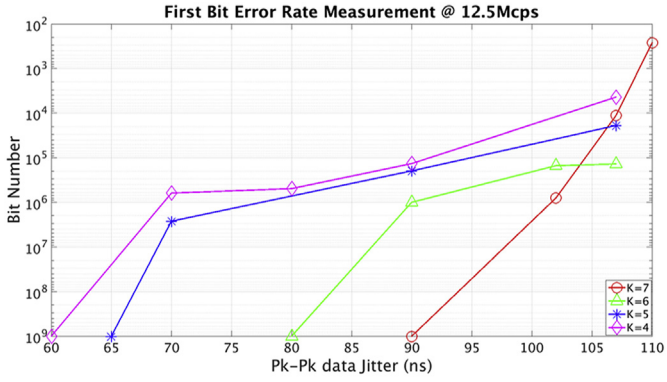

Fig. 16. Performance of the proposed design with different constraint lengths and CID of 2.

Fig. 17. Performance of the proposed BCC transceiver compared with other methods.

Table 2
Summary of the proposed BCC transceiver.

Data rate	780 kbps–3.125 Mbps
Chip rate	1.56 Mcps–6.25 Mcps
Transmission Distance	10–140 cm
Core Voltage	1.0 V (for FPGA)
Power Consumption	77 mW (TX) 81 mW (RX) 0.486 W (AFE circuit)
Sensitivity	−18.87 dBm
BER	$<10^{-8}$ (No bit error after transmitting 10^8 bits)
Energy/bit	50.56 nJ/b(without AFE circuit)

Table 3
Performance comparisons.

	[14] JSSC′07	[15] JSSC′09	[21]Sensors'15	[18] JSSC′17	[22] JSSC′19	[23] JSSC′17	Proposed
Process	0.25 μm	0.18 μm	0.18 μm	65 nm	65 nm	65 nm	FPGA
Data Rate	2 Mb/s	60 kb/s ~ 10 Mb/s	164 kb/s ~ 2.625 Mb/s	1 Mb/s	1.25 Mb/s ~ 5 Mb/s	200 kb/s ~ 2 Mb/s	780 kb/s ~ 3.125 Mb/s
Modulation	Wideband Signaling	FSK	FSDT	OFDM+FSK	mHBC+OOK	OFDM+FSK	Wideband Signaling
Supply	1 V	1.0 V	1.2 V	1.1 V	0.6 V	1.1 V	1 V
Area	0.85 mm^2	2.3 mm^2	1.05 mm^2	2.13 mm^2	0.12 mm^2	0.542 mm^2	N/A
BER	1.1×10^{-7}	$<10^{-5}$@ (10 Mbps)	$<10^{-2}$ (packet error rate)	$<10^{-7}$	$<10^{-3}$@(RX input power −63.5 ~ −56 dBm)	10^{-7}@(2 Mbps)	$<10^{-8}$@ (3.125 Mbps)

780 kbps to 3.125 Mbps. In the FPGA measurement results, no bit errors occurred after receiving and decoding over 108 bits. The maximum signal transmission distance of the proposed FPGA-based BCC transceiver is 140 cm. The core voltage of FPGA was 1.0 V. The sensitivity of the BCC receiver, which is determined by the VGA circuit, is −18.87 dBm and is enough for data transmission in 140 cm distance. The power consumption is reported by FPGA design software. The proposed design had a relatively high power consumption because it was implemented on an FPGA board with discrete analog front-end ICs.

Table 3 presents a comparison with other BCC designs. Also, the proposed BCC transceiver uses a robust digital approach to implement the CDR circuit. In terms of reliability, the proposed design outperformed other BCC designs in BER performance. BCC transceiver [16] operates in the far-field band (frequency > 30 MHz); they suffer from multi-path effects and exhibits considerable variations due to human activities in wearable scenarios [19]. Therefore, the proposed design operates in the quasi-static band (frequency < 30 MHz) which more stable and has deterministic characteristics.

5. Conclusion

In this paper, a wideband signaling BCC transceiver using the convolutional encoding method is proposed. In the transmitter side, the data are encoded by the convolutional encoding method to enhance data reliability. After that, the encoded data are stuffed by a bit stuffer to restrict the CID to 2 and then are modulated to the NRZI format. In the receiver side, the oversampling phase-detection CDR recovers data and clock based on the output from an AFE board, and the Viterbi decoder decodes the demodulated data. The proposed OSPD CDR with a convolutional encoding method can increase 1.8x random data jitter tolerance (i.e., 50ns–90ns) at 10^{-9} BER. Also, the proposed design was implemented and verified using an FPGA board, and the measurement results show that data rate ranged from 780 kbps to 3.125 Mbps and no bit errors occurred after receiving and decoding over 10^8 bits, implying the BER is less than 10^{-8} at 3.125 Mbps (6.25 Mcps). Thus, the proposed wideband signal BCC transceiver is very suitable for human body channel communication applications.

Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Ching-Che Chung: Conceptualization, Methodology, Resources, Writing - original draft, Writing - review & editing, Supervision, Project administration, Funding acquisition. **Duo Sheng:** Writing - review & editing. **Ming-Hsuan Li:** Conceptualization, Methodology, Data curation, Visualization.

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References

[1] Sasan Adibi, Link technologies and BlackBerry mobile health (mHealth) solutions: a review, IEEE Trans. Inf. Technol. Biomed. 16 (4) (Jul. 2012) 586–597.
[2] S.L. Cotton, A. McKernan, A.J. Ali, W.G. Scanlon, An experimental study on the impact of human body shadowing in off-body communications channels at 2.45 GHz, in: " Proceedings of Antennas and Propagation, EUCAP), Apr. 2011, pp. 3133–3137.
[3] Ramona Rosini, Raffaele D'Errico, Roberto Verdone, Body-to-body communications: a measurement-based channel model at 2.45 GHz, in: Proceedings of IEEE International Symposium on Personal Indoor and Mobile Radio Communications, PIMRC), Sep. 2012, pp. 1763–1768.
[4] Yu Wang, Ivan B. Bonev, Jesper Ø. Nielsen, István Z. Kovács, Gert F. Pedersen, Characterization of the indoor multiantenna body-to-body radio channel, IEEE Trans. Antenn. Propag. 57 (4) (Apr. 2009) 972–979.
[5] Patrick Van Torre, Luigi Vallozzi, Lennert Jacobs, Hendrik Rogier, Marc Moeneclaey, Verhaevert Jo, Characterization of measured indoor off-body MIMO channels with correlated fading, correlated shadowing and constant path loss, IEEE Trans. Wireless Commun. 11 (2) (Feb. 2012) 712–721.
[6] Akram Alomainy, Hao Yang, Abdus Owadally, Clive G. Parini, Yuri Nechayev, Costas C. Constantinou, Peter S. Hall, Statistical analysis and performance evaluation for on-body radio propagation with microstrip patch antennas, IEEE Trans. Antenn. Propag. 55 (1) (Jan. 2007) 245–248.
[7] Marshed Mohamed, Michael Cheffena, Fernando Pérez Fontán, Arild Moldsvor, A dynamic channel model for indoor wireless signals: working around interference caused by moving human bodies, IEEE Antenn. Propag. Mag. 60 (2) (Feb. 2018) 82–91.
[8] Zedong Nie, Jingjing Ma, Kamen Ivanov, and Wang Lei, "An investigation on dynamic human body communication channel characteristics at 45 MHz in different surrounding environments, IEEE Antenn. Wireless Propag. Lett. 13 (Feb. 2014) 309–312.
[9] J.H. Hwang, J.B. Sung, C.H. Hyoung, J.K. Kim, D.G. Park, S.W. Kang, analysis of signal interference in human body communication using human body as transmission medium, in: Proceedings of IEEE Antennas and Propagation Society International Symposium, Jul, 2006, pp. 495–498.
[10] Sang-Yoon Chang, Yih-Chun Hu, Hans Anderson, Ting Fu, Y. Evelyn, L. Huang, Body area network security : robust key establishment using human body channel, in: In Proceedings of HealthSec'12, the 3rd USENIX Conference on Security and Privacy, Aug. 2012.
[11] Ching-Che Chung, Ru-Hua Chang, and Ming-Hsuan Li, "An FPGA-based transceiver for human body channel communication using Walsh Codes,", in: Proceedings of IEEE International Conference on Consumer Electronics – Taiwan, ICCE-TW), May 2018.
[12] IEEE, IEEE 802.11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, IEEE std 802.11-2007 edition, 2007.
[13] Ching-Che Chung, Chih-Yu Lin, Jia-Zong Yang, Time-domain characteristics of body channel communication (BCC) and BCC transceiver design, in: Proceedings of International Symposium on VLSI Design, Automation, and Test, VLSI-DAT), Apr. 2016.
[14] Seong-Jun Song, Namjun Cho, "A 0 Hoi-Jun Yoo, 2-mw 2-mb/s digital transceiver based on wideband signaling for human body communications, IEEE J. Solid State Circ. 42 (9) (Sep. 2007) 2021–2033.
[15] Namjun Cho, Loan Yan, Joonsung Bae, Hoi-Jun Yoo, A 60kb/s - 10Mb/s adaptive frequency hopping transceiver for interference-resilient body channel communication, IEEE J. Solid State Circ. 44 (3) (Mar. 2009) 708–717.
[16] Chee Keong Ho, Hao Cheong Jia, Junghyup Lee, Vishal Kulkarni, Li Peng, Xin Liu, Je Minkyu, High bandwidth efficiency and low power consumption Walsh code implementation methods for body channel communication, IEEE Trans. Microw. Theor. Tech. 62 (9) (Sep. 2014) 1867–1878.

[17] Ping-Yuan Tsai, Yu-Yun Chang, Shu-Yu Hsu, Chen-Yi Lee, An OFDM-based 29.1Mbps 0.22nJ/bit body channel communication baseband transceiver, in: Proceedings of International Symposium on VLSI Design, Automation, and Test, VLSI-DAT), Apr. 2015.
[18] Wala Saadeh, Muhammad Awais Bin Altaf, Haneen Alsuradi, Jerald Yoo, A pseudo OFDM with miniaturized FSK demodulation body coupled communication transceiver for binaural hearing aids in 65 nm CMOS, IEEE J. Solid State Circ. 52 (3) (Mar. 2017) 757–768.
[19] Ji-Hoon Lee, Kwangmin Kim, Minsoo Choi, Jae-Yoon Sim, Hong-June Park, Byungsub Kim, A 16.6-pJ/b 150-Mb/s body channel communication transceiver with decision feedback equalization improving >200% area efficiency, in: Proceedings of Symposium on VLSI Circuits, Jun. 2017, pp. C62–C63.
[20] Zhen-zhi Wu, Chen Gong, Dake Liu, Computational complexity analysis of FEC decoding on SDR platforms, J. Sign. Process. Syst. 89 (2) (Nov. 2017) 209–224.
[21] Yu Lin Tsou, Cihun-Siyong Alex Gong, Nai Chen Cheng, Yu Lee, Christina F. Jou, Integrated biosensing platform based on a 1.74-mW -90-dBm sensitivity dual-mode-operation receiver for IEEE 802.15.6 human body communication standard, IEEE Sensor. J. 15 (6) (Jun. 2015) 3317–3327.
[22] Jiwoong Park, Patrick P. Mercier, A sub-10-pJ/bit 5-Mb/s magnetic human body communication transceiver, IEEE J. Solid State Circ. 54 (11) (Nov. 2019) 3031–3042.
[23] Wala Saadeh, Muhammad Awais Bin Altaf, Haneen Alsuradi, Jerald Yoo, A 1.1, -mW ground effect-resilient body-coupled communication transceiver with pseudo OFDM for head and body area network, IEEE J. Solid State Circ. 52 (10) (Oct. 2017) 2690–2702.
[24] Jiwoong Park, Harinath Garudadri, P. Patrick, Mercier, "Channel modeling of miniaturized battery-powered capacitive human body communication systems, IEEE (Inst. Electr. Electron. Eng.) Trans. Biomed. Eng. 64 (2) (Feb. 2017) 452–462.
[25] Wala Saadeh, Haneen Alsuradi, Muhammad Awais Bin Altaf, and Jerald Yoo, "A 1.1 mW hybrid OFDM ground effect-resilient body coupled communication transceiver for head and body area network," in Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 201-204, Nov. 2016.