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A fast phase tracking reference-less all-digital CDR circuit for human body channel communication☆

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ABSTRACT

This paper presents a fast phase tracking and reference-less all-digital clock and data recovery circuit (ADCDR) for body channel communication (BCC) applications. The proposed ADCDR uses the novel phase-error calculation without a reference clock signal to improve the phase-tracking ability and reduce overall power consumption by eliminating the requirement for an external quartz crystal oscillator. In addition, the proposed gain-calibration method can automatically calibrate the gain value under different process-voltage-temperature (PVT) conditions to quickly compensate for the phase error. The wideband signaling (WBS) transceiver, including the proposed ADCDR is implemented using a 90-nm CMOS process with a core area of 0.36 mm^2. The maximum transmission data rate of the proposed design is 20 Mb/s and power consumption is 2.2 mW, which are very suitable for the wearable device applications as compared with the traditional designs.

1. Introduction

As integration circuit and biomedical technologies continue to develop rapidly, wearable personal entertainment and healthcare devices have become very popular electronics products in recent years. Conventional medical healthcare devices, such as electromyography (EMG) and electrocardiography (ECG), use the wireline to transfer the physiological signals, which may cause inconvenience for the patients. Thus, wireless communication techniques are considered more suitable for wearable device applications. In relation to this, the IEEE 802.15 Task Group 6 formulated a body area network (BAN) standard [1] that defines the multimedia transportation protocols and the industrial scientific medical (ISM) around the human body. Bluetooth and ZigBee are two major radio frequency (RF) transmission technologies to realize wireless BAN (WBAN). Although Bluetooth is more suitable than ZigBee for the high-speed transmission due to its high data rate, it still has some serious design issues, such as higher power consumption and interferences with other devices using the same 2.4 GHz ISM band [2]. Moreover, the RF transceiver also suffers from the body shadowing effect [3]. Thus, the body channel communication (BCC) was proposed to solve these problems. In contrast to other wireless communication technologies, the BCC transmits the data through the human body. Moreover, the BCC has relatively low signal attenuation and less interference in the nearby environment. The BCC is almost insensitive to the motion of a human [4] and can achieve a high data rate.

Recently, several different architectures have been proposed to realize the BCC [5–15]. The frequency-shift keying (FSK) modulation scheme, which uses two different frequencies to represent two binary values, is proposed to implement BCC in Ref. [11]. The receiver of the FSK modulation can be realized easily because it just distinguishes only two signals. However, the specific frequencies of the FSK approach can easily suffered from noise interference. A past study [5] investigated the use of the orthogonal frequency-division multiplexing (OFDM) method in encoding digital data on multiple carrier frequencies. An OFDM signal consists of a number of closely spaced modulated carriers. The OFDM-based architecture can achieve high data rate with a narrow channel frequency band. However, the OFDM increases power consumption and the chip area. In order to increase the data rate, [13] proposed the frequency-selective digital transmission architecture, which can achieve 60 Mb/s by using the Walsh codes, but this approach

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requires a high signal-to-noise ratio, which is not available in actual conditions. In our previous work [7], a BCC transceiver with wideband signaling (WBS) is proposed. The WBS-based architecture has a smaller chip area and lower power consumption. The data are encoded by non-return to zero inverted (NRZI) modulation and transmitted directly to the human body, after which the oversampling-based CDR circuit recovers the data to the original data in the receiver. This wideband signaling transceiver supports a maximum 40 Mb/s data rate. However, a large frequency drift between transmitter and receiver may cause a high bit error rate (BER).

In this paper, a WBS BCC transceiver with NRZI modulation and a reference-less, all-digital clock and data recovery circuit (ADCDR) is proposed. In the transmitter part, the data are modulated by an NRZI encoder with a bit stuffer and transmitted in a packet format. In the receiver part, the proposed reference-less ADCDR can reduce the overall power consumption by eliminating the requirement for an external quartz crystal oscillator and enhance the frequency drift tolerance. The proposed phase error calculation method, which uses the multi-phase signals to quantize the phase error, can enhance the ADCDR phase tracking ability and quickly compensate for the phase error. The proposed gain calibration method can also automatically calibrate the gain value under different process–voltage–temperature (PVT) conditions to quickly compensate for the phase error.

The rest of this paper is organized as follows. The architecture of the proposed WBS transceiver is presented in Section 2. The proposed automatic phase track gain calibration of ADCDR is presented in Section 3. Section 4 describes the circuit implementation of the proposed design. Section 5 presents the experimental results. Finally, the conclusion is given in Section VI.

2. The proposed WBS transceiver

Fig. 1 presents the architecture of the proposed WBS BCC transceiver, which consists of a transmitter (TX), a receiver (RX), and an analog front-end (AFE) circuit. The desired TX frequency is generated by setting the digitally controlled oscillator (DCO) control code and the divider ratio. The pattern generator and the modulator generate the transmission data (TX_DATA), after which the data are transmitted to the human body. In the receiver part, the received data (RX_DATA) are amplified and converted to the digital signal by the AFE circuit. Subsequently, the CDR and demodulator recover the data from the analog front-end output (AFE_OUT) to the original data (RCY_DATA). Finally, the BER_Flag signal generates the BER information.

Fig. 2 illustrates the architecture of the proposed WBS BCC transmitter, which consists of a clock generator (CLK_Gen), a pattern generator (Pattern_Gen), a modulator, and a TX state machine. The TX operation is described as follows. First, according to the input DCO control code (DCO_CODE), the CLK_Gen generates the clock (TX_CLK) to the other circuits. Second, the Pattern_Gen generates the preamble data and the random data in the normal mode of Pattern_Gen. In the test mode, the Pattern_Gen generates the preamble data and the regular data for chip debugging. Finally, the modulator modulates the DATA to the NRZI_DATA and the bit stuffer performs bit stuffing, which limits the maximum continuous identical digits (CID) to 3. The TX_StateMachine can generate the start signal or the finish signal to control the state of the other circuits and select the output data of the Pattern_Gen.

Fig. 3 shows the packet format of the WBS BCC transceiver. In the

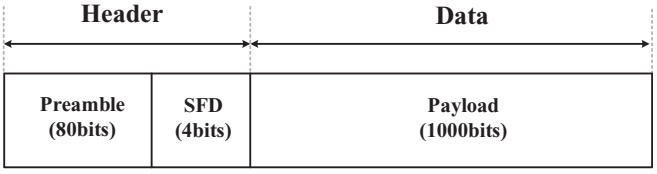


Fig. 3. The packet format of the WBS BCC transceiver.

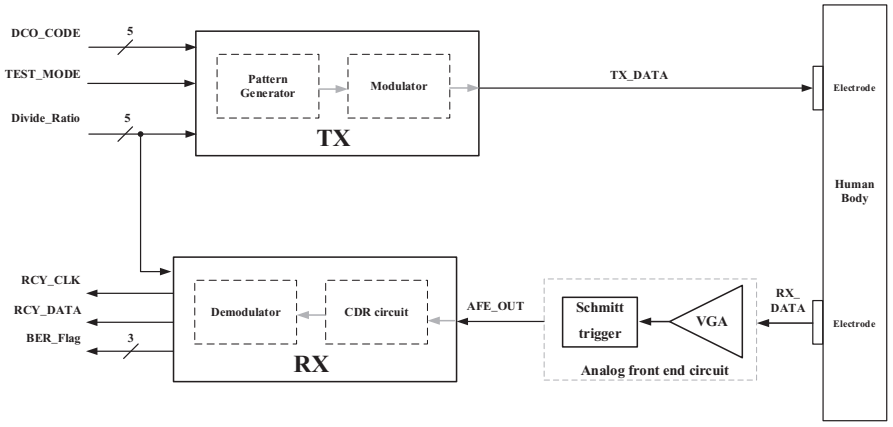


Fig. 1. Architecture of the proposed WBS BCC transceiver.

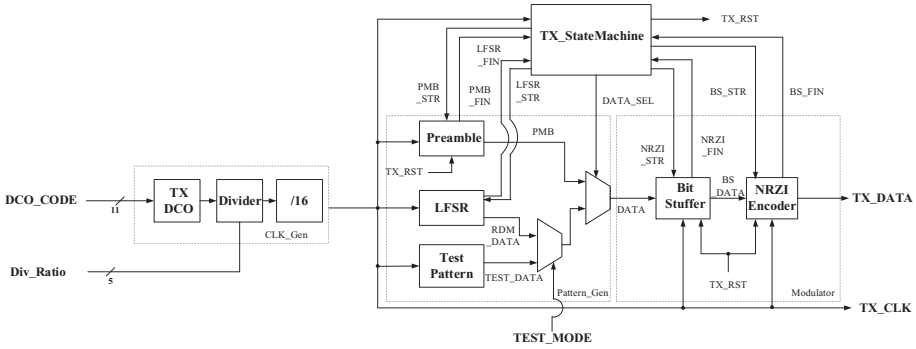


Fig. 2. Architecture of the proposed WBS BCC transmitter.

beginning, 80 preamble bits are transmitted to the human body for synchronization in the receiver. Subsequently, 4 bits start frame delimiter (SFD) which is used to detect the start bit of the random data. Finally, 1000 bits of random data are transmitted in one packet.

The flowchart of TX operation is shown in Fig. 4. Once the TX is reset, the TX starts to transmit the preamble bits. When preamble bits are sent, the TX detects the test mode signal (TEST_MODE) to choose the operation mode. If the TEST_MODE is "0," the linear feedback shift register (LFSR) generates the random data for the BER measurement. If the TEST_MODE is "1," the Test Pattern circuit generates the regular pattern for the debugging issue. Next, the bit stuffer checks the data and bit-stuffs such data to insert some data transitions. Then, the NRZI encoder will encode the data in the NRZI format. Finally, the TX will wait 200 cycles before the next packet transmission because the RX needs to take some time to recover the clock and data. After that, the TX generates the TX_RST signal to reset the circuits and begins to send the next packet.

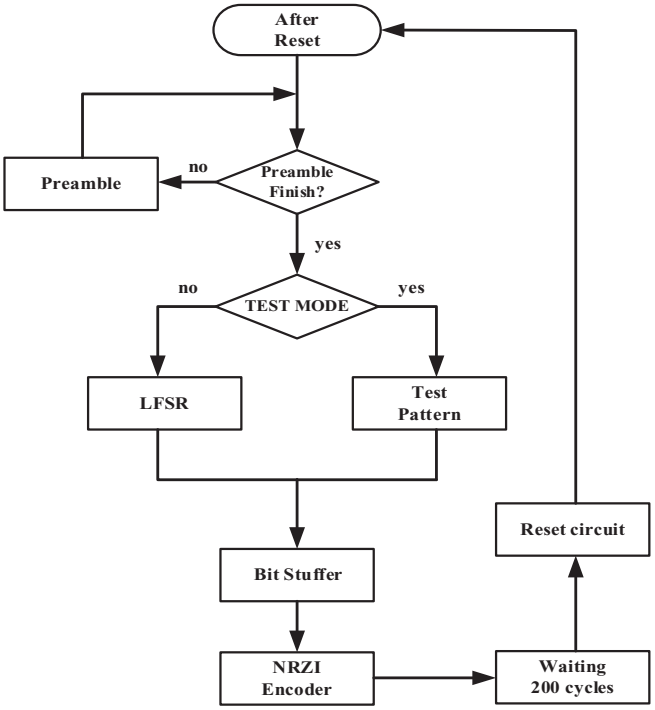


Fig. 4. TX flowchart.

Fig. 5(a) shows the architecture of the proposed reference-less receiver, which consists of an ADCDR, an RX state machine, a demodulator, and an LFSR checker. In the beginning, the gain calculator in the ADCDR uses the preamble pattern in front of the packet to calculate the gain value for the ADCDR controller. Consequently, the signal AFE_OUT sends to the ADCDR to perform the clock and data recovery. After that, the demodulator demodulates the encoding data (ENC_DATA) and generates the recovery data (RCY_DATA). The RX state machine resets the circuit if a packet is received. The LFSR checker circuit generates the random pattern sequence, which is the same as the LFSR circuit in the TX, and checks whether there are bit errors in the RCY_DATA. Fig. 5(b) shows the timing diagram of the receiver. First, the DCO_CODE is set to 2047 to calculate the period ratio (R_{max}) between the symbol period and the output of the DCO at the maximum DCO frequency output. Then, the DCO_CODE is set to 1023 to calculate another period ratio (R_{mid}) at the medium DCO frequency output. Second, the gain calculator calculates the gain value with the R_{max} and R_{mid}, and the detail operation is described in the Section 3. Third, the ADCDR starts to perform the frequency and phase tracking. Finally, when the ADCDR detects the SFD, the ADCDR starts the random data tracking.

Fig. 6 shows the receiver flowchart. First, the RX tracks the frequency and phase of the incoming data (AFE_OUT). Once the frequency and phase acquisition is complete, the ADCDR starts to recover the data. Then, after detecting the SFD, the NRZI decoder and bit unstuffer begins to demodulate the data. Finally, the RCY_DATA are sent to the LFSR checker circuit to check the bit error, and the RX state machine sends the RX_RST signal to reset the circuit.

The block diagram of the proposed ADCDR circuit is illustrated in Fig. 7. The proposed ADCDR circuit consists of a gain calculator, a phase and frequency detector (PFD), a digitally controlled oscillator (RX_DCO), a digital loop filter (DLF), an ADCDR controller, a frequency divider, a

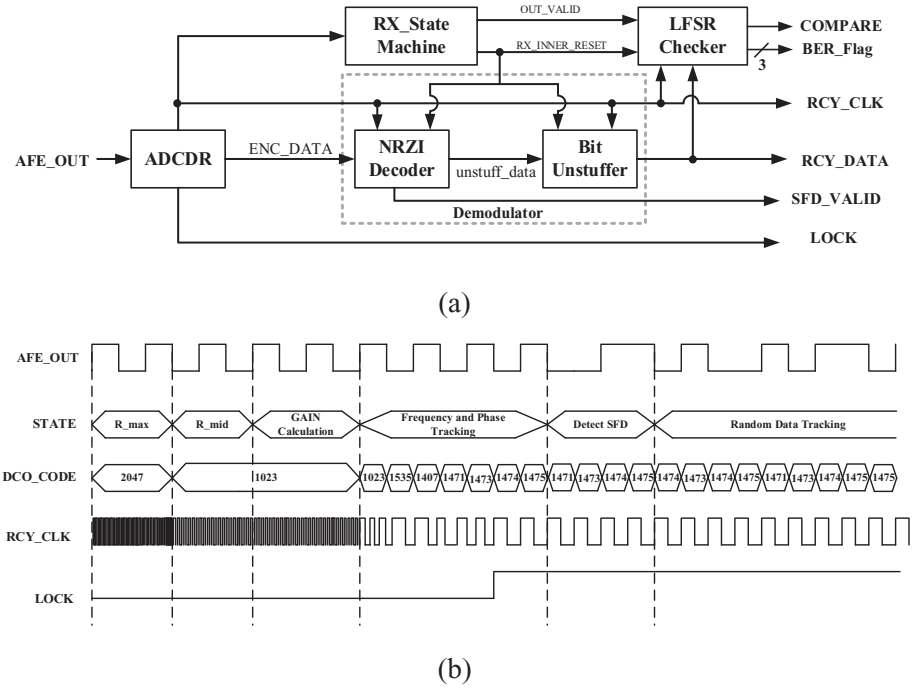


Fig. 5. (a) Architecture of the reference-less receiver and (b) Receiver timing diagram in preamble pattern.

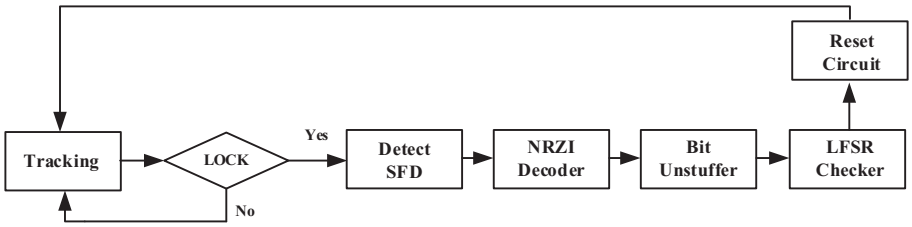


Fig. 6. RX flowchart.

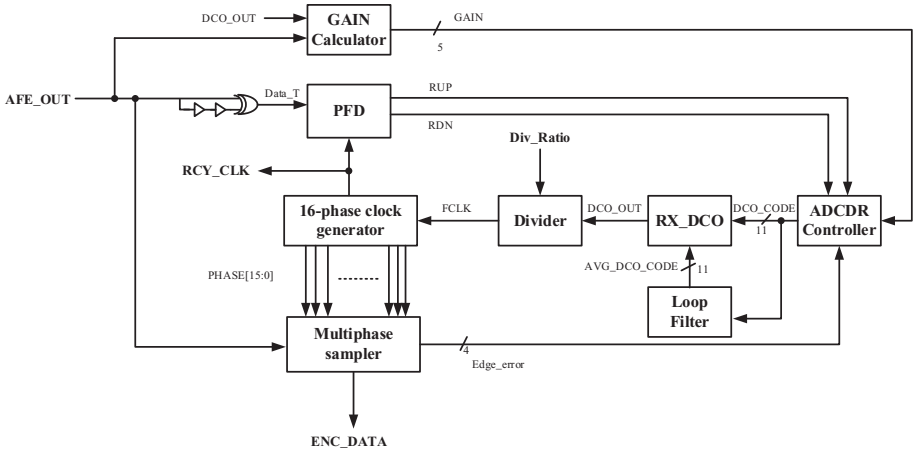


Fig. 7. The block diagram of the proposed ADCDR circuit.

divided-by-16 frequency divider, a 16-phase clock generator, and a multi-phase sampler. In the beginning, the input data are the preamble pattern and the input data (AFE_OUT) are delayed and generate the data transition signal (Data_T). Then, the PFD compares the phase and frequency error between the signal Data_T and the recovery clock (RCY_CLK), after which it generates the signal RUP or RDN to the ADCDR controller. The ADCDR controller uses the binary search approach to adjust the DCO_CODE, which speeds up the frequency and phase acquisition process. When the frequency and the phase acquisition is complete, the frequency of the RX_DCO output (DCO_OUT) is sixteen times the data rate, and the ADCDR changes to the phase tracking process and disables the PFD circuit.

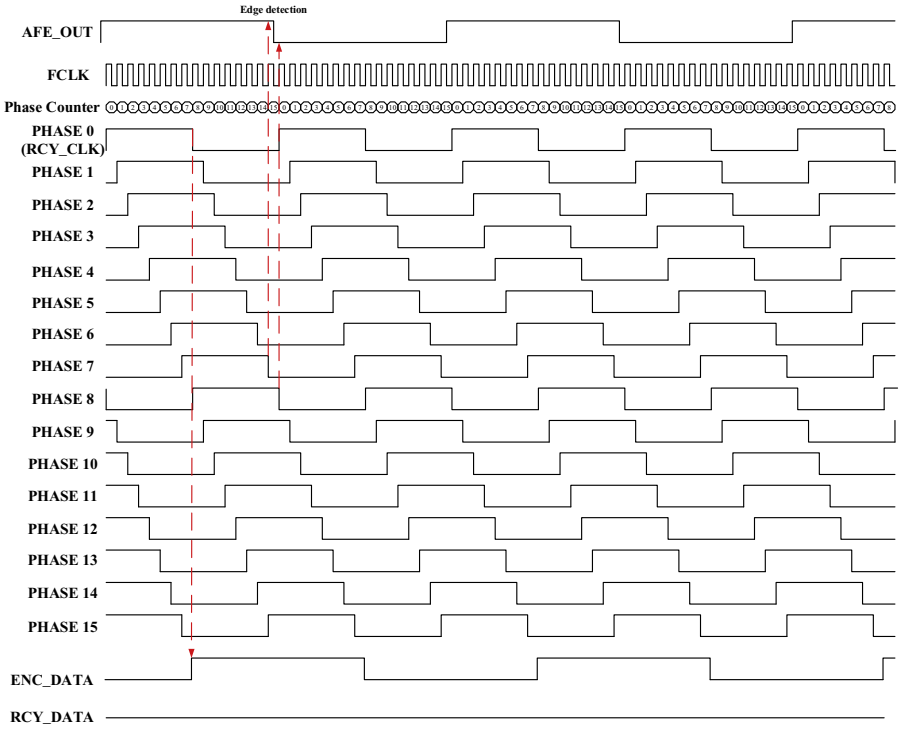
In the phase tracking with random data bits, the multi-phase sampler uses 16 multi-phases to sample the AFE_OUT and detects the edge transition of the data bits. According to the edge detection, the difference (Edge_error) between the current edge position and the ideal edge position can be calculated. Therefore, the phase error can be detected and compensated. In addition, the DCO_CODE is sent to the DLF to generate the baseline DCO control code (AVG_DCO_CODE) in order to stabilize the RX_DCO output clock (DCO_OUT). Finally, the multi-phase sampler recovers the data (ENC_DATA) and sends the data to the NRZI decoder.

When the frequency and phase acquisition is completed, the 16-phase clock generator uses the FCLK and a phase counter to generate the 16 multi-phases in one symbol period. Here, PHASE0 means the counter is 0, and PHASE1 means the counter is 1, and so on. Fig. 8(a) shows the timing diagram of the phase error detection in the no phase error case. The negative edges of the multi-phase signals are used to oversample the data. When no phase error exists, the rising transition of the PHASE0 (RCY_CLK) aligns with the data transition of the AFE_OUT, so the negative edges of the PHASE0 move to the center of the symbol period. Therefore, the data transition of the AFE_OUT falls between the negative edges of the PHASE7 and PHASE8.

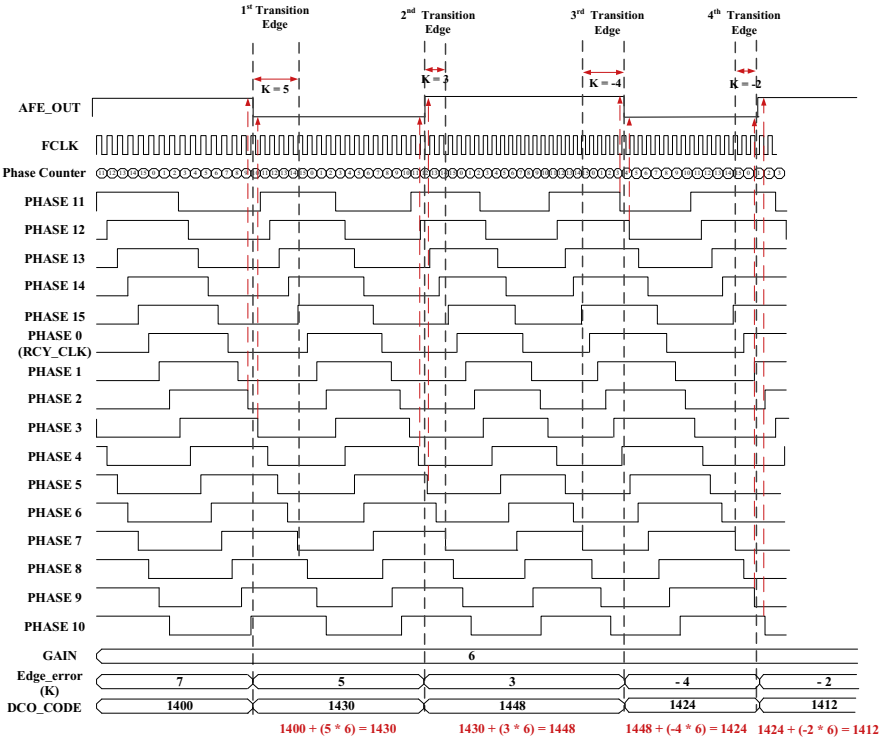
Fig. 8(b) shows the timing diagram of the phase error detection. In the phase leading case, the data transition edge of the AFE_OUT leads the rising edge of the PHASE0 (RCY_CLK). As shown in Fig. 8(b), at first transition edge (1st Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE2 and PHASE3, and the phase error to the ideal data transition position ([PHASE7, PHASE8]) is five times the FCLK periods (K is 5). Then, the phase error (Edge_error) (K) is multiplied by the GAIN and added to the DCO_CODE. At the second transition edge (2nd Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of PHASE4 and PHASE5, which means the phase error is three times the FCLK periods. Then, the phase error (Edge_error) (K) is multiplied by the GAIN and be added to the DCO_CODE.

In the phase lagging case, the data transition edge of the AFE_OUT lags the rising edge of the PHASE0 (RCY_CLK). As shown in Fig. 8, at the third transition edge (3rd Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE11 and PHASE12, and the phase error (Edge_error) (K) is quantized as −4. Then, the phase error (Edge_error) (K) is multiplied by the GAIN and added to the DCO_CODE, thus decreasing the DCO_CODE latter. At the fourth transition edge (4th Transition Edge), the data transition edge of the AFE_OUT falls between the negative edges of the PHASE9 and PHASE10, and the phase error (Edge_error) (K) is quantized as −2. Then, the phase error (Edge_error) (K) is multiplied by the GAIN and added to the DCO_CODE. Therefore, the 16 multi-phases can be used to detect the data transition edge, quantize the phase error, and then quickly compensate for the phase error.

Fig. 9 shows the compensation flow of the controller with the random data input. If there are phase polarity changes, the DCO_CODE is restored to the AVG_DCO_CODE of the loop filter and is added by the Edge_error (K) multiplied by the GAIN. If there is no polarity change, the DCO_CODE adds the current DCO_CODE by the Edge_error (K) multiplied by the GAIN.



(a)



(b)

Fig. 8. (a) Timing diagram of the phase error detection in no phase error case and (b) Timing diagram of the phase error detection.

3. Automatic phase track gain calibration

The function of the gain calculator is to calculate the gain value. Given that the DCO resolution varies with the PVT variations, we propose a method to calibrate the value of GAIN and ensure the compensation for the same phase error is maintained at different PVT conditions. In order to calculate the gain, we denoted the P_{mid}, P_{min}, and P_{ref} as follows. The proposed DCO has 11-bit control, and the P_{mid} and P_{min} mean the DCO period when the DCO_CODE is set to the medium (i.e., DCO_CODE = 1023) and maximum (i.e., DCO_CODE = 2047) values, respec-

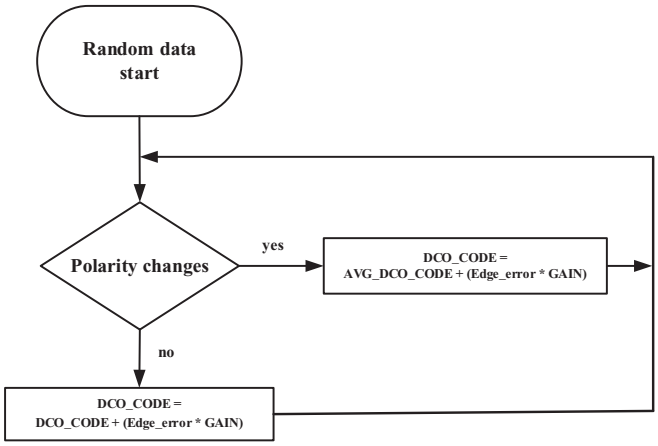


Fig. 9. Compensation flow with random data input.

tively. Here, P_{ref} refers to the symbol period of the data. Then, the definition of the R_{mid} and the R_{max} are the ratio between a symbol period (P_{ref}) and the DCO clock (DCO_OUT) period at the median and maximum frequencies, respectively. The counters are used to calculate the R_{mid} and the R_{max}, and their mathematical formulas are expressed in Eqs. (1) and (2), respectively.

$$R_{mid} = \frac{P_{ref}}{P_{mid}} \tag{1}$$

$$R_{max} = \frac{P_{ref}}{P_{min}} \tag{2}$$

Moreover, the period of the DCO is linear with the DCO_CODE, and thus, P_{mid} can be expressed with P_{min} and the DCO resolution (Δ). Therefore, the R_{mid} can be expressed as Eq. (3). In addition, the R_{mid} is the period ratio when the DCO_CODE is set to 1023, thus Eq. (4) is derived. Consequently, Eqs. (5) and (6) are derived. In Eq. (7), the R_{mid} is expressed in terms of R_{max}, Δ, and P_{ref}.

$$R_{mid} = \frac{P_{ref}}{P_{min} + (2047 - DCO\_CODE)\Delta} \tag{3}$$

$$R_{mid} = \frac{P_{ref}}{P_{min} + 1024\Delta} \tag{4}$$

$$R_{mid} = \frac{1}{\frac{P_{min}+1024\Delta}{P_{ref}}} \tag{5}$$

$$R_{mid} = \frac{1}{\frac{P_{min}}{P_{ref}} + \frac{1024\Delta}{P_{ref}}} \tag{6}$$

$$R_{mid} = \frac{1}{\frac{1}{R_{max}} + \frac{1024\Delta}{P_{ref}}} \tag{7}$$

According to Eq. (7), we can derive Eqs. (8)–(10).

$$\frac{1}{R_{max}} + \frac{1024\Delta}{P_{ref}} = \frac{1}{R_{mid}} \tag{8}$$

$$\frac{1024\Delta}{P_{ref}} = \frac{1}{R_{mid}} - \frac{1}{R_{max}} \tag{9}$$

$$\frac{\Delta}{P_{ref}} = \frac{\left(\frac{1}{R_{mid}} - \frac{1}{R_{max}}\right)}{1024} \tag{10}$$

According to Eq. (10), we can derive Eqs. (11)–(13). Finally, the ratios between the symbol period (P_{ref}) and the DCO resolution (Δ) can be expressed in terms of R_{mid} and R_{max}.

$$\frac{P_{ref}}{\Delta} = \frac{1024}{\left(\frac{1}{R_{mid}} - \frac{1}{R_{max}}\right)} \tag{11}$$

$$\frac{P_{ref}}{\Delta} = \frac{1024}{\left(\frac{R_{max} - R_{mid}}{R_{mid} \times R_{max}}\right)} \tag{12}$$

$$\frac{P_{ref}}{\Delta} = \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \tag{13}$$

When the frequency and phase acquisition is complete, the symbol period (P_{ref}) is 16 times of the DCO period (FCLK), as shown in Fig. 8. Thus, the symbol period (P_{ref}) can be expressed as Eq. (14), where N is the divided ratio of the frequency divider, which is shown in Fig. 7. Therefore, we express the $\frac{P_{ref}}{\Delta}$ in another way, as shown in Eq. (15). Hence, Eq. (16) is derived.

$$P_{ref} = 16 \times P_{FCLK} = 16 \times (N \times (P_{min} + (2047 - DCD\_CODE) \times \Delta)) \tag{14}$$

$$\frac{P_{ref}}{\Delta} = \frac{16 \times (N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta))}{\Delta} \tag{15}$$

$$\frac{P_{ref}}{\Delta} = 16 \times N \times \left(\frac{P_{min}}{\Delta} + (2047 - DCO\_CODE)\right) \tag{16}$$

According to Eq. (16), we can obtain the ratio between the minimum DCO clock period (P_{min}) and the DCO resolution (Δ), as shown in Eq. (17).

$$\frac{P_{min}}{\Delta} = \frac{P_{ref}}{16 \times N \times \Delta} - (2047 - DCO\_CODE) \tag{17}$$

The multi-phase generated from the FCLK are used to quantize the phase error. If the phase error (Edge_error) is equal to K FCLK cycles, then the phase error is K multiplied by the period of the FLCK, as shown in Eq. (18).

$$Phase\ Error = K \times (N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta)) \tag{18}$$

The value of the K is changed in each phase error detection (edge detection). In Fig. 7, the DCO_OUT is divided by a frequency divider (N) and a divided-by-16 divider to generate the multi-phase signals. Moreover, we compensate for eighth of the detected phase error in order to stabilize the DCO_CODE. Then, the gain value (GAIN) is described as Eq. (19). Here GAIN means the required addition/subtraction value to the DCO_CODE when K is equal to 1.

$$GAIN = \frac{N \times (P_{min} + (2047 - DCO\_CODE) \times \Delta)}{8 \times 16 \times N \times \Delta} \tag{19}$$

$$GAIN = \frac{1}{8 \times 16} \times \left(\frac{P_{min}}{\Delta} + (2047 - \text{DCO\_CODE})\right) \tag{20}$$

The variable $\frac{P_{min}}{\Delta}$ in Eq. (20) can be substituted by Eq. (17), so that Eq. (21) can be derived. Moreover, $\frac{P_{ref}}{\Delta}$ in Eq. (21) can be substituted by Eq. (13), from which Eq. (22) can be derived.

$$GAIN = \frac{1}{8 \times 16} \times \frac{P_{ref}}{16 \times N \times \Delta} \tag{21}$$

$$GAIN = \frac{1}{8 \times 16 \times 16 \times N} \times \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \tag{22}$$

The gain value is expressed in terms of the divide ratio of the frequency divider (N), R_{mid} and R_{max}. Therefore, we can estimate the gain value by Eq. (22) with the preamble patterns, and we can have the same amount compensation for the detected phase error under the PVT

variations.

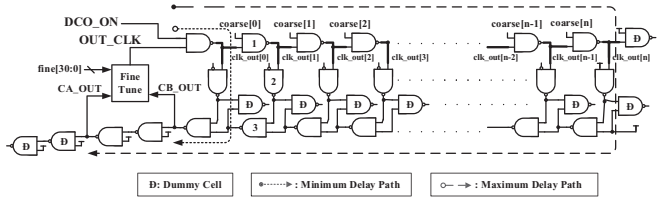
4. Circuit implementation

Fig. 10(a) shows the architecture of the monotonic response DCO, which consists of a coarse-tuning delay line [16] and a fine-tuning delay line [17] in our previous works. The coarse-tuning delay line uses 63 coarse-delay cells (CDCs), and each CDC is composed of four NAND gates. The 1st NAND gate is used to decide whether the CDC is enabled or disabled. Then, the 2nd and 3rd NAND gates are used to provide the delay. Therefore, the coarse-tuning resolution is the delay time of the two NAND gates. In addition, to balance the rise time and fall time, the 4th NAND gate is used as the dummy cell so that the duty cycle will not be distorted. The delay of the CDC is controlled by the 63 bits of the coarse control code (coarse [62:0]). If all of the 63 bits are set to the logic 1, the CDC will provide the maximum delay. Conversely, if all of the 63 bits are set to logic 0, the CDC provides the minimum delay.

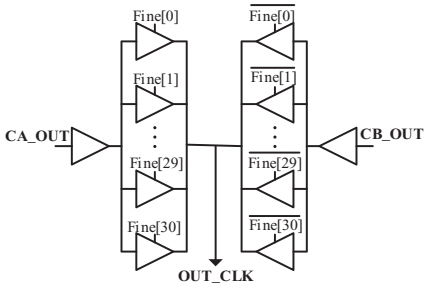
Fig. 10(b) shows the fine-tuning architecture of the DCO. It consists of two parallel connected tri-state buffer arrays [17] in our previous work. The two parallel connected tri-state buffer arrays are controlled by the 31 bits of the fine control code (Fine [30:0]). As the total delay controllable range of the fine-tuning range is equal to the resolution of the coarse-tuning stage, the DCO maintains the monotonicity. In addition, the DCO decoder is used to convert the DCO_CODE into the thermometer code. The DCO_CODE is 11 bits, the DCO_CODE [10:5] is converted to coarse [62:0], and the DCO_CODE [4:0] is converted to Fine [31:0].

The goal of the DLF [18] in our previous works (shown in Fig. 7) is to stabilize the DCO_CODE and maintain the output frequency. In the beginning, the DCO_CODE is sent to the DLF from the ADCDR controller. When the DLF receives the four DCO control codes, it generates the baseline DCO control code (AVG_DCO_CODE). Consequently, every two new DCO control codes are sent to the DLF and the DLF sorts the DCO control codes. Then, the DLF removes the maximum and the minimum DCO control codes in its register file, and takes the average of the rest DCO control codes to generate a new baseline DCO control code to maintain the frequency. Finally, the AVG_DCO_CODE is used in the ADCDR when there occurs a polarity change in maintaining the phase, as indicated in Fig. 9.

The proposed WBS BCC transceiver is implemented using a 90-nm standard performance (SP) CMOS process with standard cells. The layout of the WBS BCC transceiver is shown in Fig. 11. The core area is



(a)



(b)

Fig. 10. (a) The proposed DCO (b) The fine-tuning circuit of the proposed DCO.

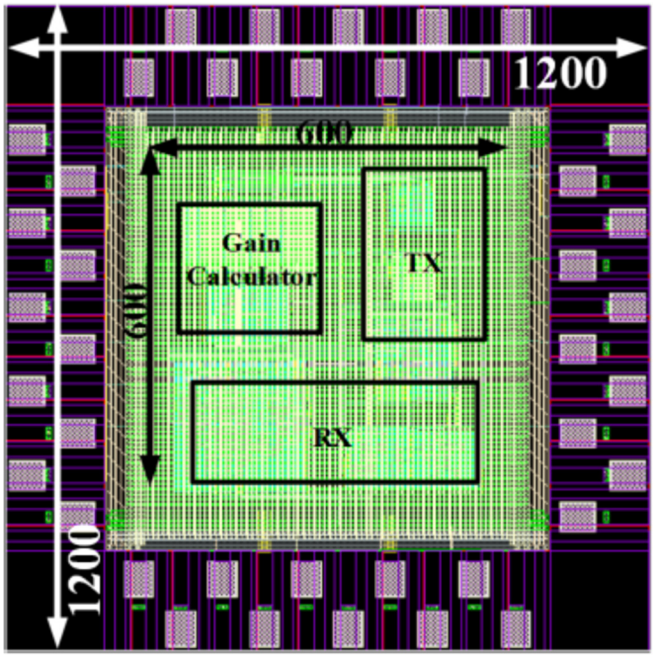


Fig. 11. Layout of the proposed WBS BCC transceiver.

$600 \times 600\ \mu m^2$, and the chip area, including the I/O pads, is $1200 \times 1200\ \mu m^2$. The chip consists of a TX circuit, an RX circuit, and a gain calculator.

Fig. 12 shows the gain values at different data rates of the proposed WBS BCC transceiver by the post-layout simulation. As the data rate increases, the gain value decreases. In addition, for low-frequency generation, we add a frequency divider to increase the frequency range of the DCO. At high data rate, the divided ratio of the divider (N) is set to 1. However, at low data rate, the divided ratio (N) is not 1, and the gain value must be divided by N, as shown in Eq. (22). Therefore, the gain value shows a non-linear increase as the data rate decreases. Moreover, because the body temperature range is very narrow, Fig. 12 shows the gain value with different supply voltages at 36 °C and 40 °C. At all listed conditions, the gain values are similar. Therefore, temperature and voltage variations do not seriously affect the gain value.

Fig. 13 shows the first bit error simulation results with different CID at 20 Mbps. As CID is reduced, more data transitions occur. Therefore, the ADCDR can track the phase error more easily and improve its BER performance. In the proposed ADCDR, CID is set to 3, and the BCC transceiver has a BER $<10^{-7}$ with 10 ns peak-to-peak random data jitter.

Fig. 14 shows the first bit error simulation result at 20 Mbps with different oversampling rates. The simulation results show that the BER

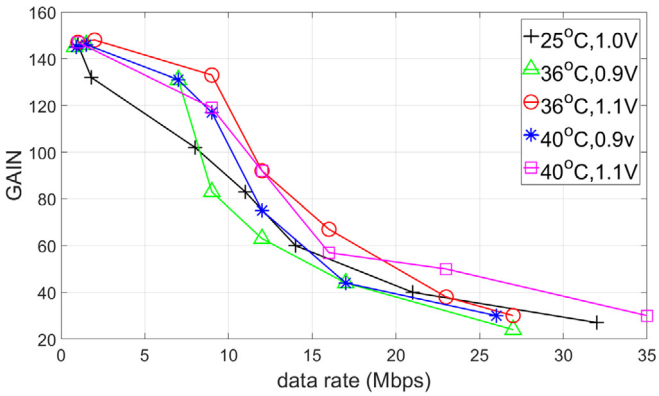


Fig. 12. The gain value at different data rate.

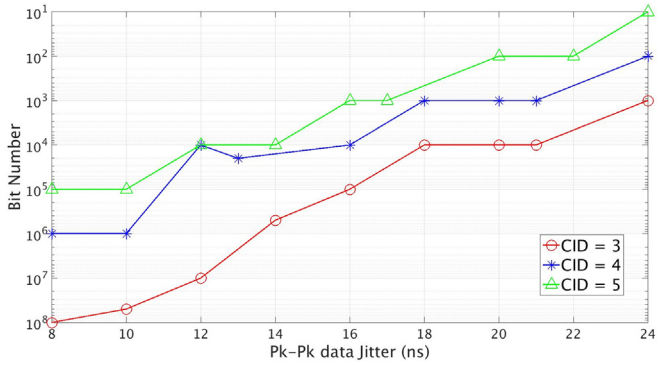


Fig. 13. Error-Free simulation result at 20 Mbps with different CID.

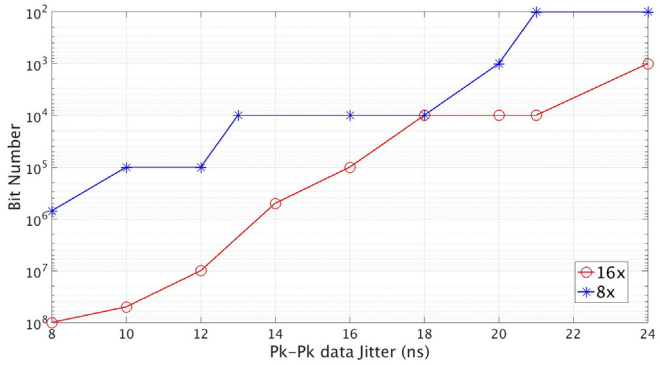


Fig. 14. Error-Free simulation result at 20 Mbps with different oversampling rate.

performance with 10 ns peak-to-peak random data jitter of 16× and 8× oversampling rate in the ADCDR circuit are $<10^{-7}$ and $<10^{-5}$, respectively. Thus, the proposed ADCDR uses 16× oversampling rate.

In order to stabilize the DCO_CODE, the ADCDR controller only compensates for eighth of the detected phase error (gain ratio is 1/8), as explained in Eq. (19). Fig. 15 shows the bit error-free simulation result at 20 Mbps with different gain ratios. If the gain ratio is too large, the DCO_CODE will have large variations and the data jitter tolerance would decrease accordingly. In addition, when the gain ratio is reduced, the jitter tolerance converges; thus, the gain ratio 1/8 is chosen.

In the jitter tolerance testing of the BCC receiver, the data transmitted are modulated with a sinusoidal jitter. Therefore, the input data have a regular jitter frequency and the data rate has variations. Fig. 16 shows the sinusoidal jitter tolerance of the proposed ADCDR circuit at 20 Mbps. The corner frequency is at 1 MHz with 0.8 UI (unit interval) jitter tolerance.

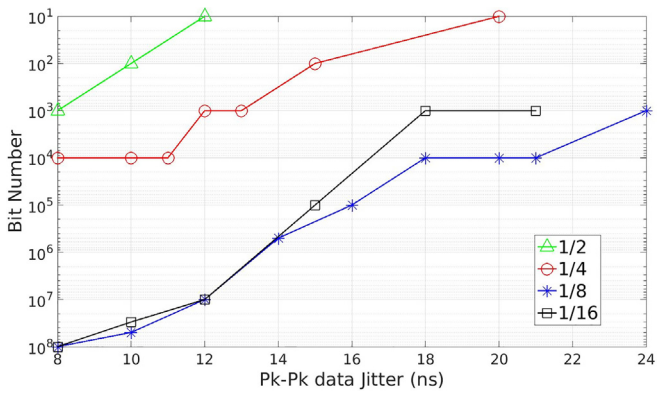


Fig. 15. Error-Free simulation result at 20 Mbps with different gain ratio.

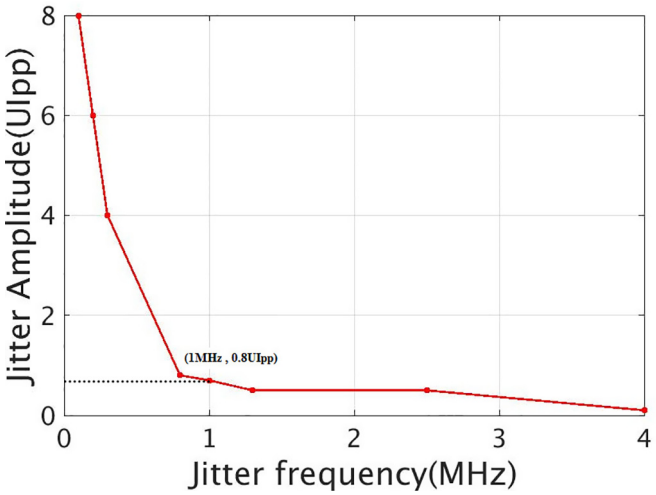


Fig. 16. Sinusoidal jitter tolerance performance.

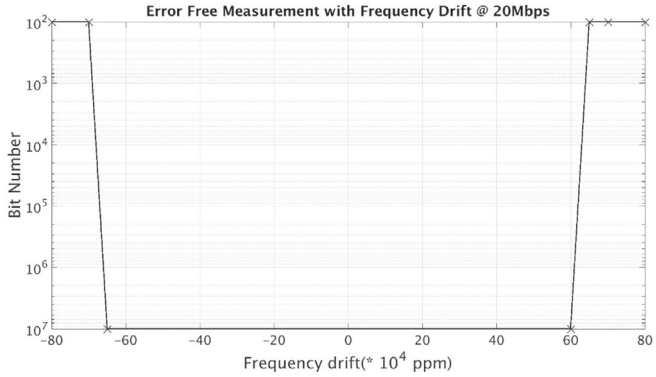


Fig. 17. Error-Free measurement with different frequency drift at 20 Mbps

When the baud rate of the transmitter differs from the expected data rate, this leads to the frequency drift problem in the BCC receiver. Fig. 17 shows the bit error-free simulation results with different frequency drifts at 20 Mbps. The performance of the ADCDR has a BER $<10^{-7}$ within the frequency drift range from −650,000 to +600,000 ppm at 20 Mbps. The adjustable DCO frequency range is from 110 to 512 MHz. If the ratio of the frequency divider (N) is set to 1, the RCY_CLK frequency range is from 6.875 to 32 MHz. Therefore, if the data rate of the TX is beyond the range of 6.875 to 32 Mbps, it may lead to bit errors. The proposed reference-less ADCDR circuit has the frequency and phase tracking ability. Thus, if the DCO can generate the required 16× oversampling clock, the BER becomes $<10^{-7}$ within the frequency drift range in the proposed reference-less ADCDR circuit.

Table 1 lists the performance comparison of the proposed design and state-of-the-art BCC designs. The area of the proposed design is smaller than those of other BCC designs. Although [9,10] achieved higher data rate, they also have required higher power consumption as compared with the proposed design. In addition, they also use the high frequency band to transmit the data so that they may interfere with other electronic products. Moreover, the proposed design also has higher data rates than those reported in Refs. [5,8,14,15].

5. Conclusion

In this paper, the proposed ADCDR circuit for human body channel communication adopts the reference-less architecture, which has no external reference clock nor a frequency synthesizer, to reduce the power

Table 1
Performance comparisons.

	[14] JSSC'07	[15] BioCAS'17	[8] JSSC'12	[9] ISSCC'14	[5] JSSC'17	[10] JSSC'16	Proposed
Communication Method	Wideband Signaling	GFSK	FSK	3-level Walsh Coding	OFDM	BPSK	Wideband Signaling
Process	0.25 μm	0.18 μm	0.18 μm	65 nm	65 nm	65 nm	90 nm
Supply	1 V	1.8 V	1 V	1.1 V	1.1 V	1.2 V	1 V
Frequency band	Wideband	200 kHz	40–120 MHz	40–80 MHz	20–120 MHz	20–60 MHz、140–180 MHz	1–40 MHz
Data Rate	2 Mb/s	100 kb/s	1 kb/s ~ 10 Mb/s	60 Mb/s	1 Mb/s	80 Mb/s	1 Mb/s ~ 20 Mb/s
Bit Error Rate	$<10^{-7}$	$<10^{-3}$	$<10^{-5}$	$<10^{-5}$	$<10^{-7}$	$<10^{-5}$	$<10^{-7}$
Frequency Drift Tolerance	N/A	±12.5%	±10%	N/A	N/A	N/A	±60%
Power Consumption	0.2 mW	2.65 mW	4.4 mW	10.87 mW	2.5 mW	6.3 mW	2.2 mW (w/o AFE circuit)
Area	0.85 mm^2	0.47 mm^2	4.5 mm^2	0.85 mm^2	2.13 mm^2	5.76 mm^2	0.36 mm^2
Experimental Results Type	Measurement	Measurement	Measurement	Measurement	Measurement	Measurement	Simulation

consumption and enhance the frequency drift tolerance. Moreover, by using the 16 phases to detect the data transition edge position and quantize the phase error, we are able to enhance the frequency and phase tracking ability. The proposed automatic phase track gain calibration can maintain the gain value under PVT variations to enhance the stability of the ADCDR circuit. As a result, the proposed WBS BCC transceiver can achieve a BER performance $<10^{-7}$ at 20 Mbps with 2.2 mW power consumption and 0.36 mm^2 chip area.

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