20.5 A sub-mW Multi-Tone CDMA Baseband Transceiver Chipset for Wireless Body Area Network Applications

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Ubiquitous personal healthcare inspection (uPHI) in a wireless body area network (WBAN) requires continuous signal monitoring up to several days or even longer. To enable cable-free body monitoring with μW biomedical acquisition devices [1,2], a sub-mW wireless transceiver is required for long-term observation. However, existing systems [3,4] have large power dissipation with poor interference-rejection capability, limiting device coexistence and the use of thin-film flexible-batteries. For better operation reliability in an environment with interference, the wireless medical telemetry service (WMTS) constraints defined in [5] are collectively considered. As a result, a multi-tone CDMA (MT-CDMA) baseband processor with a 31-chip spreading code is implemented in a wireless sensor node (WSN) and a central processing node (CPN), respectively, as shown in Fig. 20.5.1, for interference-free and reliable communications in body monitoring. In the battery-capacity-limited WSN, both dynamic and leakage power are optimized, comprising μW-scale power dissipation for extended body-signal monitoring. This power optimization is achieved using a power island approach with the techniques of multi-V_t CMOS (MVTCMOS), multiple supply voltage (MSV) domains, and distributed coarse-grain power-gating cells (DCG-PGC), improving the operating duration by 11×. For better system performance, the CPN applies both adaptive I/Q-mismatch calibration (A-IQMC) and dynamic sampling-timing control (DSTC) with phase-tunable clock generation (PTCG) [6] to further improve system SNR by 2.2dB and reduce power dissipation in the ADC by 43.75%.

Figure 20.5.1 shows the proposed uPHI-WSN and uPHI-CPN in a coexistence scenario. This transceiver pair may connect with various possible sensor categories and achieves a maximum datarate of 143kb/s for a maximum 10-WSN coexistence, providing large interference-rejection capability and better system reliability. Because uPHI-WSN/CPN communicates with a datarate much higher than a human body's sensor signal rate in this work, a WSN stays asleep for most of time (sleep-phase) and transmits data in a burst mode (active-phase). Therefore, leakage power minimization is emphasized for this long-sleep operation. When an ECG is considered as a body signal source with 16b samples at a sampling rate of 500-samples/s, a 2048×16b SRAM is designed into the WSN. This SRAM size has an optimum leakage saving efficiency, resulting in a 6.96% active-sleep duty cycle. The sampled signals from the sensor are modulated by QPSK with a 16-point IFFT, where the subcarrier allocation follows the conjugate-symmetric rule to further reduce by 50% the DAC and front-end circuit area and power. Then, the baseband signal is transmitted at 5M chip/s. In the CPN on the receiver side, the A-IQMC circuit is provided to compensate for gain and phase signal distortion. Also, a DSTC is applied for best sample timing search with the aid of the PTCG circuit, which provides 5MHz 8-phase evenly spaced clock phases for selection. Each clock phase is separated by 25ns.

Figure 20.5.2 shows the proposed WSN design, including the main functional blocks, MVTCMOS, MSV domains, and DCG-PGC. In the sleep-phase, the SRAM continuously stores the sensed body-signals. As the SRAM becomes nearly full, the MT-CDMA modulator is powered-on (active-phase) to modulate the stored data using the main functional blocks, including constellation mapper, conjugate-symmetric frequency-domain spreading, IFFT, and time-domain user-code spreading. To minimize the dynamic power consumed in the active-phase, the supply voltage for the modulator is scaled from 1.2V to 0.8V, which is implemented in low-V_t cells to enable low voltage supply operation, resulting in 60.89% dynamic power reduction. To further reduce the modulator's leakage power consumed during the sleep-phase, the column-style NMOS DCG-PGC is distributed between the global VCC and local virtual-VCC (VCCV) as a power controlling switch to cut off any possible leakage current path, resulting in a 99.92% leakage power reduction. In the always-on power domain, only low-rate operation components are activated, including both the SRAM and control unit, which consumes more leakage power than dynamic power. Therefore, low-leakage (high-V_t) cells are selected for this domain. Between these two power domains level-shifters are used to establish correct signal levels and isolation cells for tie-high/low signal levels when the signal source comes from a power-off domain.

Figure 20.5.3 shows the CPN architecture. A DSTC is applied to enable ADC circuits to sample the incoming signals with the symbol rate and maintain the sampled signal integrity. This is achieved by a PTCG, which consists of an ADDLL providing 8-phase evenly-spaced clock phases for selection. This DSTC approach prevents ADC circuits from sampling data above the Nyquist rate, saving 43.75% ADC power. To further improve the system reliability and signal decoding quality, an adaptive I/Q-mismatch calibration is applied with 2dB gain error (GE) and 20° phase error (PE) calibration range [6].

Figure 20.5.4 shows the MT-CDMA modulator power profile during active-to-sleep and sleep-to-active phases. In the sleep phase, the modulator sinks only 15.2nA with the proposed DCG-PGC design, resulting in 99.92% leakage reduction compared to the non-DCG-PGC approach. The averaged simulation current consumed 95.8μA and 18.89μA in the active-phase and sleep-phase, respectively. The turn-on time takes 9.16ns for VCCV to be restored to a stable voltage level. Figure 20.5.5 shows the overall system performance decoded in the CPN. With DSTC, the PER is improved by 0.9dB SNR due to higher integrity in the sampled signals. With A-IQMC, the performance yields a 1.3dB SNR improvement, more than the non-adaptive approach in [6]. With respect to coexistence performance, the MT-CDMA enables 10 uPHI-WSN/CPN cooperation (9-interferer to 1-victim) within 1 meter, shortening the interference-free operation distance by 95% compared to existing systems [3,4].

The MT-CDMA WBAN baseband transceiver is fabricated in 0.13μm 1P8M CMOS. Figure 20.5.6 presents the chip summary and Fig. 20.5.7 shows the chip micrograph. The MT-CDMA is designed in the uPHI system for 10-WSN/CPN 1-meter reliable coexistence. For extended monitoring, the WSN consumes 21μW with 60.89% dynamic and 99.92% leakage power reduction (a total of 90.91% power reduction in a 6.96% duty cycle) using duty-cycle control with a power island approach. For system performance, the CPN with the proposed A-IQMC and DSTC has a total 2.2dB SNR improvement. Therefore, this uPHI system with the WSN and CPN achieves ubiquitous extended operation time and high system reliability for WBAN applications.

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References:
[1] Refet Firat Yazicioglu, et. al., "A 60μW 60nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems," *ISSCC Dig. Tech. Papers*, pp. 56-57, Feb., 2006.
[2] Honglei Wu, and Yong Ping Xu, "A 1V 2.3μW Biomedical Signal Acquisition IC," *ISSCC Dig. Tech. Papers*, pp. 58-59, Feb., 2006.
[3] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)*, IEEE Standard 802.15.4, 2003
[4] *Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Wireless Personal Area Networks (WPANs)*, IEEE Standard 802.15.1, 2005.
[5] Federal Communications Commission, "Amendment of Parts 2 and 95 of the Commission's Rules to Create a Wireless Medical Telemetry Service," FCC Washington, D.C., Rep. FCC00-211, 2000.
[6] J.Y. Yu, et. al., "A 31.2mW UWB Baseband Transceiver with All-Digital I/Q mismatch Calibration and Dynamic Sampling," Symp. VLSI Circuits, pp. 290-291, June, 2006.

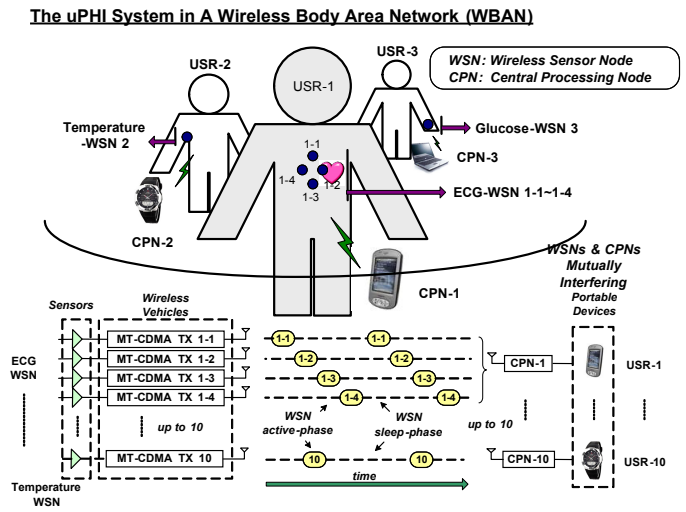

Figure 20.5.1: The proposed uPHI system in a WBAN.

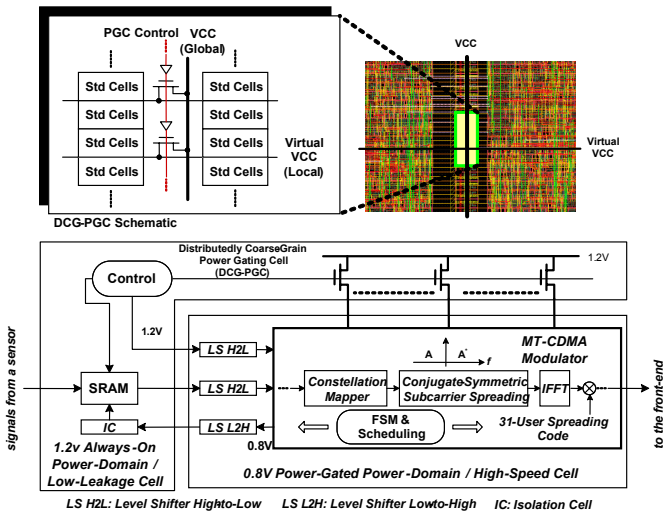

Figure 20.5.2: The WSN design.

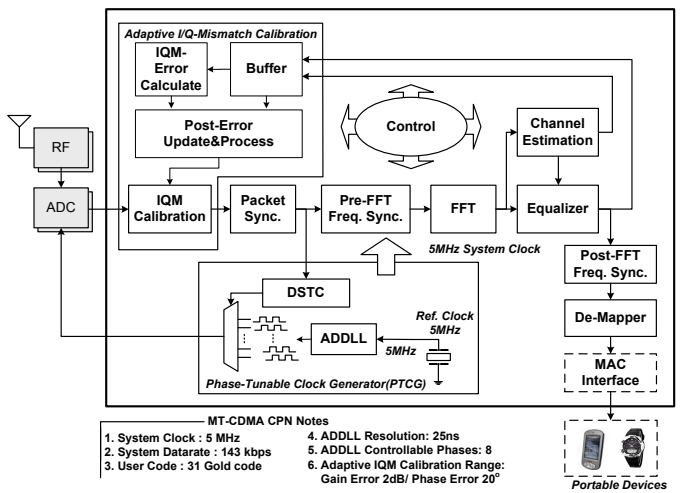

Figure 20.5.3: The CPN design.

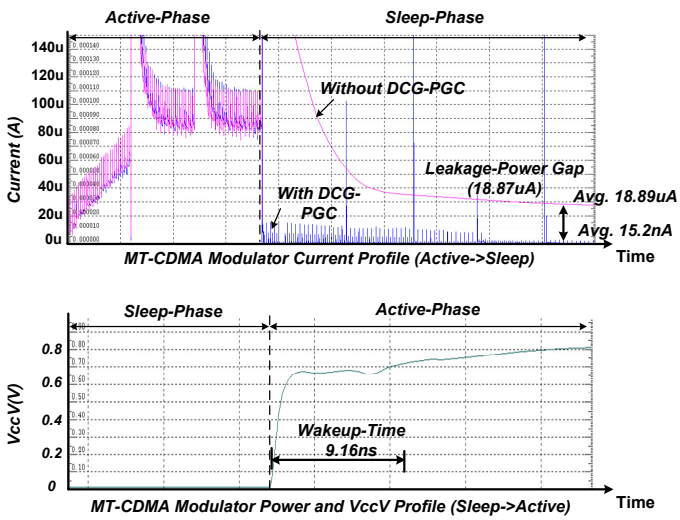

Figure 20.5.4: WSN behavior between active and sleep phases.

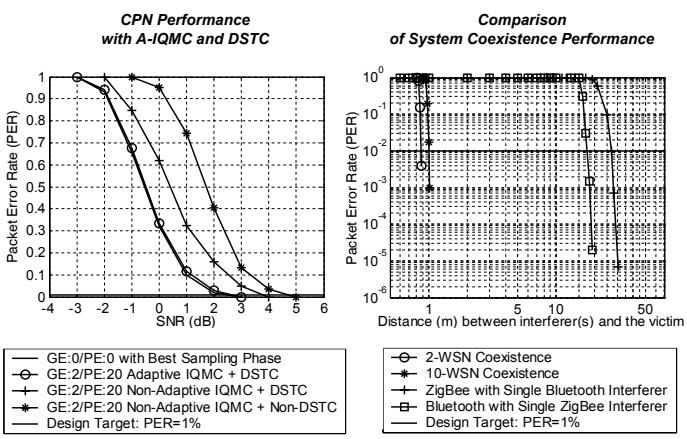

Figure 20.5.5: Single WSN-CPN and coexistence performance.

Technology		Standard 0.13µm High-Speed/Low-Leakage CMOS
Max Datarate		143kb/s
Max Signal Bandwidth		5MHz
Max WSN Coexistence		10
MT-CDMA WSN		
Die Size		1252µm x 1358.8µm
Measured Core Power		21µW@0.8V
MT-CDMA CPN		
Die Size		1842µm x 1842µm
Measured Core Power		566.4µW@0.8V
IQM Error Tolerance	Gain	2dB
	Phase	20°
PTCG Phase		8

Figure 20.5.6: Chip summary.

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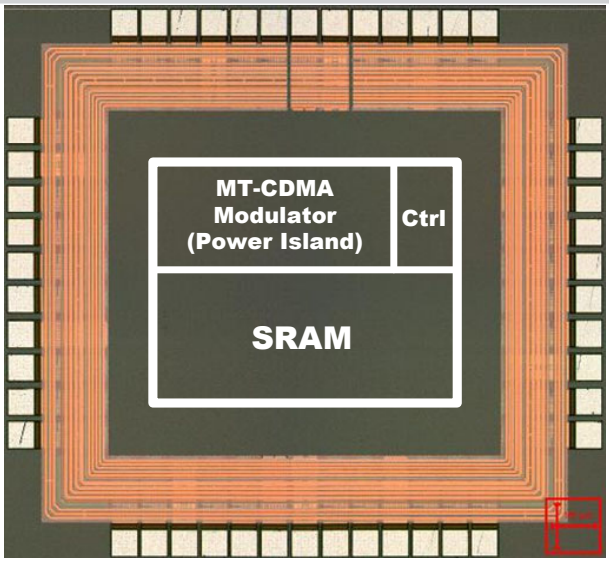

Figure 20.5.7: Chip micrograph.

