24.2 A 480Mb/s LDPC-COFDM-Based UWB Baseband Transceiver

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Coded OFDM (COFDM)-based baseband solutions provide up to 480Mb/s data rates for 528MHz ultra wideband (UWB) systems in the 3.1GHz to 10.6GHz RF band [1]. The design challenge for the baseband transceiver is to extend the signal bandwidth to 26.4 times wider than a WLAN system with acceptable design complexity and energy consumption. In this paper, a low-density parity-check (LDPC)-COFDM-based baseband transceiver achieving a 480Mb/s data rate and a 1.2nJ/bit energy use is presented. The circuit includes the LDPC codec, which has high parallelism for high-speed error correction. Figure 24.2.1 shows the system block diagram of the half-duplex transceiver. The circuit uses a 1.056GHz 5b I/Q DAC in the transmitter, a 528MHz 5b I/Q ADC in the receiver, and a low-rate 7b DAC for automatic gain control (AGC). It also achieves <6.0dB peak-to-average power ratio (PAPR) and satisfies the power spectral mask defined in [1]. The semi-regular LDPC codec provides 480Mb/s error correction with a partially-parallel architecture. A 128-point parallel pipelined (I)FFT and division-free channel equalizer are exploited to achieve the high throughput requirement. A 1.056GS/s transmitter throughput and 528MS/s receiver throughput are achieved.

Figure 24.2.2 shows the architecture of the LDPC decoder with block length 600 and code rate 3/4. The semi-regular and non-structured parity check matrix, which contains a fixed number of 1's in each column (3) and a variable number of 1's in each row (11~14), provides better performance than regular or structured LDPC codes. The decoder comprises 50 check-node units (CU) and 150 message-node units (MU). Pipelined registers are inserted to break down the combinational feedback into path 1 and path 2, leading to less routing congestion and shorter critical path delay. In the CUs, since each row of the parity-check check matrix contains at most 14 1's, the proposed algorithm finds the minimum value and the second minimum value from the 14 inputs, and each output takes its value from any input. The CS14 block shown in Fig. 24.2.2 implements the simple sorting to simultaneously update all edges connected to the same check node. To simplify the circuit in the CU, we use sign-magnitude notation to represent the metrics in memory. The MUs consist of adders and converters between two kinds of notations, 2's-complement (TC) and sign-magnitude (SM). The summed values are clipped with a slight loss of performance. The LDPC codec occupies 53.7% of the gate count of the baseband transceiver.

Figure 24.2.3 shows the architecture of the proposed 128-point (I)FFT design for UWB system. The throughput can be up to 528 MS/s with minimal hardware cost and low power consumption. This performance was achieved by adopting a novel parallel pipelined architecture. In the proposed (I)FFT, the mixed-radix FFT algorithm is realized to save power consumption by reducing the complex multiplications. A four-parallel architecture is adopted to implement the radix-2 FFT algorithm in stage 1. In order to reduce the required memory size, as shown in Fig. 24.2.3, a radix-8 FFT algorithm is implemented using two different structures in stage 2 and stage 3. Note that the hardware cost of the complex multiplier in stage 1 and stage 3 can be saved by rescheduling the time of the complex multiplications. Based on the proposed mixed-radix parallel pipelined architecture, the proposed FFT requires only 36.4% as much memory and 47.2% as many complex multipliers as a current high-throughput FFT design [2]. The FFT block uses 10.1% of the total gate count of the baseband transceiver.

Since the proposed baseband transceiver applies QPSK modulation, coded bits can be de-mapped without amplitude information. Thus a division-free channel equalizer that corrects symbols phases is developed to increase design throughput and reduce hardware complexity. Figure 24.2.4 shows the architecture of the division-free channel equalizer. In front of the proposed equalizer, an arc-tangent design converts received symbol from I/Q to phase. Hence the phase addition and subtraction can replace the symbol multiplication and division in a conventional equalizer. Moreover this arc-tangent design is improved by using a logarithm-based architecture. The logarithm-based subtraction can replace the division of the real and imaginary parts of input symbols to reach a true division-free equalizer. The proposed equalizer with a two-parallel architecture can achieve 528MS/s throughput. Including the arc-tangent design, the channel equalizer only uses 3.85% of the total gate count of the baseband transceiver.

Figure 24.2.5 shows the simulated maximum transmission distance for 8% packet error rate (PER) compared with the system requirements defined in [1]. The transmission distance is derived from sensitivities and 6.6dB noise figure [1]. Figure 24.2.6 and Fig. 24.2.7 show the chip micro-photo and chip performance summary respectively. The receiver energy consumption is 1.2nJ/bit, which is 60% of that used in a current WLAN approach [3]. By integrating these new LDPC, FFT, and equalizer designs, the proposed UWB baseband transceiver can achieve high data rates with acceptable system performance and low energy consumption.

References:

[1] A. Batra, et al., "Multi-Band OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a," submitted to *IEEE 802.15 TG3a,* March, 2004.

[2] J. García, J. A. Michel, and A. M. Burón, "VLSI Configurable Delay Commutator for A Pipeline Split Radix FFT Architecture," *IEEE Trans. Signal Processing,* vol. 47, pp. 3098-3107, Nov., 1999.

[3] W. Eberle, et al., "A Digital 72 Mb/s 64-QAM OFDM Transceiver for 5GHz Wireless LAN in 0.18μm CMOS," *ISSCC Dig. Tech. Papers,* pp. 336-337, Feb., 2001.

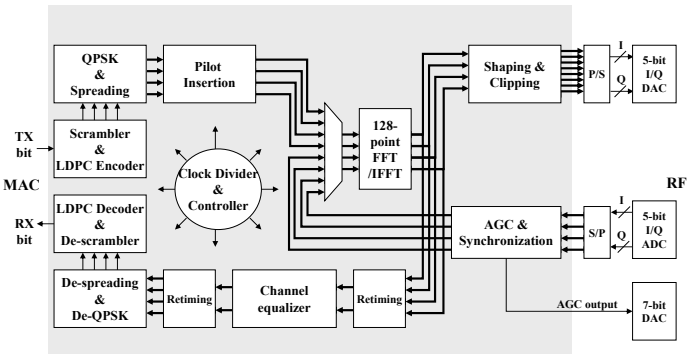

Figure 24.2.1: System block diagram.

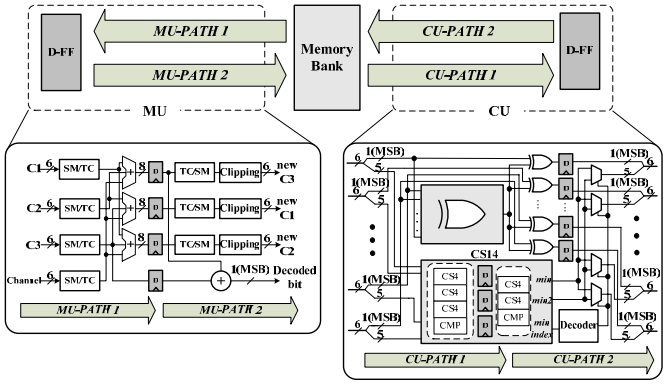

Figure 24.2.2: Architecture of the semi-regular LDPC decoder.

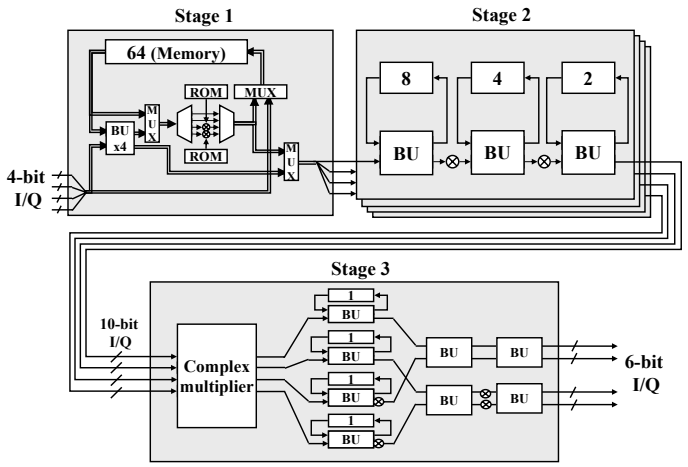

Figure 24.2.3: Architecture of the parallel pipelined (I)FFT design.

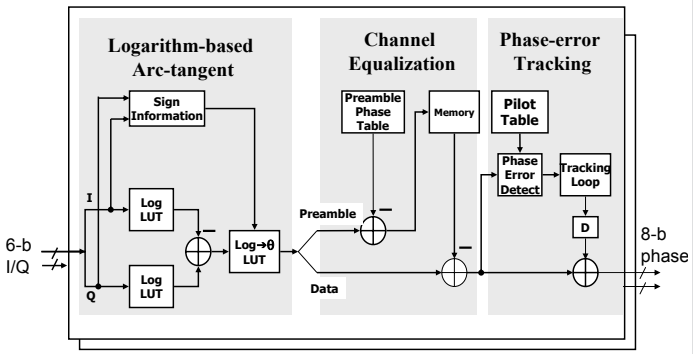

Figure 24.2.4: Architecture of the division-free channel equalizer.

Modulation and Coding Rate	Spreading Gain	Data Rate (Mb/s)	Proposed Design (meters)	System Requirement (meters)
QPSK 3/4	4	120	13.6	10
	2	240	11.2	4
	1	480	7.5	2

Figure 24.2.5: Maximum transmission distance for 8% PER.

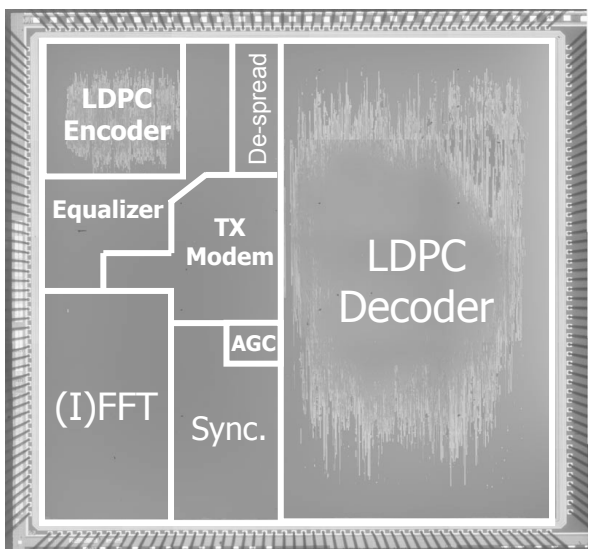

Figure 24.2.6: Chip micro-photo.

Continued on Page 609

Technology	Standard 0.18μm CMOS 1.8V core, 3.3V I/O
Die Size	6.5mm × 6.5mm
Package	208-pin CQFP
Transistor Count	4.26M
Max. Data Rate	480Mb/s
Max. Signal Bandwidth	528MHz
Max. System Clock	264MHz
Core power @ 480Mb/s (TX/RX)	523mW/575mW

Figure 24.2.7: Chip summary.

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