IEICE TRANS. FUNDAMENTALS, VOL.E87–A, NO.12 DECEMBER 2004

LETTER *Special Section on VLSI Design and CAD Algorithms*

A Novel Digitally-Controlled Varactor for Portable Delay Cell Design*

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SUMMARY In this paper, a novel digitally-controlled varactor (DCV) for portable delay cell design is presented. The proposed varactor uses the gate capacitance differences of NAND/NOR gates under different digital control inputs to build up a digitally-controlled varactor. Then the proposed varactor is applied to design a high resolution delay cell and to achieve a fine delay resolution. Different types of NAND/NOR gates (2-input or 3-input) for DCV design are also investigated in this paper. The proposed DCV can be implemented with standard cells, thus it can be easily ported to different processes in a short time. A test chip fabricated on a standard 0.35 μm CMOS 2P4M process proves that the proposed delay cell has a fine delay resolution about 1.55 ps. As a result, the proposed DCV exhibits finer resolution, better linearity, and better portability than traditional delay elements, and is very suitable for portable delay cell design.

key words: *portable delay element, digitally-controlled varactor (DCV), DLL, DCO, cell-based*

1. Introduction

Delay cells are extensively used in many applications, such as digitally-controlled oscillator (DCO) [1], Phase-Locked Loops (PLLs) [3], Delay-Locked Loops (DLLs), digital signal processor [4], [5] and memory circuits [6]. Among these circuits, delay cell is one of the key building blocks. Its precision and resolution directly affects overall system performance.

There are two major techniques for designing a fine resolution delay cell. One changes MOS driving strength dynamically with a fixed capacitance loading and achieves a fine delay resolution [1], [2]. The other uses shunt capacitor technique to change the capacitance loadings finely and achieves high delay resolution. Figure 1 shows the shunt capacitor circuit. In Fig. 1, M2 acts as a capacitor. The gate voltage of transistor M1 (V_{ctrl}) controls the discharge/charge current. As a result, the delay from In to Out can be controlled by V_{ctrl}.

Traditionally, analog approaches are used to design the delay cell. However, intensive circuit simulation and layout design are needed to overcome Process variations, Voltage variations, and Temperature variations (PVT variations) before an acceptable performance can be achieved. And because of these complicated factors, they often result in a long design cycle as the design product transfers to different process or design specifications are changed. Thus, our goal is to propose new digitally-controlled delay cell by using standard cells only.

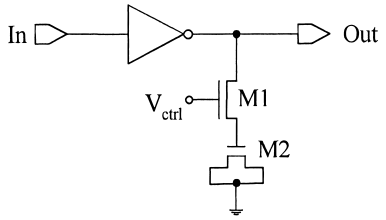

Fig. 1 Conventional delay element with shunt capacitor.

For most digital applications, a standard cell description of the digitally-controlled delay line simplifies the design, and it can be easily ported to different processes in a short time. One simple delay cell directly using an inverter as delay cell is reported in [5], but its resolution is not fine enough for most applications. The other example, a delay cell consists of a bank of tri-state inverter buffers was proposed in [1]. The delay resolution of this cell can be controlled by the number of enabled tri-state buffers. Nevertheless, this variable delay cell has disadvantages in large area and high power consumption.

Another example of delay cell implemented by an or-and-inverter (OAI) cell with two parallel tri-state inverters was proposed in [2]. This digitally-controlled delay cell [2] has less area and power consumption than [1]. However, its resolution step is non-uniform and sensitive to power-supply variation because it is based on OAI cell to change the delay resolution. In addition, this technique also requires an additional decoder for mapping OAI cell control inputs.

In this paper, the proposed digitally-controlled varactor exhibits improved delay characteristics and demonstrates a monotonic delay behavior with respect to the digital input control. It has been successfully verified by a test chip fabricated in 0.35 μm 2P4M CMOS processes and achieves a high delay resolution as 1.55 ps.

2. Proposed Portable Delay Cell

A DCV cell using NAND/NOR gate is shown in Fig. 2(a).

Manuscript received March 18, 2004.
Final manuscript received August 5, 2004.

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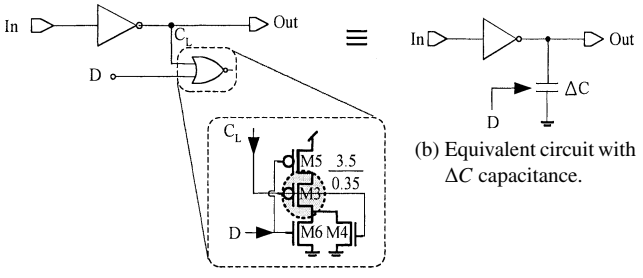
*Work supported by the National Science Council of Taiwan, ROC, under Grant NSC92-2220-E-009-019.

As described in [7], the gate-to-channel capacitance contributes to the total gate-capacitance. Our method is to control the capacitance between gate and source or between gate and drain. In Fig. 2(a), the NOR gate capacitance at node C_L depends on the control input D. The total gate capacitance of transistors M3 and M4 varies with D input states.

The equivalent circuit of the proposed digital-controlled varactor is shown in Fig. 2(b). The D input controls the capacitance difference (ΔC) in the output (Out) node. The gate-capacitance difference characteristic is shown in Fig. 3, which is simulated by HSPICE circuit simulator. The swing-averaged capacitance, as D-node is 0 state or 1 state, is given by



(a) Circuit with digital control.

Fig. 2 Proposed digitally-controlled varactor (DCV).

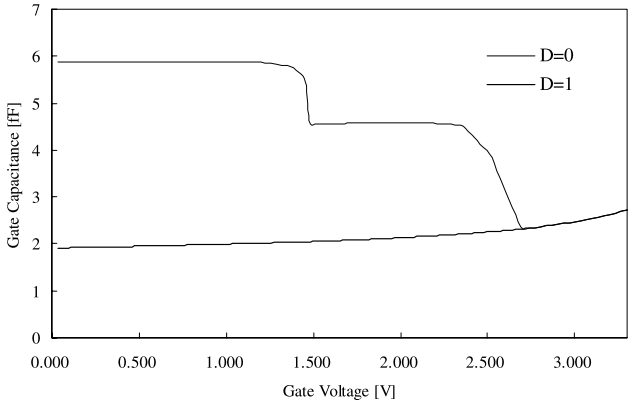


Fig. 3 Variations of two-input NOR gate's capacitance corresponding to $D = 0$ and $D = 1$.

$$C_{average}(D) = \frac{1}{V_{dd}} \int_0^{V_{dd}} C(V_{gate}, D) dV_{gate} \quad (1)$$

with $C_{average}(D)$ the simulated gate-capacitance as in Fig. 3. Based on equation (1), ΔC is the capacitance difference between $C_{average}(0)$ and $C_{average}(1)$. Consequently, the variable delay (ΔT) can be calculated easily by the following linear equation

$$\Delta T = K \times \Delta C \quad (2)$$

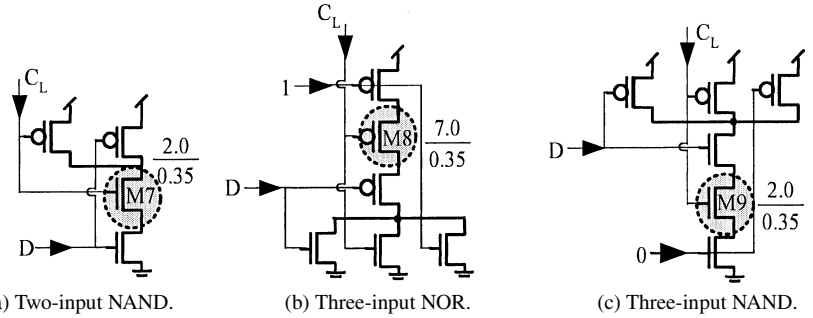
where K is the delay factor of driving inverter and can be gained from cell library. In 0.35 μm 2P4M CMOS cell library, the K value of driving inverter is 0.509 (ns/pF). The ΔC of Fig. 3 is roughly calculated around 2.8 fF. Therefore, ΔT of 1.425 ps (=0.509 × 2.8) can be easily obtained. If N NOR gates are attached to the C_L node, then the delay time becomes $N \times \Delta T$. When different ΔT is needed, it can be achieved by changing the cell type of the driving inverter.

Similarly, a NAND gate can also be applied to DCV cell. Figure 4 shows three different DCVs: (a) two-input NAND gate, (b) three-input NOR gate, and (c) three-input NAND gate. For three-input NOR and three-input NAND gate, the extra input pin is fixed to 1 state and 0 state respectively. The marked transistors (M7, M8, M9) produce a large capacitance difference under different D states.

Table 1 lists the comparisons among these DCVs. The three-input NAND/NOR gate varactor has better noise immunity and less power consumption than the 2-input NAND/NOR gate varactor, but costs more area. In general, the smaller MOS width, the better delay resolution can be obtained. Thus three-input NAND gate has better delay resolution than three-input NOR gate.

Table 1 Comparisons among different types of proposed DCV cells.

Items \ Types	Two-input NOR	Two-input NAND	Three-input NOR	Three-input NAND
Transistors	4	4	6	6
Size of transistor (W/L) unit:μm	3.5 / 0.35	2.0 / 0.35	7.0 / 0.35	2.0 / 0.35
Delay resolution	1.52 ps	0.80 ps	3.2 ps	0.80 ps
Power consumption	15.5 μw/MHz	18.1 μw/MHz	14.5 μw/MHz	14.3 μw/MHz



(a) Two-input NAND. (b) Three-input NOR. (c) Three-input NAND.

Fig. 4 3 different types of DCV cell.

Table 2 Comparisons with other approaches.

Items / Functions	Proposed	ISSCC'03 [1]	JSSC'03 [2]	ISQED'02 [4]	TCASII'00 [6]
Process	0.35 μm	0.6 μm	0.35 μm	0.13 μm	0.35 μm
Delay Resolution	1.55 ps	10 ps	5 ps	40 ps	26 ps
Transistors	4	> 4	< 3	7	6
Protability	Yes	Yes	Yes	No	No

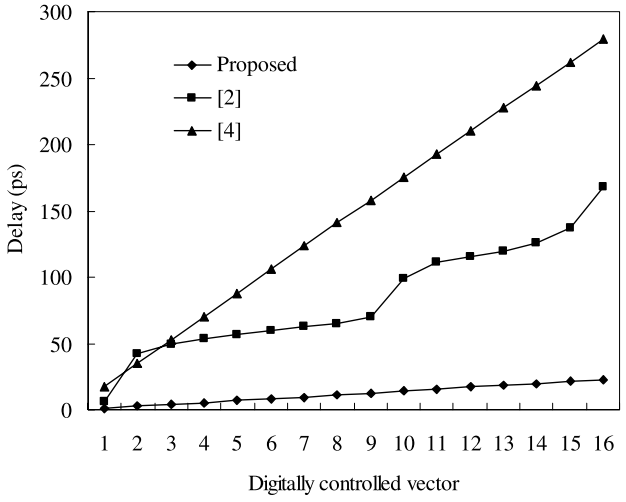


Fig. 5 Comparisons among the proposed delay cell and other approaches.

3. Circuit Simulation and Measurement

HSPICE circuit simulation is performed to estimate the performance of the proposed delay cell, OAI cell [2], and pass transistor [4] on a standard 0.35 μm CMOS 2P4M process. In this simulation, 47 inverters are used in the ring oscillator's coarse-tuning stage, and we use the proposed delay cell as the fine-tuning delay cell. Totally sixteen DCVs are used in the fine-tuning delay cell (N = 16). Figure 5 shows the delay resolution of fine-tuning stage. The delay time of fine-tuning stage is increased when input vector is increased. Figure 5 shows that the proposed delay cell has the finest resolution (about 1.55 ps) compared to other circuits [2], [4]. The delay cell proposed by [4] has very good linearity but its resolution is not good and it has large transistor counts. In contrast, OAI cell [2] has less transistor counts and less power consumption, but its linearity is non-uniform.

The proposed portable delay element is applied to design a digitally-controlled oscillator (DCO) with 15 bits binary weighted control and was fabricated on a standard 0.35 μm CMOS 2P4M process. It includes 128-to-1 path selector as coarse-tuning stage, and 256 DCVs with different NOR gates are added after coarse-tuning to achieve high resolution. The measured output frequency of DCO ranges from 18 to 214 MHz (4.672 ns to 55.555 ns). The measured average resolution of least significant bit (LSB) is 1.55 ps and it is close to linear equation (2). Therefore, equation (2) can provide a quick calculation when designing the DCO. Table 2 lists the chip measurement results as compared with conventional approaches [1], [2], [4], [6]. The proposed DCO has the finest resolution among them and with best portability.

4. Conclusion

A portable delay cell with digitally-controlled varactors (DCVs) has been presented in this paper. Different DCV configurations based on NAND/NOR gates have also been investigated by using HSPICE circuit simulator. Delay resolution of the proposed delay cell can be easily obtained by simple linear equation. From test chip measurement results, it shows that the average delay resolution of the proposed DCV is 1.55 ps. The proposed portable delay cell achieves better delay resolution and portability to speed up all-digital DLL/PLL designs.

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