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A cell-based 5-MHz on-chip clock generator

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Abstract: A cell-based 5-MHz on-chip clock generator for smart sensing applications is presented. By exploiting relative reference modeling, our proposed design can dynamically track both voltage and temperature variations after four-point chip calibrations. The proposed on-chip clock generator is fabricated using a 90-nm CMOS process, the frequency stability is 160 ppm/°C and 72 ppm/mV over 0 °C to 75 °C and 0.9 V to 1.1 V, and the settling time of the proposed on-chip clock generator is 5.12 μs. The proposed on-chip clock generator was implemented with standard cells that can greatly reduce the design complexity and design time for on-chip oscillators.

Key words: MOSFET oscillator, crystal-less clock, frequency stability, PVT compensation, digitally controlled oscillator

1. Introduction

In recent years, many studies [1–23] have been devoted to designing on-chip oscillators with a constant frequency over process, voltage, and temperature (PVT) variations. Fully integrated CMOS-compatible on-chip oscillators that replace quartz crystal oscillators are required for low-cost and low-power wireless and biomedical sensors. In addition, on-chip oscillators should be low-jitter and fast-settling in order to provide a stable reference clock for the system with PVT variations.

Most current on-chip oscillators [6,7,9–13,16–20,22,23] need to perform one-point or multipoint RC trimming or circuit calibration to adjust their center frequency. For example, without calibration and trimming techniques, a 30-MHz on-chip oscillator [4] and a 6.66-kHz on-chip oscillator [8] have maximum 10% and 3.2% frequency errors, respectively, with only process variations. In addition, a special R trimming procedure is required to cancel the temperature coefficient of the reference voltage generator in the oscillators [6,7,16–20]. However, the opposite sign temperature coefficient resistors are not usually available in advanced CMOS processes. In addition, a trade-off exists between the trimming cost and output frequency error. Considerable measurements are necessary in the batch trimming or calibration process, and the trimming or calibration cost can make these on-chip oscillators even more expensive than crystal oscillators.

The frequency compensation loop involving a temperature sensor in [9] and [11] has a relatively long settling time due to the low conversion rate of the temperature sensor. In addition, the temperature sensor is easily affected by voltage variations and causes large frequency errors, and the high-order polynomial compensation discussed in [9] and [11] also increases the area cost of the on-chip oscillators. An integrated bandgap regulator can reduce the frequency error of on-chip oscillators with voltage variations. However, the bandgap regulator could occupy about 50%–70% of the area of the integrated oscillator [1,17,21] and the bandgap regulator requires one or two extra point trimming process.

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In [13], the ratio of the propagation delay times between two delay cells is called the delay ratio. Relative reference modeling (RRM) that uses the delay ratio to estimate the absolute value of the gate delay under PVT variations was proposed in [13]. Subsequently, an all-digital approach was proposed to compute the control code for the oscillator to produce the target frequency under PVT variations. In this paper, a cell-based, low-jitter, fast-settling 5-MHz on-chip clock generator using RRM is proposed. As compared to [13], the voltage effects and temperature effects are separated in the proposed design. Therefore, the required calibration points can be reduced to four points with the proposed linear interpolation and extrapolation approaches, and the proposed high resolution digitally controlled oscillator (DCO) also reduces the output frequency error.

The rest of this paper is organized as follows: Section 2 introduces the architecture of the RRM-oscillator. Section 3 shows the experimental results of the test chip and compares the performance with previous works. Finally, Section 4 concludes this work.

2. Proposed RRM-oscillator architecture

Figure 1 shows the block diagram of the proposed RRM-oscillator. The proposed design consists of a delay ratio estimator (DRE), a temperature and voltage classifier, a linear calculator, and a DCO. After chip fabrication, the proposed RRM-oscillator needs to be calibrated at four calibration points. The required coefficients, $R1_{det}(V_n)$, $R2_{det}(T_j)$, $a(V_n)$, and $b(V_n)$, where n = 1 to 9 and j = 1 to 4, and COARSE_CODE can then be calculated in the off-chip process. Subsequently, these coefficients are input to initialize the proposed RRM-oscillator.

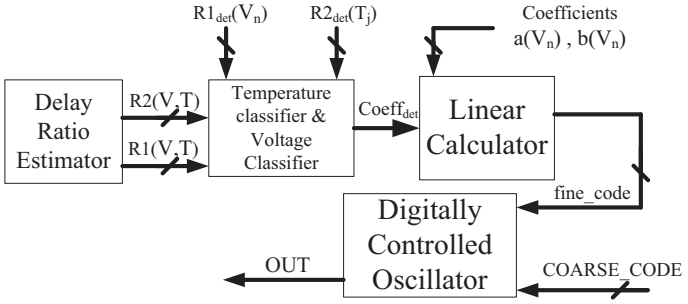

Figure 1. The proposed RRM-oscillator.

After chip calibration, the RRM-oscillator is ready to generate the desired output frequency. When the operating voltage and temperature of the RRM-oscillator are changed, the RRM-oscillator uses the delay ratios to determine the current operating voltage and temperature of the chip. The temperature and voltage classifier can then use delay ratios to choose the suitable coefficients for the linear calculator. Subsequently, the linear calculator uses the linear equation to calculate the DCO control code (fine_code) for the DCO. Finally, the proposed RRM-oscillator can keep the constant frequency output with PVT variations. In this paper, the desired target frequency of the RRM-oscillator is 5 MHz over 0 °C to 75 °C and 0.9 V to 1.1 V.

Figure 2 shows the architecture of the proposed DCO. The DCO consists of a coarse-tuning stage and a fine-tuning stage implemented with compared delay cells 2 (CDC2s) and lattice delay units (LDUs), respectively. The output of the ring oscillator triggers the DCO counter, and whenever the output value of the DCO counter (DCO_{CNT}) equals the input coarse-tuning control code (COARSE_CODE), the signal cdc_in is set to high. According to the fine-tuning enable signals (fine_en[511:0]), the fine-tuning delay stage can insert a different delay between cdc_in and cdc_out. After the fine-tuning delay stage, the cdc_out pulse triggers a D-type flip-flop

and resets the DCO counter. The signal cdc_in is then set to low. A divided-by-2 circuit is added before the output to generate the clock with a 50% duty cycle.

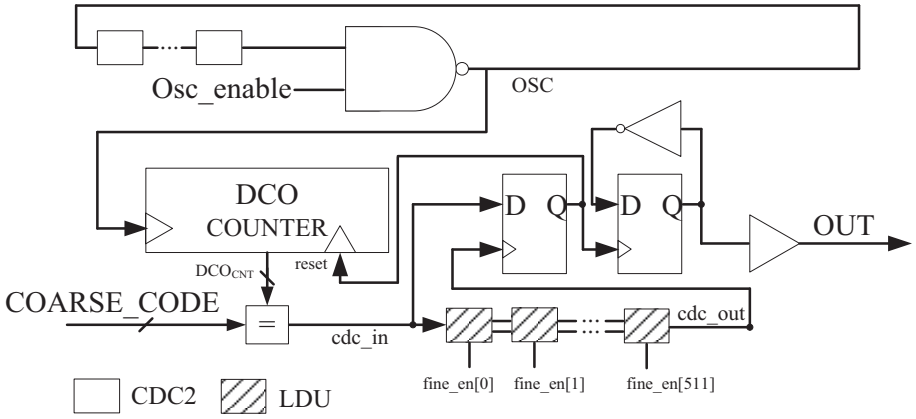

Figure 2. The architecture of the proposed DCO.

In Figure 3, the fine-tuning stage consists of 512 LDUs. The DCO fine-tuning resolution (D_{LDU}(V,T)) is the delay time of two NAND gates, and the intrinsic delay of the fine-tuning stage is the delay time of three NAND gates. In the proposed DCO, the 9-bit fine-tuning control code (fine_code) is encoded as a 512-bit thermal meter code (fine_en[511:0]) to control the fine-tuning stage. The coarse-tuning control code (COARSE_CODE) is fixed after chip calibration, and thus the frequency tunable range of the fine-tuning stage should be sufficient for covering voltage and temperature variations.

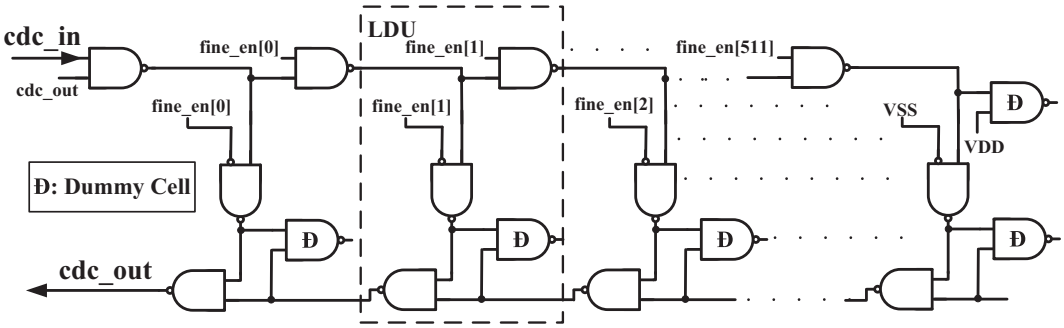

Figure 3. The proposed fine-tuning delay stage.

As shown in Figure 2, whenever the reset signal is set to high, the signal cdc_in is set to low and the signal cdc_out is set to high. Then the coarse-tuning control code determines when the signal cdc_in is set to high. Subsequently, as shown in Figure 3, when cdc_in and cdc_out are both set to high, the signal cdc_out is set to low after the delay time provided by the fine-tuning stage. Then, after the same fine-tuning delay time, the cdc_out is set to high again. The rising transition of the signal cdc_out triggers the D-flip/flop and the signal reset is set to high again to clear the DCO counter and change the state of the output (F_{OUT}). Therefore, the half cycle time of the output (F_{OUT}) is composed of the delay time of the coarse-tuning stage and the two times delay time of the fine-tuning stage. Thus, the output frequency of the DCO (F_{OUT}) can be expressed as in Eq. (1), where P_{OSC}(V,T) is the period of the ring oscillator, F_{INT} (V,T) is the intrinsic delay of the fine-tuning

delay stage, *COARSE* is the coarse-tuning control code, and *fine* is the fine-tuning control code. In addition, F_{INT} is equal to 1.5 times D_{LDU}(V,T). On the basis of Eq. (1), at calibration points, the DCO control code (fine_code and COARSE_CODE) for generating the target frequency (i.e. 5 MHz) can be calculated.

$$F_{OUT}=\frac{1}{2}\times\frac{1}{P_{OSC}(V,T)\times COARSE+D_{LDU}(V,T)\times fine\times 2+F_{INT}(V,T)\times 2} \tag{1}$$

Figure 4 shows the proposed DRE for computing the delay ratios: R1(V,T) and R2(V,T). In Figure 4, CDC1 refers to the compared delay cell 1, CDC2 refers to the compared delay cell 2, and RDC refers to the reference delay cell. Three different logic cells [(RDC, CDC1, CDC2) = (MXI4X2, NOR4BBX1, NAND3BXL)] are selected from the cell-library as delay cells to build up three ring oscillators (RRO, CRO1, CRO2). The output of the ring oscillator is connected to the counter to record the oscillation cycles of the oscillator. When the RRO counter counts from 0 to N_{TIME}, all three counters are stopped. Then the counter values of $CRO1_{CNT}$ and $CRO2_{CNT}$ can be used to calculate delay ratios. The delay ratio between these logic cells can be expressed as in Eq. (2). N_{TIME} is set to 1023 to avoid having to use dividers when computing the delay ratios.

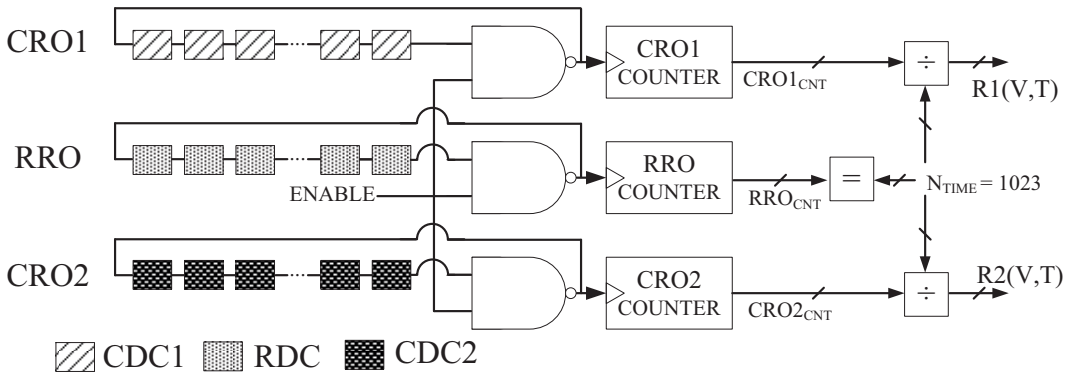

Figure 4. The proposed DRE.

$$R1(V,T)=\frac{CRO1_{CNT}}{RRO_{CNT}}\quad R2(V,T)=\frac{CRO2_{CNT}}{RRO_{CNT}} \tag{2}$$

Figure 5 shows the measured R1(V,T) curves vs. temperature at different voltages. In this paper, voltage (V_n) varies from V_1 to V_9 (V_1 = 0.9 V, V_2 = 0.925 V, V_3 = 0.95 V, V_4 = 0.975 V, V_5 = 1.0 V, V_6 = 1.025 V, V_7 = 1.05 V, V_8 = 1.075 V, and V_9 = 1.1 V) and temperature (T_j) varies from T_1 to T_4 (T_1 = 0 °C, T_2 = 25 °C, T_3 = 50 °C, and T_4 = 75 °C). In the design of the DRE, CDC1 and RDC are chosen to make R1(V_n, T) monotonically increasing with operating temperature at different voltages V_n. For example, at voltage V_1, R1(V,T) should increase monotonically as the temperature value is increased from 0 °C to 75 °C.

Figure 6 shows the measured R2(V,T) curves vs. DCO fine-tuning control code (fine_code) to generate the desired 5-MHz output frequency at different temperature. At certain (V_n, T_j) chip operating conditions, where n = 1 to 9 and j = 1 to 4, we set the coarse-tuning control code (COARSE_CODE) of the DCO to any value and then we can measure the periods of the DCO output with fine_code set to 9'd0 and 9'd511, respectively. From the measured DCO periods, the fine-tuning resolution of the DCO (D_{LDU}(P,V,T)) and the coarse-tuning resolution (P_{OSC}(P,V,T)) of the DCO can be calculated. Next, the coarse-tuning control

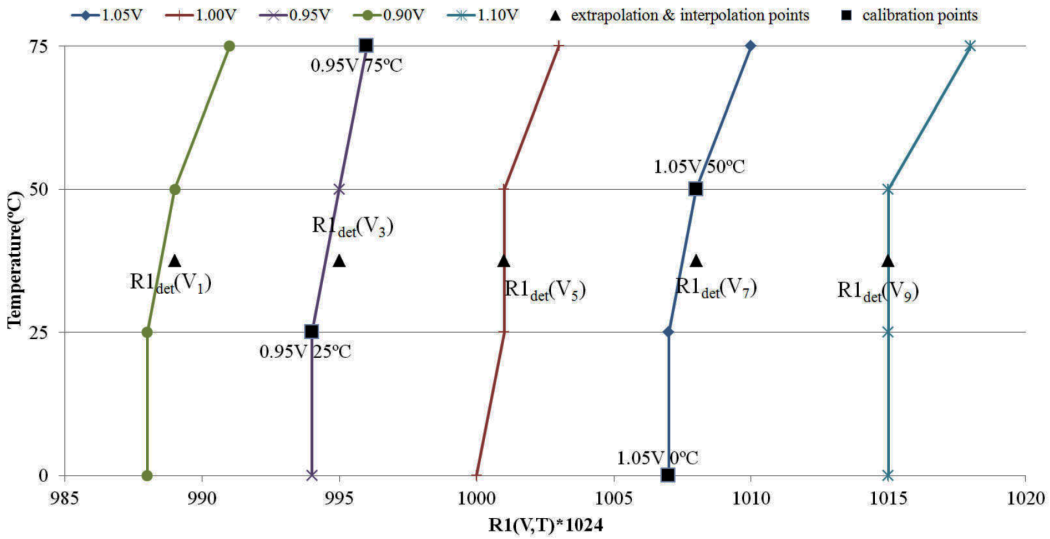

Figure 5. Measured R1(V, T) curves.

code (COARSE_CODE) can be determined, and the fine-tuning control code (fine_code) to generate the desired 5-MHz output frequency can be calculated according to Eq. (1). In the design of the DRE, CDC2 and RDC are chosen so that R2(V, Tj) curves are nonoverlapping at different temperatures T_j. For example, as illustrated in Figure 6, the maximum value of R2(V,T) at T_4 should be smaller than the minimum value of R2(V,T) at T_3.

Figure 7 shows the same measurement results of Figure 6 but at different voltages. At voltage V_n, the relationship between R2(V_n, T) and fine_code can be approximately expressed as a linear equation with slope a(V_n) and intercept b(V_n). For example, as illustrated in Figure 7, at 0.95 V, the fine_code to generate the desired 5-MHz output frequency decreases as the temperature value increases from 0 °C to 75 °C.

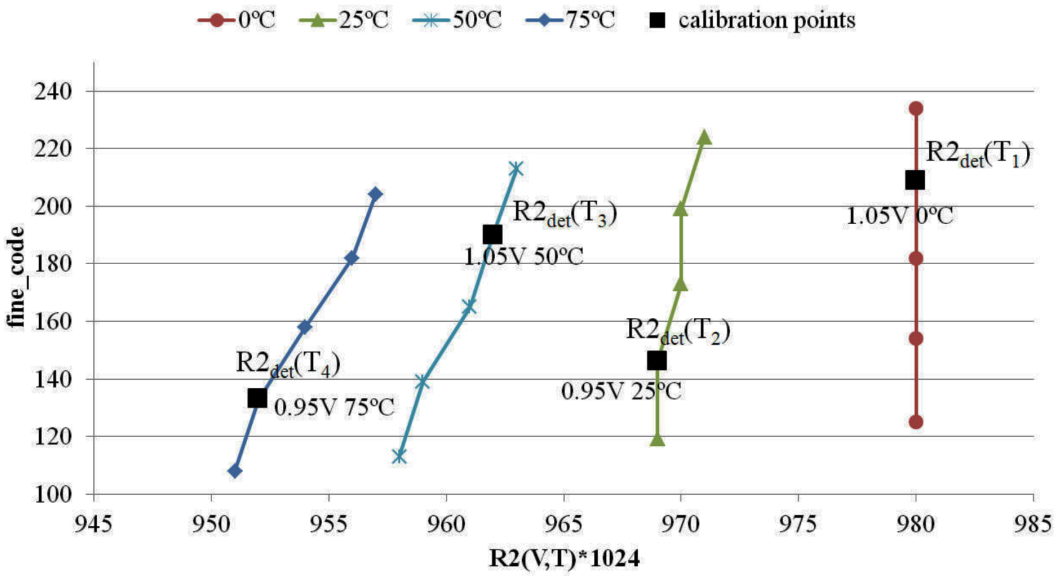

Figure 6. Measured R2(V, T) curves at different temperatures.

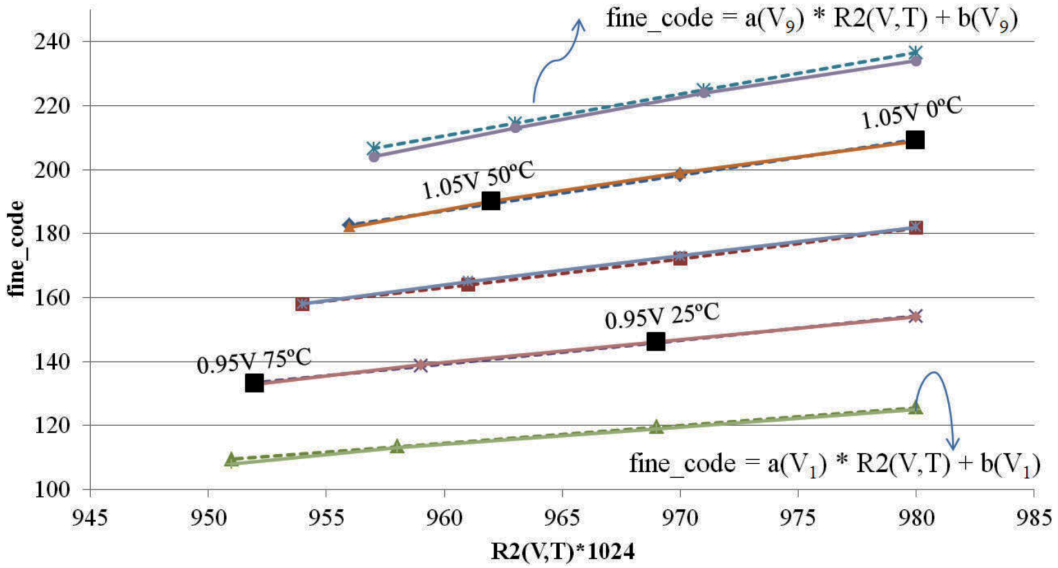

Figure 7. Measured R2(V, T) curves at different voltages.

In the proposed DCO shown in Figure 2, both voltage and temperature variations affect the oscillation frequency of the ring oscillator. Therefore, the fine_code of the proposed DCO will be automatically adjusted according to variations in voltage and temperature. However, as shown in Figure 7, voltage variations have more impact on the output frequency than temperature variations.

The chip calibration flow for the proposed RRM-oscillator is explained as follows. As shown in Figure 5, at calibration points (0.95 V, 25 °C), (0.95 V, 75 °C), (1.05 V, 0 °C), and (1.05 V, 50 °C), we measured the periods of the DCO to obtain the coarse-tuning and fine-tuning resolution of the DCO in the off-chip process. Then the DCO control code, COARSE_CODE and fine_code, to output the target frequency can be determined according to Eq. (1). The DRE output values of R1(V, T) and R2(V, T) at the calibration points are simultaneously recorded. As illustrated in Figure 5, the average value of R1(V,T) at (0.95 V, 25 °C) and (0.95 V, 75 °C) is recorded as $R1_{det}(V_3)$. Similarly, the average value of R1(V,T) at (1.05 V, 0 °C) and (1.05 V, 50 °C) is recorded as $R1_{det}(V_7)$. Subsequently, a linear interpolation and extrapolation are applied to compute $R1_{det}(V_n)$, where n = 1 to 9.

As shown in Figure 6, the measured values of R2(V,T) at the same calibration points of (0.95 V, 25 °C), (0.95 V, 75 °C), (1.05 V, 0 °C), and (1.05 V, 50 °C) are recorded as $R2_{det}(T_j)$, where j = 1 to 4. In addition, as shown in Figure 7, at different voltages, the fine_code that produces a 5-MHz output frequency will be linearly proportional to R2(V,T). Thus, slope $a(V_3)$ and intercept $b(V_3)$ of the linear equation at V_3 (0.95 V) can be computed using the values of R2(V,T) at two calibration points of (0.95 V, 25 °C) and (0.95 V, 75 °C). Similarly, the values of $a(V_7)$ and $b(V_7)$ can be computed by the values of R2(V,T) at the other two calibration points of (1.05 V, 0 °C) and (1.05 V, 50 °C). Subsequently, a linear interpolation and extrapolation are applied to compute $a(V_n)$ and $b(V_n)$, where n = 1 to 9. Then these coefficients, $R1_{det}(V_n)$, $R2_{det}(T_j)$, $a(V_n)$, and $b(V_n)$, are input to initialize the proposed RRM-oscillator.

As shown in Figure 1, the DRE computes R1(V,T) and R2(V,T) at chip run time. The temperature and voltage classifier uses the threshold values $R1_{det}(V_n)$ and $R2_{det}(T_j)$ to determine the current operation voltage and temperature. For example, as shown in Figure 5, if R1(V,T) is 1000/1024 and R2(V,T) is 960/1024,

then the values of R1(V,T) and R2(V,T) are close to $R1_{det}(V_5)$ and $R2_{det}(T_3)$, respectively. This means that the current operation condition (V, T) = (V_5, T_3) = (1.00 V, 50 °C). Subsequently, the linear calculator of the RRM-oscillator will use slope $a(V_5)$ and intercept $b(V_5)$ of the linear equation to compute the fine_code needed for the DCO to produce 5-MHz output frequency. Then, if the operation voltage and temperature have changed, the temperature and voltage classifier will determine which threshold values $R1_{det}(V_n)$ and $R2_{det}(T_j)$ are close to the current delay ratios output by the DRE, and the slope and intercept of the linear calculator will be changed accordingly. Therefore, the fine_code of the DCO can be adjusted to keep the constant output frequency with PVT variations.

As shown in Figure 5, $R1(V_n, T)$ is monotonically increasing with operating temperature at different voltages V_n. Thus, if the value of R1(V,T) falls in the middle of $R1_{det}(V_n)$ and $R1_{det}(V_{n+1})$, R2(V,T) can be used to determine the current operation voltage. If R2(V,T) is close to $R2_{det}(T_1)$, V_n will be chosen as the current operation voltage. Otherwise, if R2(V,T) is close to $R2_{det}(T_4)$, V_{n+1} will be chosen. In addition, if R2(V,T) is close to $R2_{det}(T_2)$ or $R2_{det}(T_3)$, the RRM-oscillator will use slope $[a(V_n)+a(V_{n+1})]/2$ and intercept $[b(V_n)+b(V_{n+1})]/2$ of the linear equation to compute the fine_code for the DCO.

3. Experimental results

The proposed RRM-oscillator is implemented using a standard performance 90-nm CMOS process. A microphotograph of the test chip is shown in Figure 8. In the test chip, the coefficient register block is used to store the input coefficients of the RRM-oscillator. The active area is 250 × 200 μm^2 and the chip area including the I/O pads is 765 × 815 μm^2.

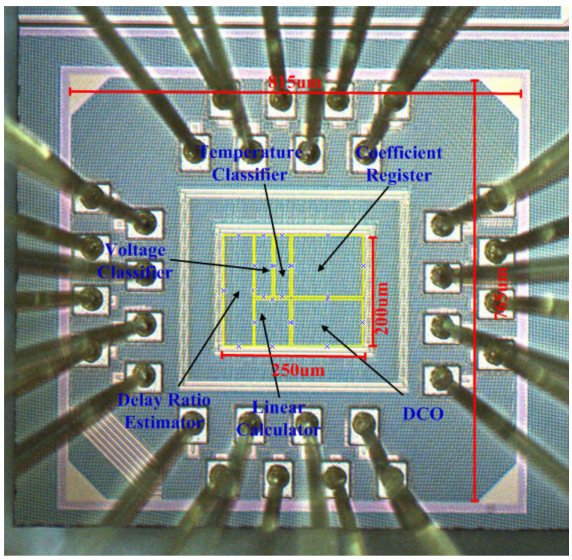

Figure 8. Microphotograph of the test chip.

Figure 9 shows the measured output frequency of the proposed RRM-oscillator in three samples. The maximum frequency error with PVT variations is smaller than 1.47%. Figure 10 shows the period jitter measurement results of the proposed RRM-oscillator at (1.0 V, 25 °C). The root-mean-square jitter and peak-to-peak jitter are 23.8 ps and 153.4 ps, respectively. The proposed RRM-oscillator has relatively small jitter compared to current on-chip oscillators.

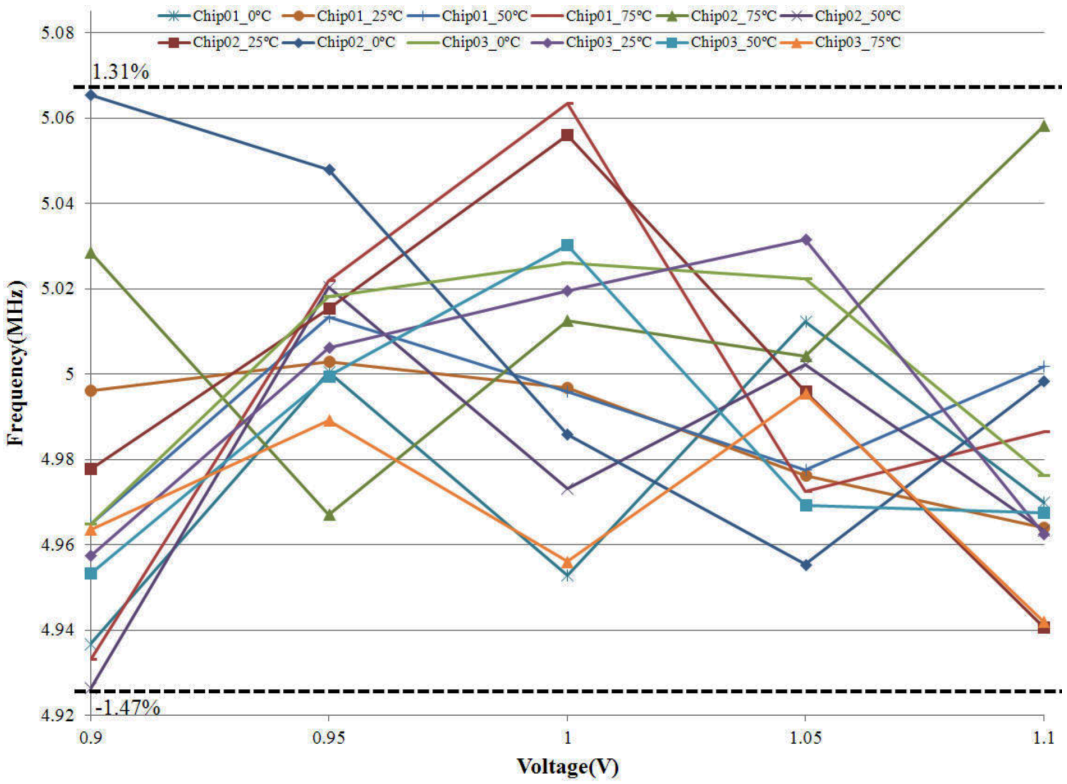

Figure 9. The measured output frequency in three samples at 5-MHz output frequency with voltage and temperature variations.

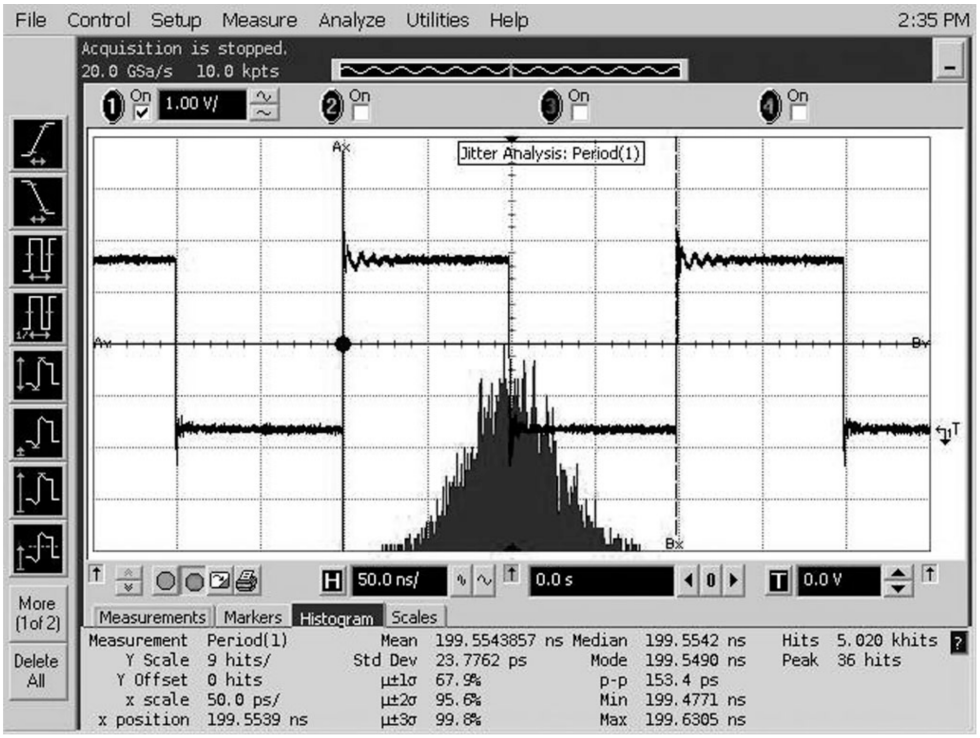

Figure 10. The measured period jitter performance at (1.00 V, 25 °C).

The Table shows that the proposed RRM-oscillator has a relatively fast settling time for quickly tracking and adjusting to voltage and temperature variations. The cell-based design approach also makes the RRM-oscillator more portable than other types of on-chip oscillators. Although the oscillator in [6] has a relatively small voltage coefficient, the small residual reference voltage error after the trimming process can greatly increase frequency error. In addition, the high resolution trimming process will increase the cost in mass production. Moreover, as compared to [13], the proposed high resolution DCO also reduces the jitter of the output clock. The proposed RRM-oscillator only needs to perform four-point calibrations, and it is more suitable for mass production. By recording the values of R1(V,T) and R2(V,T) at four calibration points and computing the required coefficients in the off-chip process, the proposed RRM-oscillator can maintain constant frequency output within ranges of 0.9 V to 1.1 V and 0 °C to 75 °C.

Table. Performance comparisons.

Parameter	This work	[9] JSSC'11	[11] JSSC'12	[4] ESSCIRC'09	[6] JSSC'10	[13]TVLSI'12
Technology (nm)	90	65	160	350	180	90
Frequency (MHz)	5	0.15	16	30	14	5
Temp. range	0–75	–55 to 125	–55 to 125	–20 to 100	–40 to 125	0–75
Variation with temp.	±0.6%	±0.5%	±0.1%	–2.30%	±0.75%	±1%
Temp. coeff. (ppm/°C)	160	55.6	11.2	192	90.9	266.7
Voltage range	0.9–1.1	Fixed 1.2 V	Fixed 1.8 V	1.8–3.0	1.7–1.9	0.9–1.1
Variation with voltage	±0.72%	N/A	N/A	–7%	±0.16%	1.6%
Voltage coeff. (ppm/mV)	72	N/A	N/A	58.3	16	80
Max error (with voltage variation and temperature variation)	1.47% (in three samples)	N/A	N/A	–8.30%	N/A	2.40%
Power (mW)	0.25	0.051	2.1	0.18	0.045	0.65
Area (mm^2)	0.05	0.2	0.5	0.08	0.04	0.04
RMS jitter (ps)	23.8	6666	45	65	30	240
Settling time	5.12 μs	300 μs	$>$ 0.5 s	N/A	10 μs	10 μs
Design approach	Cell-based	Full-custom	Full-custom	Full-custom	Full-custom	Cell-based

4. Conclusion

In this paper, we presented a cell-based 5-MHz on-chip clock generator using RRM. The proposed RRM-oscillator uses delay ratios R1(V,T) and R2(V,T) to determine the operation voltage and temperature at chip run time. Subsequently, the linear calculator of the RRM-oscillator will use the suitable slope and intercept value to compute the DCO control code needed for the DCO to produce a 5-MHz output frequency. Therefore, the frequency error of the RRM-oscillator with PVT variations can be significantly reduced by a linear equation-based compensation approach. The proposed design can be implemented by standard cells and is suitable for low-power and low-cost system-on-a-chip applications.

Acknowledgments

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