A fast lock-in all-digital phase-locked loop in 40-nm CMOS technology

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Abstract: A system-on-a-chip (SoC) requires several phase-locked loops (PLLs) for providing different clock frequencies to different modules. Usually, analog PLLs cannot be stopped due to their long setting time. Hence, these PLLs dominate the system's standby power consumption. In this paper, a fast lock-in all-digital PLL (ADPLL) that can achieve lock-in within 4.5 clock cycles is proposed to ensure that it can be switched off in the low power mode. The output frequency of the proposed ADPLL ranges from 125 MHz to 1.47 GHz, and the power consumption is 0.98 mW (at 0.9 V, 1.47 GHz).

Keywords: all-digital phase-locked loop, fast lock-in, low power

Classification: Integrated circuits

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1 Introduction

A system-on-chip (SoC) usually requires several phase-locked loops (PLLs) to provide different clock frequencies for different modules and I/O interfaces. Compared with analog PLLs, an all-digital phase-locked loop (ADPLL) can replace passive components with digital circuits and reduce chip area. In addition, ADPLLs can operate at low voltage in advanced CMOS processes. Thus, recently, ADPLLs have attracted increasing attention for clock generator design.

Fast lock-in ADPLLs [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 18, 19, 20, 21] have been developed and applied in biomedical electronic devices, wireless

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devices with frequency hopping, spread spectrum clock generators, and implantable medical devices. These applications require reduction in standby power consumption and rapid frequency switching. Moreover, when high-speed clock is not required, the fast lock-in ADPLL can be switched off to minimize power consumption. Subsequently, the ADPLL can quickly relock and provide a stable clock to the system when back in the normal mode.

The binary search algorithm [5, 7, 8, 9] is a well-known approach used in frequency acquisition to shorten the lock-in time. However, the algorithm requires many reference clock cycles in frequency acquisition. The gear-shifting algorithm [1, 12] changes the ADPLL bandwidth by adjusting the weighted coefficients of the loop filter during frequency acquisition to shorten the lock-in time. In [11], a modified bang-bang algorithm is presented. If the phase and frequency detector (PFD) outputs n consecutive leadings or laggings, the proportional gain (β) of the loop filter outputs $\beta \times \mathrm{n}$ as output code to shorten the ADPLL's lock-in time. However, these ADPLLs [1, 11, 12] still take over several hundred reference clock cycles to achieve lock-in. In addition, when migrating to a different CMOS process, the coefficients of the loop filter require re-simulation from the viewpoint of stability.

A time-to-digital converter (TDC)-based ADPLL, which has a seven-cycle lock-in time, is proposed in [13]. However, the TDC resolution limits the maximum frequency of the input reference clock. The ADPLL [13] can only accept reference clock frequencies lower than 340 kHz, which is insufficient for most applications. A similar two-level TDC-based ADPLL to achieve fast lock-in was proposed in [4]. However, the limited TDC resolution resulted in >3% frequency error after ADPLL locking.

An ADPLL with a fast-lock engine (FLE) that achieves a lock-in time of two reference cycles was proposed in [14]. However, this ADPLL requires three digitally controlled oscillators (DCOs) and occupies a large chip area. In addition, on-chip variations increase the frequency error after ADPLL locking. A frequency estimation algorithm (FEA)-based ADPLL using only one DCO was proposed in [10]. The embedded-cyclic TDC improved the accuracy of the period ratio computation and achieved fast setting time with small frequency errors in four clock cycles. However, to improve the TDC resolution and reduce the frequency estimation error, pulse-latch D-type flip/flops (PLDFFs) are required.

In this paper, we propose a fast lock-in ADPLL with a FEA calibration method to reduce chip area and improve the accuracy of frequency estimation. The rest of this paper is organized as follows. The architecture of the proposed ADPLL is presented in section 2. Section 3 describes the circuit implementation of the proposed ADPLL. Section 4 shows the experimental results of the proposed ADPLL. Finally, the conclusions are given in section 5.

2 Proposed ADPLL architecture

Fig. 1 shows the block diagram of the proposed ADPLL. The proposed ADPLL consists of a phase and frequency detector (PFD), an ADPLL controller with a digital loop filter, a DCO, frequency divider, frequency finder, cyclic counter, and

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an output divider. After the ADPLL is reset, the PFD and frequency divider are both stopped until the frequency finder estimates the target DCO control code (init_code). Subsequently, the ADPLL controller sends the DCO control code (init_code) to the DCO and enables the DCO. Thereafter, the PFD and the frequency divider are enabled, and frequency acquisition and phase acquisition are finished within 4.5 clock cycles.

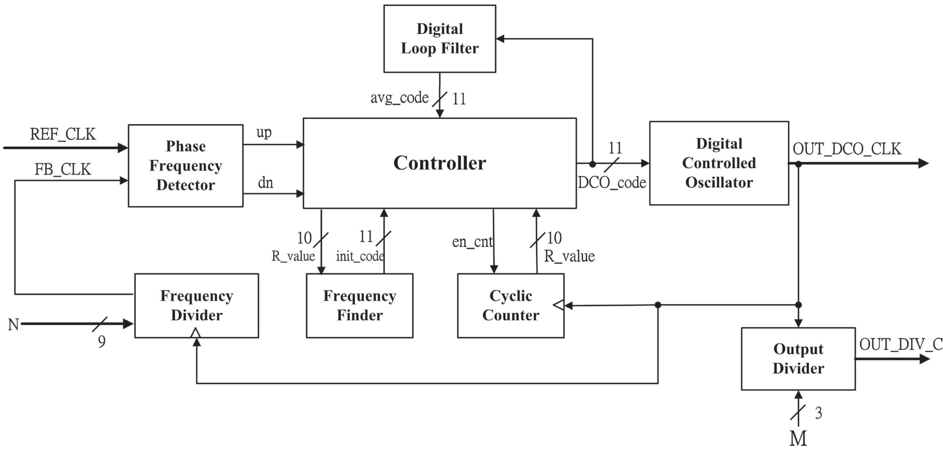

Fig. 1. The proposed ADPLL.

However, there remain residual frequency errors after the ADPLL is locked owing to the frequency estimation error of the frequency finder. Therefore, the PFD continuously detects phase and frequency errors between the feedback clock (FB_CLK) and the reference clock (REF_CLK). Subsequently, the ADPLL controller updates the DCO control code according to the PFD output. Moreover, the digital loop filter generates the baseline DCO control code (avg_code) for the ADPLL controller to reduce reference clock jitter and stabilize DCO output clock.

In the proposed ADPLL, when the 11-bit DCO control code is set to the medium value of the DCO control code (i.e. 1023), the DCO operates at the median frequency with the median period, denoted as $\mathrm{P_{mid}}$. Additionally, when the DCO control code is set to the maximum value of the DCO control code (i.e. 2047), the DCO operates at the maximum frequency with the minimum period, denoted as $\mathrm{P_{min}}$. The period ratio is the ratio between the reference clock period ($\mathrm{P_{ref}}$) and the DCO clock period. The definition of the period ratio $\mathrm{R_{mid}}$ and $\mathrm{R_{max}}$ is shown in Eq. 1.

$$R_{mid} = \frac{P_{ref}}{P_{mid}}, \quad R_{max} = \frac{P_{ref}}{P_{min}} \tag{1}$$

In the proposed ADPLL, the cyclic counter triggered by the DCO is used to calculate the period ratios. In addition, the reciprocals of the period ratios $\mathrm{R_{mid}}$ and $\mathrm{R_{max}}$ are defined as $\mathrm{W_{mid}}$ and $\mathrm{W_{min}}$, respectively, and are given by Eq. 2.

$$W_{mid} = \frac{2^{11}}{R_{mid}}, \quad W_{min} = \frac{2^{11}}{R_{max}} \tag{2}$$

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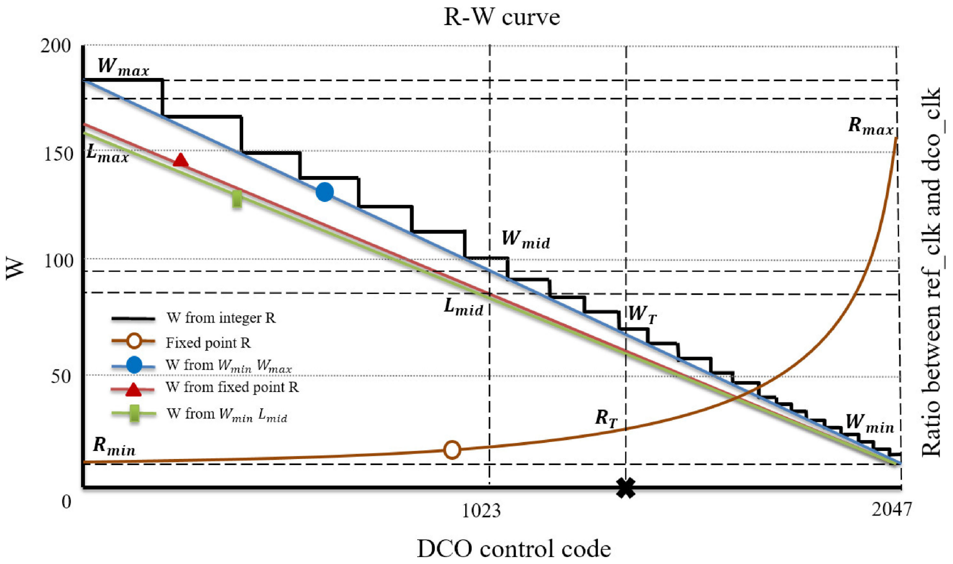

Fig. 2. The relationship of R value and W value.

Fig. 2 shows the R and W values corresponding to the DCO control code (DCO_code). For an ADPLL [10] with a cyclic TDC, the period ratio (R value) can be estimated as a fixed-point number, but doing so warrants the use of a high-resolution TDC. In the proposed ADPLL, we use a simple cyclic counter triggered by the DCO to compute the period ratio (R value); thus, the R value is an integer number. Given that the W value is the reciprocal of the R value, the W value curve obtained from the integer R value is serrated, as shown in Fig. 2. Compared to the W value curve obtained from the fixed-point R value, the error in the W value affects the accuracy of frequency estimation in the frequency finder. As a result, in this paper, we propose a method to reduce the error in the W line due to quantization error of the period ratio (R value).

In the proposed ADPLL, the cyclic counter runs only for one half of the reference clock period for speeding up the lock-in time. In addition, we assume that the output period of the DCO has linear and monotonic responses to the DCO control code, and the DCO period can be formulated by a linear equation. Thus, the period ratios R_{max} and R_{mid} can be rewritten as Eq. 3.

$$R_{max} = \frac{\frac{T}{2}}{T_0}, \quad R_{mid} = \frac{\frac{T}{2}}{T_0 + 1024\Delta} \tag{3}$$

where T refers to the reference clock period, T_0 denotes the minimum period of the DCO, and Δ denotes the fine-tuning resolution of the DCO. According to Eq. 3, Δ and T_0 can be expressed in terms of R_{mid} and R_{max}, as shown in Eq. 4.

$$T_0 = \frac{\frac{T}{2}}{R_{max}}, \quad \Delta = \frac{\frac{T}{2} \times (R_{max} - R_{mid})}{1024 \times R_{max} \times R_{mid}} \tag{4}$$

The general formula of the period ratio corresponding to the DCO control code (DCO_code) can be expressed as Eq. 5. As we explained earlier, Eq. 5 is valid under the assumption that the DCO has linear and monotonic responses. Sub-

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sequently, by substituting Eq. 4 into Eq. 5, Eq. 6 can be derived. Since the W value is the reciprocal of the R value, Eq. 7 can be derived easily. Therefore, we obtain the relationship between the W value and the DCO control code by the proposed method. Consequently, by setting DCO_code to 1023 into Eq. 7 and substituting Eq. 2 into Eq. 7, Eq. 8 for calculating the required calibration value (L_{mid}) can be derived.

$$R(DCO\_code) = \frac{\frac{T}{2}}{T_0 + (2047 - DCO\_code) \times \Delta} \tag{5}$$

$$R(DCO\_code) = \frac{1024 \times R_{max} \times R_{mid}}{1024 \times R_{mid} + (2047 - DCO\_code) \times (R_{max} - R_{mid})} \tag{6}$$

$$W(DCO\_code) = \frac{1024 \times R_{mid} + (2047 - DCO\_code) \times (R_{max} - R_{mid})}{1024 \times R_{max} \times R_{mid}} \times 2^{11} \tag{7}$$

$$L_{mid} = W(1023) = W_{min} + \frac{R_{max} - R_{mid}}{R_{max} \times R_{mid}} \times 2^{11} \tag{8}$$

When the frequency acquisition in the ADPLL is complete, the ratio between the reference clock period and the DCO clock period should be the frequency multiplication factor (N). Thus, the target period ratio (R_T) of the ADPLL is equal to N; accordingly, the target W value (W_T) should be equal to $2^{11}/N$. As shown in Fig. 2, from the values of W_{min} and L_{mid}, a linear equation can be obtained, as expressed in Eq. 9. Thus, when W(DCO_code) is equal to W_T, by using Eq. 9, the target DCO control code (init_code) can be derived as Eq. 10.

$$W(DCO\_code) = \frac{(W_{min} - L_{mid})}{2^{10}} \times DCO\_code + (-W_{min} + 2L_{mid}) \tag{9}$$

$$init\_code = \frac{W_T + W_{min} - 2L_{mid}}{W_{min} - L_{mid}} \times 2^{10} \tag{10}$$

As shown in Fig. 2, the fixed-point period ratio (R value) for different DCO control codes can be measured during SPICE circuit simulation or by using a high-resolution TDC circuit. Because the W value is the reciprocal of the R value, the red line shows the W value obtained from the fixed-point R value, and the black line shows the W value obtained from the integer R value. Moreover, the green line plotted using the values of W_{min} and L_{mid} represents Eq. 9. As discussed earlier, in the proposed ADPLL, we use a simple cyclic counter triggered by the DCO to compute the period ratio (R value); thus, the R value output by the cyclic counter is an integer number. The green line (Eq. 9) is close to the red line, which means the proposed method illustrated in Eqs. 3–9 can achieve almost the same performance in frequency estimation with the fixed-point period ratio (R value). Compared to the ADPLL [10] with a cyclic TDC, the proposed ADPLL can eliminate the requirement of a high-resolution TDC circuit and reduce the frequency error in frequency estimation.

Fig. 3 shows the timing diagram of the proposed ADPLL. After the ADPLL is reset, the frequency finder computes the reciprocal of the multiplication factor (N) by using a divider. Subsequently, R_{mid} is calculated by the cyclic counter, and W_{mid} is computed by the divider. Then, R_{max} and W_{min} are calculated. Thereafter, in the

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calibration state, the required calibration value (L_{mid}) is computed using Eq. 8. Finally, the frequency finder calculates the target DCO control code (init_code) by using Eq. 10. Then, init_code is sent to the DCO, and the ADPLL controller enables the DCO. Thereafter, the PFD and the frequency divider are enabled, and frequency acquisition and phase acquisition are finished within 4.5 clock cycles. In addition, only one divider is required in the proposed ADPLL.

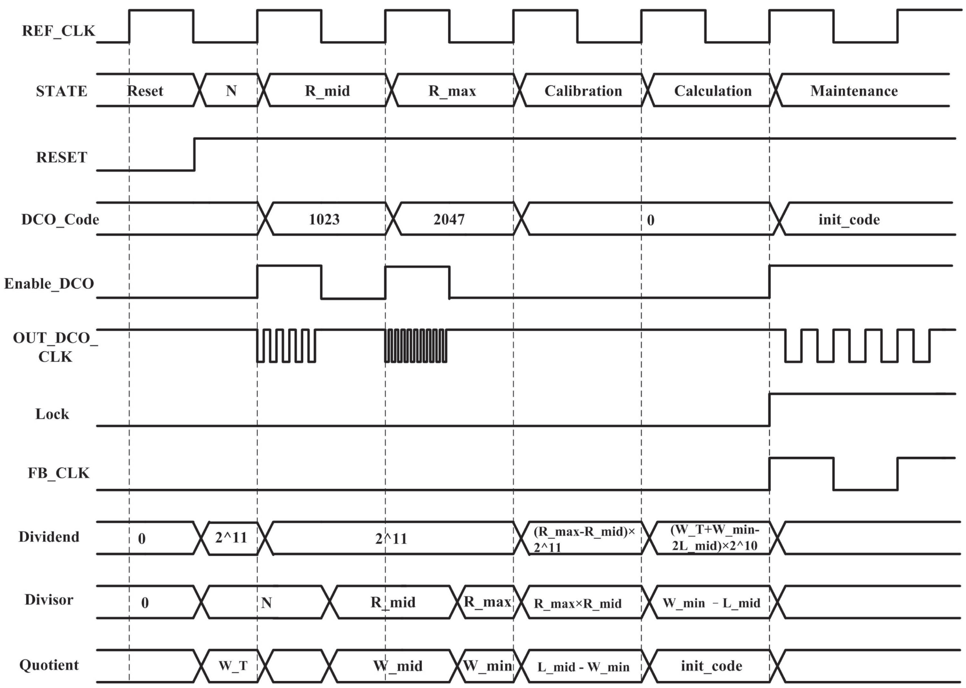

Fig. 3. Timing diagram of the ADPLL.

3 Circuit implementation

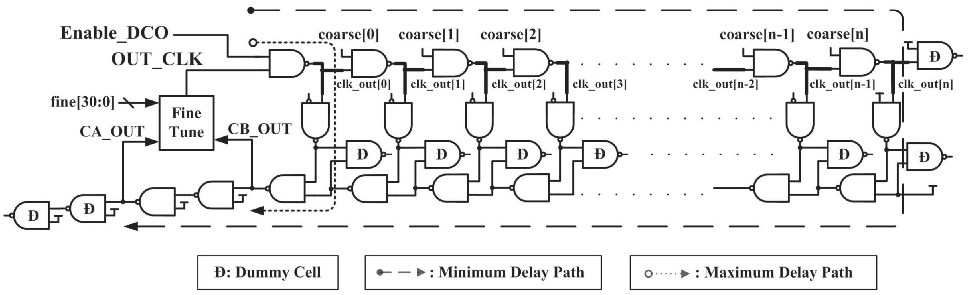

Fig. 4. The proposed DCO.

As we explained earlier, in Eqs. 3–10, a DCO which has linear and monotonic responses is required. Therefore, the DCO should be carefully designed to reduce the frequency error in frequency estimation. The proposed DCO [17] is composed of 63 coarse-tuning stages and 31 fine-tuning stages, as shown in Fig. 4. Four NAND gates constitute a coarse-tuning delay unit (CDU). The 1st NAND gate is operated as a switch that controls the CDU's on and off states. The second and the third NAND

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gates provide the delay time. Thus, the coarse-tuning resolution of the DCO depends on the second and the third NAND gates. The fourth dummy NAND gate is used to balance capacitance loading. The fine-tuning stage architecture of the DCO is composed of two parallel connected tri-state buffer arrays [16]. The two parallel connected tri-state buffer arrays operate as an interpolator circuit controlled by the fine control code. We use 31 tri-state buffers to interpolate the CA_OUT and the CB_OUT signals. The total controllable delay range of the fine-tuning stage is equal to the coarse-tuning resolution of the DCO.

In advanced CMOS processes, interconnection wire delay greatly affects the total delay calculation. Therefore, the relative placement of delay cells during automatic placement and routing (APR) is important from the viewpoint of controlling the wire length between the delay cells. In the proposed DCO, the regular placement approach [17] is adopted to avoid large wire length variations between two neighboring CDUs. Thus, the differential nonlinearity (DNL) of the coarse-tuning stage can be improved. The proposed DCO is implemented in the TSMC 40-nm CMOS process with standard cells. Fig. 5 shows the DNL comparison results of the DCO between the regular placement approach and the random placement approach in an area of $150 \times 80\,\mu\text{m}^2$. The maximum DNL of the DCO with the regular placement is lower than 0.3 least significant bits (LSB) and higher than −0.2 LSB. Therefore, the proposed DCO has linear and monotonic responses, and the period of the DCO can be formulated by a linear equation, as shown in Eq. 5.

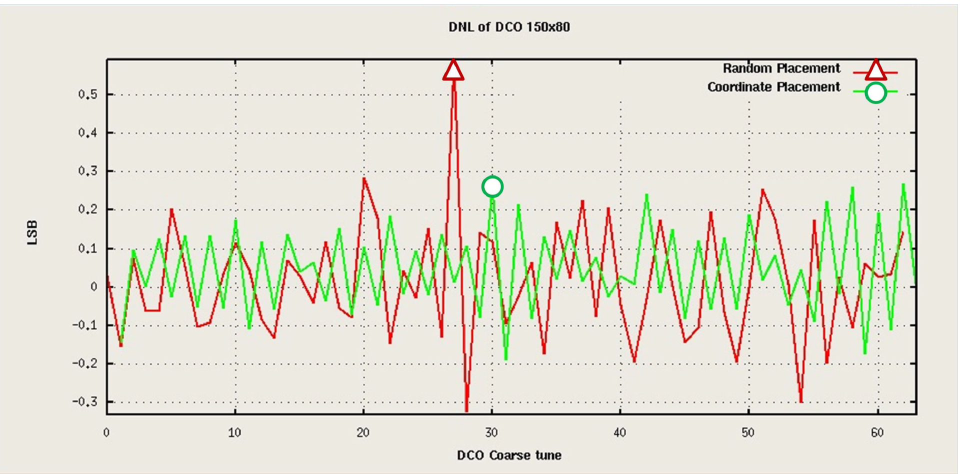

Fig. 5. The DNL of the DCO.

The cell-based bang-bang PFD [2] is implemented in the proposed ADPLL, and the dead zone of the PFD is 17 ps at 0.9 V. The digital loop filter [5] is implemented in the proposed ADPLL to reduce the reference clock jitter effects. The digital loop filter, frequency divider, cyclic counter, frequency finder, and output divider were designed using hardware description language (HDL) and following the cell-based design flow to implement the circuit.

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4 Experimental results

The proposed ADPLL is implemented in the TSMC 40-nm CMOS process with standard cells. The chip layout is shown in Fig. 6. The active area is 120 × 120 µm^2, and the chip area including I/O pads is 620 × 620 µm^2. The output frequency of the proposed ADPLL ranges from 125 MHz to 1.47 GHz, and the power consumption is 0.98 mW (at 0.9 V, 1.47 GHz). Fig. 7 shows the frequency error after 4.5 reference clock cycles with different frequency multiplication factors (N), and the reference clock is a 5 MHz clock. Compared to the ADPLL [10], the proposed ADPLL eliminates the requirement for a high-resolution TDC circuit and reduces the frequency error of the frequency estimation to less than 1%. Table I shows a performance comparison with previously published fast lock-in ADPLLs.

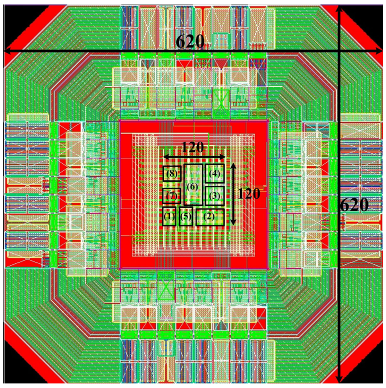

Fig. 6. The layout of the proposed ADPLL.

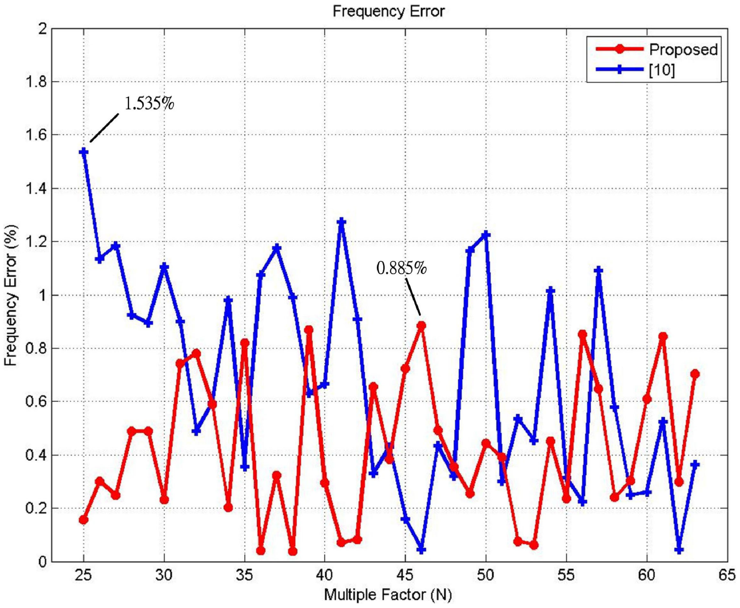

Fig. 7. Frequency error with different multiplication factor.

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Table I. Performance comparison.

Parameter	Proposed	[18] TCAS-II ’13	[20] ICECS ’14	[14] TCAS-II ’10
Process	40-nm	28-nm	65-nm	180-nm
Core Area (μm^2)	120 × 120	52 × 45	360 × 270	250 × 300
Category	ADPLL	ADPLL	ADPLL	ADPLL
Lock-in Time (cycles)	4.5	< 50	45	2
Supply Voltage (V)	0.9	1.0	1.0	1.8
Output Frequency (MHz)	129.8~1465	83~2000	1500~2800	223~446
Power (mW)	0.981 @1.47 GHz	0.64 @2 GHz	8.85 @2.4 GHz	14.5 @446 MHz

5 Conclusion

In this paper, we proposed a fast lock-in ADPLL with a frequency estimation algorithm. The proposed frequency estimation algorithm only requires the period ratio that is calculated by the cyclic counter. In addition, the target DCO control code can be calculated by the frequency finder within 4.5 cycles, and the frequency error after frequency estimation is smaller than 1%. As a result, the proposed ADPLL is suitable for system-on-a-chip applications, which require that ADPLLs be switched off to reduce standby power consumption.

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