ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.11, No.3, 1–6

High-resolution and all-digital on-chip delay measurement with low supply sensitivity for SoC applications

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Abstract: An all-digital on-chip delay measurement (OCDM) architecture with high delay measurement resolution and low supply voltage sensitivity for efficiently detection and diagnosis in the high performance system-on-chip (SoC) applications is presented. Based on the proposed differential delay line pair (DDLP) and an cascade-stage delay line, the quantization resolution of the proposed OCDM not only has a high immunity to supply voltage variations without an extra self-biasing or calibration circuit, but also achieves to several picoseconds. Simulation results show that delay measurement resolution can be improved to 1.04 ps, and the average delay resolution variation is 11 fs with ±10% supply voltage variations. In addition, the proposed design can be implemented in all-digital design manner, making it very suitable for SoC applications as well as system-level integration.

Keywords: OCDM, delay line, low supply sensitivity

Classification: Integrated circuits

References

[1] S. Pei, H. Li and X. Li: IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **20** (2012) 1565.

[2] A. Jain, A. Veggetti, D. Crippa and P. Rolandi: ETS Tech. Dig. Papers (2012) 1.

[3] T. Iizuka and K. Asada: IEICE Trans. Electron. **E95-C** (2012) 627.

[4] K. Katoh, K. Namba and H. Ito: ATS Tech. Dig. Papers (2010) 343.

[5] R. Rashidzadeh, M. Ahmadi and W. C. Miller: IEEE Trans. Instrum. Meas. **59** (2010) 463.

[6] S. Schidl, K. Schweiger, W. Gaberl and H. Zimmermann: Electron. Lett. **48** (2012) 910.

[7] D. Sheng and J.-C. Lan: MWSCAS Dig. Tech. Papers (2011) 1.

DOI: 10.1587/elex.11.20131011
Received December 20, 2013
Accepted December 25, 2013
Publicized January 14, 2014
Copyedited February 10, 2014

1 Introduction

As the semiconductor device size scales down and the performance requirement of electronic product raises, the operating frequency of the advanced system-on-chip (SoC) exceeds several gigahertzes, leading to narrow down the timing margin in the digital circuit. The delay uncertainty, such as clock skew and jitter, degrades the overall system performance and increases the design effort to meet the timing constraints, thus it cannot be ignored particularly in small timing margin [1, 2]. In addition, the timing related defects which are caused by manufacturing process-related problems, such as resistive opens and shorts, device mismatch, etc., become serious problems [1]. Besides, the non-ideal effects, such as negative bias temperature instability (NBTI), hot career injection (HCI), and electromigration (EM), will induce serious reliability issues after shipment [3]. As a result, a technology is required for measuring the delay of critical path or timing uncertainty to ensure the functionality and performance of the high-performance system [1, 4, 5, 6].

Traditionally, the delay characterization can be achieved by the off-chip method. However, due to the accuracy of off-chip delay measurement is dominated by parasitic capacitance, resistance of probe, and transmission line impedance, it is not suitable for the internal-nodes whose timing resolution is required at picoseconds as the timing margin narrows down [2]. Thus, an on-chip delay measurement (OCDM) technique for the high-frequency SoC applications is necessary. Moreover, the at-speed delay measurement can provide the information to improve the overall performance and reduce the power consumption of system with the dynamic voltage and frequency scaling (DVFS) scheme [4].

Fig. 1 illustrates the application scope of OCDM. For example, in the DVFS system, the OCDM circuit can measure the specified timing-critical path delay in a digital block, and then provides such delay information to the frequency/voltage controller. Based on the measured delay provided by the OCDM module, the operating frequency and supply voltage of chip can be adjusted to improve the overall performance and reduce the power consumption. In addition to the timing-critical path delay measurement, the OCDM module can also measure the clock skew between different

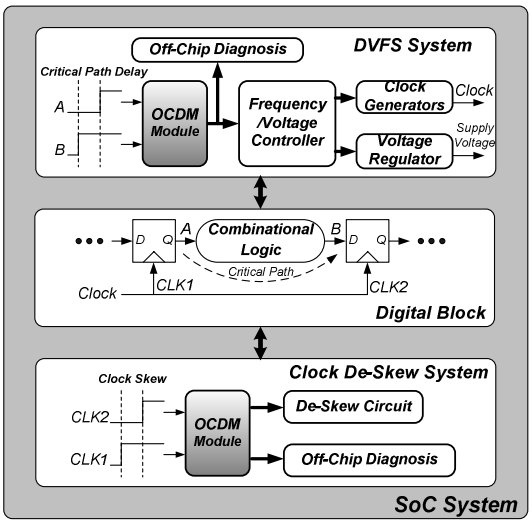

Fig. 1. Application scope of OCDM.

DOI: 10.1587/elex.11.20131011
Received December 20, 2013
Accepted December 25, 2013
Publicized January 14, 2014
Copyedited February 10, 2014

clocks and output the measured data for clock de-skew circuit or diagnosis in off-chip tester machine. Generally, because the considered timing-critical path and clock signal can be specified in the design phase, the number and the location of OCDM modules can be determined before chip fabrication.

The most important criterion of the OCDM is the quantization resolution and stability of timing quantization which determine the accuracy and quality of delay measurement. Basically, the digital approach utilizes delay of delay cell, such as buffer, as the overall quantization resolution. Unfortunately, the supply voltage of the OCDM will be varied due to the nearby circuit influence or other non-ideal effects in the complexity SoC system, leading to change the delay resolution of delay line. Thus, the measurement accuracy of the OCDM will be degraded significantly by supply voltage variations, and the OCDM with low immunity to supply variations is not suitable for high-precision demanded applications. In this paper, an all-digital, high-resolution, and high-immunity to supply voltage variations OCDM scheme is proposed for high-performance SoC applications. Furthermore, all design of the proposed OCDM can be implemented in an all-digital manner, making their integration into digital system easy and very suitable for SoC applications.

2 Proposed OCDM design

2.1 Architecture overview

Fig. 2 illustrates the proposed all-digital OCDM architecture that consists of two digitally controlled delay lines (DCDLs), a phase detector, and a controller. The inputs of digitally controlled delay lines A and B (DCDL_A and DCDL_B) are SignalA and SignalB, respectively, with timing difference which will be measured. The delay of DCDL_A and DCDL_B are controlled by digital control codes DCCA[6:0] and DCCB[6:0], respectively. After SignalA and SignalB propagate through the DCDLs, the delayed version signals (SignalA_D and SignalB_D) are sent into the phase detector (PD) which generate the phase comparison results Lead and Lag. In the beginning, DCCA and DCCB are initialized to zero. Subsequently, the phase detector asserts a digital signal, either Lead or Lag, based on the relation of the SignalB_D rising edge to the SignalA_D rising edge. If the phase detector asserts Lead, the controller increments DCCB by one to enlarge delay of SignalB_D. Conversely, if the phase detector asserts Lag, the controller increments DCCA by one to enlarge

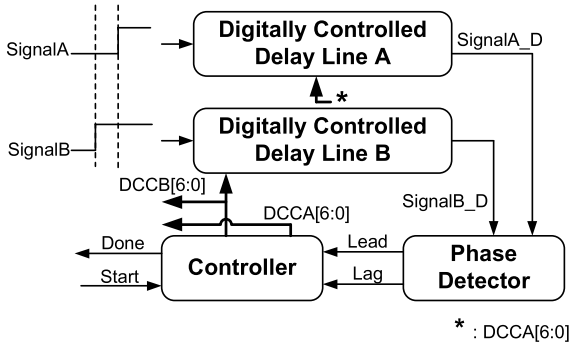

Fig. 2. Proposed OCDM Architecture.

DOI: 10.1587/elex.11.20131011
Received December 20, 2013
Accepted December 25, 2013
Publicized January 14, 2014
Copyedited February 10, 2014

delay of SignalA_D. Phase comparison continues until the phase detector senses a change in the phase polarity of the SignalB_D relative to the SignalA_D. At this point, DCCA and DCCB will be saved and the delay measurement is complete.

The delay between SignalA and SignalB is quantized by the finest delay step of DCDL, and the measured delay can be calculated by the quantization resolution, DCCA, and DCCB. It can be formulated as

$$\begin{aligned} T_M &= ((DCCB \times T_R) + T_I) - ((DCCA \times T_R) + T_I) \\ &= (DCCB - DCCA) \times T_R \end{aligned} \tag{1}$$

where T_M is the delay between SignalA and SignalB, T_R is the quantization resolution (finest delay step) of DCDL, and T_I is the intrinsic delay of DCDL. According to Eq. (1), if T_R is insensitive to supply voltage variations, the same measured delay (T_M) will have the same quantization results ($DCCB$-$DCCA$) under the supply voltage variations. As a result, the delay measurement results of the OCDM will not be affected by supply voltage variations. Thus, this paper attempts to propose a DCDL whose finest delay step is insensitive to supply voltage variations.

2.2 Circuit implementation

The proposed DCDL employs a cascade-stage structure which is composed of a DDLP, and a two-stage delay interpolator: first interpolation stage (1^{st}_IS) and second interpolation stage (2^{nd}_IS), as shown in Fig. 3. The proposed DCDL employs a two-stage delay interpolation structure to improve the delay quantization resolution from one gate delay to several picoseconds [7]. Because the delay interpolator can divide the delay between two input signals into equal part, if the timing difference between LD_OUT and SD_OUT is T_D and the interpolation step of 1^{st}_IS and 2^{nd}_IS are N and M, respectively, the overall delay resolution of DCDL will be T_D/(N*M). According to the design specification, the design parameters are determined as follows: N=8 and M=8.

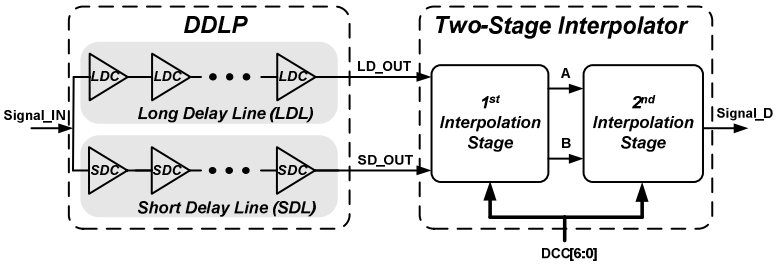

Fig. 3. Proposed DCDL Architecture.

The proposed DDLP has a long delay line (LDL) and short delay line (SDL) that consists of long delay cells (LDCs) and short delay cells (SDCs), respectively. When the supply voltage change, the propagation delay of LDL and SDL can be formulated as

$$T_{LDL1} = T_{LDL0} + \Delta T_{LDL},\ T_{SDL1} = T_{SDL0} + \Delta T_{SDL} \tag{2}$$

$$\text{if } \Delta T_{LDL} = \Delta T_{SDL},\ T_{LDL} - T_{SDL} = T_{LDL0} - T_{SDL0} \tag{3}$$

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where T_{LDL1} and T_{SDL1} are the propagation delay of LDL and SDL after supply changes, respectively. T_{LDL0} and T_{SDL0} are the propagation delay of LDL and SDL before supply changes, respectively. ΔT_{LDL} and ΔT_{SDL} are the delay variation of LDL and SDL caused by supply changes, respectively. If ΔT_{LDL} is equal to ΔT_{SDL}, the delay difference between LDL and SDL (T_D) will maintain the constant value under different supply voltage, as shown in Eq. (2) and (3). The SDC and LDC refer to the standard cell library design to reduce design effort. In the beginning, one delay cell type has been selected from the standard cell library. After the delay cell type has been selected, the delay variation caused by supply changes of all the different driving capability delay cells in the selected delay cell type needs to characterize. According to the delay characterization, it can find out the ratio of delay variation of two different driving capability delay cells. For example, if the ratio of delay variation of BUFX1 and BUFX8 is P/Q, the delay variation of P BUFX8s is equal to Q BUFX1s. The block diagram of the proposed LDL and SDL is shown in Fig. 4. Besides, in order to maintain the output loading matching and input driving capability matching between two delay lines, it needs to employs third delay cell (BUFX4) to construct the SDC and LDC. Because the timing difference between outputs of the DDLP (T_D) and the interpolation step of two interpolation stages (M, N) are not affected by supply variation, the delay quantization resolution of the proposed DCDL ($T_D/(N*M)$) is insensitive to supply voltage variations. As a result, the proposed DCDL not only can achieve delay resolution, but also has a constant delay resolution while the supply voltage of DCDL variation.

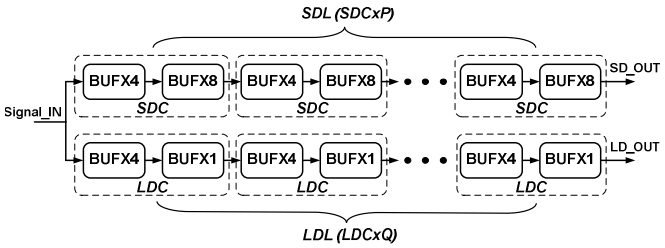

Fig. 4. Block diagram of the proposed SDL and LDL.

3 Experimental results

The proposed all-digital OCDM is implemented in 90 nm 1P9M CMOS process. The simulation results of the proposed OCDM show that the target measured delay is converted to the quantization value, as shown in Fig. 5. The HSPICE simulation results of proposed DCDL are shown in

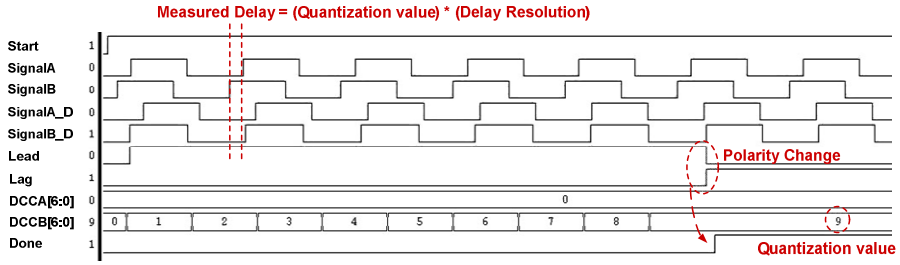

Fig. 5. Simulation results of the proposed OCDM.

DOI: 10.1587/elex.11.20131011
Received December 20, 2013
Accepted December 25, 2013
Publicized January 14, 2014
Copyedited February 10, 2014

Fig. 6. The simulation results show that delay measurement resolution can be improved to 1.04 ps, and the maximum and average variation are 46 fs and 11 fs, respectively, both with ±10% supply voltage variations (from 0.9 V to 1.1 V). As a result, the proposed OCDM can achieve high delay measurement resolution and high immunity to supply voltage variations.

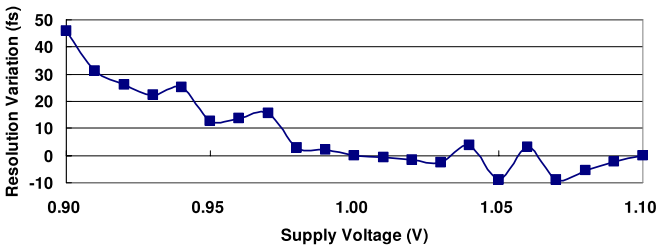

Fig. 6. Simulation results of quantization resolution with supply variations.

4 Conclusions

In this paper, an all-digital, high-resolution, and low-supply sensitivity ODCM design for the advanced SoC applications is presented. The quantization resolution of the proposed OCDM not only has a high immunity to supply voltage variations without an extra self-biasing or calibration circuit, but also achieves to several picoseconds; leading to improve the accuracy and quality of delay measurement. Furthermore, the proposed design can be implemented in all-digital design manner, making it very suitable for SoC applications as well as system-level integration.

Acknowledgments

The authors would like to thank the EDA tool supports of National Chip Implementation Center (CIC), and this project was supported in part by the National Science Council of Taiwan under Grant NSC 101-2221-E-030-025-.

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