

A counter-based all-digital spread-spectrum clock generator with high EMI reduction in 65 nm CMOS

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Abstract: An all-digital spread-spectrum clock generator (ADSSCG) with direct modulation on the digitally controlled oscillator (DCO) is presented. The proposed ADSSCG can generate an accurate triangular modulation on the output frequency, and thus it can achieve high electromagnetic interference (EMI) reduction with a smaller spreading ratio as compared with existing designs. In addition, the proposed frequency counter-based mechanism can maintain the long-term frequency stability of the ADSSCG. The proposed ADSSCG is implemented in a standard performance 65 nm CMOS process, the active area is $85\mu\text{m} \times 85\mu\text{m}$. It consumes $163.9\mu\text{W}$ at 270 MHz with a 1.0 V power supply. The EMI reduction of the proposed ADSSCG is 13.99 dB with a 0.5% spreading ratio at 270 MHz, and 20.23 dB EMI reduction is achieved with a 1.5% spreading ratio at 162 MHz. Moreover, the proposed ADSSCG is designed with standard cells, and thus it can be ported to different process in a short time.

Keywords: EMI reduction, ADPLL, SSCG

Classification: Integrated circuits

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1 Introduction

In a digital system, clock signals become the largest contributor and primary source of electromagnetic interference (EMI). Reducing EMI in digital systems has become an important design issue for electronic system designers. There are many efforts to reduce the EMI, and among these EMI solutions, the spread spectrum clock generator (SSCG) is the most effective. Recently, many types for SSCG have been reported [1, 2, 3, 4]. The direct modulation on a voltage controlled oscillator (VCO) based SSCG [1] usually makes better EMI reduction performance than other modulation methods. However, modulation on VCO usually requires a large on-chip capacitor for the loop filter, and thus it occupies a large chip area. In addition, the capacitance variations can be up to 34% with process variations, and then, it may cause a loop stability problem, as discussed in [3].

The modulation on a frequency divider based SSCG with a delta-sigma modulator (DSM) switches the divider ratio of the frequency divider by $N/N+1$ to make the output frequency modulation profile being close to a triangular modulation. This modulation method can maintain the frequency stability in the spread spectrum state. Moreover, the circuit cost is less than the VCO modulated SSCG because it requires a small on-chip capacitor. Therefore, more and more prior works adopted this modulation method in their SSCG. However, since the phase-locked loop (PLL) still tracks the phase and frequency of the reference clock during the triangular profile generation, the reference clock jitter could influence the triangular profile generation. Therefore, as shown in [2], the measured modulation profile is more close to a sinusoidal modulation profile, and then the EMI reduction is reduced due to the peak power occurs at certain frequencies. In order to disperse peak power averagely, the Hershey-kiss modulation is adopted with a digitally controlled delay-line (DCDL) cascaded with a PLL [4]. This approach can perform sharper modulation profile on both side of frequency domain. Nevertheless, the Hershey-kiss modulation is a very complicated profile, and it may require an extra memory space to perform the profile. Moreover, the DCDL [4] receives the clock from PLL, and thus, it operates at a higher frequency which results in high power consumption. This phenomenon will make this architecture become more complex and will increase the design complexity of the SSCG.

In this paper, we propose an all-digital SSCG (ADSSCG) with a direct modulation on a digital controlled oscillator (DCO). The proposed ADSSCG controls the DCO control code to produce an accurate triangular modulation profile, and thus it can achieve better EMI reduction than the other SSCGs with the same spreading ratio. During the triangular profile generation, the ADSSCG becomes an open loop, and the proposed

frequency counter-based mechanism can maintain the frequency stability of the output frequency at the end of each modulation cycle. With the all-digital approach, the proposed ADSSCG can also achieve relatively low power consumption and a small chip area than existing designs. Besides, the proposed ADSSCG is implemented with standard cells, and thus it can be easily ported to different processes in a short time.

2 Proposed ADSSCG

Fig. 1 shows the block diagram of the proposed ADSSCG. The proposed ADSSCG is composed of a phase and frequency detector (PFD), a DCO with the delta-sigma modulator (DSM), a spread-spectrum clock (SSC) controller, a digital loop filter, a frequency divider, and a frequency detector. The operation of the ADSSCG is based on the all-digital phase-locked loop (ADPLL) [5] with the low-power monotonic DCO which is proposed in [6]. The frequency detector contains two counters to accumulate the cycles of the reference clock (REF_CLK) and the divided clock (DIV_CLK) for the SSC controller to maintain the frequency stability of the output frequency. The SSC controller directly changes the SSC control code (control_code) to modulate the output frequency of the DCO. With the direct modulation method, the spreading ratio can be easily controlled by the SSC controller. A DSM is added in front of the DCO to enhance the DCO resolution.

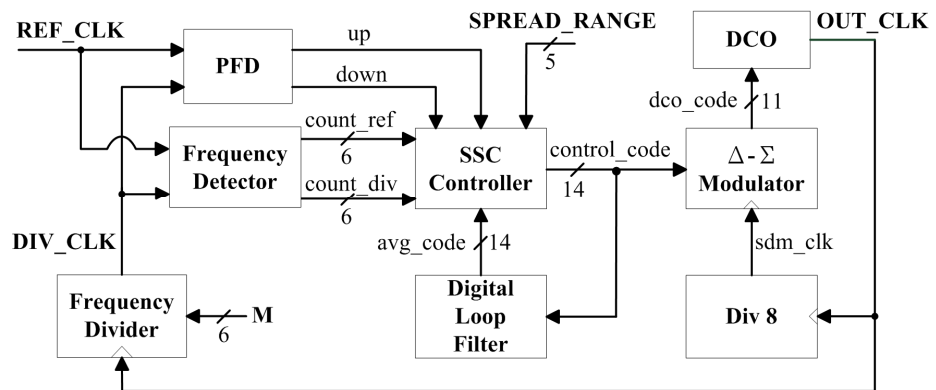


Fig. 1. Proposed ADSSCG.

The operation of the proposed ADSSCG is explained in Fig. 2. When system is reset, the SSC controller performs frequency and phase tracking with the lead/lag information provided by the PFD. After that, the controller starts to perform spread spectrum operation. There are four states (state_ssc) in the SSCG. In the first three states, the SSC controller directly modulates the SSC control code (control_code) to generate a triangular modulation profile. Because the first three states perform spread spectrum with an open-loop scheme, the ideal triangular modulation profile can be realized very easily. The spreading range is programmable to provide the corresponding spreading ratio, and it makes the proposed ADSSCG have a more flexible spreading range. The fourth state is frequency adjustment state. In the fourth state, the SSC controller uses the values of count_ref and count_div from the frequency detector to adjust the output frequency. After frequency adjustment, the new modulation cycle continues repeatedly. In the frequency adjustment state, the loop filter [5] receives the

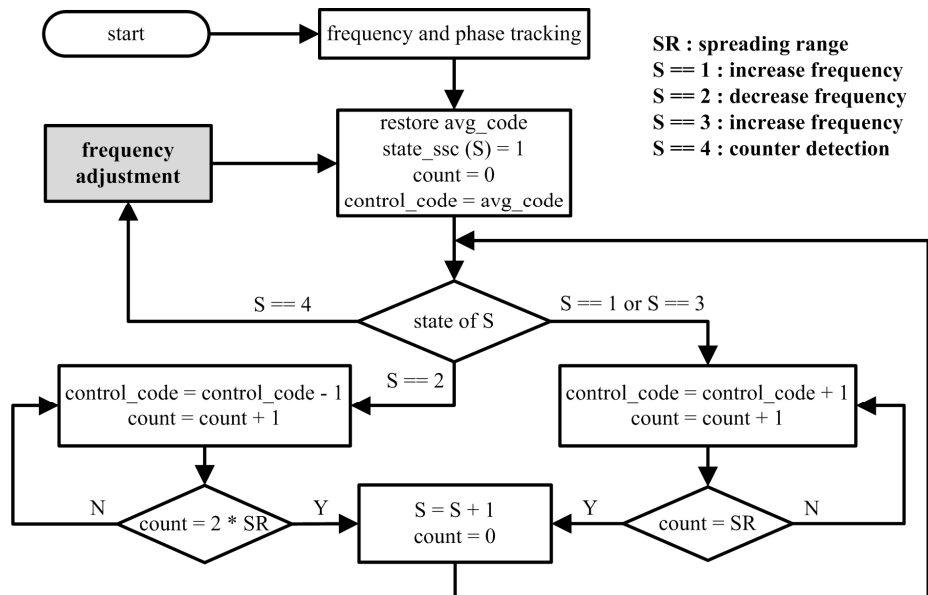


Fig. 2. Flowchart of the spread spectrum operation.

SSC control code (control_code), and it will keep updating the baseline SSC control code (avg_code) to maintain the long-term frequency stability.

The difference between two counter values: count_ref and count_div provides the information about the long-term average frequency deviations between the reference clock and the divided clock. The SSC controller compares these values in the end of each modulation cycle, as shown in Fig. 3 and Fig. 4. If two counter values are the same, the frequency drift between the reference clock and the divided clock is very small. If count_ref is larger than count_div, it means the average frequency of the divided clock is slower than the reference clock, and thus the SSC controller increases the SSC control code (control_code) to speed up the DCO. Oppositely, if counter_ref is smaller than count_div, the SSC controller decreases the SSC control code (control_code) to slow down the DCO.

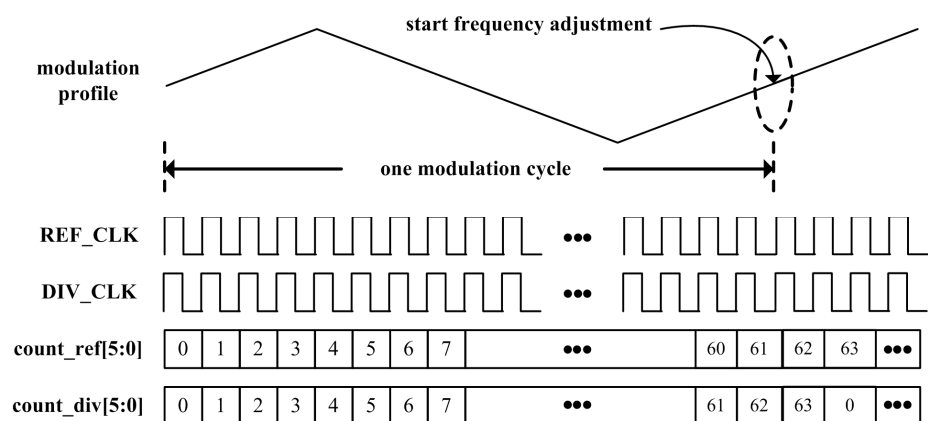


Fig. 3. Modulation profile and frequency adjustment.

However, since the modulation frequency is around 30 kHz, there are many reference clock and divided clock cycles within one modulation cycle. The bit size of these counters is set to 6 bits to reduce the hardware cost. Thus when the difference between two counters are larger than 32, it means one counter is overflowed. For example, if count_div is overflowed, and

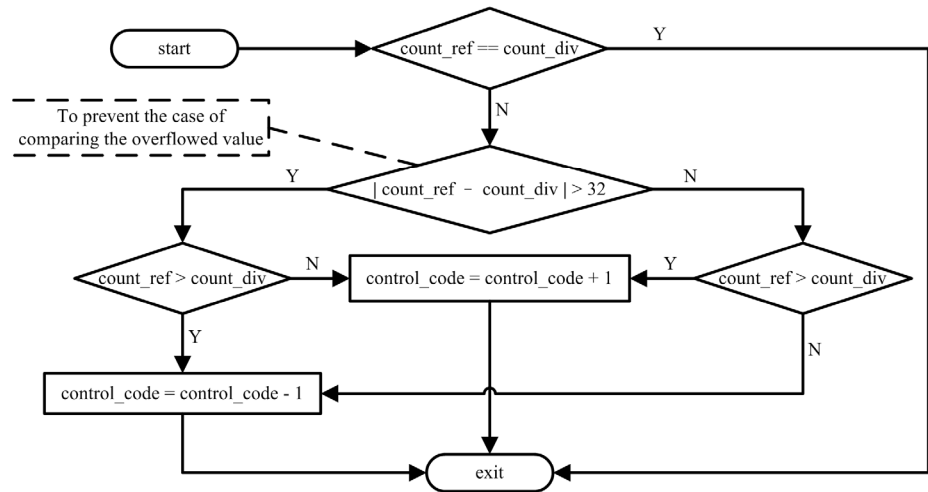


Fig. 4. Flowchart of frequency adjustment.

count_ref is larger than count_div, then it means the SSC controller should decrease the SSC control code (control_code) to slow down the DCO, as shown in Fig. 4. With the frequency adjustment mechanism, the average frequency can be easily maintained and against process, voltage, and temperature (PVT) variations with the proposed frequency detector.

3 Simulation results and comparisons

The proposed ADSSCG is implemented in a standard 65nm CMOS process. The operation frequency ranges from 162 MHz to 270 MHz for DisplayPort main link application. The active area of the ADSSCG is $85\mu\text{m} \times 85\mu\text{m}$, and the power consumption is $163.9\mu\text{W}$ at 270 MHz. The lock-in time of the proposed ADSSCG is 77 cycles with an input 6.75 MHz reference clock. The peak-to-peak period jitter of the output clock with spread-spectrum function turned off at 270 MHz and 162 MHz are 21.1 ps and 20.2 ps, respectively. Figs. 5a and 5b show the simulated power spectral density of the proposed ADSSCG. The EMI reduction is 13.99 dB at 270 MHz with a 0.5% spreading ratio, as shown in Fig. 5a, and the EMI reduction is 20.23 dB at 162 MHz with a 1.5% spreading ratio, as shown in Fig. 5b. With the modulation method on DCO, the proposed ADSSCG can

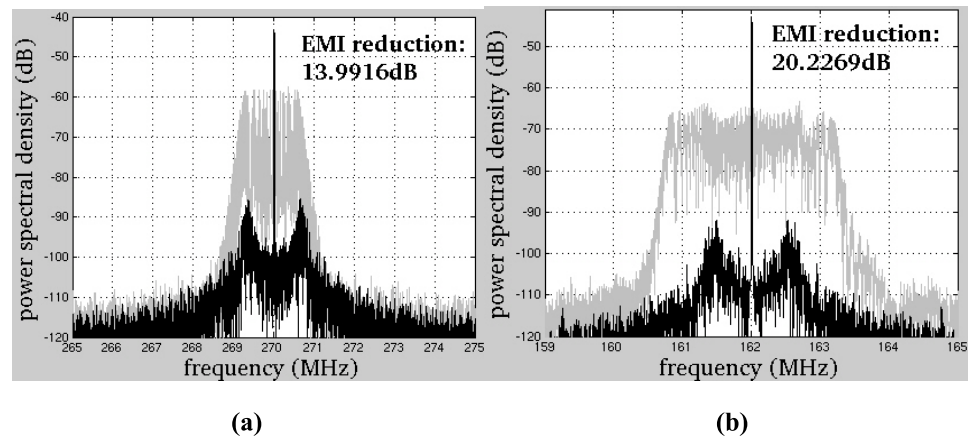


Fig. 5. Simulated power spectral density. (a) 270 MHz with a 0.5% spreading ratio. (b) 162 MHz with a 1.5% spreading ratio.

make an accurate triangle modulation profile and provides better EMI reduction as compared with the existing designs.

The comparison table is shown in Table I. From Table I, we can see that the proposed ADSSCG outperforms better EMI reduction than prior works. The proposed ADSSCG also occupies the smallest chip area and lowest power consumption than prior works.

Table I. Comparison Table.

	Proposed	[1]	[2]	[3]	[4]
Modulation profile	Triangular	Triangular	Triangular	Triangular	Arbitrary
Modulation method	DCO	VCO	$\Delta\Sigma$	VCO	Digital Delay-Line
EMI reduction	13.99dB @270MHz	11dB @266MHz	10.48dB @1.5GHz	8.75dB @270MHz	10.6dB @750MHz
Output frequency	162MHz~ 270MHz	66MHz~ 266MHz	1.5GHz	162MHz~ 270MHz	180MHz~ 1.27GHz
P_K-P_K Jitter	21ps	162ps	28.4ps	42.8ps	93ps
Process	65nm	0.35 μ m	0.18 μ m	0.18 μ m	65nm
Core area	0.007225mm ²	2.0mm ²	0.2mm ²	1.8mm ²	0.044mm ²
Power consumption	163.9 μ W @270MHz	300mW @266MHz	15mW @1.5GHz	19mW @270MHz	44mW @1.27GHz
Experimental Results Type	Simulated	Measured	Measured	Measured	Measured

4 Conclusion

In this paper, we propose a direct modulation on DCO based ADSSCG with a counter-based frequency adjustment mechanism. The direct modulation method on the DCO can make better EMI reduction. The frequency counter can maintain the frequency stability while performing spread spectrum. Moreover, due to the counter-based mechanism, the design complexity can be reduced. With an all-digital approach, the chip area and power consumption can also be reduced substantially. Finally, the proposed ADSSCG is implemented with standard cells, and therefore, it is very suitable for system-on-a-chip (SoC) applications.

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