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A wide-range all-digital duty-cycle corrector with output clock phase alignment in 65 nm CMOS technology

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Abstract: A wide-range all-digital duty-cycle corrector (ADDCC) with output clock phase alignment is presented in this paper. The proposed ADDCC can correct the duty-cycle error of the input clock to 50% duty-cycle. The acceptable duty-cycle range and frequency range of input clock is from 20% to 80% and from 250 MHz to 1 GHz, respectively. The proposed ADDCC is implemented on a standard performance 65 nm CMOS process, and the power consumption is 1.52 mW at 250 MHz and 5.83 mW at 1 GHz, respectively.

Keywords: clocks, delay lines, duty cycle corrector

Classification: Integrated circuits

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1 Introduction

In high-speed applications, such as double data rate (DDR) SDRAM or double sampling analog-to-digital converter (ADC), the positive edge and the negative edge of the clock are utilized for sampling the input data. Thus, these systems require an exact 50% duty-cycle of input clock. However, the clock is distributed over the chip using clock buffers, and thus, the duty-cycle of the clock is affected by the unbalanced rise time and fall time of the clock buffers with process, voltage and temperature (PVT) variations. In order to overcome such problem, many approaches have been proposed to adjust the clock duty-cycle to 50% to meet the system requirements, such as pulse-width control loop (PWCL) [1, 2] and duty-cycle corrector (DCC) [3, 4, 5, 6, 9, 10].

The conventional PWCL changes the feedback control voltage to adjust the duty-cycle of the input clock. Based on the architecture requirements, it requires a ring oscillator to produce 50% duty-cycle reference, and the operating range and the acceptable input duty-cycle error are very restricted in this architecture [1]. The operating range of the PWCL can be improved by the linear control stage and the digitally controlled charge pump (DCCP) [2]. However, it takes long lock-in time, and the leakage current problem of the charge-pump makes it not suitable for a nano-meter CMOS process.

Recently, different architectural solutions have been proposed to implement the DCC. The synchronous mirror delay (SMD) based all-digital DCC (ADDCC) uses a half-cycle delay line (HCDL) to produce a 50% duty-cycle clock [4, 5]. Although it consumes low power consumption, the HCDL has delay mismatch problems in a nano-meter CMOS process. The time-to-digital converter (TDC) based ADDCC quantizes the period information of the input clock into digital codes, and then a clock with a HCDL is generated using the delay line of the TDC to produce a 50% duty-cycle clock [5, 6]. Nevertheless, the length of the delay line limits the operating frequency range of this architecture, and the output duty-cycle error is restricted by the timing resolution of the TDC.

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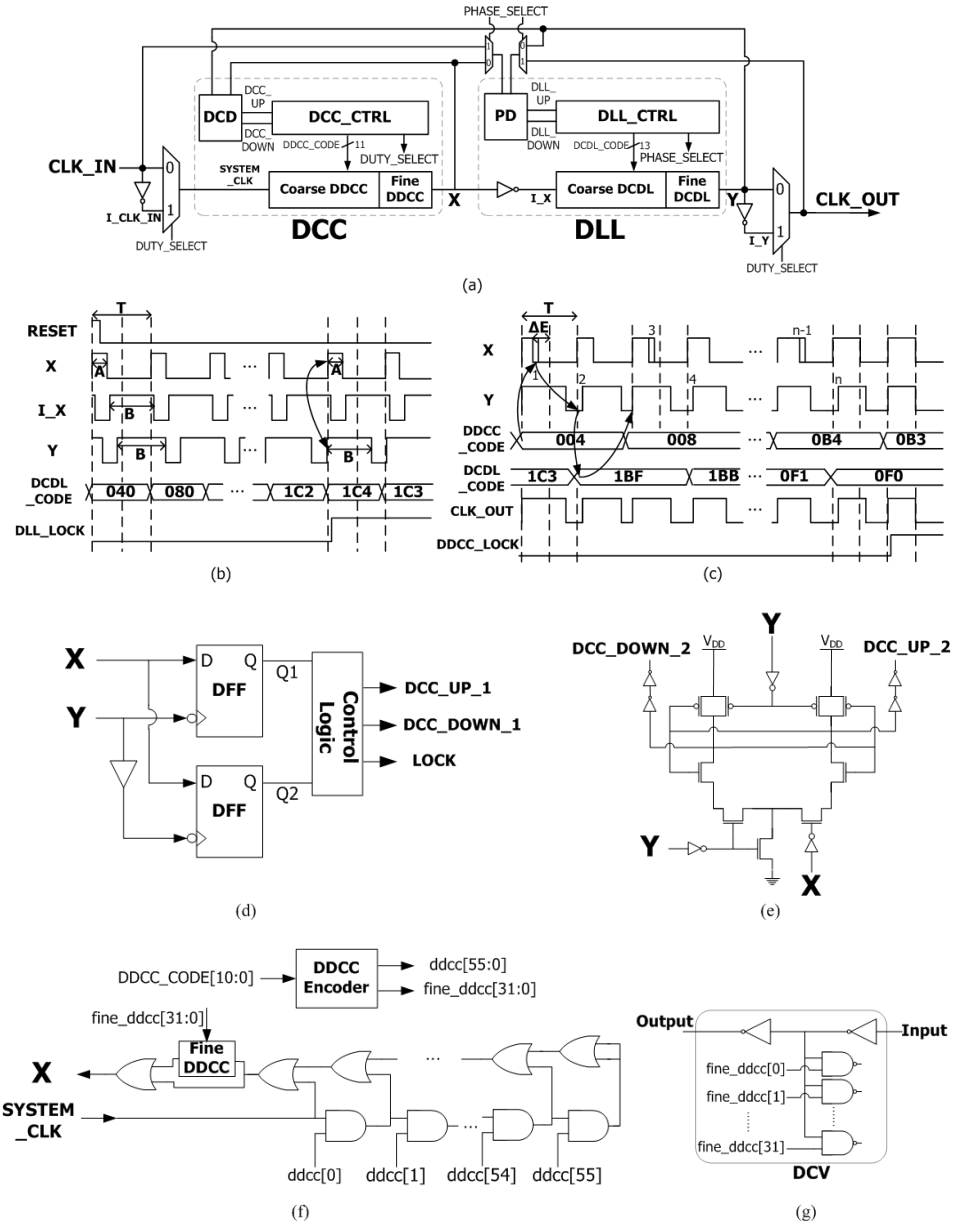

Fig. 1. (a) The proposed ADDCC, Timing diagram: (b) DLL and (c) DCC, (d) Sampled-based bang-bang phase detector, (e) Tiny dead zone phase detector, (f) Coarse DDCC circuit, (g) Fine DDCC circuit.

In this paper, a wide-range ADDCC with output clock phase alignment is presented. The proposed high resolution duty-cycle detector with an all-digital duty-cycle correction delay line can overcome the TDC resolution limitations, and the proposed architecture can avoid the half-delay line delay mismatch problems in prior studies.

2 Overall circuit description

The block diagram of the proposed ADDCC is shown in Fig. 1 (a). It is composed of an all-digital duty-cycle corrector (DCC) and an all-digital delay-

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locked loop (DLL). The all-digital DCC consists of a duty-cycle detector (DCD), a coarse-tuning digital controlled duty-cycle correction delay line (Coarse DDCC), a fine-tuning digital controlled duty-cycle correction delay line (Fine DDCC), and a DCC controller (DCC_CTRL). The all-digital DLL consists of a phase detector (PD), a coarse-tuning digitally controlled delay line (Coarse DCDL), a fine-tuning digital controlled delay line (Fine DCDL), and a DLL controller (DLL_CTRL).

The timing diagram for the DLL operation is shown in Fig. 1 (b). After system is reset, the DUTY_SELECT signal is set to "0," and the PHASE_SELECT signal is also set to "0". The input clock (CLK_IN) is passed through the DCC's delay line and outputted as X signal. Subsequently, the inverted X signal is then passed through the DLL's delay line and outputted as Y signal. The phase detector (PD) of the DLL compares the phase error between the positive edges of X and Y, and then it outputs DLL_UP/DLL_DOWN control signals to the DLL_CTRL. The DLL_CTRL adjusts the delay line control code (DCDL_CODE) to compensate for the phase error. When the phase error between X and Y is eliminated, the DLL is locked. After that, two clocks (i.e. X and Y) with complementary duty cycles are generated. Thus, if the period of the input clock (CLK_IN) is T, and the duty-cycle of X and Y is A/T and B/T, respectively, the period T is equal to (A+B).

After the DLL is locked, the proposed all-digital DCC starts to compensate for the duty-cycle error of the output clock (CLK_OUT). The duty-cycle detector (DCD) detects the phase error between the negative edges of X and Y, and then it outputs DCC_UP/DCC_DOWN control signals to the DCC_CTRL. The DCC_CTRL adjusts the duty-cycle correction delay line control code (DDCC_CODE) to enlarge the pulse width of the X signal according to the outputs of the DCD. The timing diagram for the DCC operation is shown in Fig. 1 (c). In the first cycle, the DCC extends the pulse width of the X signal. Then, in the next cycle, the positive edge of the Y signal will lag behind the positive edge of the X signal due to the pulse extension in the previous cycle. Thus in the second cycle, the DCDL_CODE is decreased to align the positive edges of X and Y. The same process will be repeated until that both the positive edge and negative edge of X and Y are phase aligned, and then the DCC is locked.

The pulse width of the X signal is increased by ΔE, and ΔE is equal to (B-A)/2. Since the period of input clock (CLK_IN) is T, (A+ΔE) is equal to $T/2(= A + (B - A)/2 = (A + B)/2)$. As a result, after the DCC is locked, the duty-cycle of the CLK_OUT is 50%. Once the DCC is locked, PHASE_SELECT signal is set to "1". The inputs of the DLL's PD are switched to the CLK_IN and the CLK_OUT. Then, the DLL will adjust the DCDL_CODE to compensate for the phase error between the CLK_IN and the CLK_OUT. Therefore, the output clock (CLK_OUT) can be phase aligned with the input clock (CLK_IN).

In Fig. 1 (b), after the DLL is locked, if the negative edge of the X signal lags behind the negative edge of the Y signal, which means the duty-cycle of

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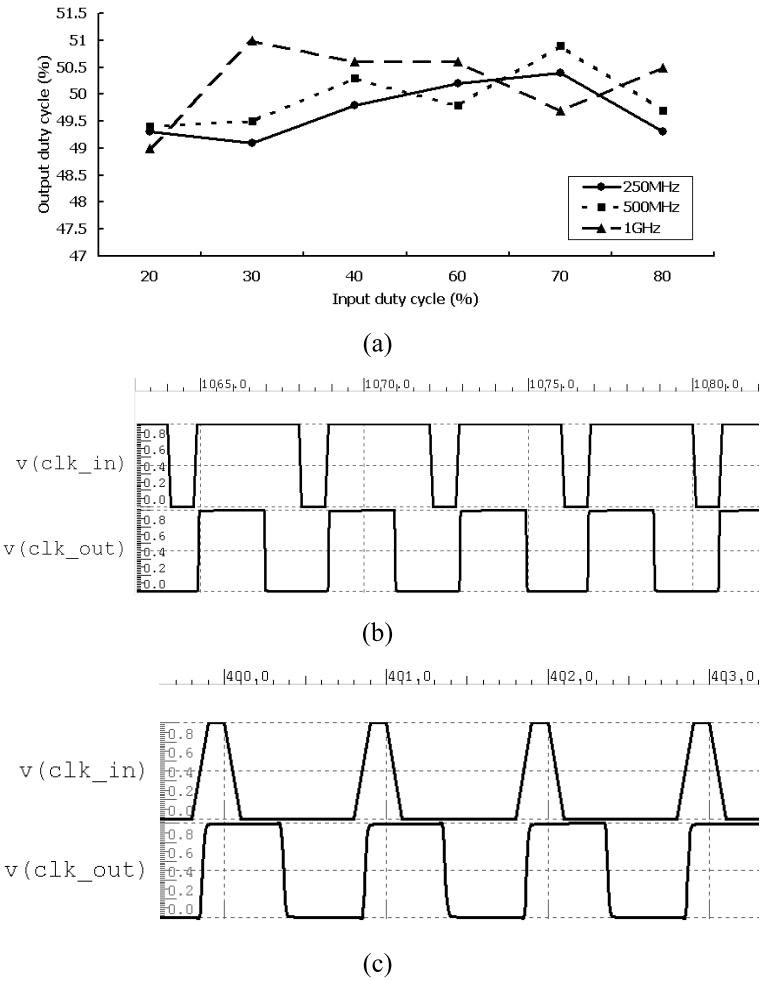

Fig. 2. (a) Simulation results of 20% ∼ 80% input duty-cycle at 250 MHz, 500 MHz and 1 GHz, (b) Simulation waveform of 80% input duty-cycle at 250 MHz, (c) Simulation waveform of 20% input duty-cycle at 1 GHz.

the input clock is larger than 50%. Then, the DUTY_SELECT signal is set to "1", and therefore, the input clock is switched to the inverted CLK_IN to guarantee the duty-cycle of X signal is always smaller than 50%. In addition, the output clock is switched to the inverted Y signal, and the DLL will also eliminate the phase error between the CLK_IN and the CLK_OUT.

The operating frequency range of the proposed ADDCC is limited by the length of the DDCC and the DCDL. Based on the requested frequency range for DDR2 and DDR3 I/O bus application, the length of delay line is determined to meet the system requirements. For example, when the input clock frequency is 250 MHz (period=4000 ps) and input duty-cycle is 20%, the DCDL needs to provide a delay time larger than 3200 ps (=4000 ps × 80%). Meanwhile, the DDCC needs to compensate for a duty-cycle error with 1200 ps (=4000 ps × 30%).

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3 Circuit implementation

The proposed DCD is composed of a sampled-based PD and a tiny dead zone PD, as shown in Fig. 1 (d) and Fig. 1 (e), respectively. The dead zone of the sampled-based PD is restricted by the dead zone of the D-Flip/Flops. In order to improve the detectable phase error, a sense-amplifier-based PD [7] which can detect a phase error larger than 1 ps in 65 nm CMOS process is applied in the DCD design. Although the tiny dead zone PD has good phase error detection ability, when phase error between X and Y is very large, it will output wrong UP/DOWN pulses due to the MOS leakage current in the internal floating nodes. As a result, in the beginning, the DCC_CTRL adjusts the DDCC_CODE according to the sampled-based PD's outputs (DCC_UP_1 and DCC_DOWN_1). After the sampled-based PD is locked, the DCC_CTRL continues to adjust the DDCC_CODE by the tiny dead zone PD's outputs (DCC_UP_2 and DCC_DOWN_2). The proposed DCD can detect a tiny phase error between the negative edge of X and Y. Therefore, the duty-cycle error of the output clock can be further reduced.

The detail circuits of the Coarse DDCC and the Fine DDCC are shown in Fig. 1 (f) and Fig. 1 (g), respectively. The Coarse DDCC is composed of a chain of OR gates to enlarge the pulse width of the SYSTEM_CLK. The DDCC Encoder is used to convert the binary control code (DDCC_CODE [10:0]) into the thermometer codes (ddcc[55:0] and fine_ddcc[31:0]). The Fine DDCC is added to further improve the resolution of the proposed duty-cycle correction circuit. In the Fine DDCC, the digitally controlled varactors (DCVs) [8] are applied to improve the resolution of the fine-tuning delay cell to about 3 ps.

4 Experimental results

The proposed ADDCC is implemented on a standard performance 65 nm CMOS process with 1.0 V power supply, and the core area is 0.01 mm^2 including the test circuit. The simulation results of the proposed ADDCC are summarized in Fig. 2 (a). The frequency range of the input clock is 250 MHz to 1 GHz, and the duty-cycle range of the input clock is from 20% to 80%. Fig. 2 (b) and Fig. 2 (c) show the simulation waveform of the proposed ADDCC under different input frequencies and duty-cycle errors. The power consumption of the proposed all-digital DCC is 5.83 mW (@1 GHz) and is 1.52 mW (@250 MHz).

The performance comparisons are shown in Table I. In [3, 6, 10], the TDC-based all-digital DCC architecture must have a high resolution TDC to minimize the duty-cycle error. However, it is not easy to design a wide-range high resolution TDC. Therefore, they are not suitable for wide frequency range operation. In [9], the output clock is not phase aligned with the input clock. Compared to prior studies, the proposed ADDCC not only has a wider frequency range, but also has a wider input duty-cycle range.

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Table I. Performance Comparisons.

	This Work	[3]	[6]	[9]	[10]
Process	65nm	0.35μm	0.18μm	0.18μm	0.18μm
Supply voltage	1.0V	3.3V	1.8V	1.8V	1.8V
Max. Frequency (MHz)	1000	600	1200	1250	1500
Min. Frequency (MHz)	250	400	800	800	440
Input Duty Cycle Range	20%~80%	30%~70%	40%~60%	40%~60%	40%~60%
Output 50% Duty Cycle Error	-0.9%~0.4%@250MHz -0.6%~0.9%@500MHz -1.0%~1.0%@1GHz	±0.64%	-1.5%~1.4%	±0.6%	±1.8%
Align with input clock	Yes	Yes	Yes	No	Yes
Power consumption	5.83mW@1GHz 3.03mW@500MHz 1.52mW@250MHz	20mW@500MHz	15mW@1GHz	16mW@1GHz	43mW@1.5GHz
Area (mm^2)	0.01	0.68	0.23	0.09	0.053
Experimental Results Type	Simulation	Measurement	Measurement	Simulation	Measurement

5 Conclusion

In this paper, a wide-range all-digital DCC with output clock phase alignment is presented. The proposed DCC architecture can achieve wide-range operation with input frequency ranges from 250 MHz to 1 GHz and input duty-cycle ranges from 20% to 80%. Furthermore, it overcomes the TDC resolution limitations and HCDL delay mismatch problems in prior studies. As a result, it is very suitable for duty-cycle correction applications in system-on-a-chip (SoC) era.

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