IEICE Electronics Express, Vol.7, No.9, 634–639

Fast-lock all-digital DLL and digitally-controlled phase shifter for DDR controller applications

Duo Sheng[1a)], **Ching-Che Chung**[2], **and Chen-Yi Lee**[1]

[1] *Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University,*
1001 University Road, Hsinchu 300, Taiwan

[2] *Department of Computer Science & Information Engineering, National Chung-Cheng University,*
168 University Road, Minhsiung, Chia-Yi 621, Taiwan

a) *hysteria@si2lab.org*

Abstract: A fast-lock and portable all-digital delay-locked loop (ADDLL) with 90° phase shift and tunable digitally-controlled phase shifter (DCPS) for DDR controller applications are presented. The ADDLL can achieve small phase-shift error in 1.3° at 400 MHz and locking time of less than 13 clock cycles, making it very suitable for low-power DDR controller with power-down mode. The proposed DCPS provides the suitable phase shift of control signals for DDR interface where precise control is the key to reliable high-performance operation. Besides, the cell-based implementation makes it easy to target a variety of technologies as a soft silicon intellectual property (IP).

Keywords: ADDLL, DCPS, portable, fast lock, DDR controller
Classification: Integrated circuits

References

[1] JEDEC, "DDR2 SDRAM Specification," *JESD79-2E*, April 2008.
[2] T. Yoshimura, Y. Nakase, N. Watanabe, Y. Morooka, Y. Matsuda, M. Kumanoya, and H. Hamano, "A delay-locked loop and 90-degree phase shifter for 100 Mbps double data rate memories," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 66–67, June 1998.
[3] J.-H. Bae, J.-H. Seo, H.-S. Yeo, J.-W. Kim, J.-Y. Sim, and H.-J. Park, "An All-Digital 90-Degree Phase-Shift DLL with Loop-Embedded DCC for 1.6 Gbps DDR Interface," *CICC Dig. Tech. Papers*, pp. 373–376, Sept. 2007.
[4] K.-I. Oh, L.-S. Kim, K.-I. Park, Y.-H. Jun, and K. Kim, "Low-jitter multiphase digital DLL with closest edge selection scheme for DDR memory interface," *Electron. Lett.*, vol. 44, no. 19, pp. 1121–1123, Sept. 2008.
[5] C.-C. Chung, P.-L. Chen, and C.-Y. Lee, "An All-Digital Delay-Locked Loop for DDR SDRAM Controller Applications," *Proc. IEEE VLSI-DAT*, pp. 199–202, Apr. 2006.

DOI: 10.1587/elex.7.634
Received March 12, 2010
Accepted April 12, 2010
Published May 10, 2010

[6] D. Sheng, C.-C. Chung, and C.-Y. Lee, "An ultra-low-power and portable digitally controlled oscillator for SoC applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 11, pp. 954–958, Nov. 2007.

1 Introduction

As the operating frequency of electronic systems increases, double data rate (DDR) memories have been widely used for memory performance enhancement. The data transfers are based on the bidirectional data strobe (DQS) that is transmitted along with data (DQ) for capture [1]. In order to enlarge the data valid window in the DDR controller and device, DQS delayed by 90° phase shift to the center of the data period by the DDR controller generally. Many delay-locked loops (DLLs) and phase shifters have been proposed to provide the 90° phase-shift clock or DQS required to transfer data correctly in the high-speed DDR memory controller [2, 3, 4]. In the physical implementation, the phase shifters may have long wire distance from DLL. Because the digital control signal is more robust when it has long wire path propagation, the digitally-controlled phase shifter (DCPS), controlled by digital control signal, is more suitable for high-performance DDR controller applications. Thus, many all-digital DLLs (ADDLLs) providing the digital control code for the DCPS have been proposed [3, 4]. However, these ADDLLs take long locking time, implying that they are not suitable for the low-power DDR controller whose clock signals should be generated in a short time when the controller switches from power-down to active mode. Furthermore, because of delay mismatches from interconnection of multi-chip, the effective data valid window will be reduced and the maximum attainable frequency will be further limited even DQS has been delayed by 90° phase shift.

In this work, the proposed ADDLL utilizes a time-to-digital converter (TDC) to reduce locking time and a digitally-controlled delay line (DCDL) to achieve high speed and keep high delay resolution to generate 90° phase-shift clock with small phase-shift error. The phase shift of DQS can be tuned by the proposed DCPS to provide the suitable phase adjustment instead of the fixed 90° phase shift, resulting in a wider data capture window. Furthermore, the proposed ADDLL and DCPS use cell-based design approach, making it easily be integrated into digital system and ported to different processes.

2 The proposed ADDLL and DCPS

The architecture of the proposed ADDLL which consists of five major functional blocks: TDC, DCDL, phase detector (PD), ADDLL controller, and control code decoder as shown in Fig. 1 (a). The locking procedure is divided into two steps: coarse locking by TDC and fine locking by the binary search algorithm. In the beginning, ADDLL takes four clock cycles to generate TDC control code to determine the coarse controlling code of DCDL for the output clock signal CLOCK1 (P360) which is delayed by one clock period

DOI: 10.1587/elex.7.634
Received March 12, 2010
Accepted April 12, 2010
Published May 10, 2010

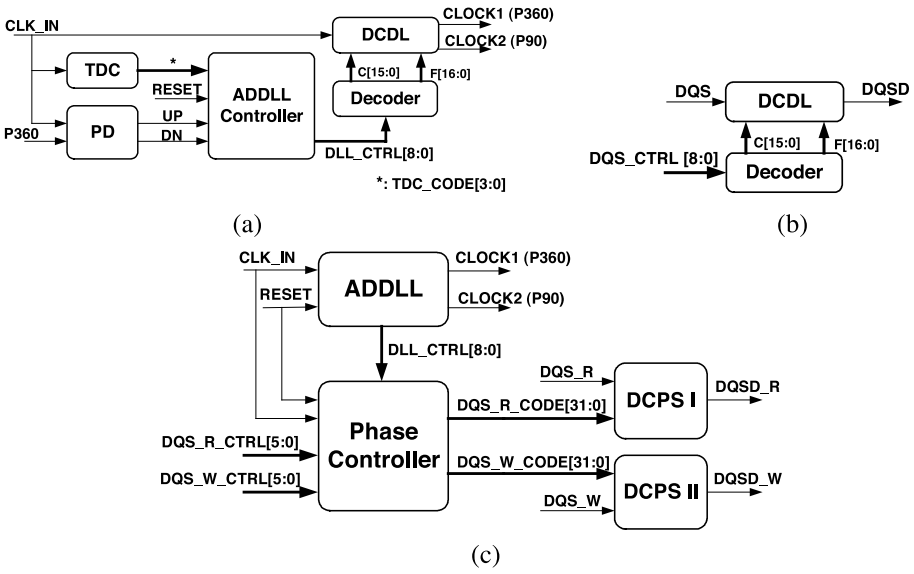

Fig. 1. Architecture of (a) ADDLL (b) DCPS (c) clock generator and phase shifter of DDR controller

approximately. After coarse locking, DCDL control code will be fine tuned by ADDLL controller based on UP/DN from PD to control the delay of DCDL to align phase between CLK_IN and CLOCK1 (P360). The worst case for lock time of the binary search algorithm, in terms of input clock cycle, is

$$T \quad = \left(2 \times \log_2 2 \quad \right) - 1 \tag{1}$$

where T is the lock time of fine tuning and N is number of bits of the binary search control code. The entire phase locking procedure takes 13 clock cycles including 4 cycles TDC operation and 9 cycles (N=5) for the fine-tuning phase locking. In addition, control code decoder converts the DCDL control code from binary to thermal format. Fig. 1 (b) illustrates the structure of the proposed DCPS including one decoder and one DCDL which are the same as the design in ADDLL for delay matching.

Fig. 1 (c) illustrates the clock generator and phase shifters of DDR controller that consists of four major functional blocks: phase controller, ADDLL, and two DCPSs. After ADDLL is locked, it generates two clock signals: CLOCK1 (phase aligned with input clock) and CLOCK2 (90° delayed with input clock), and the DLL control code (DLL_CTRL) for phase controller. In the beginning, DCPS uses the DLL_CTRL without any adjustment (DQS_R_CTRL and DQS_W_CTRL are both set to zero), it will generate delayed DQS with 90° phase shift which is the same as CLOCK2 in ADDLL. If the core system has detected that DDR memory system fails to meet performance specification, the control code of read/write DQS (DQS_R_CODE/DQS_W_CODE) will be increased or decreased sequentially by the phase adjustment codes to generate the suitable phase shift of the delayed read/write DQS (DQSD_R/DQSD_W) to compensate the delay mismatching by interconnection between DDR devices and core system.

DOI: 10.1587/elex.7.634
Received March 12, 2010
Accepted April 12, 2010
Published May 10, 2010

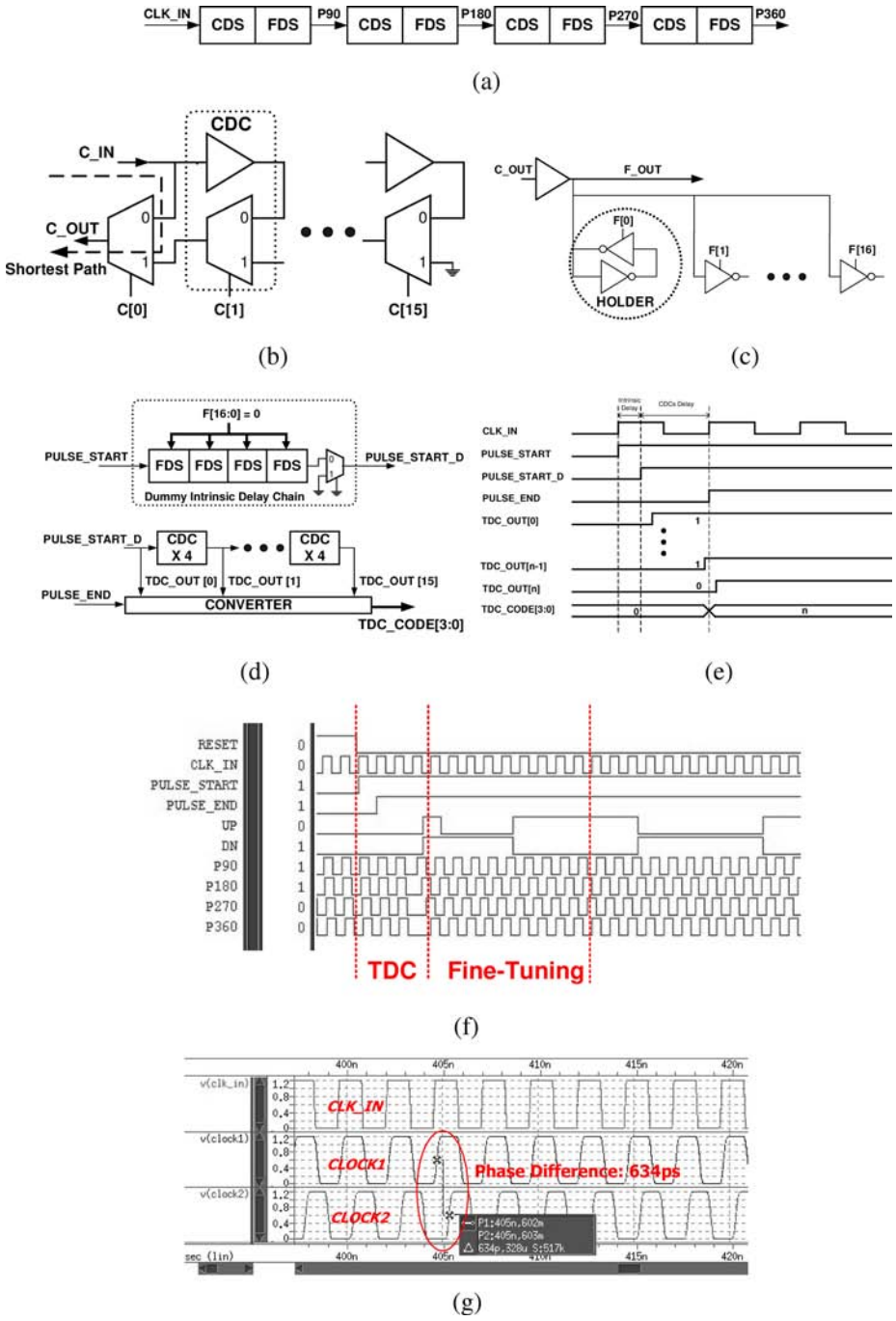

Fig. 2. (a) Proposed DCDL (b) coarse-delay stage (CDS) (c) fine-delay stage (FDS) (d) proposed TDC (e) TDC waveform, simulation results: (f) locking procedure of ADPLL (g) phase shift between CLOCK1 and CLOCK2 at 400 MHz

3 Circuit description

3.1 Digitally-controlled delay line

According to the requirements of ADDLL, it has to provide 4-phase clock signal with equal delay space within one input cycle. The proposed DCDL employs this cascade-stage structure to achieve high delay resolution and high speed at the same time [6]. The proposed DCDL has four duplicated delay

DOI: 10.1587/elex.7.634
Received March 12, 2010
Accepted April 12, 2010
Published May 10, 2010

stages, and each of which has one coarse-delay stage (CDS) and one fine-delay stage (FDS) as shown in Fig. 2 (a). The minimum delay of each delay stage should be shorter than 1/4 of clock period to provide 90° phase-shift signal within the same clock cycle. Each CDS has 16 coarse-delay cells (CDCs), consisting of one buffer and one multiplexer, and the coarse-tuning control code (C[15:0]) determines the propagation paths from CDCs. The intrinsic delay of CDS is only the gate delay of one multiplexer as shown in Fig. 2 (b). In order to achieve better delay resolution, a tri-state holder cell and 16 tri-state inverters are added as shown in Fig. 2 (c). When the tri-state holder cell is enabled (F[0] is high), output signal of the enabled tri-state inverter has the hysteresis phenomenon in the transition state to produce different delay times. Furthermore, the gate capacitance of a tri-state inverter can be change slightly by the fine-tuning control code (F[16:1]) to obtain high delay resolution in FDS. Because a tri-state holder cell can provide larger delay than a tri-state inverter, it can replace many tri-state inverters to reduce power consumption and the intrinsic delay. The simulation results show that the minimum delay resolution of one FDS is 4 ps; hence the total delay resolution of DCDL is 16 ps.

3.2 Time-to-digital converter

Fig. 2 (d) illustrates the architecture of the proposed TDC. The dummy intrinsic delay chain is the same as the minimum delay path of DCDL. PULSE_START and PULSE_END rises at the first and second rising edge of input clock respectively. PULSE_START will pass through the dummy intrinsic delay chain in the front of the CDC chain to generate PULSE_START_D with the intrinsic delay of DCDL, and then the delay between PULSE_START_D and PULSE_END will be quantized by 4 CDCs and converted to TDC control code (TDC_CODE) as shown in Fig. 2 (e). As a result, the intrinsic delay effect can be removed to improve the precision of quantization and conversion.

4 Implementation and performance comparisons

The proposed design is implemented by 0.13 μm CMOS standard process, and area of ADDLL and DCPS is 0.026 mm^2 and 0.01 mm^2 respectively. For DDR2 400/800 applications, the operation range of the proposed ADDLL is from 200 MHz to 400 MHz, and the simulation results show that the total power consumption is 5.5 mW at 400 MHz with 1.2 V supply and peak-to-peak period jitter is 20 ps at 400 MHz. Fig. 2 (f) shows the locking procedure of ADDLL after system is reset. The entire phase locking procedure takes 13 clock cycles. The phase difference between CLOCK1 (P360) and CLOCK2 (P90) is 634 ps at 400 MHz, hence the phase-shift error is 1.3° (compared with 90°) as shown in Fig. 3 (g). Table I lists comparison results with the state-of-the-art DLLs for clock generation in DDR controller applications. The proposed ADDLL has the shortest locking time, the smallest phase-shift error, and the lowest power consumption compared with other DLL designs.

DOI: 10.1587/elex.7.634
Received March 12, 2010
Accepted April 12, 2010
Published May 10, 2010

Table I. Performance Comparisons

Performance Indices	Proposed	VLSI-DAT'06 [5]	CICC'07 [3]	E.LETTERS'08 [4]
Process	0.13µm CMOS	0.13µm CMOS	0.13 m CMOS	0.18 m CMOS
Supply Voltage (V)	1.2	1.2	1.2	1.8
Lock Time (clock cycles)	13	NA	40	< 80
Operation Range (MHz)	200 ∼ 400	100 ∼ 200	333.5 ∼ 800	510 ∼ 1100
Phase Error (degrees)	1.3	5.47 (7.6%)	2	NA
Power Consumption (mW)	5.5 @400MHz	9 @200MHz	19.2 @800MHz	12 @800MHz
Phase Shift within Single Cycle	Yes	No	Yes	Yes
Portability	Yes	Yes	No	No

Furthermore, the proposed ADDLL not only has good portability, but also provides the 90° phase-shift clock within the same clock cycle.

5 Conclusion

A fast-lock portable ADDLL and a tunable DCPS for the timing block of DDR interface solution is presented. The proposed ADDLL that employs the high-performance DCDL and TDC can achieve fast phase lock and keep small phase-shift error compared with other ADDLLs. The proposed DCPS provides an all-digital and suitable phase shifting to eliminate the non-ideal effect of data transmission between multi-chip interconnections especially for high data rate interconnection applications.

DOI: 10.1587/elex.7.634
Received March 12, 2010
Accepted April 12, 2010
Published May 10, 2010