Monotonic and low-power digitally controlled oscillator with portability for SoC applications

D. Sheng, C.-C. Chung, J.-C. Lan and H.-F. Lai

A monotonic and low-power digitally controlled oscillator (DCO) with a cell-based design for system-on-chip applications is presented. The proposed monotonic DCO not only can achieve high delay resolution and wide operation range at the same time, but also maintain the delay monotonicity. Moreover, based on the proposed varactor-interpolator fine-tuning stage, the proposed DCO can provide monotonic delay with low power consumption and low circuit complexity as compared with conventional approaches. Simulation results of the DCO show that power consumption can be improved to 0.21 mW (at 840 MHz) with 2.95 ps resolution. In addition, the proposed design can be implemented with standard cells, making it easily portable to different processes and very suitable for SoC applications.

Introduction: The phase-locked loop (PLL) is a very important clocking circuit for many electronic systems such as digital communication and microprocessors. Traditional PLLs are designed by analogue approaches. However, it is hard to design an analogue PLL with lower supply voltage and advanced process technology, owing to serious leakage current problems and narrow working range. Also, as technology migrates, the analogue blocks in the PLL need to be re-designed. In contrast, the all-digital phase-locked loop (ADPLL) does not utilise any passive components and uses digital design approaches, making it easily integrated into digital and low-supply voltage systems [1, 2]. The digitally controlled oscillator (DCO) is the kernel module among the functional blocks of the ADPLL, because it dominates overall performance and power consumption [1–4]. To improve the control code resolution and simultaneously extend the operation range, the cascading structure DCO has been proposed [2]. However, this structure requires that the controllable range of each stage must be larger than the finest delay step of the previous stage to ensure that it does not have any dead zone larger than the LSB resolution of the DCO. Because of such a design constraint, the cascading structure DCO not only needs over-design, but also the non-monotonic problem will occur when the DCO code switches at the boundary of different tuning stages. The non-monotonic characteristic will increase jitter and induce the unlock phenomenon in the ADPLL. Also, the non-monotonic DCO is not suitable for frequency modulation applications such as the spread spectrum clock generator (SSCG) [3]. In this Letter, a monotonic, low-power, high-resolution and wide-range DCO with high portability is proposed for SoC applications. The proposed DCO not only uses a cascading structure to preserve the control code resolution and operation range, but also it employs the novel varactor-interpolator fine-tuning stage (VIFTS) to save power consumption and obtain a monotonic gain curve. In addition, all the design of the proposed DCO can be described by HDL language and implemented with standard cells, making it easily portable to different processes and very suitable for SoC applications.

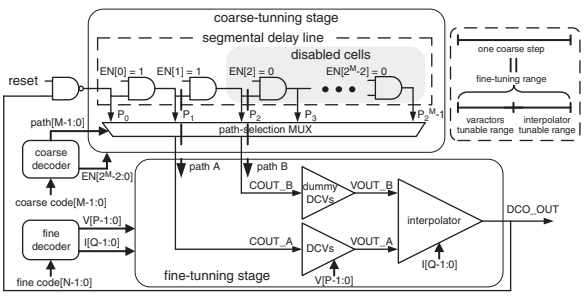

Fig. 1 *Architecture of proposed DCO*

Proposed DCO: Fig. 1 illustrates the proposed monotonic and low-power DCO which consists of a coarse-tuning stage (CTS) and a fine-tuning stage (FTS). The CTS is composed of $2^M - 1$ two-input AND gates that form a segmental delay line and a path-selection multiplexer. It can provide 2^M different delay values by selecting different delay paths (P0–P2$^M - 1$), and the path-selection multiplexer selects two delay paths from among these delay paths by the path selection signals (Path[M-1:0]). The delay difference between two selected delay paths is one delay step of the CTS. Also, as the operating frequency changes, some enabling input controlled signals (EN[$2^M - 2$:0]) are set to low level to disable those redundant two-input AND gates, leading to a saving in power consumption. Because the resolution of the CTS is not sufficient for typical DCO applications, an FTS is added to improve further the overall delay resolution of the DCO. The design challenge of the FTS is how to improve delay resolution while keeping a delay monotonic characteristic. Traditionally, the FTS employs an interpolation scheme to preserve the delay monotonicity. However, the interpolator has two major drawbacks. First, because the interpolator induces the short current when it operates, the power consumption will increase significantly as its complexity increases. Secondly, to achieve high delay resolution, it will take large hardware cost and consume high power.

The proposed VIFTS consists of digitally-controlled varactors (DCVs), dummy DCVs and an interpolator. The gate capacitance of a DCV can be changed slightly by the control code (V[P − 1:0]) to achieve high delay resolution [2]. The controllable delay range of both DCVs and the interpolator is half of one delay step of the CTS. If the required delay of the VIFTS is smaller than half of one delay step of the CTS, the delay of the VIFTS is obtained from the DCVs and the interpolator is not active. The interpolator control code (I[P − 1:0]) is set to a high level to pass the signal to the DCO output (DCO_OUT). Conversely, if the required delay of the VIFTS is larger than half of one delay step of the CTS, the delay of the VIFTS is combined by delay of all turned-on DCVs and delay of the interpolator. Under such conditions, the outputs of the DCVs and dummy DCVs (VOUT_A and VOUT_B) will interpolate through the interpolator, the delay of which can be changed by the control code. Because the tunable range of the VIFTS is equal to one delay step of the CTS, the delay monotonicity of the proposed cascading structure DCO can be maintained. Furthermore, the low-power and high-resolution DCVs reduce the circuit complexity of the interpolator, so the overall power consumption can be reduced. Based on the required frequency range and resolution for our application, the design parameters are determined as follows: $M = 4$, $N = 6$, $P = 20$ and $Q = 20$. The detailed circuit diagrams of the DCVs and interpolator are shown in Figs 2*a* and *b*, respectively.

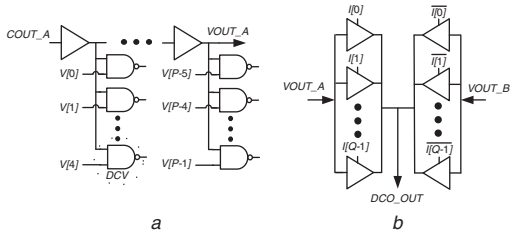

Fig. 2 *Circuit diagrams of DCVs and interpolator*

a DCVs
b Interpolator

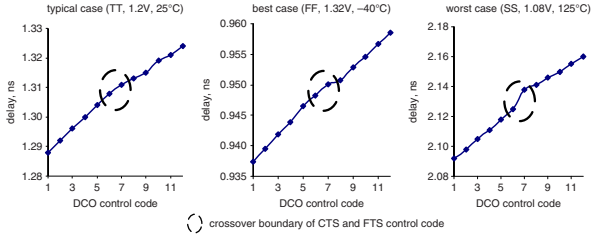

Fig. 3 *Simulation results under different PVT conditions*

Results: The proposed DCO has been implemented in the 90 nm 1P9M CMOS process, and HSPICE simulation results are shown in Fig. 3. The Figure shows that the proposed DCO keeps the monotonic gain curve when the control code switches cross over CTS and FTS under different process, voltage and temperature (PVT) conditions. Table 1 lists comparison results with state-of-the-art monotonic DCOs. Based on the power index comparison, it is clear that the proposed DCO can provide better power-to-frequency ratio, implying that it is more effective in power saving for a given operating frequency. Furthermore, the proposed low-power solution does not induce any performance loss. Additionally, since the proposed DCO can be implemented with

standard cells, it has a good portability. As a result the proposed DCO has the benefits of better resolution, monotonicity and portability.

Table 1: Performance comparisons

Performance indices	Proposed	[4]	[5]	[6]
Process	90 nmCMOS	65 m CMOS	0.18 μm CMOS	0.35 μm CMOS
Operation range (MHz)	324–840	47.8–538.7	300–1300	33–1040
Resolution (ps)	2.95	17.4	5.9	NA
Power consumption (mW)	0.21 at 840 MHz	0.205 at 481.6 MHz	4.5 at 950 MHz	7.85 at 1040 MHz**
Power index (mW/GHz)	0.25	0.43	4.74	7.55
Monotonicity	Yes	Yes*	Yes	Yes
Portability	Yes	Yes	No	No

* with extra calibration
** power consumption calculated from 50% of PLL [1]

Conclusions: A monotonic and low-power DCO with a cell-based design for SoC applications is presented. The proposed monotonic cascading structure not only can maintain the monotonic delay, but also can achieve high resolution and wide range at the same time. Based on the proposed VIFTS, the overall power consumption and circuit complexity of the DCO is lower than the conventional approaches. Moreover, because the proposed DCO has a good portability as a soft intellectual property (IP), it can reduce both design time and complexity. As a result, it is very suitable for SoC applications as well as system-level integration.

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D. Sheng, J.-C. Lan and H.-F. Lai (*Department of Electrical Engineering, Fu Jen Catholic University, No. 510, Zhongzheng Road, Xinzhuang District, New Taipei City 24205, Taiwan*)

E-mail: duosheng@mail.fju.edu.tw

C.-C. Chung (*Department of Computer Science and Information Engineering, National Chung Cheng University, 168 University Road, Minhsiung Township, Chiayi County, 621, Taiwan*)

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