A Body Channel Communication Transceiver with a 16x Oversampling CDR and Convolutional Codes

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***Abstract*—In this paper, a transceiver for human body channel (BCC) transmission is presented. BCC has the advantage of being less susceptible to interference from the external environment and consuming less power. First, the convolutional code encodes the data on the transmission side, and then the bit buffer and NRZI code are used to make the transmission more reliable, and the CRC32 code is inserted. On the receiver side, the proposed 16 times oversampling clock and data recovery (CDR) circuit recover the clock and data, and then the data are decoded by the Viterbi decoder. Finally, the correctness of the packet data is checked by the CRC32 code. The proposed BCC transceiver was implemented in TSMC 90nm CMOS process and can achieve a 5Mbps data rate with BER < 10^{-9} with energy/bit 0.34nJ/b (TX) and 0.4654nJ/b (RX).**

Index Terms—Body channel communication, clock, and data recovery, Transceiver, Convolutional encoder.

I. INTRODUCTION

In wearable devices, the acquisition or transmission of biosignals is made by sensors or implantable chips. Therefore, wearable devices are becoming more popular, and the network with wearable devices and sensors is called body area network (BAN). After the body data is collected, it must be sent to the cloud server on time. Generally, the use of wireless techniques is more common. BAN using wireless techniques is called a wireless body area network (WBAN). The range of WBAN is between one and two meters. In this range, WBAN can establish a connection between sensors or wearable devices. In addition, WBAN devices must be lightweight, consume low power, and have a small size.

There are two ways to implement WBAN: One uses air transmission, such as Bluetooth and ZigBee. However, these methods have some disadvantages. The data rate of these methods is low, and these methods can be easily interfered with by other users. The other way to realize BAN uses the human body as the transmission medium is called body channel communication (BCC). BCC has relatively high energy efficiency than other methods. The power consumption of BCC is less than 10 mW; in contrast, the power consumption of Bluetooth is nearly 100 mW.

The basic idea of BCC is that two electrodes are attached to the human body. The signal is modulated and transmitted from the transmitting electrode (TX) to the receiving electrode (RX) via the human body. Then the RX restores the data of the original signal. Once the signal leaves the human body, the signal is quickly attenuated so that it can prevent eavesdropping. The BCC characteristics are studied in [1]. When the signal frequency is below 4 MHz, the impedance of the human body can be neglected because it is much lower than the impedance of the capacitive return path. Therefore, the transmission distance does not have much effect on the channel gain. However, at frequencies above 10 MHz, the air coupling capacitance between TX and RX decreases with increasing frequency, resulting in less signal loss. Then, the signal loss depends on the transmission distance [2].

Common BCC transmission methods with capacitive coupling such as orthogonal frequency division multiplexing (OFDM), frequency-shift keying (FSK), frequency selective digital transmission (FSDT), and wideband signaling (WBS) are explained below. The OFDM-based BCC architecture can transmit at a high data rate. However, the chip size and power consumption are quite large due to the inverse Fourier transform and Viterbi decoder [3]. The FSK-based BCC architecture transmits digital signals by changing the discrete frequency of the carrier signals and using the two frequencies to represent one or zero. However, this modulation requires a specific frequency band that can be easily interfered with by other devices using the same frequency band [4].

In an FSDT-based BCC architecture, the data are distributed over some frequencies, which are used for data transmission. With Walsh codes, the FSDT transceiver can achieve a high data rate. However, this requires a high signal-to-noise ratio (SNR), which is challenging to realize in practice [5]. The WBS BCC architecture has low complexity, low power consumption, does not require complex modulation, and requires a small chip area [6, 7]. However, due to the human body antenna effects, many devices in the environment, such as cordless phones and FM

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radios, can cause tremendous data jitter. Therefore, a clock and data recovery (CDR) circuit that has good jitter tolerance is needed.

In this paper, a WBS BCC transceiver with a 16x oversampling CDR is presented. The proposed transceiver is implemented in a TSMC 90nm CMOS process, and the energy/bit is 0.34nJ/b (TX) and 0.4654nJ/b (RX) at 5Mbps. Moreover, the bit error rate (BER) is less than 10^{-9}. Section II describes the architecture of the proposed BCC TX, and Section III explains the design of the BCC RX. Then Section IV shows the experimental results. Finally, a conclusion is given in Section V.

II. Proposed TX Architecture

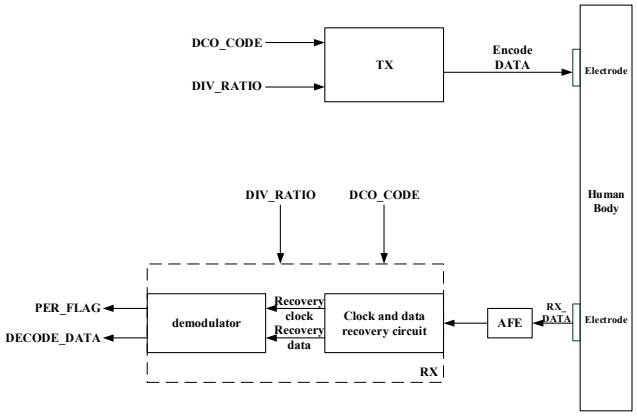

Fig. 1. The overall architecture of the proposed BCC transceiver.

Figure 1 shows the overall architecture of the proposed BCC transceiver. First, the DCO_CODE and the DIV_RATIO of TX and RX are set to the same value. Next, the TX_Modulator generates the data to be transmitted, and the data are encoded by the convolutional encoder and the NRZI encoder, then the data are transmitted through the human body. Then RX_DATA is amplified by the analog frontend (AFE) circuits. Next, the oversampling clock samples the amplified signal, and the CDR circuit recovers the data. Next, the RX_Modulator decodes the recovered data and verifies the correctness of the transmission using the CRC32 code. Finally, the packet error rate is calculated to show the BER performance.

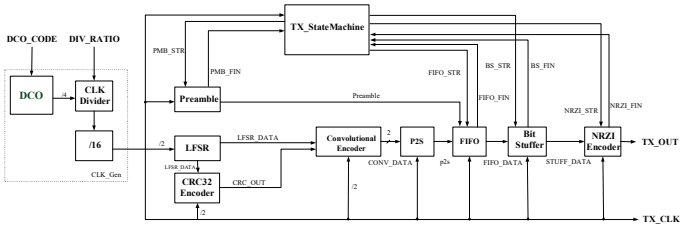

Fig. 2. The block diagram of the proposed BCC transmitter.

Figure 2 shows the block diagram of the proposed BCC transmitter. First, a pattern generator with a linear feedback shift register (LFSR) generates random data to test the BCC. Then, the CRC32 encoder generates the corresponding CRC32 check code. The convolutional encoder encodes the random data and CRC32 check code, and the encoded data is 2-bit symbols, so the parallel-to-serial module is used to serialize the encoded data. Then, the first-in-first-out (FIFO) block arranges the preamble bits, the start-fame delimiter (SFD), the convolutionally encoded data, and the guard bits into the packet format. The random data may have the longest 19 consecutive identical bits (CIDs). Therefore, the bit stuffer inserts 0 to increase data transitions and avoid burst errors. For the proposed BCC transceiver, the value of the CID can be 2, 3, or 4. Then the data packets are sent with non-return to zero inverted (NRZI) modulation. If the input for the NRZI encoder is 0, the output is inverted. Conversely, if the input is 1, the NRZI encoder retains the output state.

A packet consists of 20 preamble bits for synchronization, 8 start frame delimiter (SFD) bits to detect the start of the packet, 2,000 data bits, 32 bits of CRC32 check code, and the guard bits. The data are encoded with the convolutional code, which has a code rate of 1/2 so that 1,000 bits of data with one packet. The guard bits are intended for the Viterbi decoder, and the length of the guard bits depends on the constraint length of the convolutional code. The convolutional coded format can be expressed as (m, n, k), where m is the number of outputs, n is the number of inputs, and k is the constraint length. The longer the constraint length is, the better the BER performance is, and the constraint length is proportional to the circuit complexity. In this paper, the coded format is (2, 1, 7).

III. Proposed RX Architecture

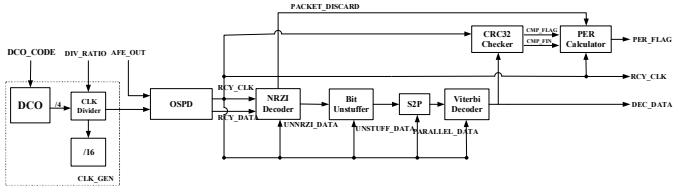

Fig. 3. The block diagram of the proposed BCC receiver.

Figure 3 shows the block diagram of the proposed BCC receiver. It consists of a DCO, clock dividers, an oversampling phase detector (OPSD), the NRZI decoder, a bit unstuffer, a serial-parallel module (s2p), a Viterbi decoder, a CRC32 checker, and a PER calculator. The clock generated by the DCO is used to oversample the AFE_OUT, which contains the received data preamplified by the AFE circuit. The OPSD module recovers the data and the clock, and then the system uses RCY_CLK as the clock for the other modules. The NRZI decoder decodes RCY_DATA and also detects the SFD of the packet. If the SFD cannot be detected, this packet is discarded. After the NRZI decoder, the bit unstuffer removes the data inserted on the transmit side and then converts the serial data to 2-bit parallel data since the Viterbi decoder requires 2-bit data for input. Finally, the DEC_DATA is sent to the CRC32 checker to check whether the data are correct or not. The result is sent to the

PER calculator, and the PER calculator outputs the PER_FLAG to present the performance of the BCC transceiver.

The block diagram of OPSD is shown in Figure 4. The DCO_CLK is divided by the divider, and the DIVIDED_CLK is used to oversample the AFE_OUT. The DIVIDED_CLK generates sixteen phases, and the OPSD_STATEMACHINE restores the clock and data.

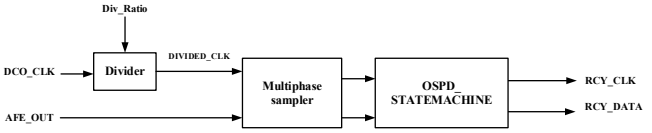

Fig. 4. The block diagram of the OPSD.

First, the situation without data jitter and frequency drift is considered, as shown in Figure 5. The AFE_OUT is oversampled by sixteen phases (PHASE0 to PHASE15). If the data sampled by the adjacent phases are different, there is a data transition. The ideal data transition occurs when the counter value is 15. However, there are interferences and frequency drift in body channel communication between TX and RX so that the AFE_OUT may have data jitter and frequency drift. Figure 6 shows the situation with data jitter and frequency drift. When a data transition occurs, the TRANSITION_EDGE is set to "1" for one FCLK period, and the counter is set to zero. When the counter value becomes 5, the first RCY_CLK is triggered, and the counter is reset to zero. If the counter continues counting to 17 and no data transition is detected, RCY_CLK is triggered at this time, and the counter is reset to zero. Typically RCY_CLK is triggered when the counter is at 5. The reason for the values 5 and 17 is that the rising edge of RCY_CLK is in the middle of 16 phases when the data transition is detected and the counter is at 5, and the reason for counting up to 17 is that there are 16 phases in a symbol.

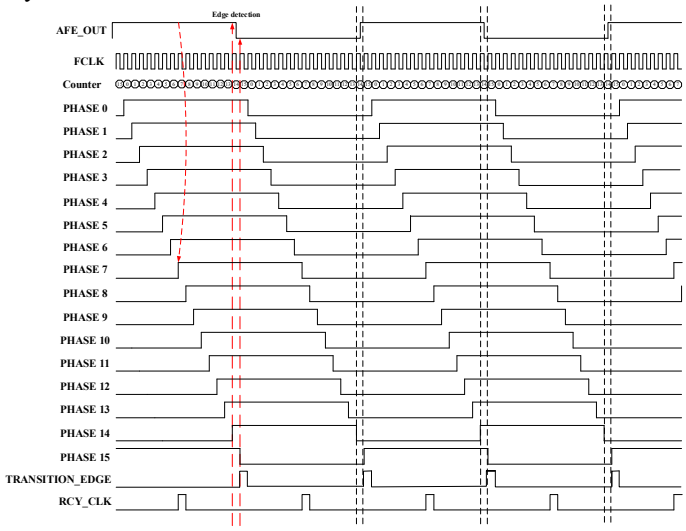

Fig. 5. The situation without data jitter and frequency drift.

The demodulator shown in Figure 3 consists of the NRZI decoder and the bit unstuffer. The NRZI decoder continues to decode the incoming RCY_DATA and also detects whether the data contains the SFD or not. If the SFD is not included in the data, the PACKET_DISCARD signal is set to 1. Thereupon UNNRZI_DATA becomes zero, and the packet is discarded. If an SFD is detected, the bit unstuffer removes the zero inserted by the bit stuffer on the TX side. Finally, the UNSTUFF_DATA are sent to the S2P module and then to the Viterbi decoder.

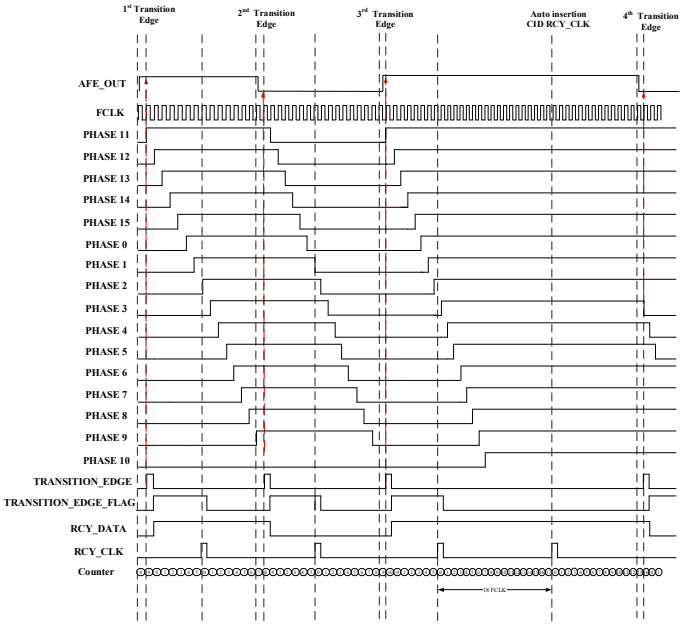

Fig. 6. The situation with data jitter and frequency drift.

The Viterbi algorithm is used in this work to decode the convolutional codes transmitted by the transmitter. First, the Viterbi algorithm can find the most likely sequence in the retrieved data called the Viterbi path. Then, it traces back the path, finds out the decoded data, and corrects the erroneous data.

IV. Experimental Results

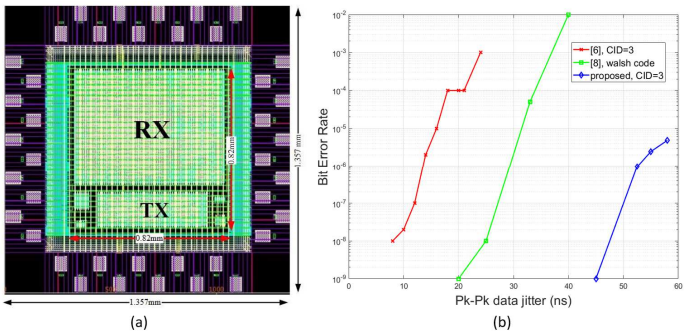

Fig. 7. (a) The layout of the BCC transceiver and (b) BER performance.

The layout of the BCC transceiver chip is shown in Figure 7(a). The test chip is implemented in TSMC 90nm CMOS process with a 1.0 V power supply. The chip size including I/O pads is 1357 μm × 1357 μm, and the core size is 820 μm × 820 μm. The operating range of this BCC transceiver is between 1Mbps and 5Mbps. The power consumption without the AFE

TABLE I
COMPARISON TABLE

	[9] TBioCAS'19	[10] EMBC'17	[11] IEEE Sensor's 15	[8] ICCETW'18	[3] JSSC'17	This work
Process	N/A	Texas Instruments TM4C123G	180nm CMOS	FPGA	65nm CMOS	90nm CMOS
Supply voltage	3.7V	3.3V	1.2V	1.0V	1.1V	1.0V
Communication method	OOK	N/A	FSDT	Wideband signal	8-P OFDM BPSK	Wideband signal
Sensitivity	N/A	N/A	-65dBm	-18.87dBm	-78dBm	-18.87dBm
Max data rate	15kbps	500kbps	2.625Mbps	3.9Mbps	1Mbps	5Mbps
Max transmission length	120cm	30cm	120cm	140cm	N/A	140cm
Power consumption	7.95nW	4.8mW @9.8kbps	1.74mW	13.5 W 13.7W 0.441 W	1.4mW	2.327mW (RX) 1.7mW (TX) @5Mbps
Area	N/A	N/A	1.05 mm^2	N/A	2.13 mm^2	1.842 mm^2
BER	N/A	$< 10^{-7}$	$< 10^{-2}$ (PER)	$< 10^{-5}$	$< 10^{-7}$	$< 10^{-9}$
Energy/bit	0.53nJ/b	500nJ/b @9.8kbps	0.66nJ/b	7.08μJ/b	1.4nJ/b	0.4654nJ/b (RX) 0.34nJ/b (TX) @5Mbps

circuit is 2.327mW (RX) and 1.7mW (TX), respectively.

Figure 7(b) shows the BER performance of the proposed BCC. The bit error rate under different data jitter is simulated. In [6], a referenceless CDR architecture is used in the receiver of the BCC. In [8], the Walsh code is used. The data rate of the proposed design is 5 Mbps, and the CID is set to 3. Due to the convolutional code, the jitter tolerance performance of the proposed BCC transceiver is better than the other two designs.

Table I shows the comparison table with other BCC designs. The proposed BCC transceiver has a relatively high data rate than these works [9,10]. In [3,11], the relatively low sensitivity is achieved, but the data rate is lower than the proposed design. The BER performance of the proposed design is also better than these works [3, 8, 10].

V. CONCLUSION

In this paper, a BCC transceiver with a 16x oversampling CDR and the convolutional code is presented. The proposed design can provide a maximum data rate of 5Mbps with excellent data jitter tolerance.

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