A Reference-Less All-Digital Transceiver for Human Body Channel Communication

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***Abstract*— In this paper, a reference-less all-digital wideband signaling (WBS) transceiver for body chancel communication (BCC) is presented. In the transmitter part, data are encoded in NRZI format, and the bit stuffer is used to increase the data transitions. In the receiver part, the received signals are amplified and restored to digital waveforms with analog frontend circuits. Then, the proposed reference-less all-digital clock and data recovery circuit (ADCDR) can recover the data. The proposed ADCDR can quickly compensate for the phase error. Thus, the proposed ADCDR can tolerate large data jitter and can still correctly recover the data. The automatically tracking gain calibration method is proposed to calculate the suitable gain value for the proposed ADCDR under process, voltage, and temperature (PVT) variations. The proposed all-digital WBS transceiver was implemented in TSMC 90nm CMOS process with standard cells. The data rate of the proposed transceiver ranges from 1 Mb/s to 20 Mb/s, and the power consumption is 5.5 mW at 20 Mb/s. In addition, the bit error rate is $< 10^{-8}$ at 20 Mb/s and the energy per bit is 0.275 nJ/b.**

I. INTRODUCTION

Nowadays, the wearable personal entertainments and personal healthcare devices become more and more popular. Body area network (BAN) is a type of communication for wearable devices. The BAN is organized by IEEE 802.15 Task Group 6 (TG6) to standardize the industrial scientific medical (ISM) bands and the protocols of multimedia communication around the human body [1]. Traditionally, the medical healthcare devices such as electromyography (EMG) and electrocardiography (ECG) require wireline connections to transfer the physiological signals, it is not convenient for the patients which require long-term monitoring. Therefore, wireless communication techniques, such as Bluetooth and human body channel communication (BCC) are preferred to gather the physiological signals.

BCC uses the human body as the transmission medium, and it has a relatively high data rate and low power consumption than Bluetooth. Before using the human body as the transmission medium, it is necessary to know the characteristics of the human body. Many researches had analyzed the characteristics of human body channel, such as [2, 3]. It shows that the attenuation of the human body channel is strongly affected by the transmission distance and frequency. The jitter effects are also changed according to different frequencies and distances [4]. The prior BCC transceivers are implemented in different architectures. In [5], a reference-less double frequency-shift keying (FSK) modulation scheme is adopted. An 80 MHz reference source is sent from the base station to the sensor node to calibrate the frequency of the on-chip oscillator of the sensor node periodically. The proposed architecture eliminates the external crystal oscillator and the energy consumption and system cost are greatly reduced [5]. In [5], the proposed transceiver can support a data rate up to 10 Mb/s. A full-duplex 80 Mb/s BCC transceiver using the coherent binary phase-shift keying (BPSK) modulation is presented in [6]. The proposed transceiver uses two channels of 40MHz, one centered at 40MHz (L-band) and the other at 160MHz (H-band) to realize a high data rate. However, the active filters required in the dual band receiver occupied a large chip area.

A 40 Mb/s wideband signaling (WBS) BCC transceiver is presented in [7]. The data are encoded in non-return-to-zero-inverted (NRZI) format and transmitted directly to the human body. In the receiver part, the oversampling all-digital clock and data (ADCDR) circuit recovers the data to the original data. However, the proposed ADCDR circuit requires a high-speed sampling clock (280 MHz), so it requires an external oscillator and a frequency synthesizer to generate the sampling clock. However, the frequency synthesizer and the external oscillator will increase the power consumption and the cost of the BCC transceiver.

In this paper, a reference-less all-digital WBS BCC transceiver is presented. In the ADCDR, the proposed phase compensation approach can enhance the frequency and phase tracking ability and reduce the bit error rate (BER). Moreover, the proposed automatically phase track gain calibration method can calculate the suitable gain value for the proposed ADCDR under process, voltage, and temperature (PVT) variations. The rest of this paper is organized as follows. The architecture of the proposed WBS transceiver is presented in Section II. Section III describes the method of the gain calculation. Section IV shows the experimental results. Finally, the conclusion is given in Section V.

II. THE PROPOSED ARCHITECTURE

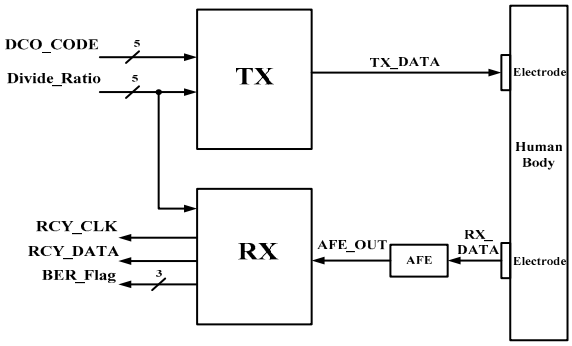

FIGURE 1. THE PROPOSED WBS TRANSCEIVER.

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The architecture of the proposed WBS transceiver is shown in Fig. 1. The transceiver consists of a transmitter (TX), a receiver (RX), and an analog frontend (AFE) circuit. The linear-feedback shifter register (LFSR) of the TX generates random data to test the proposed transceiver. After system is reset, the TX sends data to the human body through a single electrode. In the receiver part, the received signal (RX_DATA) from the electrode is amplified and restored to the digital waveform by the AFE circuit. After that, the RX starts to recover the clock (RCY_CLK) and data (RCY_DATA). The 3-bit signal BER_FLAG shows the number of bits received before the first bit error occurred. For example, 3'b111 means 10^8 bits are received, and 3'b110 means 10^7 bits are received, and so on.

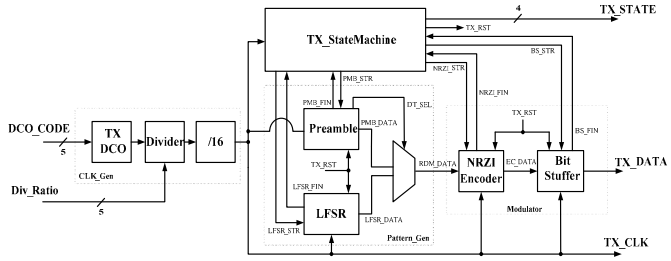

FIGURE 2. THE ARCHITECTURE OF THE TRANSMITTER.

Fig. 2 shows the detail architecture of the TX. It consists of a clock generator (CLK_Gen), a pattern generator (Pattern_Gen), a modulator, and a TX state machine. The input digitally controlled oscillator (DCO) control code (DCO_CODE) and the frequency divider ratio (Div_Ratio) can set the transmission data rate of the TX. The pattern generator (Pattern_Gen) generates transmission packets to the modulator. In the modulator, the data are encoded in non-return-to-zero-inverted (NRZI) format and transmitted directly to the human body. The bit stuffer of the modulator performs bit stuffing to limit the maximum continuous identical digits (CID). The TX state machine controls the operation of the transmitter. Fig. 3 shows the packet format. First eighty bits are preamble pattern for synchronization and followed by a 4-bit start frame delimiter (SFD). Consequently, 1000 bits data are sent.

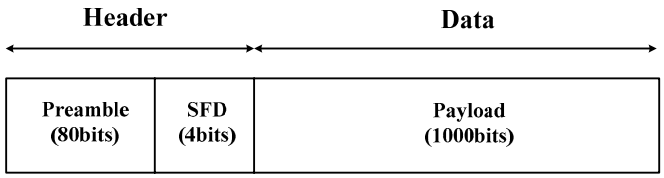

FIGURE 3. PACKET FORMAT OF THE PROPOSED TRANSCEIVER.

Fig. 4 shows the architecture of the proposed receiver. It consists of an ADCDR circuit, a GAIN calculator, a RX state machine, a demodulator, and a LFSR checker. When the RX receives preamble pattern, the GAIN calculator calculates the suitable gain for the ADCDR circuit to compensate for PVT variations. Subsequently, the ADCDR starts to track the frequency and phase of the received data using the preamble patterns. After the SFD pattern is received. The proposed ADCDR circuit starts to recover the clock and data. After bit un-stuffing, the received data are decoded by the NRZI decoder and it outputs the original data (RCY_DATA). The LFSR checker can generate the same random pattern bits which generated by the LFSR of the TX. Thus, the LFSR checker of the RX can check the bit errors in the received data. The RX state machine controls the operation of the RX when a packet is received.

Fig. 5 shows the block diagram of the proposed ADCDR circuit. It consists of a dual mode phase and frequency detector (PFD) [8], a digitally controlled oscillator (RX_DCO), a digital loop filter, a programmable frequency divider, a divided-by-16 frequency divider, and an ADCDR controller. The output of the AFE circuit (AFE_OUT) is delayed and exclusive-OR to generate the data transition signal (Data_T). The PFD compares the phase and frequency error between the signal Data_T and the recovery clock (RCY_CLK) and generates the up and down signals (RUP or RDN) to the ADCDR controller. The ADCDR controls the DCO control code of the RX_DCO to compensate for the frequency error and phase error between the signal Data_T and RCY_CLK. The digital loop filter generates the baseline DCO control code to stabilize the output of the RX_DCO. During the preamble pattern, the proposed ADCDR circuit operates as a phase-locked loop. After the frequency and phase acquisition is complete, the signal Track_Mode is set to "0", and the PFD can perform phase error detection with the random input data.

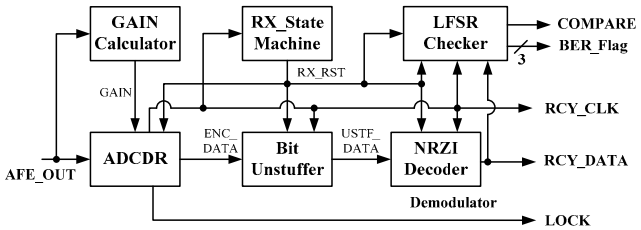

FIGURE 4. THE ARCHITECTURE OF THE RECEIVER.

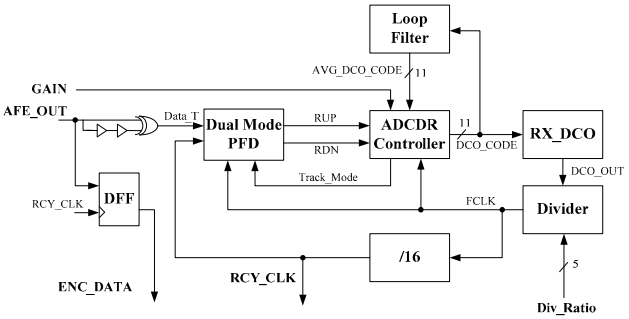

FIGURE 5. BLOCK DIAGRAM OF THE PROPOSED ADCDR.

When the ADCDR circuit is locked, the frequency of the FCLK will be 16 times the frequency of the input data. Thus, FCLK is used to quantize the phase error between the Data_T and RCY_CLK. According to the pulse width of the RUP or RDN, the ADCDR controller can quickly compensate for the large phase error due to the random data jitter. Therefore, the proposed ADCDR circuit can have a large jitter tolerance. After ADCDR circuit is locked, the output of the AFE circuit (AFE_OUT) will be sampled by the negative edge of the RCY_CLK to generate the recovery data (ENC_DATA).

III. TRACKING GAIN CALCULATION

In the proposed ADCDR, the phase error can be quantized using the FCLK, as shown in Fig. 5. Since the DCO resolution varies with PVT variations, we need a method to map the quantization phase error into the amount of the DCO control code adjustment. During the preamble pattern, in the beginning, the DCO control code of the RX_DCO is set to the medium value of the DCO control code (i.e. 1023). Thus the DCO

operates at the median frequency with the median period, denoted as P_{mid}. Then, the period ratio (R_{mid}) between the symbol period of the received data (P_{ref}) and the period of the DCO can be calculated by a cyclic counter triggered by the DCO_OUT. After that, the DCO control code of the RX_DCO is set to the maximum value of the DCO control code (i.e. 2047), and the DCO operates at the maximum frequency with the minimum period, denoted as P_{min}. Similarly, the period ratio (R_{max}) can be calculated by a cyclic counter. The definitions of the R_{mid} and R_{max} are shown in Eqs. 1 and 2.

$$R_{mid} = \frac{P_{ref}}{P_{mid}} \quad (1)$$

$$R_{max} = \frac{P_{ref}}{P_{min}} \quad (2)$$

If the period of the DCO can be expressed as a linear equation with P_{min} and DCO resolution, it can be derived that the ratio between P_{ref} and the DCO resolution can be expressed in terms of R_{mid} and R_{max}. Subsequently, if the pulse width of RUP or RDN is K FCLK cycles, the amount of addition or subtraction to the DCO control code (GAIN) can be expressed in terms of the phase error value (K), the divide ratio of the frequency divider (N), R_{mid} and R_{max}, as shown in Eq. 3. The period ratios (R_{mid}, R_{max}) will be calculated using the preamble pattern in every packet, and thus, the PVT variations to the DCO resolution can be compensated, and the quantization phase error information can increase the phase tracking ability of the proposed ADCDR. Then, the ADCDR controller can quickly compensate for the large phase error due to the random data jitter. After the tracking gain calculation, the ADCDR controller will add or subtract GAIN value to the DCO control code according to the pulse width RUP and RDN.

$$GAIN = \frac{K}{8\times16\times16\times N} \times \frac{R_{mid} \times R_{max}}{(R_{max} - R_{mid})} \times 1024 \quad (3)$$

IV. Experimental Results

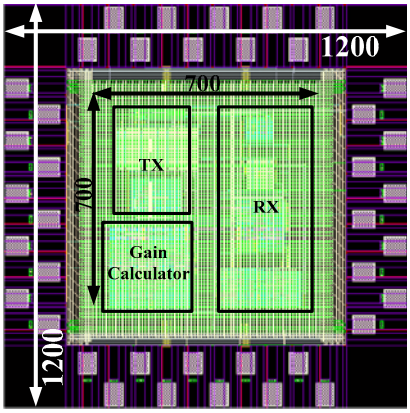

FIGURE 6. LAYOUT OF THE TEST CHIP.

Fig. 6 shows the layout of the test chip. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0V power supply. The core size of the test chip is 700× 700 μm^2. The chip size including I/O PADs is 1200× 1200 μm^2. Fig. 7 shows the error-free simulation results at 20 Mb/s, the x-axis is peak-to-peak (P_K-P_K) data jitter and y-axis is the number of received bits before the first bit error occurred. The proposed ADCDR has a BER < 10^{-5} with 13ns P_K-P_K data jitter when the maximum number of the CID is 5. If the maximum CID is reduced to 3, the BER performance can be improved to < 10^{-8}. When there has more data transitions, the phase acquisition of the ADCDR becomes more easily. Thus, in the proposed ADCDR, the maximum CID is set to 3.

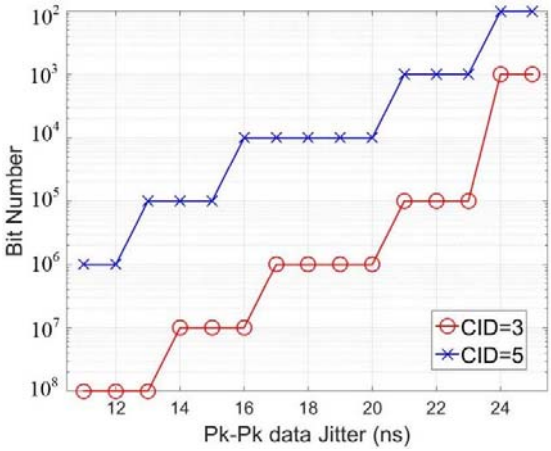

FIGURE 7. ERROR-FREE SIMULATION RESULT AT 20Mb/s.

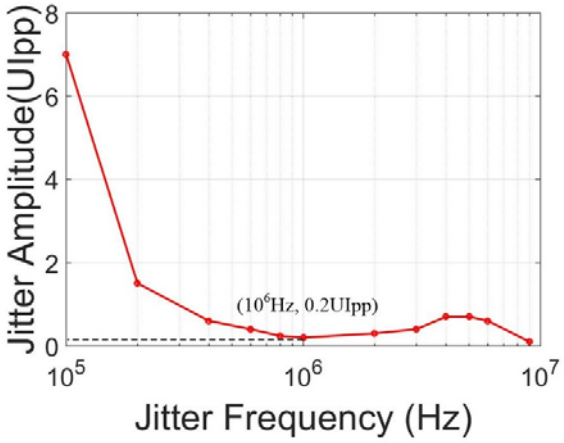

FIGURE 8. SINUSOIDAL JITTER TOLERANCE PERFORMANCE AT 20Mb/s.

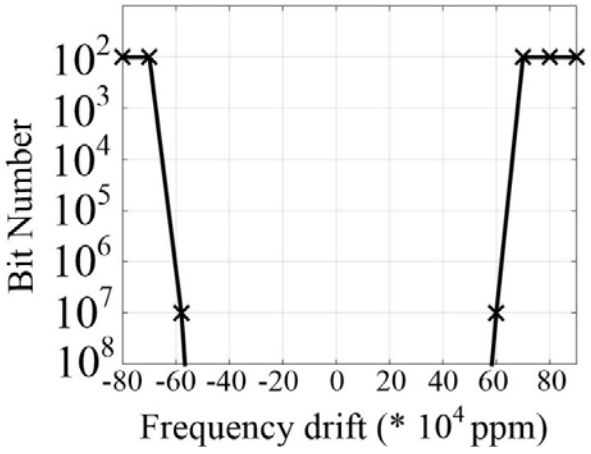

FIGURE 9. FREQUENCY DRIFT TOLERANCE PERFORMANCE AT 20Mb/s.

TABLE I
PERFORMANCE COMPARISONS

	[9] JSSC'07	[10] JSSC'09	[5] JSSC'12	[11] ISSCC'14	[12] VLSI-DAT'15	[6] JSSC'16	Proposed
Process	0.25 μm	0.18 μm	0.18 μm	65 nm	90 nm	65 nm	90 nm
Data Rate	2 Mb/s	60 kb/s ~ 10 Mb/s	1 kb/s ~ 10 Mb/s	60 Mb/s	29.1Mb/s	80 Mb/s	1 Mb/s ~ 20 Mb/s
Modulation	Wideband Signaling	Adaptive Frequency Hopping FSK	Double FSK	3-level Walsh Coding	16-QAM OFDM	Binary Phase Shift Keying	Wideband Signaling
Supply	1 V	1 V	1 V	1.1 V	0.53 V	1.2 V	1 V
Sensitivity	-36 dBm	-65 dBm	-66 dBm	-58 dBm	N/A	-58 dBm	-18.87dBm
Power Consumption	0.2 mW	3.7 mW	4.4 mW	10.87 mW	9.37mW	6.3 mW	5.5 mW (w/o AFE circuit)
Area	0.85 mm^2	2.30 mm^2	4.5 mm^2	0.85 mm^2	5.2 mm^2	5.76 mm^2	0.49 mm^2
BER	$1.1*10^{-7}$	10^{-5} (10Mb/s) $<10^{-9}$ (60kb/s)	10^{-5}(10Mb/s) 10^{-12}(10kb/s)	$<10^{-5}$ @ 60Mb/s	$<10^{-4}$	$<10^{-5}$ @ 40Mb/s	$<10^{-8}$ @20Mb/s
Energy/bit	2.5 nJ/b	0.37 nJ/b	0.44 nJ/b	0.18nJ/b	0.32 nJ/b	0.079 nJ/b	0.275nJ/b

Fig. 8 shows the sinusoidal jitter tolerance of the proposed ADCDR circuit at 20 Mb/s. Fig. 9 shows the error-free simulation results with different frequency drift at 20Mbps. The BER performance of the proposed ADCDR is $< 10^{-7}$ within the frequency drift range from -6×10^5 ppm to $+6\times10^5$ ppm at 20Mbps. The relatively large frequency drift tolerance of the proposed ADCDR as compared with an oversampling-based ADCDR [7] is due to the frequency acquisition process of the reference-less ADCDR architecture. Table I. shows the comparison table with other BCC designs. The proposed design has small chip area. Although [11] and [6] can achieve a high data rate, the BER performance becomes worse at high speed modes. Moreover, the proposed transceiver also has smaller chip area and lower energy-per-bit than [5,9,10].

V. CONCLUSION

In this paper, a reference-less all-digital WBS transceiver is proposed for human body channel communication. In transmitter part, the data are modulated by the NRZI encoder and the bit stuffer to increase the data transitions. In the receiver part, the proposed ADCDR circuit can quickly compensate for the phase error caused by random data jitter. Moreover, an automatically phase track gain calibration method is proposed to solve the DCO resolution variations with PVT variations. As a result, the proposed ADCDR has large jitter and frequency drift tolerance and is suitable for BCC applications.

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