Time-Domain Characteristics of Body Channel Communication (BCC) and BCC Transceiver Design

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***Abstract* – In this paper, time-domain characteristics of human body channel communication (BCC) are measured with an analog frontend (AFE) printed circuit board (PCB) at different transmission distances and signal frequencies. In addition, a 1 Mb/s to 40 Mb/s wideband signaling (WBS) BCC transceiver which uses the human body skin as a transmission medium is presented. As compared to wireless transmission methods, BCC is more stable and has less power attenuation. Furthermore, it is almost insensitive to the motion of the human body. However, the body antenna effects cause interferences in human body channel communication. In the proposed transceiver, at the transmitter part, the NRZI-encoded data are sent directly to the human body channel. At the receiver part, after an AFE PCB amplified the received signals, the proposed 7X oversampling clock and data recovery (CDR) circuit recovers the data with random jitter and frequency drift tolerance. The proposed WBS BCC transceiver is implemented in a standard performance 90nm CMOS process, and the core area is 0.144 mm^2. The power consumption of the WBS BCC transceiver is 1.21mW at 40Mb/s, and the bit energy is 0.03 nJ/b.**

I. Introduction

In recent years, personal healthcare devices are grown up rapidly due to the aging of population. Traditionally, electronic medical devices such as electrocardiography (ECG), electromyography (EMG), thermometers, and sphygmomanometers require wire line connection, which is inconvenient to the patients. Therefore, IEEE 802.15 Task Group 6 established a body area network (BAN) standard [1] around the human body which defines the industrial scientific medial (ISM) bands and data transportation protocols. Body area network can provide connections between wearable devices and body sensors around the human body within two meters. In addition, BAN devices should be satisfied with low weight, small size, and low power consumption.

Wireless data communications for BAN based on radio frequency (RF) have been successfully developed using protocols such as Bluetooth, and ZigBee which adopting 2.4GHz ISM band for transmission. However, RF transmission suffers from interferences (e.g. Wi-Fi) in the 2.4 GHz bands. Moreover, current wireless approaches have a relatively low data rate (e.g. 1 Mb/s in Bluetooth 4.0) and relatively high power consumption (>10nJ/b). Another problem is the multipath propagation. The RF transmission is also susceptible to the interferences in nearby environment because of the body shadowing effect [4]. Consequently, body channel communication was first proposed in [5]. Human body channel communication (BCC) uses the human body skin as a transmission medium.

The human body channel communication consists of a transmitter, human body channel, and a receiver. The BCC transmitter sends signals through a human body channel. The BCC receiver amplifies the received signals and recovers the data. As compared to wireless transmission methods, BCC has lower path loss and is without the body shadowing effect of RF communication. Furthermore, BCC is almost insensitive to the motion of the human body according to [6].

In order to transmit data via human body channel, prior researches had studied for the characteristics of human body channel. In [7], it shows that the human body channel is strongly affected by transmission distance and types of transmission signals. Body antenna effects cause severely interferences in body channel communication, as discussed in [3],[8]-[10]. An electro-magnetic field is formed around human body when the signal is transmitted through human body [11]. When many people use the BCC simultaneously, each field is formed around the human bodies so as to interfere the nearby BCC users. From above discussions, for one wants to design a BCC transceiver should measure the human body channel characteristics firstly, then design a BCC transceiver to apply on real applications.

The rest of this paper is organized as follows: Section II presents the time-domain BCC characteristics. Section III describes the architecture of the wideband signaling (WBS) BCC transceiver, and Section IV shows the experimental results of the proposed WBS BCC transceiver. Finally the conclusion is given in Section V.

II. Time-Domain Human Body Channel Communication Characteristics

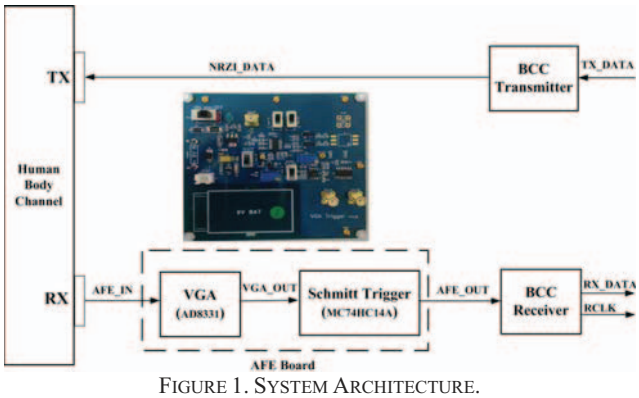

Figure 1. System Architecture.

The most important thing to design a BCC transceiver is to understand the body channel characteristics. Fig. 1 shows the proposed BCC transceiver system architecture which includes a BCC transmitter, an analog frontend (AFE) printed circuit board (PCB), and a BCC receiver. The AFE PCB is composed of a variable gain amplifier (VGA) and a Schmitt trigger. The operation of the system

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is described as follows: In the transmitter (TX) part, the input TX_DATA is encoded as non-return-to-zero-inverted data (NRZI_DATA) and transmitted to the human body channel with a driving buffer. In the receiver (RX) part, the AFE PCB receives the shark-fin-like signal from the human body (AFE_IN). The AFE_IN signal is amplified by the VGA, and after a Schmitt trigger, the signal is recovered back to digital waveform (AFE_OUT). Then, the BCC receiver recovers the data (RX_DATA) and outputs the clock signal (RCLK).

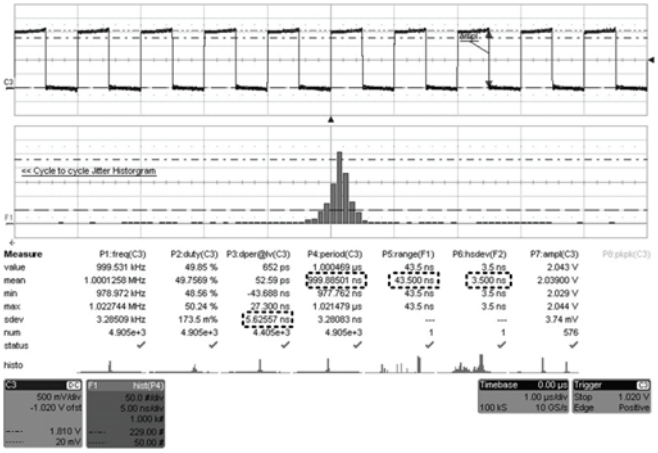

FIGURE 2. JITTER MEASUREMENT AT 140 CM, 1MHZ.

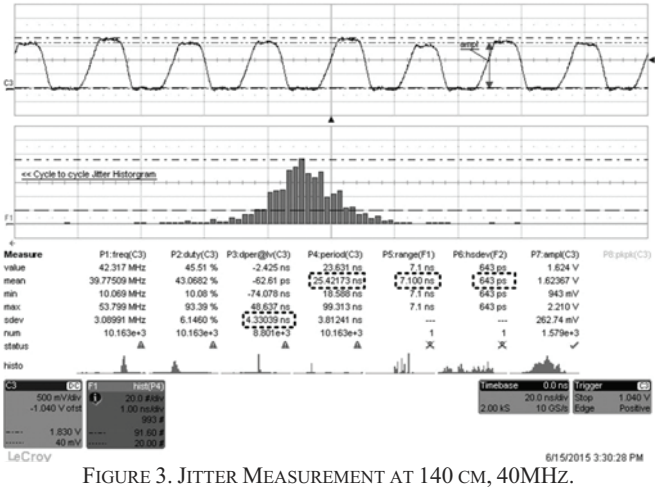

FIGURE 3. JITTER MEASUREMENT AT 140 CM, 40MHZ.

To correctly measure the BCC characteristics, the ground plane must be considered with special attention [7], thereby we use a battery-powered signal generator to replace the BCC transmitter in frequency domain and time domain measurement. In addition, the circular single electrode with 1.5 cm diameter is used during the measurement. The measured subject is 172cm in height and 75kg in weight. BCC characteristics are measured while the subject is sitting. According to the frequency domain measurement, we can decide the voltage gain setting of the VGA at different transmission distance. In time domain measurement, a clock signal is sent to the TX electrode, and the output signal of the AFE PCB (AFE_OUT) is measured. The measured clock frequency ranges from 1MHz to 40MHz at 10cm and 140cm transmission distance.

Fig. 2 shows the measured jitter histogram of the AFE output at 140cm, 1MHz. This measurement result can be used to determine the jitter performance after the AFE PCB when 101010 transitions are sent by the TX at 2Mb/s. Similarly, Fig. 3 shows the measured jitter histogram of the AFE output at 140cm, 40MHz, and the measurement result shown in Fig. 3 can be used to determine the jitter performance after the AFE PCB when 101010 transitions are sent by the TX at 80Mb/s. Table I summarizes the jitter measurement results of the recovered signal of the AFE PCB from 1MHz to 40 MHz at 10cm and 140cm transmission distances. Peak-to-peak (P_K-P_K) period jitter and root-mean-square (RMS) jitter are also specified in unit interval (UI). The jitter in the output of the AFE PCB includes the interferences in nearby environment and the non-ideal effects of the VGA and the Schmitt trigger, and the maximum P_K-P_K jitter can be up to 28% UI. We can use time domain BCC characteristics to build up the jitter model for the BCC receiver design. According to measurement results, the BCC receiver should have large jitter tolerance.

TABLE I. JITTER MEASUREMENT RESULTS

Distance	Frequency	Input Voltage	Period	Period Jitter Peak-to-Peak	Period Jitter RMS
10 cm	1 MHz	1.0 Vpp	999.99 ns	3.9 ns (3.9% UI)	471.7 ps (0.05% UI)
	10 MHz		99.99 ns	3.65 ns (3.65% UI)	271.3 ps (0.27% UI)
	20 MHz		49.99 ns	3.05 ns (6.01% UI)	314.4 ps (0.63% UI)
	30 MHz		33.33 ns	1.5 ns (4.50% UI)	160.1 ps (0.48% UI)
	40 MHz		25.01 ns	2.6 ns (10.39% UI)	155.6 ps (0.62% UI)
140 cm	1 MHz		999.88 ns	43.5 ns (4.35% UI)	3.5 ns (0.35% UI)
	10 MHz		99.96 ns	10 ns (10% UI)	1.1 ns (1.1% UI)
	20 MHz		49.99 ns	3.4 ns (6.8% UI)	253.6 ps (0.5% UI)
	30 MHz		33.35 ns	1.72 ns (5.15% UI)	219 ps (0.66% UI)
	40 MHz		25.42 ns	7.1 ns (27.93% UI)	643 ps (2.53% UI)

III. THE PROPOSED ARCHITECTURE

The proposed WBS BCC transceiver consists of a transmitter, a human body channel, an AFE PCB, and a receiver. The transmitter is composed of a spread spectrum clock generator (SSCG) [12], a preamble generator, a non-return-to-zero-inverted (NRZI) encoder with bit-stuffing control. In the transmitter part, the SSCG circuit generates the spread spectrum clock signal to trigger the transmitter for electromagnetic interference (EMI) reduction. In the transmitter, a linear feedback shift register (LFSR) circuit, which consists of twenty registers and a XOR gate, can generate random pattern sequences for bit error rate measurement. Two multiplexers are used to select the external clock input or the external data input in the normal mode. Subsequently, the TX_DATA is encoded by the NRZI encoder and transmitted to the human body channel with a driving buffer.

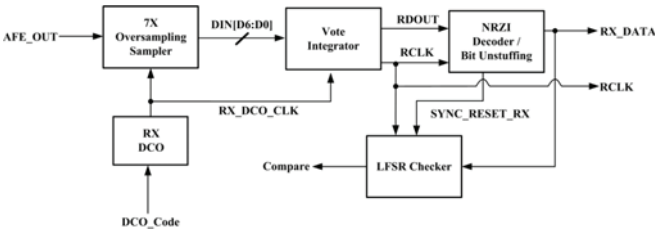

FIGURE 4. THE PROPOSED BCC RECEIVER.

Since less data transitions will increase the difficulty to recover the data in the receiver part due to the jitter accumulation and the duty-cycle distortion in the AFE PCB, and therefore, the bit stuffer in the transmitter can create enough data transitions after NRZI encoding. The maximum continuous identical digits (CIDs) are 5 bits after bit stuffing control. In a packet, sixteen preamble bits are firstly transmitted to the human body channel for synchronization, accompanied by four bits start frame delimiter (SFD). Consequently,

1000 bytes data are continuously transmitted to the human body channel. After transmitted the first packet, the second packet is transmitted to the human body, and so on.

The WBS BCC receiver is composed of an AFE PCB and an all-digital clock and data recovery (CDR) circuit. When the AFE PCB receives wideband pulse signals (AFE_IN) from the human body channel, the AFE PCB recovers them back to the digital waveforms (AFE_OUT). Finally, the proposed 7X oversampling CDR circuit recovers the AFE_OUT to the data (RX_DATA) and the clock signal (RCLK). Fig. 4 shows the architecture of the proposed 7X blind oversampling CDR circuit. The CDR circuit is composed of a digital controlled oscillator (DCO), a 7X oversampling sampler, a vote integrator, a NRZI decoder, and a LFSR checker. The LFSR checker is for automatic error free measurement. It generates random pattern sequences which is exact the same as the LFSR circuit in the transmitter. Therefore, the proposed WBS transceiver can detect whether there are bit errors in the recovered data (RX_DATA) or not.

The signal AFE_OUT represents the recovered digital waveform by the AFE PCB. The external input DCO control code (DCO_Code) controls the RX_DCO to generate a 280 MHz frequency clock (RX_DCO_CLK) for the 7X oversampling sampler and the vote integrator. The 7X oversampling sampler samples seven data points in one symbol period and outputs the DIN[D6:D0] signals. Subsequently, DIN[D6:D0] signals are sent to the vote integrator. After the voting mechanism, the vote integrator outputs the recovery data (RDOUT) and the recovery clock (RCLK). Then, RDOUT signal is sent to the NRZI decoder to output the original data (RX_DATA) after bit un-stuffing.

When the BCC receives the SFD of the packet, it outputs SYNC_RESET_RX signal to trigger the LFSR checker. Subsequently, the LFSR checker in RX generates the same random pattern sequences in TX for comparing with the recovered data. The signal Compare is set to "0" when recovered data are corrected. Oppositely, if the recovered data are not as expected, the signal Compare is set to "1" and a bit error occurs.

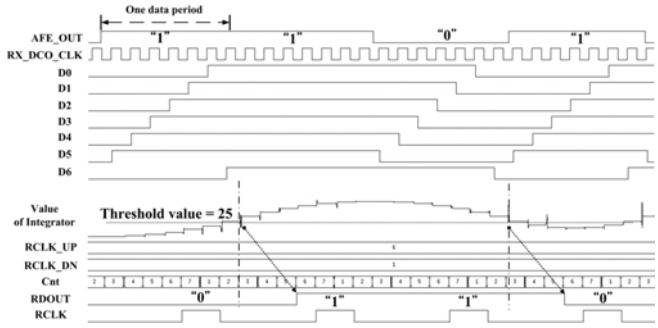

FIGURE 5. SIMULATION WAVEFORM OF THE CDR CIRCUIT

The vote mechanism of the vote integrator is described below. The 7X oversampling sampler samples seven data points in one symbol period and outputs the DIN[D6:D0] signals to the vote integrator, as shown in Fig. 5. In the vote integrator, it creates an integration window in one data symbol period. Each data period includes seven time slices. The vote integrator counts the number of "1" from D0 to D6 in the integration window. If D0 to D6 are all "1" in a time slice, the maximum number of "1"s is 7. Moreover, the maximum value of "1"s in the integration window is 49.

RDOUT signal is set by the value of the vote integrator. When the value of the integrator has a rise transition over the threshold line, the RDOUT signal is set to "1". When the value of the vote integrator has a fall transition through the threshold line, RDOUT signal is set to "0". The threshold value is set to the half of the maximum value of the integrator output (i.e. 25). As shown in Fig. 5, it takes three clock cycles to calculate RDOUT signal and RCLK signal. Whenever there has a rise or fall transition over the threshold line, the data clock position (RCLK_UP and RCLK_DN) is updated by the value of Cnt signal. For example, as illustrated in Fig. 5, at the first rise transition of the integrator value, the value of Cnt signal is 3. Then, RCLK_UP and RCLK_DN are updated as 6=[(3+3) mod 7] and 1=[(3+5) mod 7], respectively. Similarly, at the first fall transition of the integrator value, the value of Cnt signal is 3, and then, RCLK_UP and RCLK_DN are the same as previous numbers. Finally, when the Cnt value is equal to the RCLK_UP value, data clock (RCLK) is set to "1", and when the Cnt value is equal to the RCLK_DN value, RCLK signal is set to "0".

Normally, RCLK signal rises in every seven RX_DCO_CLK periods. However, if there is no rise transition or fall transition of the integrator value for a long period, the accumulated jitter or frequency drifts can cause the update of the data clock position (RCLK_UP and RCLK_DN). Thus, RCLK signal will not always rises in every seven RX_DCO_CLK periods. As a result, the vote integrator can tolerate the frequency drift or random jitter in the received signal to ensure the correctness of the recovered data.

IV. EXPERIMENTAL RESULTS

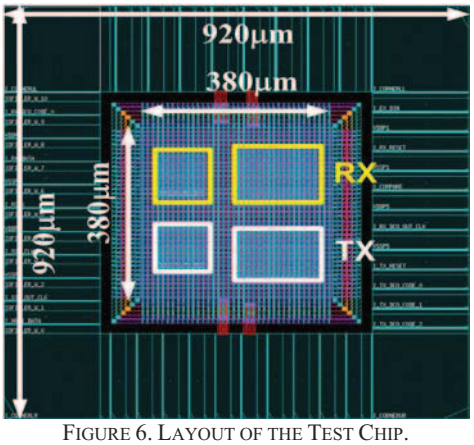

FIGURE 6. LAYOUT OF THE TEST CHIP.

TABLE II. CHIP SUMMARY

Process	90nm CMOS
Operating Range	1 Mb/s ~ 40 Mb/s
Supply Voltage	1.0V
Core Area	0.144 mm^2
Power Consumption	1.21mW (40Mb/s) (w/o AFE circuit)
AFE Power Consumption	AD8331: 0.78W MC74HC14A: 0.5W
BER	10^{-8} (40 Mb/s)
Energy/bit	0.03nJ/b (40 Mb/s)

Fig. 6 shows the layout of the test chip. The test chip is implemented in TSMC 90nm CMOS process with standard cells and a 1.0 V power supply. The core size of the chip is 380*380μm^2, and

the chip size including I/O PADs is 920*920μm^2. Table II shows the chip summary of the proposed WBS transceiver. The data rate of the proposed WBS transceiver ranges from 1Mb/s to 40Mb/s. The power consumption of the proposed WBS transceiver without the AFE PCB is 1.21 mW at 40 Mb/s. The power consumption of the AFE PCB is 1.28 W (VGA: 0.78W and Schmitt trigger: 0.75W) with a 5.0V power supply. The bit error rate (BER) is less than 10^{-8} and the energy consumption per bit is 0.03nJ/b at 40 Mb/s.

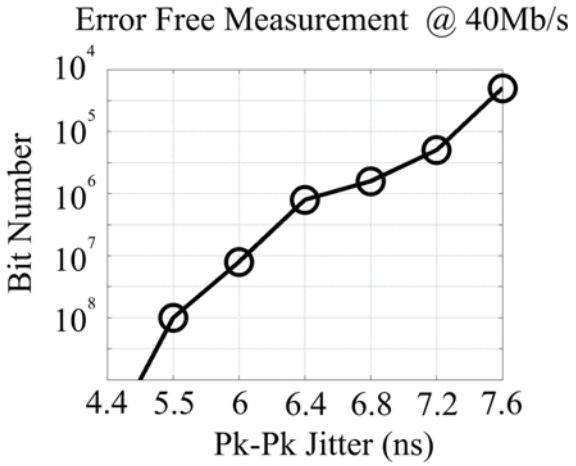

FIGURE 7. ERROR-FREE BIT ERROR RATE SIMULATION.

Fig. 7 shows the error free simulation versus different input P_K-P_K jitter at 40Mb/s and 140cm transmission distance. The proposed WBS BCC transceiver achieves a bit-error-rate (BER) < 10^{-8} with input 5.5ns P_K-P_K jitter. If the input jitter is increased to 7.2ns P_K-P_K, the BER performance can be still smaller than 10^{-5}. Table III shows the comparison table. The proposed WBS BCC transceiver has a simple architecture and thus it occupies a small chip area and consumes low-power consumption.

TABLE III. PERFORMANCE COMPARISON

	[13] JSSC'07	[3] JSSC'09	[10] ISSCC'09	[9] JSSC'12	[14] ISSCC'14	Proposed
Process	0.25 μm	0.18 μm	0.13 μm	0.18 μm	65 nm	90 nm
Data Rate	2 Mb/s	60 kb/s ~ 10 Mb/s	8.5 Mb/s	1 kb/s ~ 10 Mb/s	60 Mb/s	1 Mb/s ~ 40 Mb/s
Modulation	Wideband Signaling	Adaptive Frequency Hopping FSK	Correlation Direct Digital	Double FSK	3-level Walsh Coding	Wideband Signaling
Supply	1 V	1 V	1.2 V	1 V	1.1 V	1 V
Sensitivity	-36 dBm	-65 dBm	-36 dBm	-40 dBm	-58 dBm	-29 dBm
Power Consumption	5 mW	3.7 mW	2.75 mW	3.2 mW	9.02 mW	1.21 mW (w/o AFE) circuit)
Area	0.85 mm^2	2.30 mm^2 (with I/O pads)	0.19 mm^2	12.5 mm^2 (with I/O pads)	0.85 mm^2	0.14 mm^2
BER	1.1*10^{-7}	10^{-5} @10Mb/s	10^{-3}	10^{-5} @10Mb/s	<10^{-5} @60Mb/s	<10^{-8} @40Mbps
Energy/bit	2.5 nJ/b	0.37 nJ/b	0.32 nJ/b	0.32 nJ/b	0.15nJ/b	0.03nJ/b

V. CONCLUSION

In order to understand the characteristics of the human body channel, we measured the human body channel characteristics in frequency domain and time domain. In the proposed BCC transmitter, a SSCG is used to achieve EMI reduction. In the proposed BCC receiver, the receiver uses the 7X oversampling CDR architecture which adopts the vote mechanism to reduce the effects of jitter accumulation and the frequency drifts. The proposed WBS BCC transceiver has a simple architecture which also reduces the design complexity of the BCC transceiver and has a low area cost.

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