All-Digital Delay-Locked Loop for 3D-IC Die-to-Die Clock Synchronization

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Abstract **— In this paper, an all-digital delay-locked loop (ADDLL) for 3D-IC die-to-die clock synchronization with through silicon vias (TSVs) is presented. The proposed ADDLL can tolerate delay variations in TSVs and synchronize the clock signals in multiple layers of a given 3D-IC. Firstly, after system is reset, the proposed ADDLL uses two high resolution delay lines which composed of digital controlled varactors (DCVs) to compensate for the delay variations in TSVs. Subsequently, the proposed ADDLL can further compensate for the clock skew of clock signals in multiple layers of a 3D-IC. After ADDLL is locked, the clock skew or phase error is eliminated, and data transfer between dies can be performed synchronously. The proposed design can operate from 300MHz to 1GHz. The proposed ADDLL is implemented in a standard performance 90nm CMOS process, and the area of the ADDLL per die is 0.045mm^2. The power consumption of the proposed ADDLL is 3.27mW at 1GHz, and the maximum phase error of clock signals in multiple layers of a given 3D-IC is 21.9ps.**

Index Term **—all-digital delay-locked loop, through silicon via (TSV), 3D-IC, digitally controlled delay line.**

I. Introduction

According to Moore's Law, there are more and more transistors can be integrated in a single chip with the improvement of semiconductor technologies. However, in a system-on-a-chip (SoC), some modules, such as, dynamic random access memory (DRAM) or radio-frequency (RF) circuits require a special process technology rather than the logic process technology. Thus, they should be fabricated in different processes to minimize the overall design cost. To integrate these fabricated dies, bonding wires can be used for die-to-die connection. In recent years, the die-to-die connection through through-silicon-vias (TSVs) becomes more popular due to a much smaller delay of TSVs than the bonding wires. TSVs can be placed anywhere on the dies, and thus, the number of IOs are increased, and the wire length between dies can be greatly reduced. However, TSVs can be faulty due to incomplete fills at pre-bond or misalignment during post-bonding. As a result, sometimes it needs to re-route signals through spare TSVs. In addition, defects of TSVs can also exhibit a longer delay time than its ideal value. As a result, the propagation delay through different TSVs will have large delay variations, and for inter-die clock distribution, there should be a way to tolerate any unexpected TSV delay variations.

Many researches [5]-[8] pay attention to the TSV variation problem. In [5], the research focuses on analyzing the impact of TSV open defects. It shows that the resistive-open phenomenon will cause increasing of the TSV propagation delay. In [6]-[8], a ring oscillator (RO)-based architecture is proposed to detect the TSV variation phenomenon. In [6], the variable output threshold is proposed. They can detect the parametric delay fault by dynamically switching the inverter driving ability to observe the output frequency of RO. This research shows that the maximum TSV delay variation can be up to about 500ps. In [7], the research focuses on pre-bond TSV test. It also uses the RO architecture to detect the TSV propagation delay variation in their RC parameters. The proposed pre-bond TSV testing can detect leakage and resistive-open faults during manufacturing test. In accordance with above results, the propagation delay of TSVs will vary with process variations.

In high-speed SoC design, the global clock distribution through clock tree buffers and clock network routing should be carefully designed to minimize the clock skew between modules. The delay-locked loops (DLLs) [1] and phase-locked loops (PLLs) are widely used to eliminate the clock skew between the local clock and the global clock. Therefore, for 3D IC clock synchronization, a DLL-based data self-aligner (DBDA) [2] is presented to reduce the data confliction time of the memory's outputs with stacked dies. In the DBDA, a replica TSV delay is required for the DLL circuit. However, since unexpected TSV delay variations may occur due to faulty TSVs, the DBDA may still have large phase error after the DLL is locked.

A dual-locking DLL [3] is proposed for die-to-die clock synchronization. The dual-locking DLL does not need to replicate the delay of TSVs, and therefore, the phase error caused by the mismatch in the replica TSV delay and the real TSV delay will not happen. However, the dual-locking DLL needs to continue fine-tuning the two DLLs in an interleaved manner to keep maintaining the phase alignment between the clock signals in multiple layers of a 3D-IC. As a result, the dual-locking DLL needs to regularly switch the direction of the forward path and the feedback path, and perform fine-tuning in two DLLs, which may cause a relatively large phase error during phase maintaining mode.

A dual-delay-locked loop (D-DLL) [4] is proposed for die-to-die clock deskew circuit applications. Two analog charge-pump-based DLLs are used in this design. However, a special bidirectional buffer is required in this design to simultaneous transmit of signals in both directions on a single TSV. In addition, two DLLs are working at the same time which increases the design complexity of the D-DLL. In advanced CMOS process, the leakage current problem of the MOS transistor and high voltage control gain problem with a low supply voltage in design of the voltage controlled delay line for wide frequency range operation will be the design challenges of the D-DLL.

In this paper, an all-digital delay locked loop (ADDLL) for 3D-IC die-to-die synchronization with two TSVs is presented. The proposed ADDLL uses two high resolution delay lines with digital controlled varactors (DCVs) to compensate for the delay variations of two TSVs. Then in the proposed ADDLL, two digital controlled delay lines (DCDLs) will be used to eliminate the phase error of clock signals in two dies of the 3D-IC. After ADDLL is locked, data transfer between dies can be transmitted synchronously with a high-speed clock through a large number of TSVs concurrently

The rest of the paper is organized as follows: Section II describes the overall architecture, circuit design details, TSV delay variation compensation procedure, and the locking mechanism of the proposed

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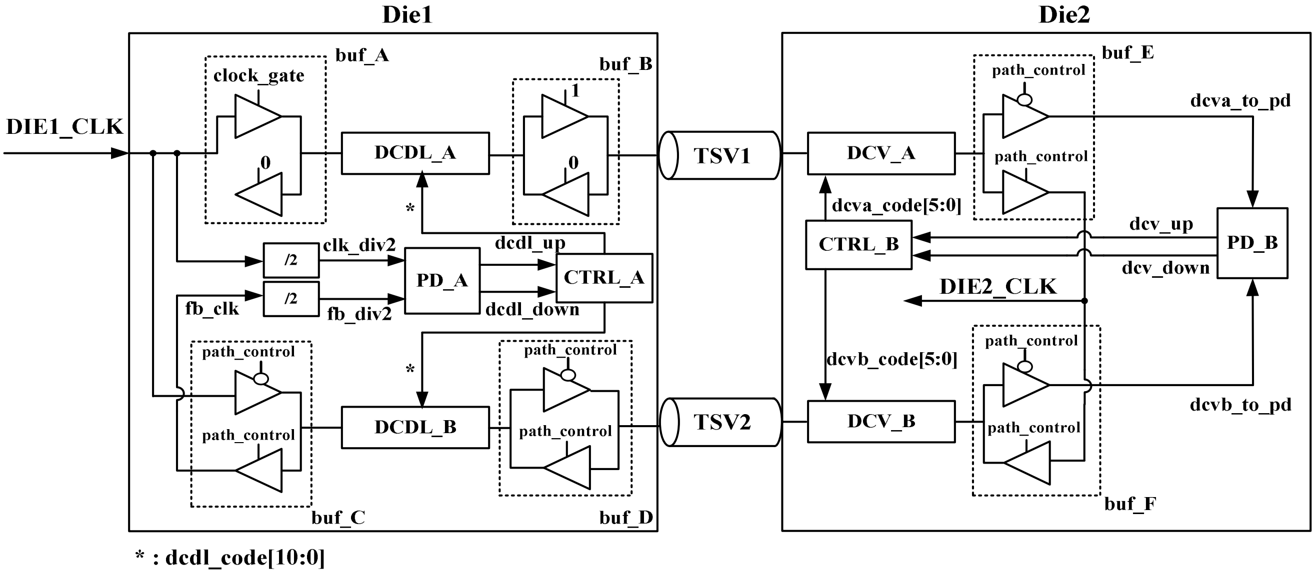

FIGURE. 1 THE PROPOSED ADDLL ARCHITECTURE.

ADDLL. The experimental results at three process, voltage, and temperature (PVT) cases are discussed in Section III. Finally, Section IV concludes with a summary.

II. SYSTEM ARCHITECTURE

Fig. 1 shows the architecture of the proposed ADDLL for die-to-die clock synchronization in a given 3D-IC. The ADDLL is composed of two digital controlled delay lines (DCDL_A and DCDL_B), two digital controlled varactor-based delay lines (DCV_A and DCV_B), two ADDLL controllers (CTRL_A and CTRL_B), two phase detectors (PD_A and PD_B), two frequency-divided-by-2 circuits, and six tri-state buffer groups (buf_A to buf_F). The DCDL [9] is composed of a coarse-tuning delay stage and a fine-tuning stage. DCV_A and DCV_B are used to compensate for the TSV delay variations. DCDL_A and DCDL_B are used to compensate for the phase error between clk_div_2 and fb_div2.

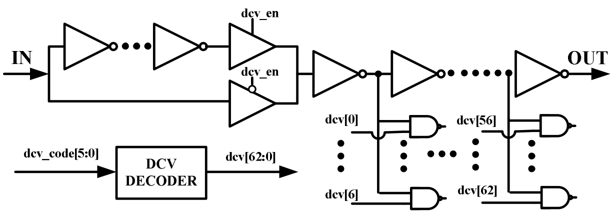

FIGURE. 2 THE PROPOSED DCV-BASED DELAY LINE ARCHITECTURE.

Fig. 2 shows the proposed DCV-based delay line architecture (DCV_A and DCV_B). It is composed of a bypass inverter chain and a DCV delay line. There are 63 NAND gates used as digital controlled varators to provide a fine resolution delay line. The DCV_A and DCV_B are used to compensate the delay variations between two TSVs. The dcv_en signal is used to control the bypass inverter chain to provide a longer propagation delay time in best case PVT conditions. When the operation condition is at worst case PVT condition, the dcv_en is set to 0 to reduce the overall delay time of the DCV-based delay line. The DCDL_A and DCDL_B are controlled by the same delay line control code (dcdl_code[10:0]). The delay line control code can adjust the propagation delay of the upper delay path and the lower delay path.

The proposed digitally controlled delay line [9] (DCDL_A and DCDL_B) is composed of a coarse-tuning delay stage and a fine-tuning stage. The coarse-tuning delay stage is composed of 63 coarse-tuning delay units. Each coarse-tuning delay unit is composed of three NAND gates and a dummy cell. The dummy NAND gate is added to balance the wire capacitance. The fine-tuning delay stage [9] is composed of two parallel connected tri-state buffers. The tri-state buffer arrays operate as an interpolator circuit to achieve a fine resolution.

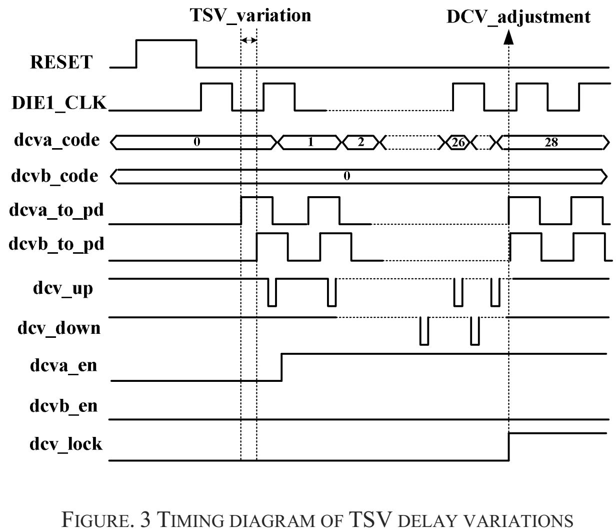

FIGURE. 3 TIMING DIAGRAM OF TSV DELAY VARIATIONS COMPENSATION.

There are three steps in the proposed ADDLL to achieve die-to-die clock synchronization. **First**, when the ADDLL is reset, the path_control signal is set to zero, and DCDL_A, DCDL_B, DCV_A, and DCV_B are set to provide a minimum delay time. In the upper delay path, the DIE1_CLK signal passes through buf_A, DCDL_A, buf_B, TSV1, DCV_A, and buf_E to the phase detector B (PD_B) denoted as dcva_to_pd. Similarly, in the lower delay path, the DIE1_CLK signal passes through buf_C, DCDL_B, buf_D, TSV2, DCV_B, and buf_F to the PD_B denoted as dcvb_to_pd. In the proposed ADDLL, six tri-state buffer groups (buf_A to buf_F) are designed with same tri-state buffers, and the delay time of the DCDL_A is the same as the DCDL_B. Therefore, the phase error between dcva_to_pd signal and dcvb_to_pd signal comes from the delay variations between TSV1 and TSV2. Fig. 3 shows the timing diagram of TSV delay variations compensation. In Fig. 3, dcva_to_pd signal leads dcvb_to_pd signal, and thus, the PD_B generates dcv_up signal to the CTRL_B to increase the delay time of the DCV_A. After two times polarity change of the PD_B from dcv_up to dcv_down or dcv_down to dcv_up, the dcv_lock signal is pulled high to stop tuning the control code of the DCV_A and the DCV_B. Then, the phase error between dcva_to_pd signal and dcvb_to_pd signal are eliminated which means the delay variations between TSV1 and TSV2 is compensated.

Second, after TSVs delay variations are compensated, the clock_gate signal is set to zero for three consecutive clock cycles to stop the DIE1_CLK signal propagating to the upper delay path. The clock-gating is performed to recognize the first positive edge transition of the fb_clk signal for the next locking procedure. **Third**, after clock-gating is performed, the path_control signal and clock_gate signal are pulled high, and the DIE1_CLK signal passes through buf_A, DCDL_A, buf_B, TSV1, DCV_A, buf_E, buf_F, DCV_B, TSV2, buf_D, DCDL_B, buf_C, and a frequency-divided-by-2 circuit to the phase detector A (PD_A) denoted as fb_div2. In addition, the DIE1_CLK signal is divided by 2 and sent to the PD_A denoted as clk_div2. The PD_A detects the phase relationship between the clk_div2 signal and fb_div2 signal, and it outputs dcdl_up signal and dcdl_down signal to the CTRL_A. The CTRL_A outputs the delay line control code (dcdl_code[10:0]) for adjusting the delay time of the DCDL_A and the DCDL_B.

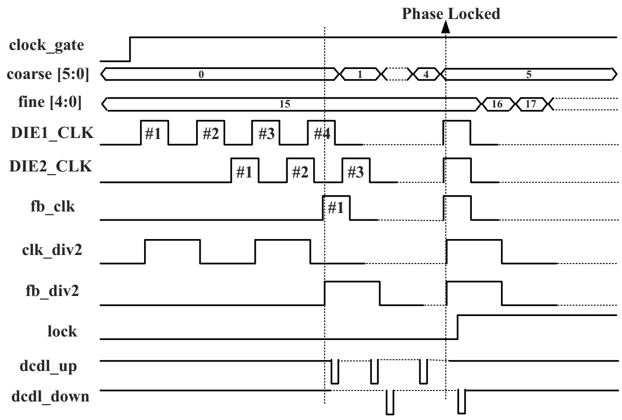

FIGURE. 4 TIMING DIAGRAM OF DIE-TO-DIE CLOCK SYNCHRONIZATION.

$$\begin{aligned} &T_{buf\_A} + T_{DCDL\_A} + T_{buf\_B} + T_{TSV1} + T_{DCV\_A} \\ &+ T_{buf\_E} + T_{buf\_F} + T_{DCV\_B} + T_{TSV2} + T_{buf\_D} \\ &+ T_{DCDL\_B} + T_{buf\_C} = 2N \times T_{DIE1\_CLK} \\ &2 \times \Big(T_{buf\_A} + T_{DCDL\_A} + T_{buf\_B} + T_{TSV1} \\ &+ T_{DCV\_A} + T_{buf\_E}\Big) = 2N \times T_{DIE1\_CLK} \end{aligned} \quad (1)$$

Fig. 4 shows the timing diagram of die-to-die clock synchronization. After clock_gate signal is pulled high, the CTRL_A starts to align the phase of clk_div2 signal and fb_div2 signal. Because the DCDL_A and DCDL_B are set to a minimum delay time in the beginning, the fb_div2 signal will lead to the clk_div2 signal. The CTRL_A will keep increasing the delay time of the DCDL_A and DCDL_B until the polarity of the PD_A changes from dcdl_down to dcdl_up. The lock condition of the ADDLL can be expressed as Eq. 1. Since the total delay in the upper delay path will be equal to the lower delay path, and thus, after ADDLL is locked, the total delay time in the upper path will be equal to $N \times T_{DIE1\_CLK}$ which means the phase error between the DIE1_CLK signal and DIE_2 signal is cancelled.

III. EXPERIMENTAL RESULTS

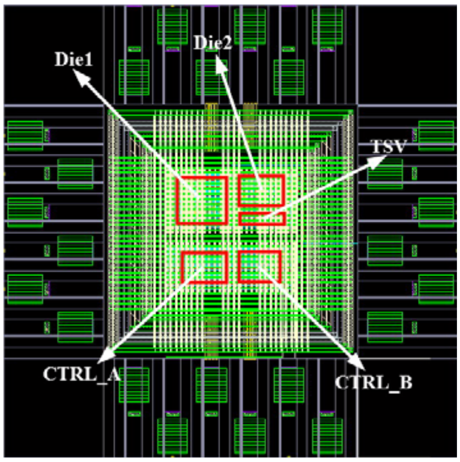

FIGURE 5. LAYOUT OF THE TEST CHIP

The proposed ADDLL is implemented in a standard performance 90nm 1P9M CMOS process with a 1.0V power supply. Fig. 5 shows the layout of the test chip, and the active area of the test chip is 300μm × 300μm. The area of the proposed ADDLL per die is 0.045 μm, and two delay lines are added in the test chip for simulation of the TSV delay. Table I shows the simulation delay time of the DCV-based delay line (DCV_A and DCV_B) with PVT variations. The worse resolution of the DCV-based delay line is 8.4ps for accurate compensation for the TSV delay variations. The proposed DCDL is composed of a coarse-tuning delay line and a fine-tuning delay line. The worse coarse-tuning resolution of the DCDL is 93ps with PVT variations.

TABLE I. DELAY TIME OF DCV-BASED DELAY LINE.

	FF	TT	SS
Intrinsic Delay	496ps	676ps	1046ps
Maximum Delay	762ps	1024ps	1585ps

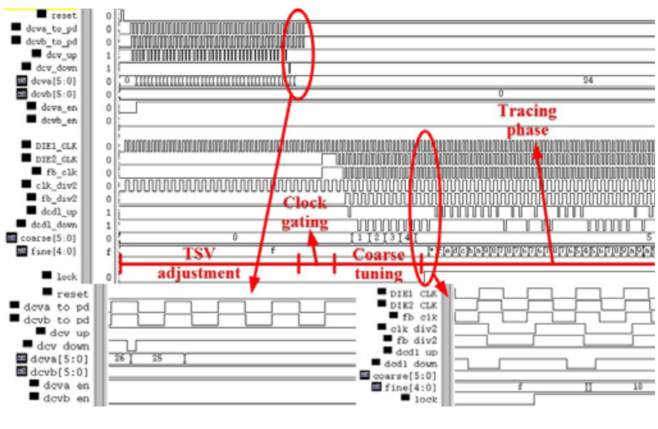

FIGURE. 6 SIMULATION WAVEFORM OF THE PROPOSED ADDLL.

Fig. 6 shows the simulation waveform of the proposed ADDLL with an 1GHz input clock. After the ADDLL is reset, the path_control signal is set to zero, and DCDL_A, DCDL_B, DCV_A, and DCV_B are set to provide a minimum delay time. The CTRL_B adjusts the DCV_A and DCV_B according to the PD_B's output to increase the delay time of the DCV_A or DCV_B until the phase error between dcva_to_pd signal and dcvb_to_pd is eliminated which means the delay variations between TSV1 and TSV2 is compensated. After TSV delay variations are compensated, the DCV-based delay line control code (dcva[5:0] and dcvb[5:0]) is fixed. Then, path_control signal is pulled high, and the CTRL_A adjusts the DCDL_A and DCDL_B according to the PD_A's output to reduce the phase error between clk_div2 signal and fb_div2 signal. After the ADDLL is locked, the phase error between clk_div2 signal and fb_div2 signal is eliminated, and the phase error between the DIE1_CLK signal and DIE2_CLK signal is also cancelled, as explained in Section II. In Fig. 6, the delay variations between TSV1 and TSV2 is 176.4ps, after the proposed ADDLL is locked, the phase error between DIE1_CLK signal and DIE2_CLK signal is reduced to 21.9ps.

TABLE II. PERFORMANCE COMPARISONS

	Proposed	**JSSC'13 [2]**	**TCAS-I'13 [3]**	**ISCAS'12 [4]**
Type	All-Digital	All-Digital	All-Digital	Analog
Process	90nm	130nm	90nm	0.18μm
Supply Voltage	1.0V	1.2V	1.0V	1.8V
Frequency	300MHz ~ 1 GHz	200MHz ~ 1.6GHz	50 MHz ~ 600 MHz	556 MHz ~ 1.5 GHz
Phase Error	< 21.9ps	<50ps*	< 15.8ps	< 2ps
Area per Die (mm^2)	0.045	0.06	0.0044	N/A
Power	3.27mW @1GHz	0.9mW @1.6GHz	1.8mW @600MHz	56mW @1.5GHz

*if replica delay matched perfectly

Table II shows the performance comparisons with the state-of-the-arts. In the DBDA [2], they needs to replicate the delay of the inter-die TSV wire delay, Therefore, the unexpected TSV delay variations can greatly increase the phase error of clock signals in multiple layers of a 3D-IC after the DLL is locked. In the dual-locking DLL [3], after the DLL is locked, the dual-locking DLL needs to continue fine-tuning the two DLLs in an interleaved manner to keep maintaining the phase alignment. However, the regularly switching the direction of the forward path and the feedback path and perform fine-tuning in two DLLs may cause a relatively large error during phase maintaining mode. The dual-delay-locked loop (D-DLL) [4] does not need to switch the direction of the forward path and the feedback path since a bidirectional buffer is applied. However, two DLLs are working at the same time which increases the design complexity to maintain the stability of the D-DLL. The relative high power consumption is also the disadvantage of the analog charge-pump-based D-DLL.

IV. CONCLUSION

In this paper, an all-digital delay locked loop (ADDLL) for 3D-IC die-to-die synchronization with two TSVs is presented. The delay variations of TSVs will be compensated before the ADDLL's normal operation. As compared with current DLLs for 3D-IC clock deskew applications, the proposed ADDLL does not need to switch the path during phase maintaining mode. The proposed ADDLL can operate with a 300MHz – 1GHz input clock, and the maximum phase error is smaller than 21.9ps. In addition, the lock-in time is 79 cycles at 1GHz. Furthermore, the proposed ADDLL is implemented with standard cells, and the proposed design can be ported to different process in a short time. Therefore, the proposed ADDLL is very suitable for 3D-IC die-to-die clock synchronization applications.

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