A Low-Power and Small-Area All-Digital Spread-Spectrum Clock Generator in 65nm CMOS Technology

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Abstract—**In this paper, a low-power and small-area all-digital spread spectrum clock generator (ADSSCG) is presented. The proposed ADSSCG can provide a programmable spreading ratio. In order to maintain the frequency stability while performing triangular modulation, a fast frequency and phase relock mechanism is proposed to overcome the process, voltage, and temperature (PVT) variations. The proposed ADSSCG is implemented in a standard performance 65nm CMOS process, and the active area is 100μm × 100μm. The simulation results show that the electromagnetic interference (EMI) reduction is 22.6dB with 1.3% spreading ratio at 270MHz and 18.9dB with 0.45% spreading ratio at 162MHz. The power consumption is 229μW at 270MHz with 1.0V power supply. Besides, the proposed ADSSCG is implemented with standard cells, and thus it can be easily ported to different processes in a very short time. Therefore, the proposed ADSSCG is suitable for system-on-chip (SoC) applications.**

I. INTRODUCTION

In recent years, the issue of electromagnetic interference (EMI) in electronic products is highly discussed. There are many techniques provided to reduce EMI, such as shielding or low-voltage differential clocking. However, the shielding technique is cost-expensive, and the other one has a complex routing. Spread spectrum clock generator (SSCG) [1]-[7] is an appropriate solution to effectively reduce EMI with low hardware cost. There are several modulation methods of SSCG, two popular methods are direct modulation on voltage-controlled oscillator (VCO) [1]-[2], and modulation on frequency divider with a delta-sigma modulator (DSM) [7]. However, direct modulation on VCO usually requires a very large on-chip capacitor as a loop filter and occupies a large chip area. The other method, modulation on frequency divider, due to the quantization noise of divider, also requires a large on-chip capacitor. Since the MOS capacitor in 65nm CMOS process has serious leakage current problem, these analog approaches must be redesigned as technology migrates.

To reduce the area of the loop filter in analog approaches, all-digital spread spectrum clock generators (ADSSCGs) [3]-[6] are proposed to reduce the capacitor area. The ADSSCG uses a digital loop filter to replace the passive loop filter in analog approaches, and therefore, it can have a much smaller area than conventional analog SSCGs. However, due to the resolution limitation of the digital controlled oscillator (DCO), the ADSSCG [5]-[6] often needs to use a larger spread ratio to achieve the same EMI reduction as compared with analog SSCGs. As a result, the jitter performance of the ADSSCGs may be worse than analog SSCGs. In addition, the design challenge to design an ADSSCG is to maintain frequency stability (i.e. average frequency) while performing spread spectrum operation with process, voltage, and temperature (PVT) variations. An ADSSCG also needs to provide a programmable spreading ratio for trade-off between the jitter performance and the EMI reduction.

Furthermore, the non-monotonic DCO response will greatly influence the performance of the EMI reduction. Thus, in [9], a built-in self-calibration circuit for monotonic DCO design is presented. In addition, an interpolation-type DCO, which the fine-tuning stage implemented with interpolator circuits, can provide a monotonic response between the DCO control code and the output frequency is presented in [8][10]. The triangular modulation is often used in the SSCG. However, the triangular modulation makes it difficult to maintain the frequency stability of the output clock. Thus, in [5], a division triangular method is proposed to overcome this problem. However, the proposed ADSSCG [5] has a large cycle-to-cycle jitter. In addition, it can not be applied to the transceiver design with SSCG, such as the serial advanced technology attachment (SATA), since it is very difficult to track the frequency deviations of the data with division triangular method.

In this paper, an ADSSCG with direct modulation on the DCO is presented. The proposed ADSSCG can perform fast frequency and phase tracking during the triangular modulation. A DSM with the DCO can enhance the DCO resolution, and thus, the direct modulation on the DCO can generate an accurate triangular modulation on the output frequency. As a result, the proposed ADSSCG can provide a better EMI reduction with a smaller spreading ratio. In order to reduce the overall power consumption of the ADSSCG, the low-power monotonic DCO is designed. The proposed ADSSCG is implemented with standard cells, and therefore, it is very suitable for system-on-chip (SoC) applications.

The rest of the paper is organized as follows: the proposed ADSSCG architecture is presented in Section II. The fast frequency and phase maintenance mechanism is discussed in Section III. The monotonic DCO circuit design is discussed in Section IV. Section V shows the experimental results of the proto-type chip. Finally, Section VI concludes with a summary.

II. ARCHITECTURE OVERVIEW

Fig. 1 shows the block diagram of the proposed ADSSCG. The ADSSCG is composed of a phase and frequency detector (PFD), a spread spectrum clock (SSC) controller, a digital loop filter (DLF), a delta-sigma modulator (DSM), a monotonic DCO, and a frequency divider. The SSC controller directly controls the DCO control code (control_code) to perform center-spread triangular modulation on the output frequency. According to the user-defined spreading range (SPREAD_RANGE), the SSC controller modulates the output frequency to achieve the corresponding spreading ratio.

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To generate a smooth triangular modulation profile, the DCO resolution is further enhanced by employing a DCO dithering scheme through a 3-bit first-order DSM. The integral part of the DCO control code has 10 bits, and the fractional part of the DCO control code has 3 bits. The operation speed of the DSM is the output clock frequency divided by 8. Due to the enhancement of the DCO equivalent resolution, the proposed ADSSCG can provide a better EMI reduction with a smaller spreading ratio.

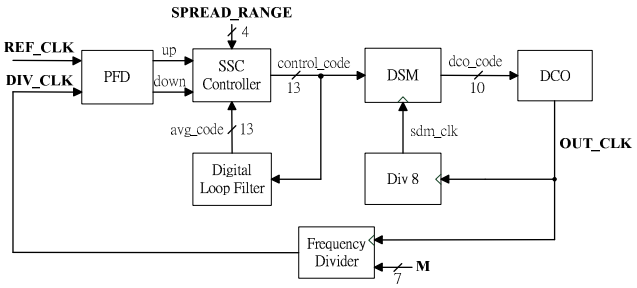


FIGURE 1. THE PROPOSED ADSSCG.

The digital loop filter [10] is applied in the ADSSCG to generate a stable average frequency to eliminate the jitter effects of the reference clock. The loop filter can generate a baseline DCO control code (avg_code) for the SSC controller. Thus, the SSC controller can keep updating the triangular modulation profile with PVT variations.

III. FREQUENCY AND PHASE MAINTENANCE

To maintain the frequency stability while performing spread spectrum, a fast frequency and phase relock mechanism is presented, as shown in Fig. 2. After system is reset, the ADSSCG performs frequency and phase tracking and operates as a normal phase-locked loop (PLL). After frequency and phase tracking is completed, the SSC controller starts the triangular modulation. There are four spread spectrum states (state_ssc). The first three states are used to modulate the DCO control code to generate a triangular profile. In the fourth state, the SSC controller performs the fast frequency and phase relock to maintain the frequency stability of the output clock. In Fig. 2, the user-defined spreading range (SR) is used to control the triangular profile, and therefore the spreading ratio can be easily adjusted.

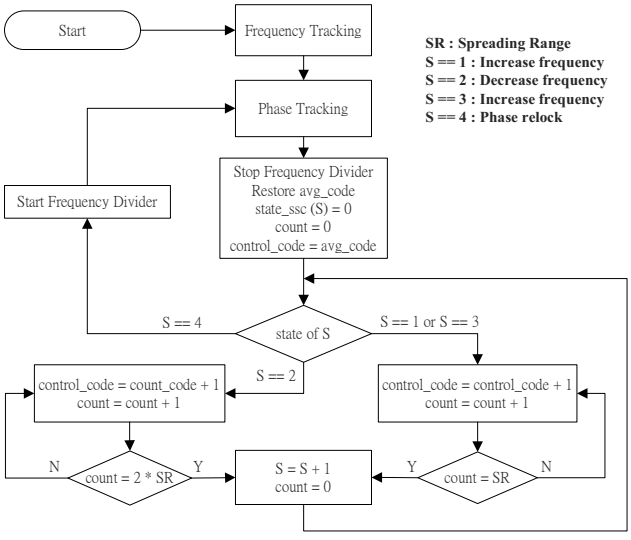


FIGURE 2. THE FLOWCHART OF THE PROPOSED ADSSCG.

The frequency divider is stopped during the triangular profile generation, as shown in Fig. 3. Thus the ADSSCG becomes an open-loop while performing spread spectrum generation. Subsequently, at the fourth state of state_scc, the frequency divider is enabled to perform frequency and phase tracking again. When the frequency divider is enabled, the phase error between the reference clock (REF_CLK) and the divided clock (DIV_CLK) is eliminated. Then, the SSC controller performs frequency and phase tracking to maintain the frequency stability of the output clock. The digital loop filter will update the baseline DCO control code (avg_code) during the frequency and phase relock process. After the phase relock process is completed, the SSC restores the baseline DCO control code and starts the triangular modulation again from the current baseline DCO control code. The fast frequency and phase relock mechanism is repeated in the end of each triangular profile to ensure the frequency stability of the output clock.

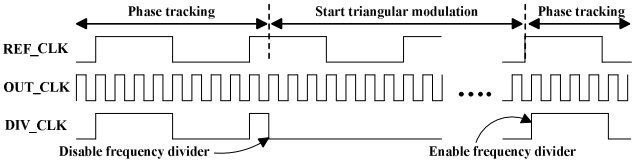
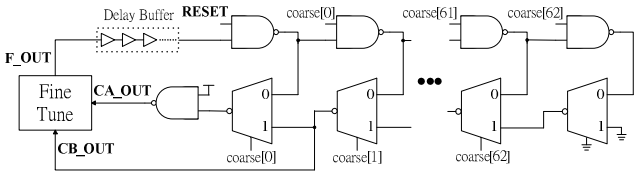
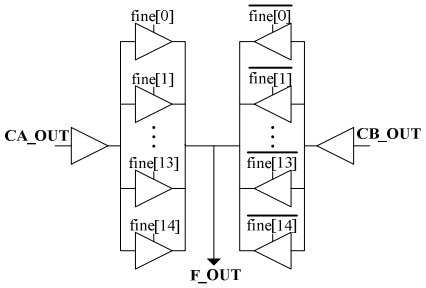


FIGURE 3. TIMING DIAGRAM OF THE FAST PHASE TRACKING.

IV. MONOTONIC LOW-POWER DCO



(a)



(b)

FIGURE 4. THE PROPOSED DCO:
(a) COARSE-TUNING STAGE (b) FINE-TUNING STAGE.

The monotonic response between the DCO control code and the output frequency is an important issue in ADSSCG design. The non-monotonic DCO response will result in poor EMI reduction. Therefore, a monotonic low-power DCO circuit [8] is presented, as shown in Fig. 4. The proposed DCO is implemented with standard cells. The DCO is composed of a ladder-shaped coarse-tuning stage and an interpolating fine-tuning stage. The coarse-tuning circuit has 64 coarse-delay cells (CDCs) and one NAND gate, as shown in Fig. 4(a). This CDC is combined with one NAND gate and one inverted MUX. Hence, the coarse-tuning resolution is equal to the delay time

of one CDC. In order to design a low power DCO, the DCO coarse-tuning code (coarse[62:0]) is used to control the NAND gate. This approach can turn off unnecessary NAND gates to reduce power consumption.

The fine-tuning stage is used to provide a fine DCO resolution in the cascaded DCO architecture. However, the total delay controllable range of the fine-tuning stage must be equal to the coarse-tuning resolution to ensure the monotonic DCO response. Fig. 4 (b) is the fine-tuning stage of the proposed DCO. The fine-tuning stage is composed of two parallel connected tri-state buffer arrays operating as an interpolator circuit. When there are more tri-state buffers turned on in the left side array, the output (F_OUT) will be more close to the CA_OUT. Oppositely, when there are more tri-state buffers turned on in the right side array, the output will be more close to the CB_OUT. The delay difference between CA_OUT and CB_OUT is the delay time of one CDC, as shown in Fig. 4 (a). Therefore, a fine-tuning stage with the average resolution equal to 1/16 of the coarse-tuning resolution can be achieved. As a result, the non-monotonic problem in conventional cascaded DCO architecture can be avoided in the proposed DCO.

The frequency range of the proposed DCO is from 138MHz to 624MHz with 87ps coarse-tuning resolution and 5.43ps fine-tuning resolution. With the enhancement of delta-sigma modulator, the equivalent DCO resolution is 0.679ps. The power consumption of the proposed DCO is 190.6μW at 624MHz. Fig. 5 shows the simulation results of the proposed DCO, and the DCO has a monotonic response when the coarse-tuning control code is switched.

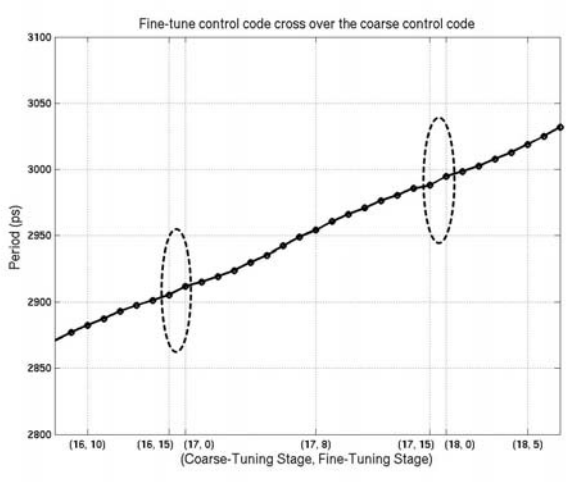


FIGURE 5. FINE-TUNING CODE CROSS OVER 2 COARSE-TUNING CODE.

V. EXPERIMENTAL RESULTS

The proposed ADSSCG is implemented in a standard performance (SP) 65nm CMOS process with 1.0V power supply. Fig. 6 shows the layout of the ADSSCG. The active area is 100μm ×100μm.

The simulation result of the proposed ADSSCG is shown in Fig. 7. After system is reset, the ADSSCG performs frequency and phase tracking until the PLL is locked. After that, the SSC function is turned on, and the frequency divider is stopped during the triangular profile generation. The spreading ratio is dependent on the user-defined spreading range. As compared with other SSCG [1]-[3],[7], the proposed ADSSCG operates as an open-loop while performing spread spectrum generation. Therefore, a perfect triangular modulation can be achieved without the disturbance comes from the PFD. However, the reference clock jitter effects and the PVT variations will influence the frequency stability of the output clock. Thus, in the proposed ADSSCG, at the end of the triangular modulation, the SSC controller performs a fast frequency and phase relock to maintain the frequency stability. In addition, the loop filter can filter out the reference clock jitter effects during the relock process.

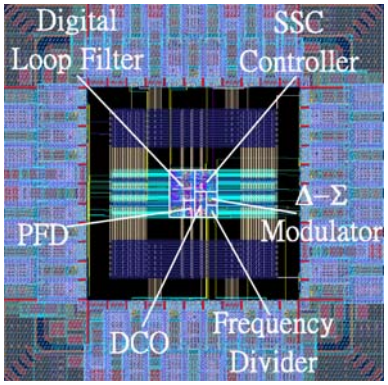


FIGURE 6. LAYOUT OF THE PROPOSED ADSSCG.

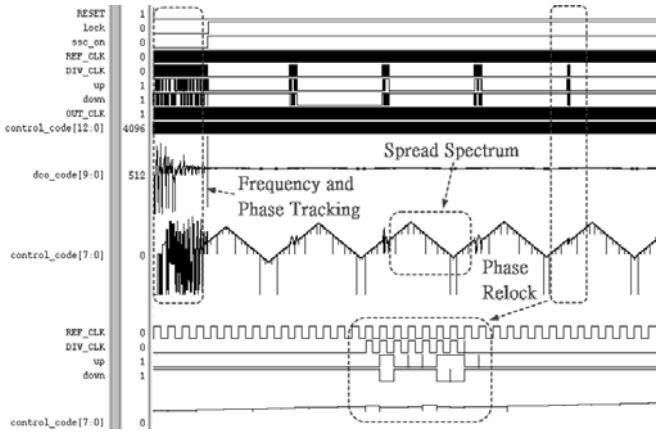


FIGURE 7. SIMULATION RESULTS OF THE PROPOSED ADSSCG.

Fig. 8 shows the simulated spectra of the output clock with center spread at 270MHz and 162MHz, respectively. The EMI reduction is 22.6dB at 270MHz with 1.3% spreading ratio, as shown in Fig. 8(a). Fig. 8(b) shows the 18.9dB EMI reduction is achieved at 162MHz with 0.45% spreading ratio. Table I lists comparison results with the state-of-the-art SSCGs. The proposed ADSSCG can provide a better EMI reduction with a smaller spreading ratio. In addition, the proposed low-power monotonic DCO also reduces the overall power consumption of the ADSSCG, and the proposed ADSSCG has smallest area as compared to the existing SSCGs.

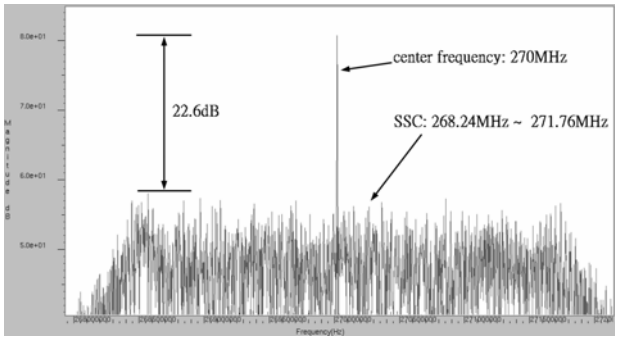
VI. CONCLUSION

In this paper, we proposed a low-power and small-area all-digital spread-spectrum clock generator with programmable spreading ratio for SoC applications. The proposed ADSSCG can generate a perfect triangular modulation without the disturbance comes from the PFD, and thus, the higher EMI reduction can be achieved with a smaller spreading ratio. As a result, the jitter performance of the ADSSCGs is better than the other SSCGs with a much larger spreading ratio to

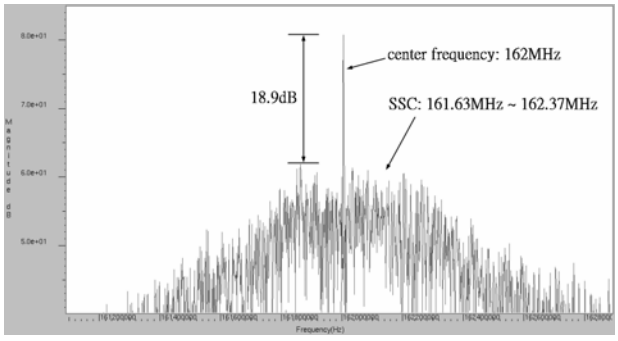
TABLE I. PERFORMANCE COMPARISONS

Parameter	Modulation profile	Modulation method	EMI reduction	Output frequency	Process	Area	Power consumption
Proposed	Triangular	All-Digital	22.6 dB (1.3%) (@270 MHz) 18.9 dB (0.45%) (@162 MHz)	162 MHz ~ 270 MHz	65nm	0.01 mm^2	229µW (@270MHz)
JSSC'03 [1]	Triangular	Analog PLL (VCO modulation)	11dB (2.5%) (@266 MHz)	66 MHz ~ 266 MHz	0.35µm	2.0 mm^2	300mW (@266MHz)
TCAS2'11 [2]	Triangular	Analog PLL (VCO modulation)	8.75dB (0.5%) (@ 270MHz)	162 MHz ~ 270 MHz	0.18µm	1.8 mm^2	19mW (@270MHz)
JSSC'09 [3]	Triangular	All-Digital	10.48dB (0.5%) (@1.5GHz)	1.5 GHz	0.18µm	0.2 mm^2	15mW (@1.5GHz)
JSSC'10 [4]	Arbitrary	Digital Delay-Line	20.5dB (6%) (@750MHz)	180 MHz ~ 1.27 GHz	65nm	0.044 mm^2 (excluding PLL)	44mW (@1.27GHz) (excluding PLL)
TVLSI'11 [5]	Division triangular	All-Digital	15dB (10%) (@27MHz) 9.2dB (1%) (@54MHz)	27 MHz ~ 54 MHz	0.18µm	0.156 mm^2	1.2mW (@54MHz)

achieve the same EMI reduction. The power consumption of the proposed ADSSCG is 229µW at 207MHz. Moreover, the proposed ADSSCG has a good portability. Therefore, it is very suitable for system level integration in SoC era.



(a)



(b)

FIGURE 8. SIMULATED SPECTRA OF (a) 270MHZ WITH 1.3% SPREADING RATIO AND (b) 162MHZ WITH 0.45% SPREADING RATIO.

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