An All-Digital On-Chip Jitter Measurement Circuit in 65nm CMOS technology

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***Abstract* — An all-digital built-in jitter measurement (BIJM) circuit is presented in this paper. A frequency divider is taken as a timing amplifier to linearly amplify the input jitter. Subsequently, a vernier ring oscillator (VRO) is used as a time-to-digital converter (TDC) to quantize the jitter information into digital codes. The proposed self-referred architecture with a cycle-controlled delay line doesn't require an external reference clock to measure the jitter of the on-chip signals. Therefore, the BIJM circuit design complexity is greatly reduced by the proposed architecture. The proposed all-digital BIJM is implemented in a 65nm CMOS process, and the input frequency range is 100MHz to 300MHz.**

***Index Term* — clocks, jitter, oscillator, vernier ring oscillator.**

I. INTRODUCTION

Phase-locked loops (PLLs) play an important role in system-on-a-chip (SoC) design. PLLs are widely used for on-chip high-speed clock generation. In a SoC, there are many PLLs placed on the chip to produce various clock rates for memory and I/O interfaces. If one PLL doesn't work correctly, it may lead to the overall system failure. Therefore, the stability of the PLL is very important. The jitter performance is one of the most important characteristics of the PLL. However, the run-time jitter performance of the PLL, which affected by power supply noise, substrate noise and wire crosstalk effects, is often not predictable. In addition, since there are many PLLs on the chip, it is not easy to measure the run-time jitter performance of the on-chip PLLs by off-chip jitter measurement instrumentations. Moreover, the PLL's output frequency is often higher than I/O pad speed limitations. Therefore, in prior studies, many jitter measurement techniques are proposed [2-9].

Traditionally, many equipments such as a real-time sampling oscilloscope, a spectrum analyzer and other dedicated jitter measurement instrumentations are required to measure the clock jitter. These techniques are known as the off-chip jitter measurement. However, the ground bounce caused by the I/O pad transitions affects the accuracy of the off-chip jitter measurement. Moreover, it needs to wait a long time to collect the jitter data. Additionally, the cost to use these equipments is very expensive.

In recent years, many built-in jitter measurement (BIJM) circuits are proposed [2-9] to measure the jitter performance of the PLL. Fig. 1 shows the concept of a built-in jitter measurement circuits. It is composed of a timing amplifier (TA) circuit and a time-to-digital converter (TDC). The PLL's output clock (Test_Clock) and an ideal reference clock are inputted to the BIJM circuit. The timing difference between the test clock and the reference clock caused by the jitters is amplified and then converted into digital codes. The timing amplifiers (TAs) are proposed in [8, 9] to amplify the input jitter. The linearity of the timing amplifier is very important to obtain a precise jitter measurement results. Moreover, the TDC resolution also affects accuracy of the jitter measurement.

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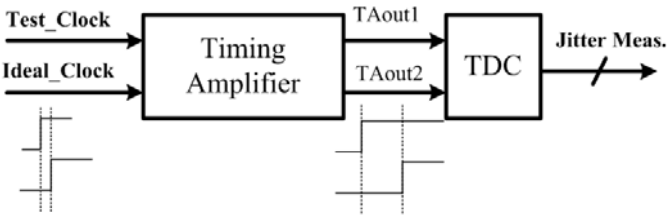

FIGURE 1. The concept of a BIJM circuit.

The time-to-digital converter (TDC) with a veriner delay line (VDL) is proposed in [2, 4, 6] for the on-chip jitter measurement. The veriner delay line structure uses two delay lines with different tapped delay to improve the resolution of the TDC, as shown in Fig. 2. The resolution of the TDC is equal to (T1 – T2) in VDL structure. Nevertheless, the TDC with VDL structure has a large area overhead and high power consumption, especially when the range of the input pulse width becomes wider. Therefore, a vernier ring oscillator (VRO) structure is proposed in [7, 8] to reduce the area overhead. In the VRO architecture, it uses two pairs of ring oscillators to quantize the pulse width information into digital codes. The vernier ring oscillator (VRO) structure can reduce the area cost of the TDC. Therefore, it is suitable for a built-in jitter measurement (BIJM) circuit design.

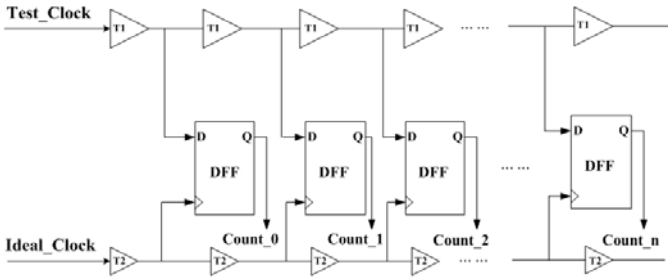

FIGURE 2. The time-to-digital converter with vernier delay line.

In prior built-in jitter measurement (BIJM) circuits [4, 5], an external reference clock is needed to measure the jitter performance of the PLL. In fact, it is very difficult to have a jitter-free clock as a reference clock input. Therefore, the self-referred structure [6-8] is proposed to avoid using an external reference clock. In the self-referred structure, a reference clock is generated from the test clock. The most popular self-referred structure uses a one-period delay circuit to produce the required reference clock. However, the input frequency range of the BIJM circuit is restricted by the range of the delay line.

In this paper, a frequency divider is taken as a timing amplifier to linearly amplify the input jitter. The TDC with VRO architecture is applied to the proposed BIJM circuit to quantize the jitter information into digital codes. The proposed self-referred architecture with a cycle-controlled delay line can reduce the area cost and improve the input frequency range of the BIJM circuit.

This paper is organized as follows. Section II describes the overall architecture of the proposed built-in jitter measurement (BIJM) circuit. The implementation of the proposed design is discussed in Section III. Section IV shows the experimental simulation results of the proposed design. Finally, Section V concludes with a summary.

II. Overview Architecture

A timing amplifier (TA) in a built-in jitter measurement (BIJM) circuit is used to amplify the input jitter. Hence, the accuracy of the jitter measurement can be further improved. However, the analog timing amplifiers (TAs) [8, 9] often have a very small linear region and this linear region is affected by process, voltage and temperature (PVT) variations. Therefore, a post-silicon calibration is often needed to improve the linearity of the timing amplifier (TA), and the calibration cost increases the total cost of the BIJM circuit.

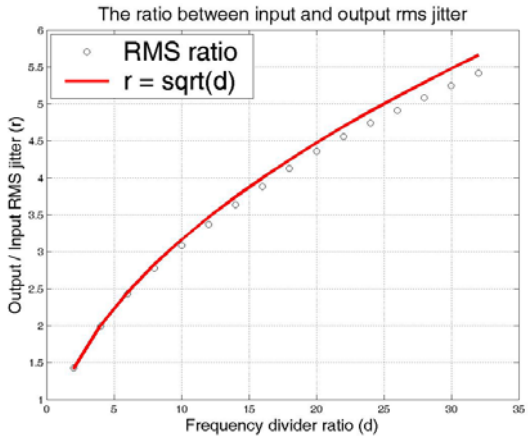

FIGURE 3. The output rms jitter with different divider ratio.

The measured jitter histogram of the PLL's output clock usually looks like a normal distribution random variable. The root-mean-square (rms) value and the peak-to-peak value are the two important parameters of the jitter histogram. In this paper, a frequency divider is used to replace the analog timing amplifier (TA) circuit to amplify the input jitter. When a clock with jitters is inputted to a frequency divider, the output jitter will become larger than the input jitter. Fig. 3 shows the simulation results of the ratio (r) of the output rms jitter value divided by input rms jitter value with different divider ratio (d). The relationship between the ratio (r) and the divider ratio (d) can be modeled as $r = \sqrt{d}$. The simulation shows that when the divider ratio (d) is smaller than 16, the tend line ($r = \sqrt{d}$) is close to the simulation value. Compared with the analog timing amplifier, the frequency divider is a simple digital circuit, and it is easy to be implemented with standard cells. Thus, the design complexity of the timing amplifiers can be greatly reduced by the proposed architecture.

The block diagram of the proposed all-digital built-in jitter measurement (BIJM) circuit is shown in Fig. 4. It is composed of a frequency divider, a self-refereed circuit, a vernier ring oscillator (VRO), a phase detector and a 10-bit counter. The proposed architecture uses a vernier ring oscillator (VRO) [7, 8] as a time-to-digital converter. In addition, a frequency divider with a fixed divider ratio (16) is taken as a timing amplifier to amplify the input jitter. In Fig. 4, the test clock (CLK) is divided by the frequency divider and then outputs as DIV_CLK. Subsequently, the self-referred circuit generates a one-period delayed test clock as a reference clock. Then, the DIV_CLK is outputted as the START signal, and the one-period delayed DIV_CLK is outputted as the STOP signal for the VRO circuit. The START signal triggers the Vernier oscillator 1 and the STOP signal triggers the Vernier oscillator 2. In the vernier ring oscillator (VRO) circuit, the oscillation frequency of the OSC1 should be slower than the OSC2. The phase detector (PD) is used to detect when the OSC2 signal catch up the OSC1 signal. When the PD detects the change of the phase polarity, the reset signal (M_RESET_) is sent to the self-referred circuit, and the self-referred circuit will produce the START signal and the STOP signal again for the next jitter measurement. The 10-bit counter records the cycle number of OSC2 until the OSC1 lags behind the OSC2. The counter value (COUNT) is the measured jitter result. The resolution (R_{VRO}) of the proposed VRO circuit is the period difference between the Vernier oscillator 1 and the Vernier oscillator 2.

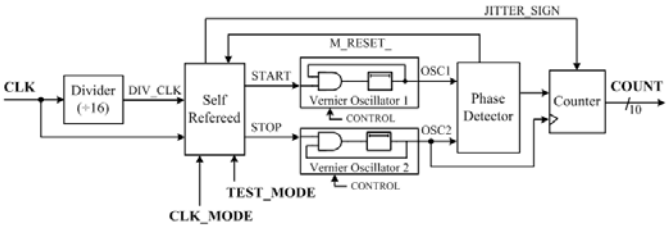

FIGURE 4. The proposed all-digital BIJM circuit.

The resolution (R_{VRO}) of the VRO circuit varies with process, voltage and temperature (PVT) variations. Thus, the counter value can not be directly used as the jitter measurement results unless the resolution of the VRO circuit (R_{VRO}) is known. The calibration process to the VRO circuit is needed before the jitter measurement, and the signal CONTROL can be used for the calibration process.

The proposed all-digital built-in jitter measurement (BIJM) circuit has two operation modes, the calibration mode and the normal mode, and the mode selection control pins are the CLK_MODE and TEST_MODE of the self-referred circuit. The calibration mode is used to obtain the resolution (R_{VRO}) of the VRO circuit with a known input test clock (CLK) frequency, and the resolution (R_{VRO}) of the VRO circuit can be adjusted by the CONTROL signal if needed. Then, in the normal mode, the BIJM circuit measures the jitter of the input test clock (CLK), and the output counter value can be used to calculate the jitter.

III. Circuit Implementation

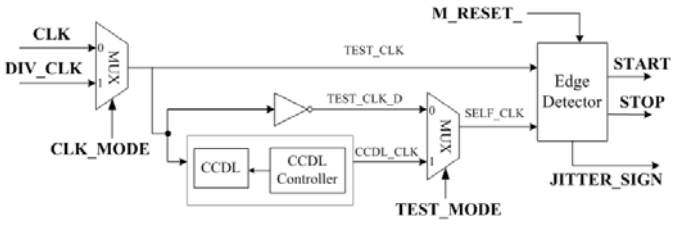

FIGURE 5. The proposed self-referred circuit.

The detail block diagram of the proposed self-referred circuit is shown in Fig. 5. In the calibration mode, the CLK_MODE is set to "0" and the TEST_MODE is also set to "0". Thus, the test clock (CLK) with a known frequency is inputted to the self-referred circuit as the TEST_CLK, and the inverted TEST_CLK is connected to the SELF_CLK. In addition, the TEST_CLK is outputted as the START signal and the SELF_CLK is outputted as the STOP signal. The timing difference between the START signal and the STOP signal is one half of the test clock (CLK) period in the calibration mode. Then, the VRO circuit can quantize the timing difference between the START signal and the STOP signal to obtain the counter value for

one half of the test clock (CLK) period. Thus, the resolution (R_{VRO}) of the VRO circuit can be calculated by Eq. 1.

$$R_{VRO} = \frac{T}{2} \times \frac{1}{|256 - N_{cal}|} \qquad (1)$$

where T is the period of the input test clock (CLK), N_{cal} is the mean of the counter values, and R_{VRO} is the resolution of the VRO circuit. In other words, it means the period difference between the Vernier oscillator 1 and the Vernier oscillator 2.

After the calibration is done, in the normal mode, the CLK_MODE is set to "1" and the TEST_MODE is set to "1". Thus, the divided clock (DIV_CLK) is inputted as the TEST_CLK. Subsequently, the TEST_CLK is delayed by one cycle and outputted as the SELF_CLK. The edge detector circuit detects the sign of the jitter, if the TEST_CLK leads the SELF_CLK, the output jitter is defined as positive. Therefore, the JITTER_SIGN signal is set to "0". Oppositely, if the TEST_CLK lags the SELF_CLK, the JITTER_SIGN is set to "1". If the JITTER_SIGN signal is set to "0", the TEST_CLK is outputted as the START signal and the SELF_CLK is outputted as the STOP signal. Otherwise, the SELF_CLK is outputted as the START signal and the TEST_CLK is outputted as the STOP signal. The timing difference between the START signal and the STOP signal is the input jitter. When the negative edge of the M_RESET_ is received, the edge detector is reset, and the self-referred circuit will produce the START signal and the STOP signal again for the next jitter measurement.

The initial value of the counter is set to "256" in each jitter measurement. If the JITTER_SIGN is set to "0", the counter will count upward until the negative edge of the M_RESET_ signal is produced. Oppositely, if the JITTER_SIGN is set to "1", the counter will count downward until the negative edge of the M_RESET_ signal is produced. The measured jitter is defined as Eq. 2.

$$J_i = |256 - N_i| \times R_{VRO} \qquad (2)$$

where J_i is the i-th value of the jitter, N_i is the i-th counter value and R_{VRO} is the resolution of the VRO circuit.

In the proposed all-digital built-in jitter measurement (BIJM) circuit, a frequency divider with a fixed divider ratio (16) is taken as a timing amplifier to amplify the input jitter. Although the jitter is amplified, the period of the test clock is also increased to 16 times of the original period. As a result, the cycle-controlled delay unit (CCDU) [10, 11] is used in the proposed self-referred circuit to reduce the area cost to generate a one-period delay. The cycle-controlled delay line (CCDL) is composed of a ring-oscillator and a counter. It utilizes the ring oscillator to generate a wide-range delay time.

IV. Experimental Results

The proposed all-digital built-in jitter measurement (BIJM) circuit is implemented in a standard performance (SP) 65nm CMOS technology. The layout of proposed circuit is shown in Fig. 6. It includes the cycle-controlled delay line (CCDL), the controller, the phase detector (PD), the frequency divider (Divider) and the two vernier ring oscillators (VROs). The core area is 0.01 mm^2, but the area occupied by the proposed all-digital BIJM circuit is 0.0027 mm^2. In addition, the gate count of the proposed all-digital BIJM circuit is 1749.

The input frequency range of the proposed design is from 100MHz to 300MHz. The timing diagram of the proposed BIJM circuit is shown in Fig. 7. In this case, the frequency of the input test clock is 125MHz. Thus, the divided frequency of the TEST_CLK is 7.8125 MHz. The initial value of the counter is 256. In this case, the TEST_CLK leads the SELF_CLK, the JITTER_SIGN is set to "0". The counter will count upward until the negative edge of the M_RESET_ signal is produced. As a result, the measured jitter value is equal to $9*R_{VRO}=((265-256)* R_{VRO})$.

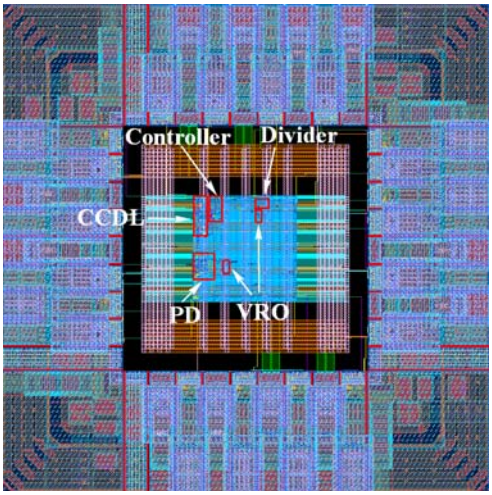

FIGURE 6. Layout of the proposed BIJM circuit.

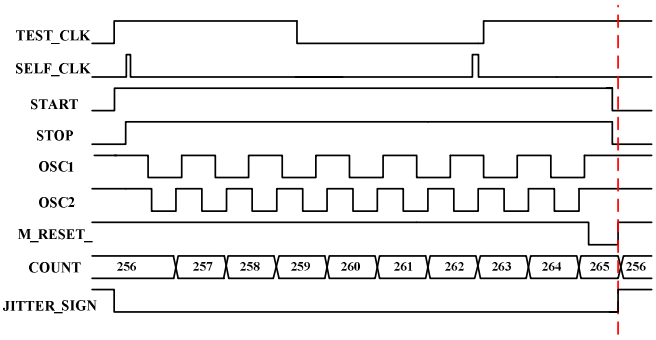

FIGURE 7. Simulation of the proposed BIJM circuit.

In the calibration mode, the frequency of the input clock signal is 125MHz with 1.2ns peak-to-peak jitter, and its period is 8ns. After the calibration, the mean of the counter values is 282.16. From the Eq. 1, we can obtain the resolution of the proposed VRO circuit is about 152.9ps. Thus, in the normal mode, the measured jitter value shown in Fig. 6 is equal to 1.376ns (=9* 152.9ps). Another example shows that the input jitter is 1.903ns, and the measured counter value is 243. Thus, the jitter value is equal to 1.987ns (=13*152.9ps). Thus, the error of the proposed all-digital BIJM circuit is about 4%.

The proposed all-digital BIJM circuit can not measure the jitter of the input clock at every clock cycle. When it starts to measure the jitter, it takes several cycles to calculate the jitter value. Thus, for on-chip jitter measurement applications, it still needs a long time to collect the jitter characteristic of the input clock.

The proposed all-digital BIJM circuit can solve the bottleneck of the analog circuit by replacing the timing amplifier with a frequency divider. Additionally, we use the cycle-controlled delay line (CCDL) to reduce the area cost to generate a one-period delay. Thus, the area cost and the power consumption of the proposed design can be further reduced.

TABLE I. COMPARISONS OF RECENT BIJM CIRCUITS

	This work	JSSC2006[4]	TIM2008[5]	TVLSI2009[6]	ISVLSI2005[7]	TVLSI2010[8]
Technology	65nm	90nm	0.18μm	90nm	0.18 μm	90nm
Architecture	TA (DIV), TDC (VRO)	TDC(VDL)	TDC	TDC(DL/VDL)	TDC(VRO)	TA, TDC(VRO)
Input frequency	100MHz ~300MHz	250MHz	1.25GHz	2.5GHz	100MHz	3GHz
Area (mm^2)	0.0027	0.24	0.09	0.075	0.004	0.038
Power (mW)	0.57mW @(100MHz)	N/A	40mW (@ 1.25GHz)	N/A	N/A	11.4mW (@ 3GHz)
RMS Jitter (oscilloscope/BIJM)	1.903/1.987*	2.03/2.0	5.45/6.25	10.1/6.2	42.7/62.7	4.15/3.78
Error	4%	1.5%	14.6%	39.0%	46.8%	8.9%
Self-reference	Y	N	N	Y	Y	Y

*：The input jitter model / BIJM

Table I. lists the comparisons of recent built-in jitter measurement (BIJM) circuit. In [4, 5], an external reference clock is needed to measure the jitter performance of the PLL. Thus, it is not suitable for the on-chip jitter measurement applications with many PLLs on a single chip. In addition, the analog circuit is easily affected by PVT variations. In [6, 8], the TDC with a vernier delay line (VDL) has a very limited input jitter range. In [7], the proposed architecture doesn't have a timing amplifier (TA), and the jitter measurement error is too large.

V. CONCLUSION

An all-digital built-in jitter measurement (BIJM) circuit which uses a frequency divider as a timing amplifier is presented in this paper. It can solve the bottleneck of the analog circuits with PVT variations. In addition, the cycle-controlled delay line (CCDL) is applied to reduce the area cost of the self-referred circuit. The proposed BIJM circuit uses the VRO architecture to reduce the error in jitter measurement. Thus, the proposed all-digital BIJM circuit is suitable for current on-chip jitter measurement applications in SoC era.

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