A 31.2mW UWB Baseband Transceiver with All-Digital I/Q-mismatch Calibration and Dynamic Sampling*

Jui-Yuan Yu, Ching-Che Chung, Hsuan-Yu Liu, Yu-Wei Lin, Wan-Chun Liao, Terng-Yin Hsu[2], and Chen-Yi Lee
Department of Electronics Engineering, National Chiao-Tung University, Taiwan R.O.C.[1]
Department of Computer Science and Information Engineering, National Chiao-Tung University, Taiwan R.O.C.[2]
Email: {blues,cylee}@royals.ee.nctu.edu.tw

Abstract

A MB-OFDM UWB baseband transceiver with I/Q-mismatch (IQM) calibration and dynamic sampling (DS) is presented. It calibrates IQM by 2dB gain and 20 degree phase errors, releasing IQM tolerance to 10x of existing designs. The DS reduces ADC sampling rate to 1/9 ~ 1/2 of existing designs, resulting in at least 43% ADC power saving. Measured power consumes 31.2mW at 480Mb/s data rate.

Keywords: carrier frequency offset, I/Q mismatch, OFDM.

Introduction

In ultra wideband (UWB) system, I/Q mismatch (IQM) from RF circuits degrades system packet error rate (PER) performance, and ADC circuit consumes about 50% analog front-end power (ADC×2+RF) [1][2]. For high IQM tolerance and ADC power saving, a Multi-Band OFDM (MB-OFDM) UWB baseband transceiver with digital IQM calibration and dynamic sampling timing controller (DSTC) is proposed here, comprising high performance and low power dissipation of wireless UWB applications.

For IQM calibration, we propose a signal-process-based design, which takes channel frequency response (CFR) and pilot signals for IQM estimation. It can compensate IQM under 2dB gain and 20 degree phase errors resulting in 3.1dB SNR saving for a typical 8% system PER. The proposed all-digital IQM calibration makes it possible to reduce RF power since the acceptable error range is enlarged to 10x of existing design [1] with 0.38mW power overhead by digital circuit. In existing wireless transceivers, ADC sampling frequency is over-sampled by a factor of 2x ~ 9x signal bandwidth [3], consuming at least 160mW×2 ADC power (I+Q). By the proposed DSTC and phase-tunable clock generator (PTCG), the sampling frequency is reduced to Baud rate, i.e. 1x signal bandwidth, resulting in 70mW×2 ADC power saving [2]. So, signals are sampled at their optimum timing, and system PER is improved by 2.3dB SNR. Therefore, the DSTC reduces ADC sampling rate and improves system performance with 1.9mW power consumption.

Proposed Architecture

Fig. 1 shows the proposed baseband transceiver. The transceiver achieves 53.3Mb/s ~ 480Mb/s data (de)modulation, including a mixed-radix 128-point FFT and divider-free channel equalizer for power saving [4-5]. This design also comprises synchronizer, IQM calibration, DSTC, and PTCG to solve the signal distortion caused by RF and channel effects. The all-digital PLL (ADPLL) generates 528MHz clock from 33MHz crystal, and PTCG generates 8-phase 528MHz clock for ADC and 1056MHz clock for DAC. It also generates 132MHz clock for baseband modules which achieve 528MS/s ~ 1056MS/s throughput with 4 ~ 8 parallel data paths. In the receiver path, the IQM calibration first bypasses received signals to the synchronizer. After packet detections, DSTC calculates preambles and gives Forward or Backward commands to PTCG. Each command results in ±236.7ps ADC clock phase shift to reach better signal sampling. After channel estimation in OFDM RX, IQM calibration extracts gain and phase errors from the estimated CFR and pilot values, and then compensates the IQM in the received signals.

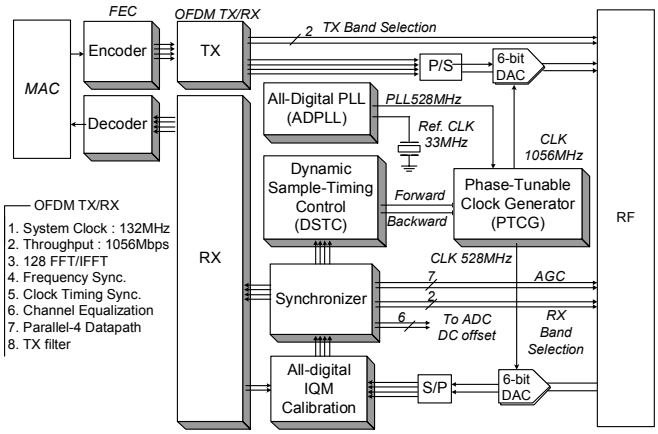

Fig. 1. System block diagram

Fig. 2 shows the architecture of IQM calibration circuit. With IQM effects, each OFDM subcarrier is interfered by the one from the symmetric index in spectrum, and the gain and phase values are thus distorted, resulting in non-square QPSK constellation. By this digital signal-process-based calibration, the transceiver automatically separates subcarrier interference and compensates signal distortion. To extract gain and phase errors, distorted pilots from two spectrum symmetric indices are subtracted from clean pilot values as shown in Fig. 2. Then the differences are compensated by estimated CFR, which is also IQM distorted. Therefore, a complex reciprocal is applied to eliminate this non-ideal channel estimation effect, and extracts the error parameters. For lower hardware cost, this reciprocal is also shared with IQM compensation circuit. The solvable IQM range with signals clipped by the 6-b I/Q ADC can be up to 2dB gain and 20 degree phase.

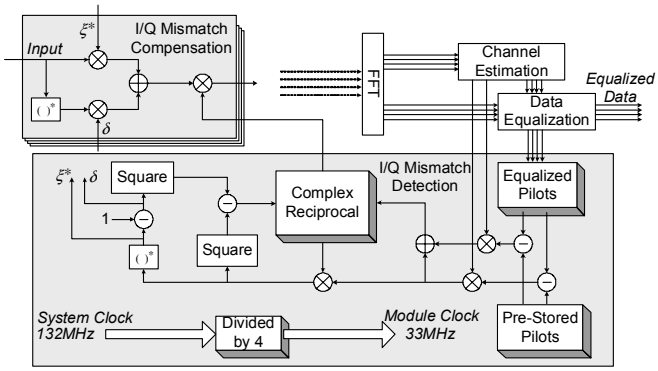

Fig. 2. Digital I/Q-mismatch calibration circuit

Fig. 3 shows the architecture of proposed DSTC. ADC sampling timing will lead or lag 236.7ps respectively according to DSTC and PTCG, and every Forward or Backward command is sent during band transitions. This guarantees each OFDM symbol is sampled from the same clock phase. To limit less than 0.3dB SNR differences in PER performance due to different sampling timing,

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each clock period is divided into 8 sampling phases. After packet detection, DSTC takes 9 OFDM symbols in preamble to determine whether a signal is sampled at eye-open positions. For each OFDM symbol, signals are correlated and accumulated by their differences. This correlation results in complexity reduction due to only calculate real numbers. As long as overflow or underflow flag occurs, a forced-decision is made to PTCG. This effectively reduces half hardware cost and computation time, resulting in less power consumption.

Fig. 4 shows the architecture of PTCG. This is an all-digital and cell-based design, thus it can reduce both design time and circuit complexity and ease the difficulty in system-level integration. The ADPLL generates 528MHz clock signal (PLL528) as PTCG's reference clock, and the PTCG generates 528MHz 8-phase even-spaced clock signals (P[0] to P[7]) for the phase rotator. Then the phase rotator changes ADC sampling phase from P[n] to P[n+1] or P[n] to P[n-1] with baseband DSTC's Forward or Backward commands respectively. To avoid extra transitions during phase rotation, the phase rotator converts the Forward command into seven times of Backward command. And the clock edge combiner is used to perform 2x frequency multiplication of PLL528 to generate 1056MHz clock for DAC. In the proposed PTCG, the TDC measures period (T) of PLL528 then limits the total delay line range into 2.5T to 3.5T, hence it avoids false-locked problem in PVT variations. The output clock of ADPLL has rms jitter: 26ps and P_K-P_K jitter: 89ps. After the all-digital multi-phase clock generator (ADMCG) and phase rotator in PTCG, the jitter performance for ADC sampling clock is rms jitter: 30ps and P_K-P_K jitter: 101ps. The PTCG consumes 10.9mW power.

Simulation and Measurement Results

The proposed MB-OFDM UWB baseband transceiver is fabricated in 0.13µm 1P8M CMOS process. Fig. 5 shows the measured data constellation and simulated 480Mb/s PER performances. With IQM calibration, data constellation becomes a square QPSK distribution. With DSTC, data distribution becomes more condensed. Fig. 6 shows the chip micro-photo and summary. Measured results show that the proposed design achieves maximum 480Mb/s data rate with 31.2mW power consumption. The power overhead is only 13.18mW with IQM calibration, DSTC, and PTCG, resulting in 5.4dB SNR improvement for typical 8% PER and 43.75% ADC power saving [2].

Acknowledgement

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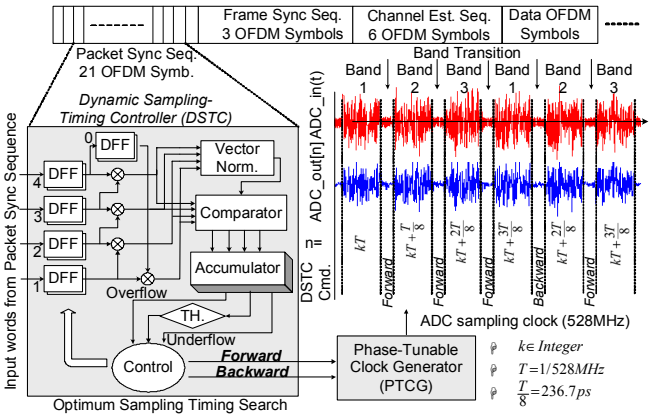


Fig. 3. Dynamic sampling-timing controller

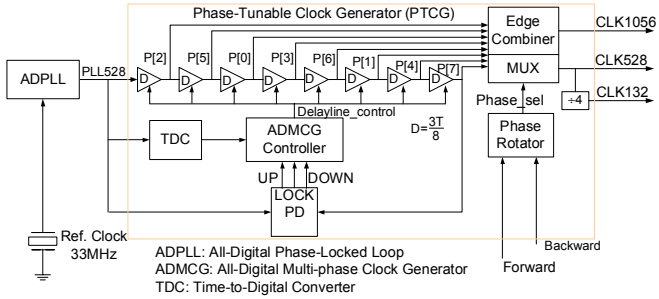


Fig. 4. The proposed phase-tunable clock generator

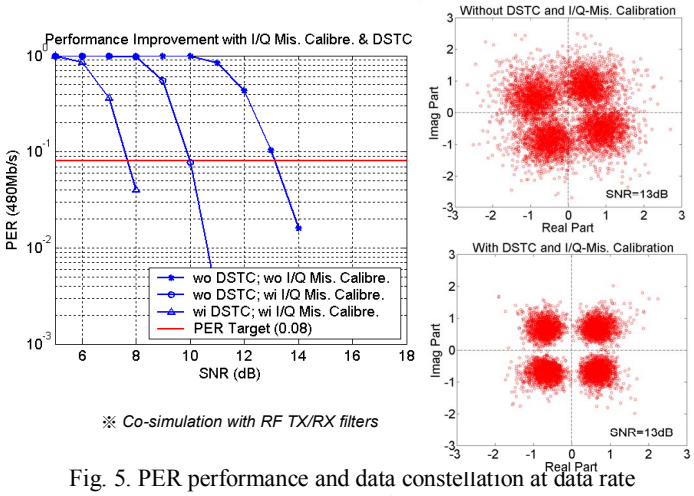
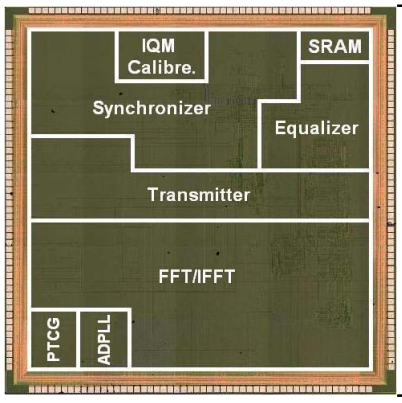


Fig. 5. PER performance and data constellation at data rate 480Mbps



Technology	Std. 0.13µm CMOS 1.2V core, 3.3V I/O
Die Size	3.975mm x 3.980mm
Package	208-pin CQFP
Transistor Count	2.25M
Max. Data Rate	480Mbps
Core power @ 480Mbps(Tx/Rx)	15.8/31.2mW
Gain Err. Tolerance	2 dB
Phase Err. Tolerance	20 degree
PTCG Resolution	236.7ps

Fig. 6. Chip micro-photo and chip summary