A COFDM Baseband Processor with Robust Synchronization for High-Speed WLAN Applications*

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Abstract

In this paper, a high-performance and low-cost COFDM baseband processor is presented. With algorithm exploration in channel estimation and phase error tracking, synchronization becomes more robust to enhance system performance. And better design SNR (1.35~7.16dB) can be achieved compared to current solutions. Moreover through architectural exploration, the proposed baseband processor designed in 0.18um CMOS process contains only 370K logic gates and 3.3Kbyte memory. Measurement results show that better hardware efficiency and performance enhancement is achieved for high-speed WLAN applications.

Key Words: COFDM, Synchronization, WLAN, channel estimation, phase error tracking.

I. Introduction

Coded Orthogonal frequency division multiplexing (COFDM) is widely applied in high-speed wireless local area network (WLAN) such as IEEE 802.11a, Hiperlan/2, and IEEE802.11g. It can enhance channel capacity and overcome multipath inter-symbol interference (ISI). In receiver, channel estimation (CE) and synchronization designs are exploited to solve the distortion issues from wireless channel model and uncertainty between transmitter and receiver [1-4]. However, these approaches demand more hardware and design complexity. For example, a programmable-coefficient channel interpolator was applied in [2] to overcome multipath fading. Although it achieves better 2.5 ~ 3.0dB gain in estimation mean-square-error (MSE) than the zero-forcing approach, it needs more hardware, including 18 parallel complex multipliers. Designing a novel CE to enhance system performance, and in the meantime, to save hardware cost with architectural exploration can solve such a problem. Another example is in [1], where the authors apply feedback phase error tracking (PET) with phase error prediction to overcome residuary CFO including phase noise and sampling clock offset (SCO) which cause constellation rotation in receiver. Although this approach achieves higher tracking range than feedforward PET, the phase error prediction is not robust to burst noise. This problem makes the system packet error rate (PER) become higher. Hence a more robust PET with low-cost tracking loop is demanded too.

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To solve the problems mentioned above, a high-performance and low-cost COFDM baseband processor comprising robust CE and PET methods is proposed in this paper. Simulation results show that our proposal achieves better design SNR for typical 10% PER and saves hardware cost than current 802.11a baseband processors. This paper is organized as follows. A low-cost architecture of baseband processor will be introduced in section II. The proposed high-performance and low-cost designs named CE and PET will be introduced in section III. Performance evaluation will be analyzed in section IV. Architecture design and test chip will be described in section V.

II. Signal Flow in Baseband Processor

Signal flow of the proposed COFDM baseband processor is shown in Fig. 1. After signal word-length is determined (include analysis of signal dynamic range and simulation of PER with possible word-length selection), baseband processor I/O connected to AD and DA are quantized as dual 10-bit I/Q in both transmitter and receiver. In the receiver data flow, first an all-digital AGC estimation detects RF amplifier gain error. Since received signal is quantized to dual 10 bits I/Q after AD, the tolerant AGC error can be ± 7dB in the short training sequence with only 2dB peak-to-average power ratio (PAPR). With this large error tolerance, AGC estimation can be implemented as an all-digital design composed of 1.6us coarse-tune and 3.2us fine-tune in the short training sequence. After coarse AGC tuning, RF amplifier gain error can be limited to ±3dB (< ±7dB as specified). Both the frame detection and CFO estimation can begin to detect valid packet and coarse CFO without any AGC degradation.

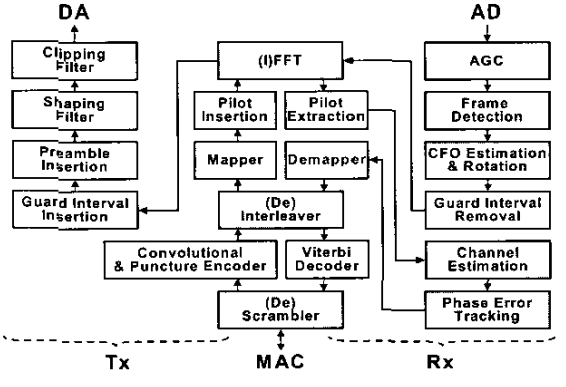

Fig. 1 Architecture of the proposed baseband processor

In low-cost design consideration, an auto-correlation circuit is shared by frame detection and CFO estimation. In the end of short training sequence, RF amplifier gain error will be limited to ± 1dB by fine AGC. The estimation accuracy is as high as analog-and-digital hybrid AGC [1]. In the long training sequence, phase error caused by estimated coarse CFO is compensated by CFO rotation. And then frame detection begins to detect OFDM symbol timing. Before long training sequence sent to FFT, fine CFO is estimated and then the phase error caused by estimated fine CFO is compensated. After guard-interval removal and FFT process in the long training sequence, CE begins to estimate channel frequency response (CFR).

In receiving of standard-defined Signal Field and data OFDM symbols. Every FFT symbol is rotated by CFO rotation and then sent to FFT. In frequency-domain, CE tracks and compensates CFR. PET tracks and then compensate the phase error caused by residuary CFO and SCO. After demapper, deinterleaver, Viterbi decoder, and descrambler, system parameters and data bits are sent back to MAC. To raise hardware efficiency of overall system, (I)FFT, (de)interleaver, (de)scrambler are shared by transmitter and receiver. This sharing scheme saves 18% of system memory.

III. High-Performance and Low-Cost Designs

A. Channel Estimation

The proposed CE scheme combines smoothing filter (SF) and decision-directed (DD) tracking. The block diagram of CE is shown in Fig. 2. In the initial estimation using the long training sequence, CFR is smoothed in SF to reduce additive noise. The proposed 5-tap SF is designed with fixed coefficients. Therefore main computation can be realized by bit-selection and adder (BSA) without any multiplier in low-cost design consideration.

In the data reception, DD tracking calculates an error vector caused by initial estimation error and then compensates it. The error vector function of DD tracking is described as equation (1). In equation (1), N is the OFDM symbol index; $X_{E,N}(k)$ is the received signal from PET; $X_{C,N}(k)$ is the compensated signal sent to demapper; ε_N is the predicted signal-to-error ratio, $X_{D,N}(k)$ is the demap vector; $X_{P,N}(k)$ is the predicted demap vector. The error vector added to received signal is described equal to $X_{P,N} \cdot \varepsilon_N$.

$$X_{C,N}(k) = X_{E,N}(k) + X_{P,N}(k) \cdot \varepsilon_N(k) \quad (1)$$

$$\text{Where } \varepsilon_N(k) = \begin{cases} 0 & , \text{ if } N = 1 \\ 1 - \left(1 - \frac{1}{N-1}\right) \cdot \varepsilon_{N-1}(k) - \frac{X_{E,N-1}(k) \cdot X_{D,N-1}(k)^{-1}}{N-1} & , \text{ Otherwise} \end{cases}$$

In the equation, calculation of $X_{D,N}(k)^{-1}$ is realized by a table-look-up (TLU)-based inverse design without any divider. In the TLU-based inverse design, the inversed vector of constellation points is pre-stored and then output according to input Demap vector. In equation (1), calculation of error vector is implemented with only 3 complex multipliers. The proposed DD tracking design saves 15 parallel complex multipliers compared to [2].

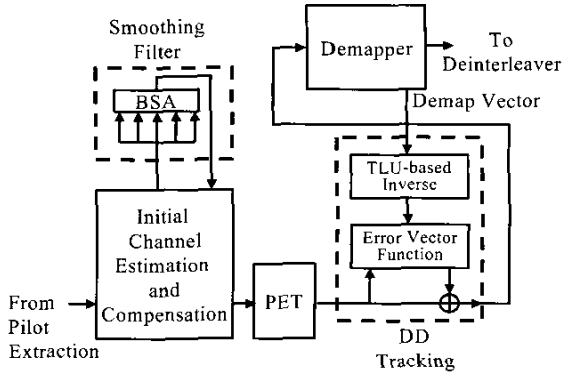

Fig.2 Block diagram of the proposed CE

B. Phase Error Tracking

The proposed PET combines both feedback pilot-compensation and feedforward data-compensation. In the conventional all-feedback PET, pilot and data carriers are all compensated with the feedback method [1]. In this conventional all-feedback architecture, phase error detection is needed to predict the phase error in the next OFDM symbol. However, phase error detection is not accurate enough because the phase error prediction easily fails due to joined burst noise. In the proposed PET, since the data flow can be revised to that all pilot carriers are sent in CE and PET first, the accurate feedforward data-compensation can be applied without any phase error prediction. The architecture of the proposed PET is shown in Fig. 3. In the proposed PET, phase error of data carrier is calculated from mean and linear phase error of pilot carriers in the same OFDM symbol. This method can compensate data carriers without any prediction. To eliminate high-frequency burst noise in tracking loop, low-cost fixed-coefficient loop filters are applying. They weight and average the phase error to reduce the degradation from noise. The tracking accuracy of the proposed PET design can be higher than conventional PET designs without use of loop filters. In the proposed PET, pilot and data carriers are compensated in a single complex multiplier. The proposed PET is designed to enhance the tracking accuracy with cost-save hardware design.

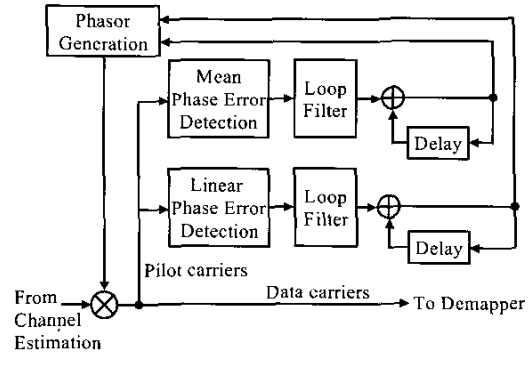

Fig. 3 Architecture of the proposed PET design

IV. Performance Analysis

A. *Channel Estimation Performance*

To analyze the performance of the proposed CE, MSE of CE is simulated in an exponentially decayed Rayleigh-fading channel model [5]. The channel impulse response (CIR) and CFR examples are shown in Fig. 4. Phase of CIR is uniform-distributed. The MSE curves simulated in multipath channel with 50ns RMS delay spread are shown in Fig. 5. Compared to the conventional zero-forcing approach, the proposed design achieves better 9 ~ 13dB gain in estimation MSE. It also achieves better 6 ~ 10.5dB gain in estimation MSE than the conventional channel interpolator [2] that only achieves better 2.5 ~ 3.0dB gain in estimation MSE than zero-forcing approach.

B. *Phase Error Tracking Performance*

To analyze the performance of the proposed PET, system PER of 54Mbits/s mode is simulated with 40ppm CFO effect including phase noise and 40ppm SCO effect. PER curves with different PET designs are shown in Fig. 6. Compared to the conventional PET design [1], the proposed PET design achieves better 1.94dB gain in SNR for 10% PER. The applied loop filters and feedforward data-compensation enhance system performance and overcome phase noise more efficiently.

C. *System Performance*

Performances of AGC, Frame detection, CFO estimation and PET are shown in Fig.7. AGC root-mean-square-error (RMSE) is less than 1dB when SNR is larger than 8.5dB. Frame error rate (FER) is lower than 10^{-3} when SNR is larger than 5dB. CFO tolerance is raised to ±60ppm (total -120 ~ 120ppm between Tx and Rx), equal to 3 times of standard requirement. SCO tolerance is raised by PET to ±25ppm (total -50 ~ 50ppm between Tx and Rx) and satisfies standard requirement (±20 ~ ±25ppm). PER curves are shown in Fig. 8. And the design SNR for 10% PER is listed in Table 1. Compared to standard requirement and current approaches [1][3], the proposed baseband processor achieves better 1.35 ~7.16dB SNR on the average.

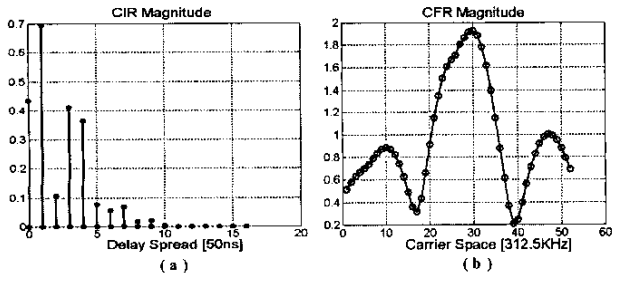

Fig. 4 (a) CIR (b) CFR examples of the applied channel model

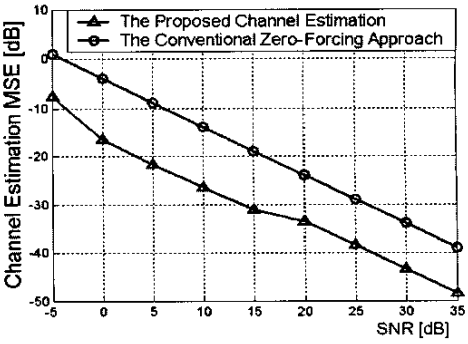

Fig. 5 MSE of the proposed CE

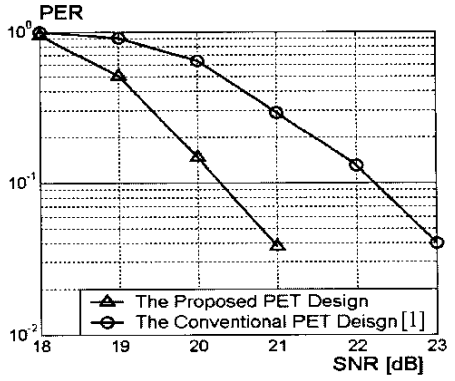

Fig. 6 PER curves of 54Mbits/s mode with PET designs

V. Chip Implementation

Based on the proposed techniques and low-power FEC design [6], a COFDM baseband processor compliant to IEEE 802.11a was designed using 0.18um standard CMOS process and tested completely. The microphoto is shown in Fig. 9 with features listed in Table 2. The proposed low-cost baseband processor only contains 370K logic gates and 3.3Kbytes memory, which is less than the solution proposed in [4].

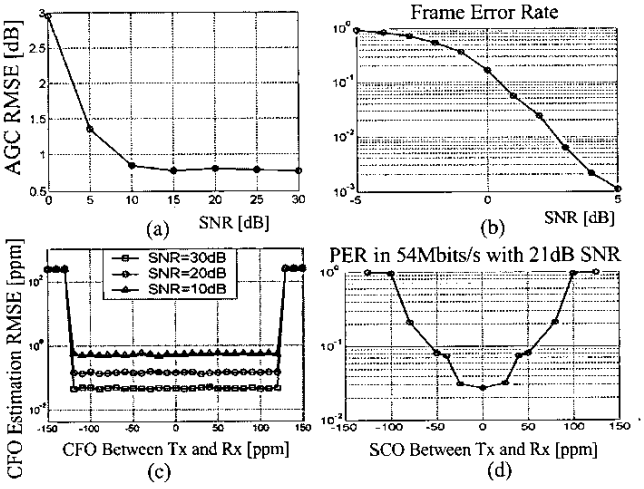

Fig. 7 Performance of synchronization designs:
(a) AGC RMSE (b) FER (c) CFO tolerance (d) SCO tolerance

Table 1 Design SNR for 10% PER

Data Rate (Mbits/s)	The Proposed Design SNR (dB)	Design SNR [1] (dB)	Design SNR [3] (dB)	IEEE 802.11a Requirement
6	2.5	4.9	5.4	9.7
9	4.0	5.8	5.8	10.7
12	5.2	8.6	7.0	12.7
18	7.4	9.9	9.5	14.7
24	10.1	12.4	11.3	17.7
36	14.2	15.9	14.9	21.7
48	18.6	20.3	18.6	25.7
54	20.3	21.7	20.6	26.7
Average gain [dB]		2.15	1.35	7.16

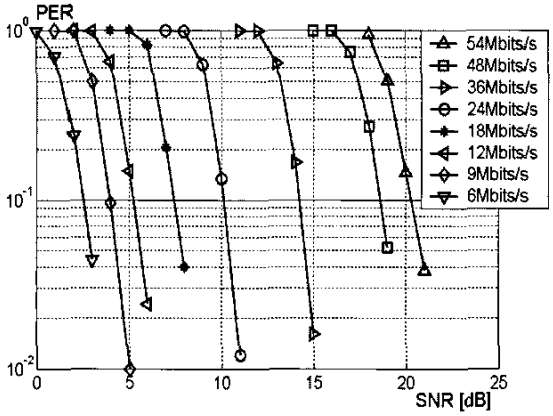

Fig. 8 Design PER of the proposed baseband processor

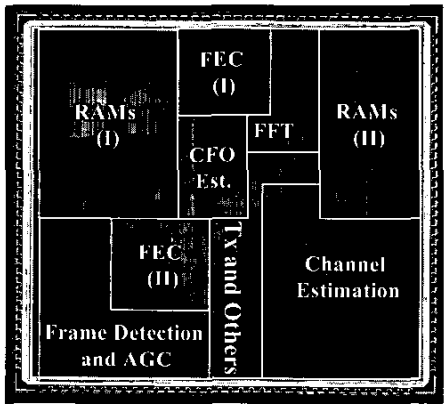

Fig. 9 Chip microphoto

Table 2 Chip feature

Technique	0.18um CMOS, 1P6M
Transistor Count	2.1M (Include I/O)
Package	144-pin CQFP
Core Size	3.8 x 3.8 mm^2
Clock Speed	80MHz
Supply Voltage	1.8V Core, 3.3V I/O
Core power at 54Mbits/s (Tx/Rx)	52.4mW/123.5mW
I/O Power	61mW

VI. Conclusion

A high-performance and low-cost COFDM baseband processor is proposed to improve hardware efficiency and system performance for high data rate WLAN. Applying low-cost hardware architecture, channel estimation, and PET, the baseband processor only contains 370K logic gates and 3.3Kbytes memory. It saves (i) 18% memory space by hardware sharing and (ii) 15 parallel complex multipliers by novel channel estimation scheme. Applying the channel estimation combining SF and DD tracking, the proposed baseband processor achieves better (i) 9 ~ 13dB gain in CE MSE than the conventional zero-forcing approach (ii) 6 ~ 10.5dB gain in CE MSE than the conventional channel interpolator. Applying the PET combining feedback pilot-compensation and feedforward data-compensation, the proposed baseband processor achieves better 1.94dB gain in SNR for 10% PER than the all-feedback PET approach. Based on the proposed techniques, the proposed design can achieve 1.35~7.16dB SNR gain than conventional solutions.

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