An All-Digital Built-in Self-Test Circuit for ADPLLs in 65nm CMOS Technology

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ABSTRACT

This paper presents the design of an all-digital built-in self-test (BIST) circuit for all-digital phase-locked loops (ADPLLs). It measures clock jitter of the ADPLL and tests the PLL function blocks. The BIST circuit does not break the PLL loop. The jitter measurement circuit takes a frequency divider as a timing amplifier to linearly enlarge the input jitter. The vernier ring oscillator-based time-to-digital converter quantizes the jitter into digital codes, and the cycle-controlled delay line generates a self-test clock which avoiding using an external reference clock. The proposed BIST circuit for jitter measurement was implemented with standard cells and fabricated in 65nm CMOS process. The measured jitter error is about 11.32% with input frequency range 100-300MHz.

1. INTRODUCTION

Phase-locked loops (PLLs) are widely used for high-speed clock generation, clock and data recovery (CDR), frequency synthesis and clock de-skew applications. It plays an essential role in system-on-a-chip (SoC) design, and there are usually many PLLs integrated on the SoC to provide various frequencies for different I/O interfaces. Nevertheless, if one of the PLLs does not work correctly, it may lead to system failure. Hence, it is essential to examine the function and jitter performance of these PLLs using the built-in self-testing (BIST) circuit. Moreover, the BIST circuit should not affect the performance of the PLLs.

The jitter performance is one of the most important characteristics of the PLLs. Moreover, the run-time jitter is easily affected by power supply noise, substrate noise, and wire crosstalk effects. As a result, it is difficult to measure run-time jitter performance of the PLLs by off-chip jitter measurement instruments. Hence, the built-in jitter measurement (BIJM) circuits are proposed in [1-5]. Most of the BIJM circuit is composed of a timing amplifier circuit and a time-to-digital converter (TDC) circuit. The timing amplifiers are used to enlarge the jitter of the input clock, and then the TDC converts measured jitter into digital codes. However, the linearity of the timing amplifiers and the resolution of the TDC circuit would affect the accuracy of the jitter measurement circuits.

Among TDC circuits, the delay line (DL) circuits [3] and the vernier delay line (VDL) structures [2] are utilized to measure the jitter information. However, the area of those circuits is quite large. The vernier ring oscillator (VRO) circuits are proposed to reduce the area overhead. Besides, most built-in jitter measurement circuits need a jitter-free clock as the reference clock to the BIJM circuit. In fact, it is difficult to have a jitter-free clock frequency. The self-referred circuit is utilized to avoid using an external reference clock. The one-period delay structure is the most popular approach to generate the reference clock. However, the frequency range of the input clock is restricted by the delay range of a delay line. Most one-period delay structure occupies large chip area to achieve wide input frequency range.

This paper is organized as follows: the proposed BIST circuit with the BIJM circuit is presented in Section 2. The experimental results are discussed in Section 3 with a summary.

2. PROPOSED BIST CIRCUIT

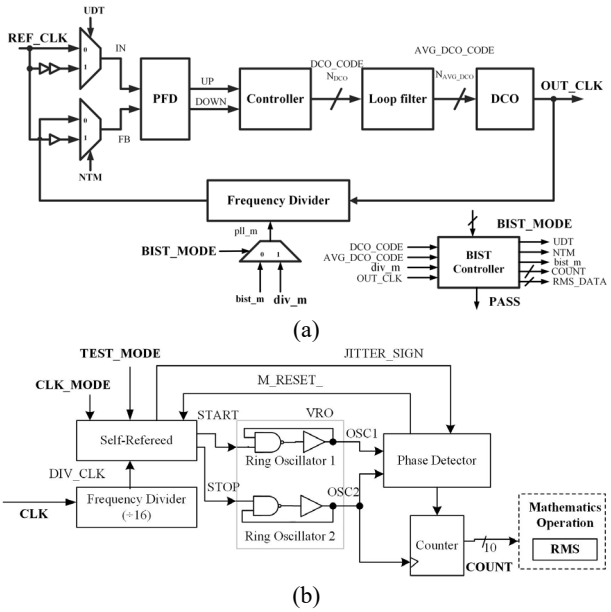

Fig. 1 (a) Proposed BIST circuit (b) BIJM block diagram

The proposed BIST circuit with an ADPLL is shown in Fig. 1(a), and the output clock (OUT_CLK) will connect to the proposed BIJM circuit which shown in Fig. 1(b) to measure the jitter performance. Three multiplexers, a BIJM circuit, and a BIST controller are added to an ADPLL, and BIST_MODE sets the testing mode of the BIST circuit. In phase and frequency detector (PFD) testing mode, the signals UDT and NTM can set that the IN signal lags the FB signal or leads the FB signal. Then, the output of the ADPLL controller (DCO_CODE) will always be decreased or increased according to the PFD output signals (i.e., UP and DOWN). From the change of the DCO control code, the BIST controller can determine whether the ADPLL controller and the PFD operate correctly. If the ADPLL cannot pass this test, the PASS signal will be pulled low.

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In the frequency divider testing mode, the BIST controller needs to wait until the ADPLL is locked. Then, the BIST controller reduces the divide ratio to make the frequency of the FB signal faster than the IN signal. Subsequently, the output of the ADPLL controller (DCO_CODE) will be increased accordingly. Oppositely, if the BIST controller increases the divide ratio, the frequency of the FB signal will be slower than the IN signal. The output of the ADPLL controller will be reduced. If the ADPLL cannot pass this test, the PASS signal will also be pulled low. After these tests, the function of the ADPLL is checked, and the PASS signal will be pulled high.

As shown in Fig. 1(b), the proposed BIJM circuit takes the frequency divider as a timing amplifier to amplify the input jitter and solve the non-linearity problem of analog timing amplifiers. Then, the jitter performance of the ADPLL will become easier to be measured. If the root-mean-square (RMS) jitter ratio between the divided clock and the original clock is *r*, and the divider ratio is *d*, the relationship between the ratio (*r*) and the divider ratio (*d*) can be modeled as $r = \sqrt{d}$ [6]. Compared with the analog timing amplifier, the structure of frequency divider is a simple digital circuit, and it is easy to be implemented with standard cells.

In the proposed BIJM circuit, the self-refereed circuit produces a clock with the delay time that is set to one period of the input clock. Subsequently, the self-refereed circuit chooses the beginning and end measurement point, namely "START" and "STOP" signals for the vernier ring oscillator. The START signal enables the oscillation of the upper ring oscillator, and the STOP signal enables the oscillation of the lower ring oscillator. The oscillation frequency of the upper ring oscillator should be slower than the lower ring oscillator. Then, the phase detector (PD) detects when the phase of the OSC2 signal catches up with the OSC1 signal, and the 10-bit counter circuit records the cycle value to supply the math block to calculate the RMS jitter value. When the PD detects the change of the phase polarity, the reset signal is sent to the self-refereed circuit for the next jitter measurement.

For the calibration of the proposed BIJM circuit, in the beginning, the timing difference between the START signal and STOP signal is set to one half of the known input clock period, and then the resolution of the vernier ring oscillator can be determined. The cycle-controlled delay line (CCDL) structure [7] is used in the proposed BIJM circuit to reduce the area overhead for one-period delay reference clock generation. Moreover, the moving average method is applied in the mathematic operation block for calculation of the mean of the jitter value.

3. EXPERIMENTAL RESULTS

The test chip is implemented with standard cells and fabricated in 65nm CMOS technology. The test chip didn't include the mathematics operation circuit, and it has 4-bit control to adjust the resolution of the BIJM circuit. The core size is 0.01 μm^2, and the gate count of the proposed BIJM circuit is 1,749. The input clock frequency range is restricted by the delay range of the cycle-controlled delay line (CCDL) and the speed limitations of the I/O pads. The frequency range of the test chip is from 100MHz to 300MHz.

Fig. 2 shows the measured jitter histogram by the oscilloscope and the test chip. In Fig. 2, the input clock frequencies are 142 MHz and 200MHz, and the divided clock frequencies to the BIJM circuit are 8.875MHz and 12.5MHz, respectively. The RMS jitter of the divided clock is 90.05ps that measured by the oscilloscope, and the test chip measured RMS jitter is 77.753ps. The measured error is about 13.7%. For 200MHz input clock, the RMS jitter of the divided clock is 89.388ps that measured by the oscilloscope, and the test chip measured RMS jitter is 99.43ps. The measured error is about 11.23%.

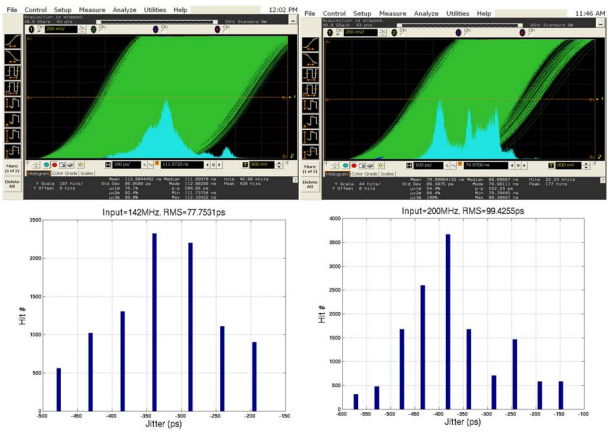

Fig. 2 Measured jitter histogram of the proposed BIJM circuit at 142MHz and 200MHz

The proposed BIST circuit with the BIJM circuit can test the function of the ADPLL. The proposed BIJM circuit which has relatively small area and low error is suitable for on-chip jitter measurement. Moreover, the proposed BIST circuit can be implemented with standard cells. Therefore, the proposed BIST circuit is suitable for testing the function and jitter performance of the integrated ADPLLs in the SoC.

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