An All-Digital On-Chip Voltage Sensor for SoC Design

Ching-Che Chung, Mei-I Sun, and Yi-Che Tsai

Department of Computer Science and Information Engineering, National Chung Cheng University,
No. 168 University Rd., Min-Hsiung, Chia-Yi, Taiwan.

ABSTRACT

Due to the high level integration of the system-on-a-chip (SoC), it becomes more and more important to monitor the IR drop of the power network during chip operation. In this paper, an all-digital on-chip voltage sensor which uses a relative reference modeling (RRM) is presented. After one-point calibration at 1.1V, the proposed all-digital voltage sensor can monitor the operating voltage of the chip and outputs digital codes for SoC chip debugging and testing. The proposed all-digital voltage sensor is implemented in 90nm CMOS process. It achieves a 0.027mV resolution and has a maximum error 16.4mV with process, voltage, and temperature (PVT) variations.

1. INTRODUCTION

Nowadays, the high level integration of the system-on-a-chip (SoC) causes that the voltage transients (IR drop) issue of the power network becomes more serious and unpredictable. IR drop may lead to unexpected performance degradation to the chip. As a result, on-chip voltage sensors which are placed in different locations of the SoC can provide useful diagnosis information to the chip designer for chip debugging and testing. Most of the current on-chip voltage sensors [1],[3] require the calibration process to map the measured analog voltage values into digital codes. However, the process, voltage, and temperature (PVT) variations affect the relationship between the measured voltage values and the output digital codes. Thus, the voltage sensor [1] needs to execute the calibration process periodically (e.g. every 1ms) for compensation for temperature variations. In addition, in each calibration process, it also requires three input reference voltages (0.8V, 0.9V, and 1.0V) for 2nd-order polynomial regression which makes the voltage sensor [1] not easily applicable for SoC design.

The voltage sensor [3] also requires three different input reference voltages for sensor calibration. Each on-chip voltage sensors are calibrated individually, and the process variation of the voltage sensor is normalized after calibration. However, the error of the voltage sensor will be increased accordingly with temperature variations after chip calibration since the calibration for each voltage sensor is performed once. The voltage sensor [2] requires adjusting the input voltage of the controllable delay block of the voltage sensor with PVT variations. However, when the operating conditions are changed, this calibration process for the proposed sensor needs to be performed again. Or the operation of the voltage sensor may be not worked correctly.

In this paper, an all-digital voltage sensor which uses a relative reference modeling (RRM) is presented. After one-point calibration at 1.1V, the proposed all-digital voltage sensor can determine the process variation of the voltage sensor and compensates for the process variations. After that, the proposed temperature sensor can measure the temperature variations and compensates for the temperature variations. Finally, the linear calculator of the proposed all-digital sensor converts the measured voltage values to digital codes. The proposed all-digital voltage sensor achieves a 0.027mV resolution and has a maximum error 16.4mV with PVT variations after one-point calibration.

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2. PROPOSED VOLTAGE SENSOR

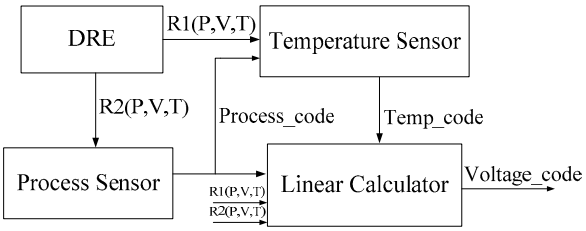

Fig. 1 Proposed all-digital voltage sensor.

The architecture of the proposed all-digital voltage sensor is shown in Fig. 1. The proposed all-digital voltage sensor consists of a delay ratio estimator (DRE), a process sensor, a temperature sensor, and a linear calculator. The delay ratio estimator consists of three ring oscillators which were made of different delay cells. The delay ratio is the ratio of the propagation delay time between two delay cells and was defined in [4]. The DRE [4] can compute the delay ratios among three delay cells and outputs as R1(P,V,T) and R2(P,V,T), respectively.

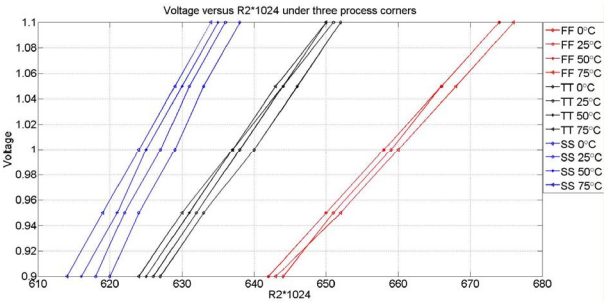

Fig. 2 Simulated R2(P,V,T) curves.

We need to perform many SPICE simulations to obtain the delay ratios with PVT variations. In addition, we can change the delay cells in the DRE to obtain the desired delay ratio characteristics. Fig. 2 shows the simulated R2(P,V,T) curves. The desired R2(P,V,T) characteristic is that the values of R2(P,V,T) at 1.1V are not overlapped in different process corners. Therefore, the simulated values of R2(P, V, T) can be used to identify the process variations of the voltage sensor when the process variation is unknown. For example, after

chip fabrication, if we calibrate the chip at 1.1V, and R2(P, V, T)*1024 is 670. Then, the value of R2(P, V, T) is close to the simulated FF process corner. Therefore, the proposed process sensor can determine that the voltage sensor is at FF process corner.

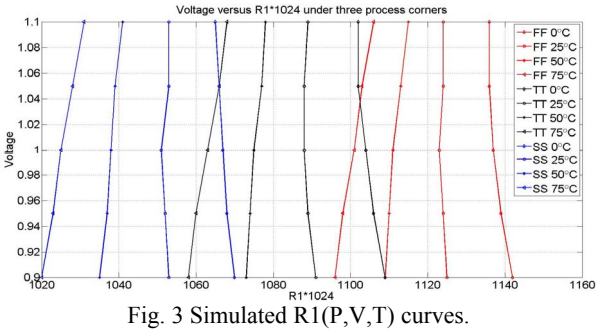

Fig. 3 Simulated R1(P,V,T) curves.

Fig. 3 shows the simulated R1(P,V,T) curves. The desired R1(P,V,T) characteristic is that at each process corner (TT, SS, FF), the values of R1(P,V,T) at different temperature are not overlapped. Therefore, the simulated values of R1(P, V, T) can be used to identify the temperature variations of the voltage sensor when the temperature variation is unknown. For example, after chip was calibrated at 1.1V, the process corner is known as SS process corner. If R1(P, V, T)*1024 is 1040. Then, the value of R1(P, V, T) is close to the simulated condition at 50°C. Therefore, the proposed temperature sensor can determine that the voltage sensor is at 50°C.

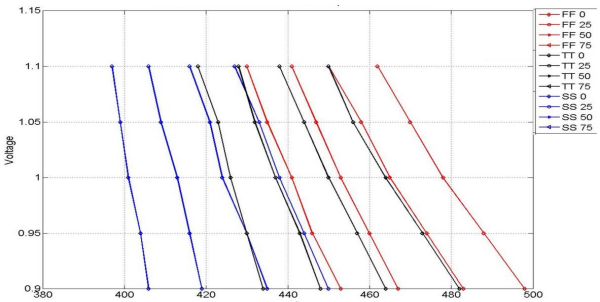

Fig. 4 Simulated (R1 - R2)/R1*1024 curves.

In the proposed all-digital voltage sensor, the relationship between the measured voltage values and the output digital codes are fixed even with PVT variations. Fig. 4 shows the simulated (R1 - R2)/R1 curves. In each process corner, at different temperature, the relationship between (R1 - R2)/R1 and the measured voltage value (i.e. voltage_code) can be approximated as a linear equation. Therefore, the simulated values of (R1 - R2)/R1 can be used to determine slope and intercept of the linear equations to compute the output voltage_code. For example, if the process corner is known as SS process corner, and the voltage sensor is at 50°C, and then the proposed linear calculator can use the suitable linear equation from the simulation results to compute the output voltage_code with the current value of (R1 - R2)/R1.

The operation flow of the proposed all-digital sensor is explained as follows. After chip fabrication, the proposed all-digital voltage sensor needs to be calibrated at 1.1V. During the calibration process, the chip operating temperature is not important, since the proposed process sensor can determine the process corner of the voltage sensor without temperature information as illustrated in Fig. 2. When the process_code shown in Fig. 1 is determined, the proposed temperature sensor can always determine the chip temperature (temp_code) when the operating voltage ranges within 0.9V to 1.1V as illustrated in Fig. 3. Subsequently, the linear calculator of the proposed all-digital voltage sensor will uses the value (R1 - R2)/R1 and selects a suitable linear equation to compute the measured voltage value (voltage_code) as illustrated in Fig. 4.

3. Simulation Results

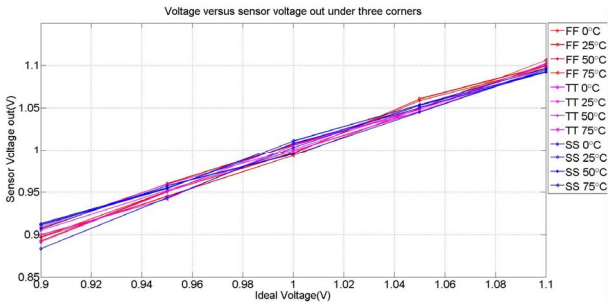

Fig. 5 The output of the voltage sensor versus ideal voltage.

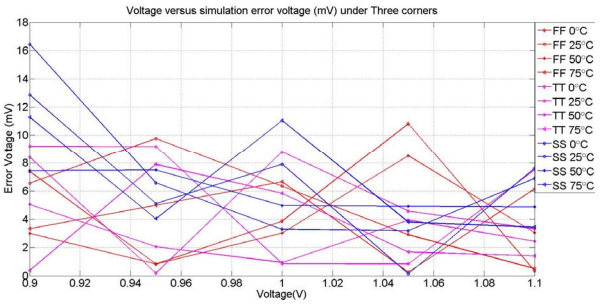

Fig. 6 The error of the proposed voltage sensor.

The proposed all-digital voltage sensor is implemented in 90nm CMOS process, and the active area of the test chip is 0.063 mm^2. It achieves a 0.027mV resolution and has a maximum error 16.4mV with process, voltage, and temperature (PVT) variations as shown in Figs. 5 and 6. The power consumption of the proposed design is 1.0068mW at 1.0V.

4. Conclusion

In this paper, we use three ring oscillators to build up the delay ratio estimator. Then the characteristics of the delay ratios can be used to identify the process and temperature variations. Subsequently, the linear calculator of the proposed all-digital voltage sensor can output an accurate voltage value with PVT variations. The proposed all-digital voltage sensor is implemented with standard cells and is suitable for SoC design.

5. References

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