A 1 Mb/s – 40 Mb/s WBS Transceiver for Human Body Channel Communication

Ching-Che Chung[1], Shu-Xian Shen[1], Chuan-Yi Wu[2], Yu-Te Liao[2], Chi-Tung Chang[1]
[1] Department of Computer Science and Information Engineering, National Chung Cheng University,
[2] Department of Electrical Engineering, National Chung Cheng University,
No. 168 University Rd., Min-Hsiung, Chia-Yi, Taiwan

ABSTRACT

In this paper, we present a low-power, high-speed and large jitter tolerance wideband signaling (WBS) transceiver for human body channel communication (BCC). The proposed WBS transceiver sends data with a spread spectrum clock generator (SSCG) to reduce electromagnetic emission. In order to improve the jitter tolerance of the receiver, we propose an add-drop FIFO algorithm with a blind oversampling clock and data recovery (CDR) circuit to recover the corrupted clock and data. The proposed WBS transceiver is implemented in a standard performance 90nm CMOS process, and the core area is 0.15mm^2. The data rate of the proposed transceiver ranges from 1-Mb/s to 40-Mb/s. The power consumption is 1.64mW at 40-Mb/s and the bit energy is 0.041nJ/b.

1. INTRODUCTION

In recent years, biomedical applications with semiconductor technologies had become more popular. The aging of the population also drives for personal healthcare applications. For body area network (BAN) communication, many methods had been proposed, such as radio-frequency transmission, near-field electrostatic coupling and electromagnetic wave transmission [1] [2]. However, these methods are susceptible to the interferences in the environment. In addition, these schemes also have high power consumption. Human body channel (HBC) communication is a method which uses the human skin as transmission medium to transmit the biomedical information. The characteristics of HBC had been studied in [3]-[5]. HBC transceivers can achieve lower power consumption than wireless approaches. Therefore, HBC schemes have been suggested for the BAN.

In this paper, we adopted the WBS transceiver with a direct-coupled interface (DCI) as the transmission method [4]. Compared to the other BAN methods, the WBS has many advantages such as low-power consumption and high data rate. However, due to the human body antenna effects [3], the human body will absorb external electromagnetic interferences. Then, it causes enormous jitter to the receiver circuit. In order to tolerate large jitter effects, we propose a 5X blind oversampling CDR circuit with an add-drop FIFO scheme. The maximum data rate of the proposed WBS transceiver can be up to 40 Mb/s with 0.041nJ/b bit energy.

2. PROPOSED WBS TRANSCEIVER

Fig. 1 shows the block diagram of the proposed WBS transceiver. It is composed of a SSCG-based transmitter and an oversampling receiver. The proposed transmitter directly transmits non-return-to-zero (NRZ) data to the HBC. Then the wideband pulse signal is recovered by the oversampling receiver circuit. The SSCG-based transmitter is composed of a spread spectrum clock generator (SSCG) circuit, a pseudo-random binary sequence (PRBS) generator and two 2-to-1 multiplexers. The SSCG circuit can reduce the electromagnetic emission with low hardware cost. The SSCG circuit generates a spread spectrum clock to trigger the PRBS generator. Then, the PRBS generator produces 2^{31}-1 PRBS random data to the HBC.

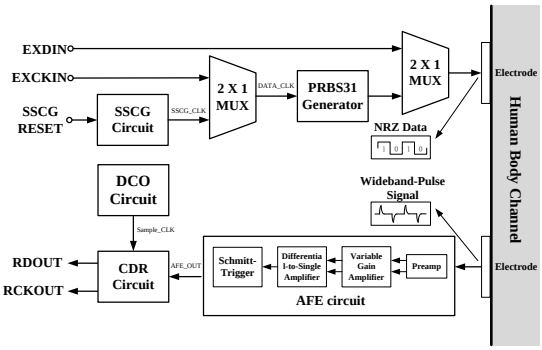

Fig. 1. Proposed WBS transceiver.

The oversampling receiver circuit is consisted of an analog frontend (AFE) circuit, a digital controlled oscillator (DCO) and a 5X blind oversampling CDR circuit. The received signal attenuation changes with transmission distance. Therefore, we propose a variable gain amplifier (VGA), which provides a 5-bit control code, EN0 to EN4, to amplify the received wideband pulse signal. The maximum magnification gain including the pre-amplifier and the VGA is 38dB. The DCO has an external control input to provide a 200MHz sampling clock rate for the CDR circuit.

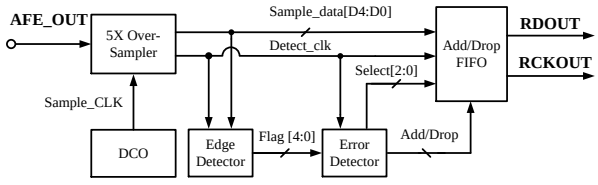

Fig. 2. Proposed 5X oversampling CDR circuit.

Fig. 2 shows the block diagram of the proposed 5X blind oversampling CDR circuit. The CDR circuit is consisted of a 5X over-sampler, an edge detector, an error detector and an add-drop FIFO. The 5X over-sampler samples five points in one symbol period. Then these sampled data (D4 to D0) are sent to the edge detector and the add-drop FIFO. The edge detector detects the edge transition by exclusive-or the two adjacent sampling data. Subsequently, the center picking method is adopted to choose one selected sampled data for the add-drop FIFO. For example, in Fig. 3(a), data transitions are located at D4 of SW2 and D4 of SW3. Thus, in sample window SW2 and SW3, the sampled data D2 will be selected to save to the add-drop FIFO.

Due to the human body antenna effects, interferences in the environment, such as cordless phones, frequency modulation (FM) radios, and walkie-talkies, may cause enormous jitter to

This work was supported in part by the National Science Council of Taiwan, under Grant NSC101-2221-E-194-063.

the received data. Therefore, it causes symbol boundary variations. Then the CDR circuit may missing one bit or duplicate one bit, as illustrated in Figs. 3(b) and 3(c). For example, in Fig. 3(b), Data2 is missing, and in Fig. 3(c), Data2 is sampled two times. The Add/Drop signals are generated by the error-detector. If the selected sampled data is changed from D4 to D0, as shown in Fig. 3(b), the "Add" signal will be activated. Oppositely, if the selected sampled data is changed from D0 to D4, the "Drop" signal will be activated.

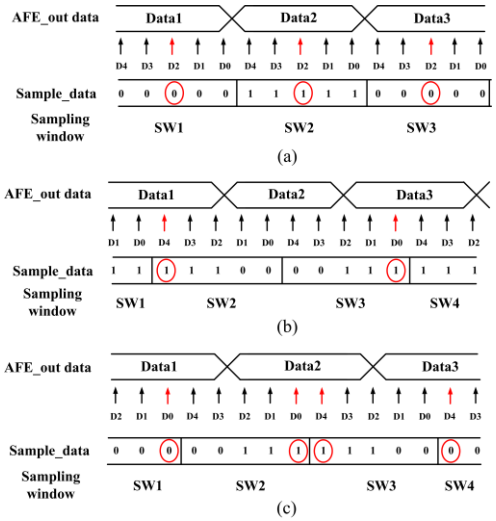

Fig. 3. (a) Center-picking method (b) Missing data case (c) Duplicate data case.

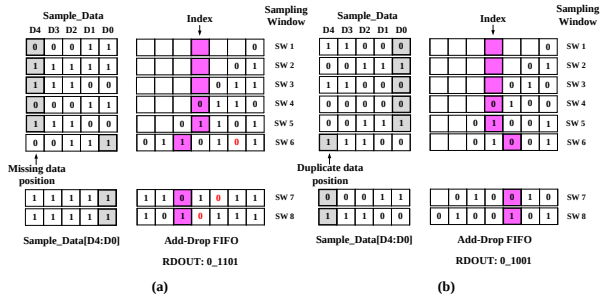

Fig. 4. (a) Add data operation (b) Drop data operation

Fig. 4 shows the operation of the proposed add-drop FIFO. In this figure, we take a 7-bit add-drop FIFO as an example. In each sampling window, the add-drop FIFO will shift to left by one, and save the current selected sampled data to the least significant bit. Then it outputs the data as pointed by the "Index" register. In addition, in the beginning, the "Index" register is pointed to the middle of the add-drop FIFO. If "Add" signal is activated, the missing data will be added to the add-drop FIFO, and the value of "Index" register is added by one. Oppositely, if "Drop" signal is activated, the add-drop FIFO stalls one cycle to drop the duplicated data, and the value of "Index" register is subtracted by one. For example, in Fig. 3(b), D4 of SW3 is the missing data, and it will be added to the add-drop FIFO. In Fig. 3(c), D4 of SW3 is the duplicated data, and it will be dropped. The proposed add-drop FIFO makes the CDR circuit can tolerate large data jitter with small hardware cost.

3. SIMULATION RESULTS

Fig. 5 shows the timing diagram of the proposed WBC transceiver. When the NRZ data is sent to the HBC, the received signal (Wideband-Pulse Signal) becomes a narrow pulse signal that comprises positive and negative pulses without DC offset. Then, this small pulse signal is amplified by the AFE circuit to a full swing voltage of 1 V. The sampling clock (Sample_CLK) generated by the DCO is applied to sample the AFE_OUT. Consequently, the binary data and clock can be recovered by the CDR circuit.

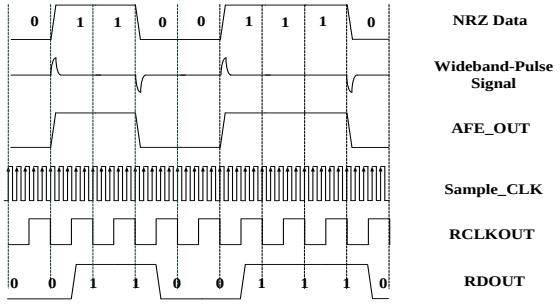

Fig. 5. Timing diagram of the WBC receiver.

Fig. 6 shows the error-free CDR circuit simulation results at 40Mb/s. If the P_k-P_k received random data jitter is smaller than 4ns, the proposed CDR circuit can achieve a bit-error-rate (BER) < 10^{-10}. In addition, the jitter tolerance of the proposed CDR circuit can be improved by increasing the size of the add-drop FIFO.

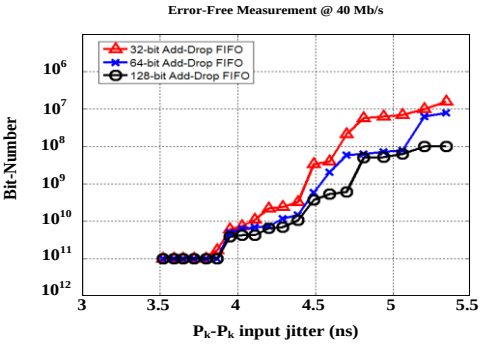

Fig. 6. Error-free CDR circuit simulation results.

4. CONCLUSION

In this paper, a low-power, high-speed and large jitter tolerance WBS transceiver for the BAN is presented. With the proposed add-drop FIFO, we can achieve large jitter tolerance with small hardware cost.

5. REFERENCES

[1] Mitsuru Shinagawa, et al., "A near-field-sensing transceiver for intrabody communication based on the electrooptic effect," *IEEE Trans. Instrum. Meas.*, vol. 53, no. 6, pp. 1533-1538, Dec. 2004.

[2] Namjun Cho, et al., "A 60 kb/s - 10Mb/s, adaptive frequency hopping transceiver for interference-resilient body channel communication," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 708-717, Mar. 2009.

[3] T. G. Zimmerman, "Personal area networks: near-field intrabody communication," *IBM Systems Journal*, vol. 35, no. 3.4, pp. 609-617, 1996.

[4] Keisuke Hachisuka, et al., "Development and performance analysis of an intra-body communication device," *in Proc. International Conference on Solid-State Sensors, Actuators and Microsystems*, Jun, 2003, pp. 1722-1725.

[5] Namjun Cho, et al., "The human body characteristics as a signal transmission medium for intrabody communication," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 5, pp. 1080-1086, May 2007.

[6] Seong-Jun Song, et al. "A 0.2-mW 2-Mb/s digital transceiver based on wideband signaling for human body communications," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 2021-2033, Sep. 2007.

[7] Joonsung Bae, et al., "A 0.24-nJ/b wireless body-area-network transceiver with scalable double-FSK modulation," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 310-322, Jan. 2012.