

A Monotonic Digitally Controlled Oscillator with Self-Calibration in 65nm CMOS Technology

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Abstract—This paper presents a self-calibration circuit to correct the non-monotonic response in the cascading digitally controlled oscillator (DCO). The proposed calibration circuit can solve the non-monotonic problem when the coarse-tuning control code is changed. The proposed DCO implemented with a standard performance 65nm CMOS process can output frequency ranges from 58.7 MHz to 481.6 MHz. And the total power consumption of the DCO with calibration circuit is 0.142 mW at 58.7 MHz and is 0.205mW at 481.6MHz. The proposed DCO with calibration circuit is easy to be implemented and thus is very suitable for ADPLL design in SoC applications.

I. INTRODUCTION

Phase-Locked Loops (PLLs) are widely used in many communication systems, such as on-chip clock generators, clock and data recovery (CDR) circuits and frequency synthesizers. Traditionally, PLLs are often designed with the charge pump-based architecture [1-2]. However, the charge pump-based PLLs suffer from serious leakage current problem in 65nm CMOS process and the jitter performance becomes unacceptable. As a result, the low leakage CMOS process is often needed when implementing the charge pump-based PLLs in 65nm CMOS process. But if the low leakage CMOS process is used, the circuit performance will be degraded, too. Hence, the all-digital PLLs [3-8] which use robust digital control code to control the digital controlled oscillator (DCO) can avoid the leakage current problem and become more and more popular now.

PLLs are sensitive to process, voltage and temperature (PVT) variations, and PLLs' output jitter performance are degraded by noise coupling and power supply noise effects. Hence when the analog PLLs are integrated into the system-on-a-chip (SoC) with advanced CMOS process, it also takes more efforts to integrate the analog circuits with the digital circuits.

The DCO is the most critical component in the all-digital phase-locked loop (ADPLL). Because the DCO usually occupies almost 50% area and power consumption of the ADPLL, and therefore how to design a DCO with lower power, smaller area and sufficient frequency resolution is very important while designing an ADPLL.

In order to achieve both wide frequency range and high resolution with smaller chip area and lower power consumption, the cascading structure is often used in designing the DCO [4-8]. In these DCOs, the coarse-tuning stage, which uses large delay cells to achieve wide-range delay control, is accompanied with a fine-tuning stage to improve the resolution of the DCO. In this cascading architecture, it is often needed to overlap the sub-frequency band to make sure that there will not have any frequency dead zone in the DCO. But this makes the DCO's output frequencies become non-monotonic with the DCO control codes. To alleviate the difficulty to design the ADPLL controller with these cascading structure DCOs, the fine-tuning stage must have a larger delay controllable range than the delay step of previous coarse-tuning stage. However, it means that the coarse-tuning DCO control code must be determined in the frequency search mode, and it must be fixed after the frequency search is done. Then the ADPLL controller only adjusts the fine-tuning DCO control code to fine-tune the output frequency and to track the phase of the reference clock in a selected sub-frequency band.

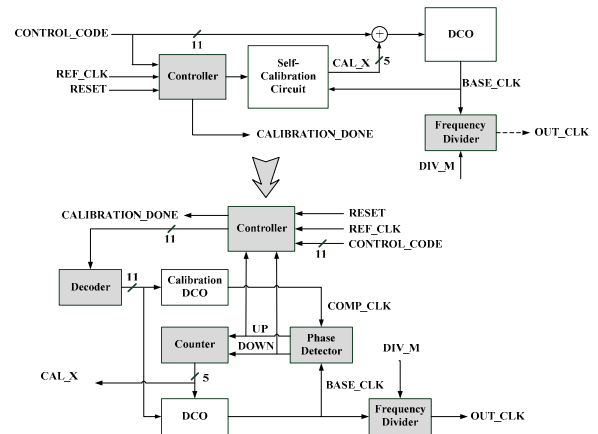


Figure 1. The proposed DCO with self-calibration circuit.

In these ADPLLs [4-8], the proposed DCOs still have monotonic response if the coarse-tuning DCO control code is

fixed while tuning the fine-tuning DCO control code. But for high frequency multiplication applications, such as in line-locked PLLs or in spread spectrum clock generator (SSCG) applications [7], it sometimes needs to change the coarse-tuning DCO control code after frequency search is done. As a result, the cascading DCO structures [4-8] are not suitable for these applications. Therefore, the DCO architecture which uses the interpolators to generate a fine-tuning delay between two coarse-tuning delays is proposed in [9]. But the interpolator is not an available logic gate which can be found in the standard cell library. To achieve better portability over different processes, it is better to reuse the standard cells in ADPLL design.

In this paper, the cell-based DCO with self-calibration circuit to overcome the non-monotonic response problem in cascading structure DCO is presented. The mechanism of self-calibration decides the compensation codes for the DCO fine-tuning control codes when the coarse-tuning control codes are changed. The proposed self-calibration method can guarantee the monotonic response of the DCO, and therefore the advantages of using the cascading structure DCOs can be retained.

Fig. 1 shows the architecture of the proposed DCO with self-calibration circuit. In Fig. 1, it shows that the DCO control code (CONTROL_CODE) which inputs to the DCO is sent to the controller of the self-calibration circuit to detect if there has changes in the coarse-tuning control code. Then the compensation code for the DCO fine-tuning control code is added to the current input DCO control code to make sure that the monotonic response of the DCO during DCO coarse-tuning control code transitions.

This paper is organized as follows: the calibration method of the proposed self-calibrated DCO is discussed in Section II. The implementation of the proposed self-calibrated DCO using a standard performance (SP) 65nm CMOS process is presented in Section III. Section IV shows the experimental simulation results of the proto-type chip. Finally, Section V concludes with a summary.

II. CALIBRATION CIRCUIT

In the cascading structure DCOs [4-8], the DCO has the coarse-tuning stage and the fine-tuning stage. But in this architecture, it is often needed to overlap the sub-frequency band to make sure that there will not have any frequency dead zone in the DCO. Otherwise the output clock may have large cycle-to-cycle jitter while the DCO operates near the frequency dead zone.

But if we overlap the sub-frequency band shown in Fig. 2, it means that when the coarse-tuning DCO control code changes from the current code to the next coarse-tuning DCO control code, the output frequencies is not monotonically increasing or decreasing. In Fig. 2, when the ADPLL controller adjusts the DCO control code from the coarse-band #K with fine-tuning control code (2^N-1) to the next coarse-band #(K+1), because the fine-tuning control code should reset to zero, and therefore the output frequency becomes slower than in previous DCO control code (i.e. coarse-band #K with fine-tuning control code (2^N-1)). And the ADPLL

controller will encounter great difficulties in frequency tracking.

To avoid this phenomenon, compensation codes should be added to the fine-tuning control code if there has changes in the coarse-tuning control code. In Fig. 2, a compensation code (X) is added to the fine-tuning control code so that the monotonic response can be retained.

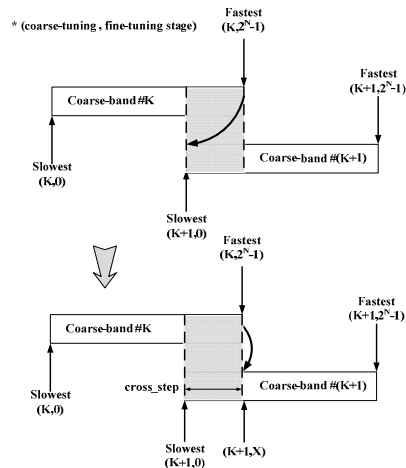


Figure 2. The compensation code when sub-frequency band is changed.

The compensation code (X) can be determined by circuit simulation with PVT variations. But if a fixed value compensation code is used in the ADPLL design, there will have too worse cycle-to-cycle jitter in worst-case conditions. In this work, we copied parts of the DCO circuit shown in Fig. 1 and named as "Calibration DCO" with the phase detector, the digital counter and the calibration controller to generate the compensation code (CAL_X) for current operating conditions. The calibration circuit starts to work when system is reset. After the calibration is done for the DCO, the compensation code is determined and then the ADPLL starts its normal operation.

The DCO control code is expressed in this format (coarse-tuning control code, fine-tuning control code). Two adjacent frequencies ($K, 2^N-1$) and ($K+1, \text{CAL_X}$) are used to do frequency comparison, where the fine-tuning control code has N-bit. The DCO control code ($K, 2^N-1$) is applied to the DCO shown in Fig. 1. Then the DCO control codes ($K+1, 0$), ($K+1, 1$), ... to ($K+1, \text{CAL_X}$) are sequentially applied to the "Calibration DCO". The phase detector detects if the frequency output of the "Calibration DCO" is higher than the DCO. Thus after several calibration cycles, the compensation code (CAL_X) can be found to guarantee the monotonic response of the DCO in ADPLL normal operation mode.

The timing diagram of the proposed calibration circuit is shown in Fig. 3. In Fig. 3, the BASE_CLK is the output clock of the DCO circuit and the COMP_CLK is the output clock of the "Calibration DCO". The signal "Disable_DCO" is used to disable both the DCO and the "Calibration DCO" after each frequency comparison so that the phase detector can be used to perform frequency comparison. The BASE_CLK and the COMP_CLK are sent to the phase detector. The phase

detector compares the phase of these two clocks. In the beginning of the calibration process, because the overlapped sub-frequency bands in the DCO, the COMP_CLK is lagged to the BASE_CLK. Then the calibration circuit keeps increasing the fine-tuning DCO control code of "Calibration DCO" until the COMP_CLK leads the BASE_CLK. Then the value X shown in Fig. 3 is saved as fine-tuning compensation code (CAL_X).

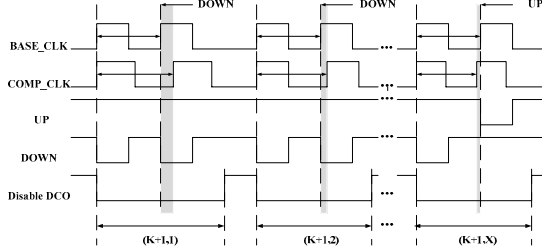


Figure 3. The timing diagram of the proposed calibration circuit.

After that, the calibration process is finished, and the ADPLL returns to its normal mode. And then the compensation code for the DCO fine-tuning control code is added to current input DCO control code to make sure that the monotonic response of the DCO during DCO coarse-tuning control code transitions.

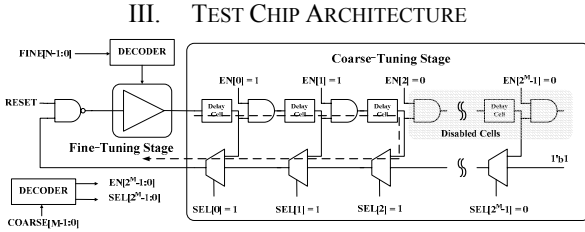


Figure 4. The proposed coarse-tuning stage of the DCO.

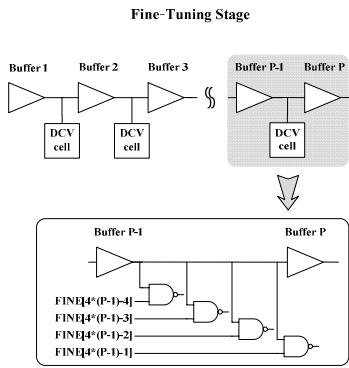


Figure 5. The fine-tuning stage of the proposed DCO.

Fig. 4 shows the architecture of the proposed DCO in the test chip. The proposed DCO is composed of the coarse-tuning stage and the fine-tuning stage. The coarse-tuning stage which has (2^M-1) delay cells with (2^M-1) multiplexers can provide 2^M different delays. In order to generate a sufficient delay time in 65nm CMOS process, the delay cells in the cell-library are used to build up the coarse-tuning stage. And the two-input

AND gates are added to each delay cell's output to disable the unused cells to save power consumption.

Fig. 5 shows the fine-tuning stage of the DCO. To achieve better DCO resolution, the digital-controlled varactors (DCVs) [6] are used in the fine-tuning stage. The fine-tuning stage has P buffers, in each buffer it connects to four NAND gates. When the fine-tuning control code (FINE[4*(P-1)-1:0]) is changed, the capacitance in the buffer's output node is also changed. Therefore a high resolution, linear fine-tuning delay stage can be created. The architecture of the "Calibration DCO" is the same as the DCO since it is a copied circuit of the DCO.

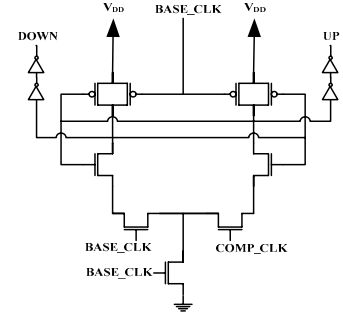


Figure 6. The phase detector in the calibration circuit.

Fig. 6 shows the schematic of the phase detector [8] used in the calibration circuit. The principle of the phase detector is to determine which rising edge in the BASE_CLK or the COMP_CLK occurs later. This phase detector has a dead zone about 1ps in 65nm CMOS process which is sufficient to detect tiny frequency difference in frequency comparison. In this work, two additional inverters are added at the output port of the phase detector to increase the driving capacity.

The other circuits such as the frequency divider, the controller of the calibration circuit are written with hardware description language (HDL), then the cell-based design flow are used to implemented the full test chip.

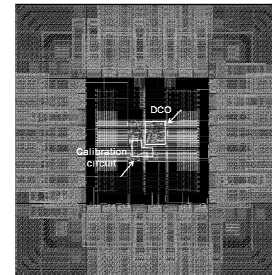


Figure 7. Layout of the test chip.

IV. EXPERIMENTAL RESULT

Fig. 7 shows the layout of the test chip. The test chip is implemented with a standard performance (SP) 65nm CMOS process. The design parameters of this test chip are determined as follows: $M=6$, $N=5$, $P=9$. It means that the proposed DCO has 64 coarse-tuning steps in the coarse-tuning stage and 32 fine-tuning steps in the fine-tuning stage.

Table I shows that the coarse-tuning step and fine-tuning range of the DCO with PVT variations. The fine-tuning range is larger than coarse-tuning step in worst operation conditions. Table II shows the operating range of the DCO with PVT variations. The DCO can output frequency ranges from 58.7MHz to 481.6 MHz with PVT variations. And the resolution in the proposed DCO is about 17.69ps in typical case.

TABLE I. TUNING RANGE AND RESOLUTION OF THE DCO.

	Coarse-Tuning Step (ns)	Fine-Tuning range (ns)	Resolution (ps)
TT	0.2888	0.5661	17.6906
FF	0.2412	0.4893	15.2910
SS	0.3557	0.6833	21.3525

TABLE II. DCO OPERATING RANGE

	TT	FF	SS
Slowest Clock Rate (MHz)	49.012	58.734	39.750
Fastest Clock Rate (MHz)	610.091	745.323	481.649

Fig. 8 shows the DCO's output period versus DCO control code in the non-calibrated DCO. Because the sub-frequency band is overlapped in coarse-tuning stage and fine-tuning stage, therefore the output period is not monotonically decreasing while the DCO control code is increasing. And after the calibration of the proposed DCO with self-calibration circuit, the output period becomes monotonically decreasing while the DCO control code is increasing. Hence the proposed self-calibration circuit can make sure that the monotonic response of the DCO during DCO coarse-tuning control codes transitions. Table III summarizes the test chip performance.

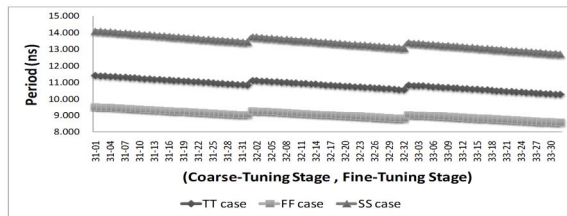


Figure 8. Period of the non-calibrated DCO.

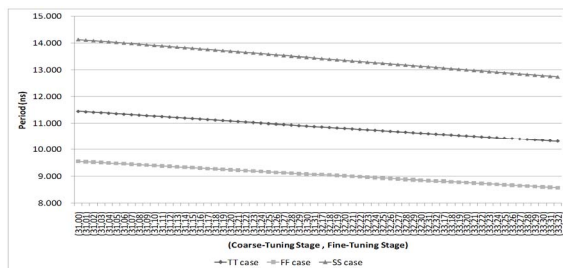


Figure 9. Period of the calibrated DCO.

TABLE III. TEST CHIP SUMMARY.

Technology	65nm
Supply Voltage	1.0v
Output Frequency	58.7 MHz to 481.6 MHz
Resolution	17.69 ps
Chip Area	0.01mm ²
Power	0.142mW@ 58.7MHz 0.205mW@ 481.6 MHz

V. CONCLUSION

In this paper, a monotonic DCO with self-calibration circuit in 65nm CMOS technology is presented. The proposed DCO can output frequency ranges from 58.7MHz to 481.6MHz with low-power consumptions. The proposed calibration circuit can solve the non-monotonic problem in cascading architecture DCOs when the coarse-tuning control code is changed thus is very suitable for ADPLL design in SoC applications.

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