# An All-Digital Temperature Sensor with Process and Voltage Variation Tolerance for IoT Applications

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***Abstract*—The embedded temperature sensor which monitors the hot spots of the chip had become an essential circuit for improving the reliability of the system-on-a-chip (SoC). However, most of the temperature sensors cannot resist the influence of voltage variations and results in significant temperature errors. In this paper, the relative reference modeling (RRM)-based temperature sensor is presented. The proposed temperature sensor uses a low-temperature sensitivity voltage classifier and a low-voltage sensitivity proportional to absolute temperature (PTAT) circuit to resist the voltage variations. Addition, the process variations can be eliminated after the three-point calibration. The proposed temperature sensor was fabricated in TSMC 90nm CMOS process. The measured results show that the temperature error of the proposed design is from -1.47°C to 1.40°C with supply voltage 0.9 to 1.1V.**

***Keywords—sensors, delay circuits, trimming, calibration, circuit reliability, digital circuits.***

## I. INTRODUCTION

As the technologies scale down, many transistors are integrated on a system-on-a-chip (SoC), which causes the increase of the power density. High power density makes the hot spot occurring more frequently which may seriously affect the chip performance. Modern CPUs and DRAMs utilize several on-chip temperature sensors for thermal monitoring which can provide temperature information and detect the hot spots. These on-chip temperature sensors require low power consumption and with small chip area.

For internet-of-things (IoT) applications and battery operated systems, the temperature sensors are easily suffered from voltage variations, and the battery is inherently less stable than the power supply. However, most of the previously published temperature sensors [1-5] cannot resist voltage variations or need a voltage regulator which occupied a relatively large chip area [6-8] and not suitable for IoT applications or battery operated systems. In the delay-line based temperature sensor, the propagation delay of the delay cells will change with voltage variations. Thus, after one-point or two-point calibration at a fixed voltage, the digital output of the temperature sensor may not present the correct temperature value under voltage variations [13].

The BJT-based temperature sensor can achieve a relatively high resolution but has high power consumption and is difficult to be integrated with other CMOS circuits [10]. CMOS time-domain temperature sensors are more suitable for the modern system, which have relatively low power consumption, small area, high portability and easy to be integrated with other circuits [3-5]. The shortcoming of CMOS time-domain temperature sensors is the high voltage sensitivity which needs to be carefully handled.

The relative reference modeling (RRM) method to separate the effects of voltage and temperature variations is proposed in [13-16]. The delay ratio of two delay cells, referenced delay cell (RDC) and compared delay cell (CDC), is used to eliminate the temperature sensitivity or voltage sensitivity of the delay cells, and the calibration process can remove the effects of process variations. If two delay cells, RDC and CDC, have similar temperature sensitivity but have different voltage sensitivity, the delay ratio will only be affected by voltage variations. Similarly, if the two delay cells have similar voltage sensitivity but have different temperature sensitivity, the delay ratio between the two delay cells will only be affected by temperature variations. However, the delay cells which meet the above conditions are not easily designed.

In this paper, the delay ratios of the proposed delay ratio estimator (DRE) can use for determining the voltage information. The voltage information will feedback to the temperature sensor to compensate for the voltage variations. As a result, the proposed all-digital temperature sensor can tolerate process and voltage variations and is suitable for IoT applications. The architecture of the proposed all-digital temperature sensor is presented in Section II. Section III describes the circuit implementation of the proposed design. Section IV shows the experimental results. Finally, the conclusion is given in Section V.

## II. THE PROPOSED TEMPERATURE SENSOR

Fig. 1 shows the test chip architecture of the proposed temperature sensor. It consists of a delay ratio estimator (DRE), an on-chip oscillator, a serial input interface with a Manchester code decoder, and a serial output interface with a Manchester code encoder. The calibration process and the non-linear mapping for the DRE and temperature sensor are performed with a field programmable gate array (FPGA) in the off-chip process. The test chip of the proposed temperature sensor uses the serial I/O interface to reduce the number of I/O pads. FPGA #1 sends the data to the serial interface of the test chip and sets up the control pins of the DRE and the on-chip oscillator. The purpose of these control pins will be discussed later. The output delay ratios, R1 and R2, will be encoded into the sequence of

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Manchester codes and send the data to the FPGA #2 for temperature value calculation.

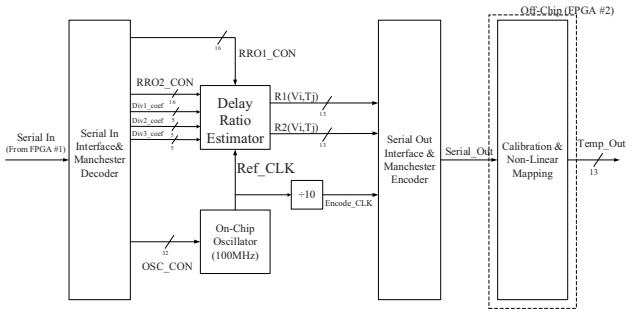



Fig. 1. Test chip architecture of the proposed temperature sensor.

Fig. 2 shows the architecture of the proposed DRE. It consists of a reference ring oscillator 1 (RRO1), a reference ring oscillator 2 (RRO2), a compared ring oscillator (CRO), frequency dividers, counters, and a subtractor. The CRO is a ring oscillator which is composed of 2-input NAND gates. The RRO1 is composed of 2-input NAND gates, but the negative voltage sensitivity MOS capacitors are added to enhance the voltage sensitivity. Also, the negative temperature sensitivity delay cells, thyristors [17] are added, and the digital control pins (RRO1_CON[15:0]) can be used for adjusting the temperature sensitivity of the RRO1 so that the RRO1 and the CRO can have similar temperature sensitivity after the trimming process. Then, the delay ratio R1 becomes sensitive to voltage variations but not sensitive to temperature variations. Subsequently, the delay ratio R1 can be used as a voltage classifier to determine the voltage information.

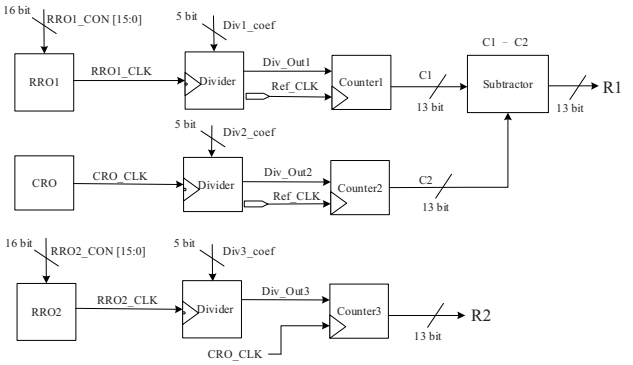



Fig. 2. Proposed delay ratio estimator (DRE).

The RRO2 is also composed of 2-input NAND gates, and thyristors are used to enhance the temperature sensitivity. In the trimming process, the digital control pins (RRO2_CON[15:0]) can be used for adjusting the temperature sensitivity of the RRO2 so that the delay ratio R2 can be used as a proportional to absolute temperature (PTAT) circuit. The voltage information provided by the delay ratio R1 is used to compensate for the voltage variations. As a result, the delay ratio R2 can become a low-voltage sensitivity PTAT circuit. The calibration process of the proposed temperature sensor after the chip is fabricated and the non-linear mapping between the delay ratio and the temperature value will be explained in section IV.

## III. Circuit Implementation

Fig. 3(a) shows the schematic of the negative voltage sensitivity MOS capacitors. When the delay cell drives this MOS capacitor, the negative voltage sensitivity of the delay cell can be enhanced. However, the positive temperature sensitivity of the delay cell is also increased accordingly. Fig. 3 (b) shows the schematic of the negative temperature sensitivity delay cell, thyristor [17]. The thyristor can be used for canceling the positive temperature sensitivity of the delay cell.

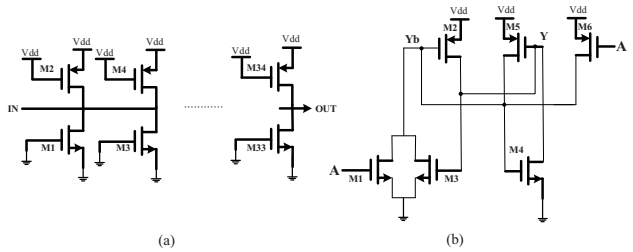



Fig. 3. (a) Negative voltage sensitivity MOS capacitor. (b) Negative temperature sensitivity thyristor.

Fig. 4 (a) shows the schematic of the CRO which is composed of 2-input NAND gates. Fig. 4(b) shows the schematic of the RRO1, the negative voltage sensitivity MOS capacitors are added to enhance the voltage sensitivity, and the path selector can be used to choose the number of thyristors enabled to adjust the temperature sensitivity of the RRO1. Fig. 4(c) shows the schematic of the RRO2. The path selector of the RRO2 can be used to choose the number of thyristors enabled to enhance the temperature sensitivity of the RRO2.

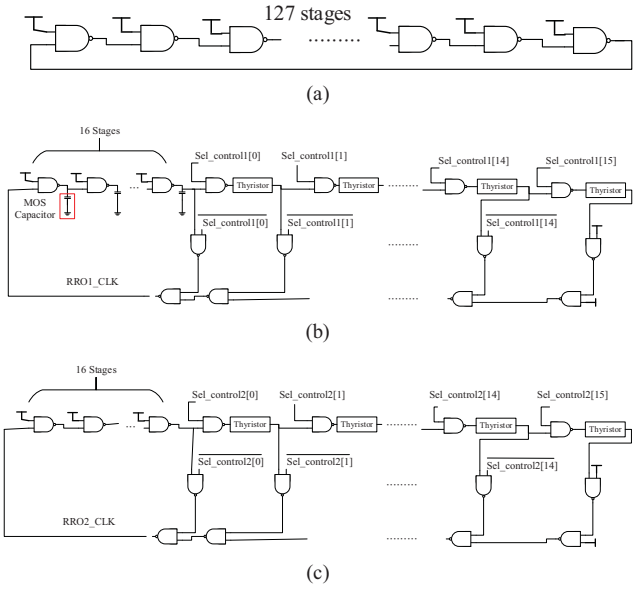


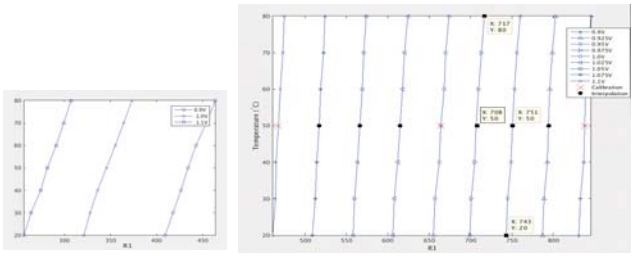

Fig. 4. Schematic of (a) CRO (b) RRO1 (c) RRO2.

## IV. Experimental Results

The test chip of the proposed temperature sensor is fabricated in TSMC 90nm CMOS process with a 1.0V power supply. The core size of the chip is 300μm×400μm, the chip size including I/O pads is 880μm×936μm.

Fig. 2 shows that the outputs of the RRO1 and CRO are divided into low-frequency clock signals and the on-chip high-

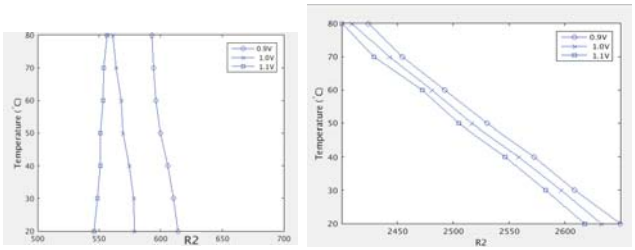
speed clock (Ref_CLK, 100MHz) is used as a time-to-digital converter (TDC) to quantize one period of Div_Out1 and Div_Out2 into digital codes (C1 and C2). The delay ratio R1 can be computed after subtraction (C1 – C2). Fig. 5(a) shows the measured delay ratio R1 of one test chip before the trimming process, and R1 has positive temperature sensitivity. The digital control pins (RRO1_CON[15:0]) shown in Figs. 1 and 2 can be used for adjusting the temperature sensitivity of the RRO1. We will adjust RRO1_CON[15:0] until the RRO1 and CRO have similar temperature sensitivity. Subsequently, R1 becomes sensitive to voltage variations but not sensitive to temperature variations, as shown in Fig. 5 (b).



(a) (b)

Fig. 5. Delay ratio R1 uses as a voltage classifier (a) Before the trimming process (b) After the trimming process.

After setting RRO1_CON[15:0] of the RRO1, the delay ratio R1 is measured at one calibration point, (50°C, 0.9V/1.0V/1.1V). Subsequently, the R1 value at other voltage points (from 0.9V to 1.1V, step size 25mV) can be calculated using the interpolation method, as indicated in Fig. 5(b). The value of the delay ratio R1 at different voltage can be used as the threshold value for determining the voltage information of the temperature sensor. For example, in the normal mode of the proposed temperature sensor, if the delay ratio R1 is 600 which is close to the threshold value of R1 at 1.025V, then the voltage of the temperature sensor can be classified as 1.025V. Then, this voltage information can be used in temperature value calculation to eliminate the voltage variation effects to the temperature sensor.



(a) (b)

Fig. 6. Delay ratio R2 uses as a PTAT circuit (a) Before the trimming process (b) After the trimming process.

Fig. 2 shows that the output of the RRO2 is divided into a low-frequency clock signal, and then the output of the CRO is used as a TDC to quantize one period of Div_Out3 into digital codes (delay ratio R2). Fig. 6(a) shows the measured delay ratio R2 of one test chip before the trimming process, and the delay ratio R2 did not have high negative temperature sensitivity. The digital control pins (RRO2_CON[15:0]) shown in Figs. 1 and 2 can be used for adjusting the temperature sensitivity of the RRO2. We will adjust RRO2_CON[15:0] until the R2 have high negative temperature sensitivity. Subsequently, R2 can be used as a PTAT circuit, as shown in Fig. 6(b).

After setting RRO2_CON[15:0] of the RRO2, the non-linear mapping between the delay ratio and the absolute temperature value shown in Fig. 6(b) can be obtained in the calibration process. The delay ratio R2 is measured at three calibration points, (20°C, 0.9V/1.0V/1.1V), (50°C, 0.9V/1.0V/1.1V), and (80°C, 0.9V/1.0V/1.1V). Subsequently, the relationship between the delay ratio R2 and the absolute temperature value at (0.9V, 1.0V, 1.1V) can be obtained by the second order curve fitting method. The second order curve equations for other voltage points (from 0.9V to 1.1V, step size 25mV) can be calculated using the interpolation method. In the normal mode of the proposed temperature sensor, the delay ratio R1 is used to detect the voltage information, and the corresponding second order curve equation can be obtained using the interpolation method. Finally, the temperature value can be computed using the second order curve equation and the delay ratio R2.

Fig. 7 shows the error of the proposed temperature sensor. Three test chips are measured, and the worst case temperature error under PVT variations is -1.47°C to 1.40°C. Table I shows the comparisons with prior temperature sensors. Temperature sensors [11, 12] cannot tolerate voltage variations, and thus, they are not suitable for IoT applications. The proposed RRM-based temperature sensor using delay ratios to design a low voltage sensitivity PTAT circuit. Thus, the proposed temperature sensor can have a relatively small error than the other designs [9, 11, 12, 18] under voltage variations.

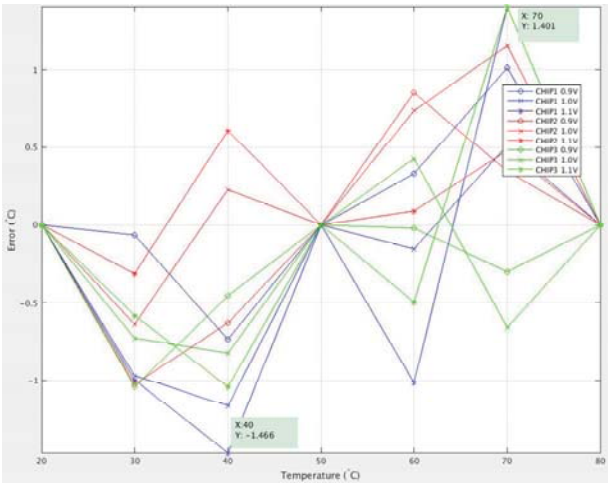



Fig. 7. Error of three temperature sensor test chips.

## V. Conclusion

In this paper, the proposed work uses high voltage sensitivity MOS capacitors and negative temperature sensitivity thyristors to build up the DRE with three oscillators. The proposed DRE can detect the voltage information under temperature variations. Subsequently, the proposed PTAT circuit can resist the voltage variations and reduce the error of the temperature sensor. The proposed all-digital temperature sensor can tolerate process and voltage variations after three-point calibration without the requirement of a voltage regulator

TABLE I
PERFORMANCE COMPARISONS

| | [11] ASP-DAC'16 | [12] TVLSI'12 | [9] JSSC'16 | [18] TBioCAS'17 | Proposed Work |
|---|---|---|---|---|---|
| Method | Digital | Digital | Analog | Analog | Digital |
| Technology(nm) | 28 | 130 | 65 | 65 | 90 |
| Voltage Insensitivity | No | No | Yes | Yes | Yes |
| Temp. Range(℃) | 0~100 | 0~100 | 0~100 | 30~70 | 20~80 |
| VDD Range(V) | Fixed 0.9V | Fixed 1.2V | 0.85~1.05 | 0.2~0.4 | 0.9~1.1 |
| Resolution(℃) | 0.44 | 0.78 | 0.3 | N/A | 0.6 |
| Conversion Rate (k sample/sec) | 5 | 5 | 45.5 | N/A | 24.2 |
| Error (℃) | -4.3 ~ 4.3 (at 0.9V) | -4 ~ 4 (at 1.2V)<br>-90 ~ 90 (1.08V~1.32V) | -5 ~ 2.2 | -5 ~ 8.1 | -1.47 ~ 1.40 |
| Power (mW) | 0.45 | 1.2 | 0.15 | 0.25 | 4.4 |
| Area($mm^2$) | 0.003738 | 0.12 | 0.0042 | N/A | 0.12 |
| Energy for one conversion (μJ) | 0.009 | 0.24 | 0.0033 | N/A | 0.18 |
| Supply Sensitivity(℃/mV) | N/A | N/A | 0.034 | 0.069 | 0.043 |
| Master Curve | $1_{st}$ | $3_{rd}$ | $2_{nd}$ | $1_{st}$ | $2_{nd}$ |
| Temp. Calibration Point | 2pt | 1pt | 2pt | 2pt | 3pt |

and is suitable for battery operated system or IoT applications. The test chip of the temperature sensor was implemented in TSMC 90nm CMOS technology and occupied an area of 0.12$mm^2$. The worst case temperature error under PVT variations is -1.47°C to 1.40°C, and the supply sensitivity can be achieved as 0.043°C/mV.

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